



30V, N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD17501Q5A](#)

FEATURES

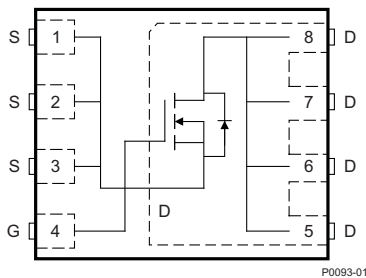
- **Ultralow Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm x 6-mm Plastic Package**

APPLICATIONS

- **Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems**
- **Optimized for Synchronous FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View


PRODUCT SUMMARY

$T_A = 25^\circ\text{C}$ unless otherwise stated		TYPICAL VALUE		UNIT
V_{DS}	Drain to Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	13.2		nC
Q_{gd}	Gate Charge Gate to Drain	3.5		nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{V}$	3	m Ω
		$V_{GS} = 10\text{V}$	2.4	m Ω
$V_{GS(th)}$	Threshold Voltage	1.3		V

ORDERING INFORMATION

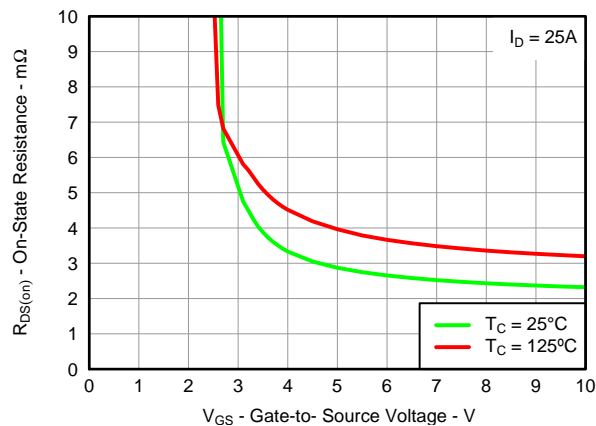
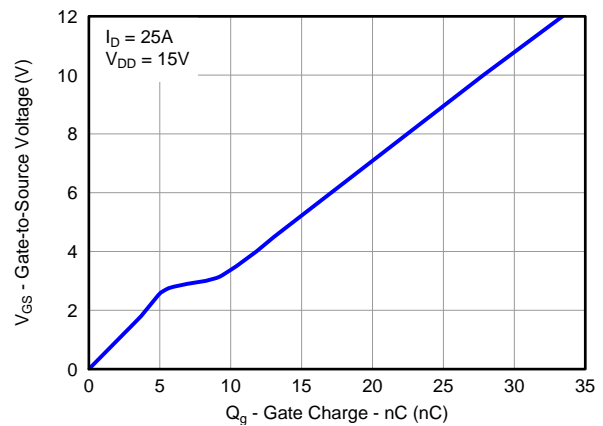
Device	Package	Media	Qty	Ship
CSD17501Q5A	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	20 / -12	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current ⁽¹⁾	28	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	187	A
P_D	Power Dissipation ⁽¹⁾	3.2	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 90\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	405	mJ

(1) Typical $R_{\theta JA} = 39^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

 $R_{DS(on)}$ vs V_{GS}

GATE CHARGE


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = 250\mu A$	30			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20/-12V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\mu A$	1	1.3	1.8	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_{DS} = 25A$		3	3.7	m Ω
		$V_{GS} = 10V, I_{DS} = 25A$		2.4	2.9	m Ω
g_{fs}	Transconductance	$V_{DS} = 15V, I_{DS} = 25A$		110		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V,$ $f = 1\text{MHz}$		2040	2630	pF
C_{oss}	Output Capacitance			1350	1700	pF
C_{rss}	Reverse Transfer Capacitance			66	85	pF
R_G	Series Gate Resistance			1.3	2.6	Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_{DS} = 25A$		13.2	17	nC
Q_{gd}	Gate Charge Gate to Drain			3.5		nC
Q_{gs}	Gate Charge Gate to Source			5.4		nC
$Q_{g(th)}$	Gate Charge at V_{th}			2.9		nC
Q_{oss}	Output Charge	$V_{DS} = 13.7V, V_{GS} = 0V$		35		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V,$ $I_{DS} = 25A, R_G = 2\Omega$		10.4		ns
t_r	Rise Time			17		ns
$t_{d(off)}$	Turn Off Delay Time			18		ns
t_f	Fall Time			7.9		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD} = 25A, V_{GS} = 0V$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 13.7V, I_F = 25A, di/dt = 300A/\mu s$		46		nC
t_{rr}	Reverse Recovery Time			32		ns

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

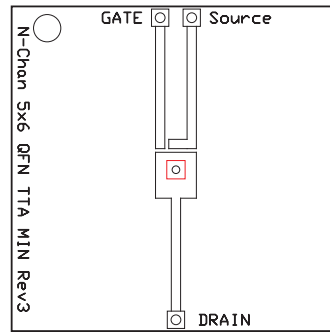
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			49	$^\circ\text{C/W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch \times 1.5-inch (3.81-cm \times 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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Max $R_{\theta JA} = 49^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

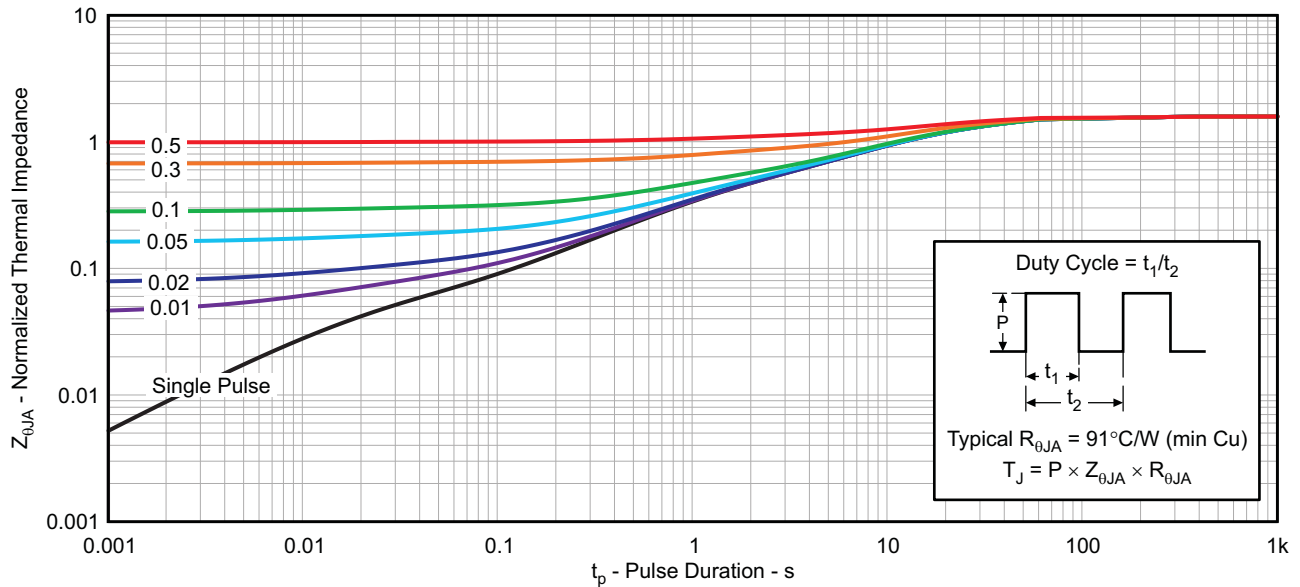


M0137-02

Max $R_{\theta JA} = 114^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

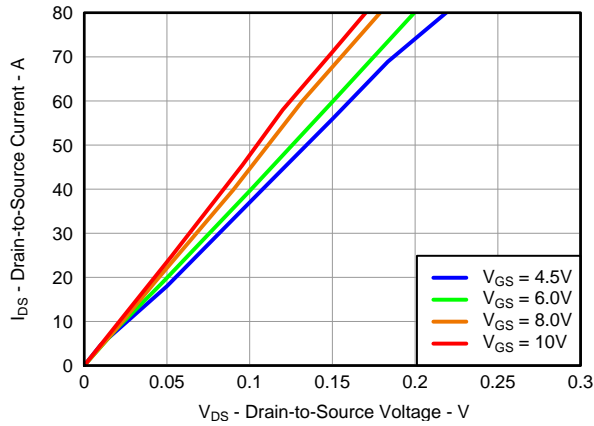


Figure 2. Saturation Characteristics

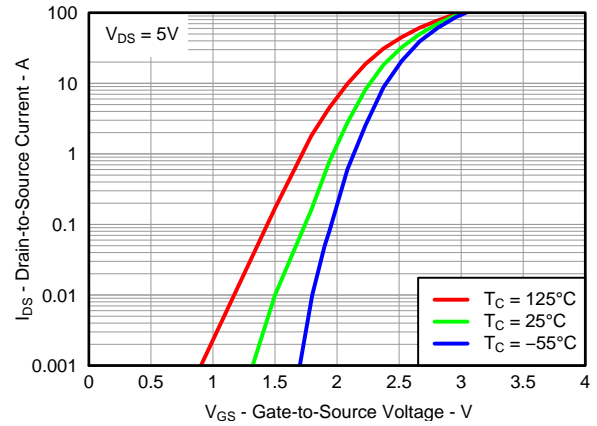


Figure 3. Transfer Characteristics

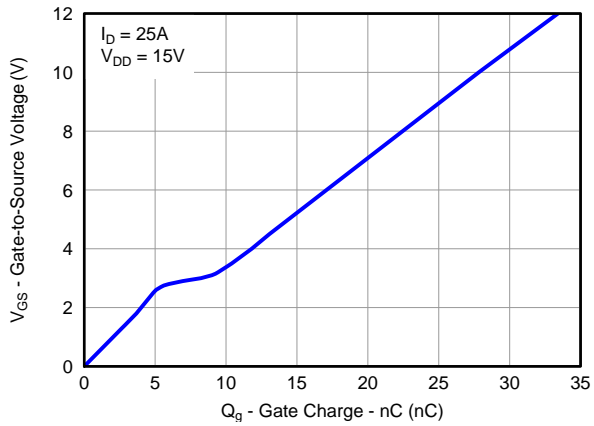


Figure 4. Gate Charge

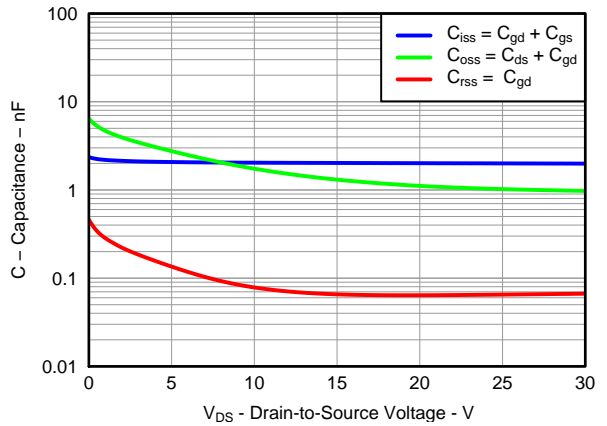


Figure 5. Capacitance

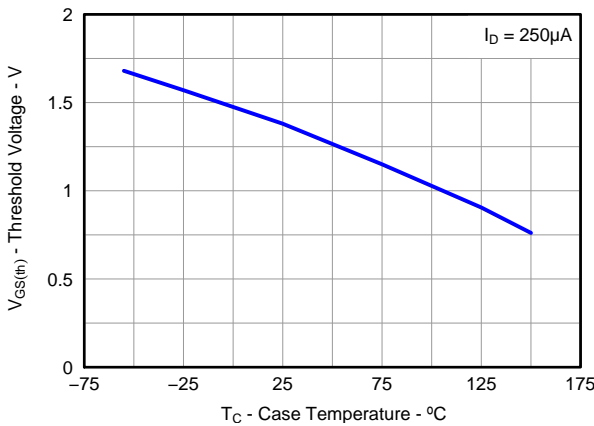


Figure 6. Threshold Voltage vs. Temperature

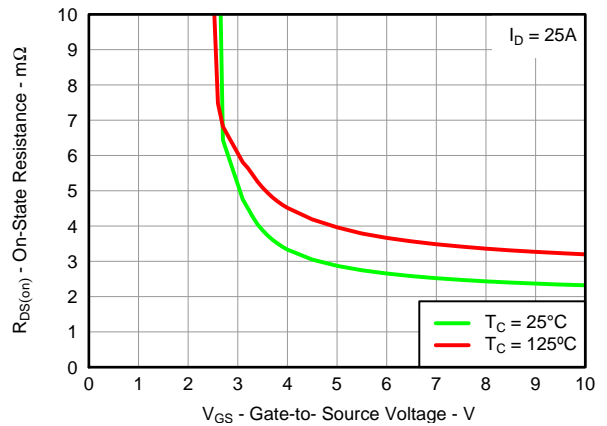


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

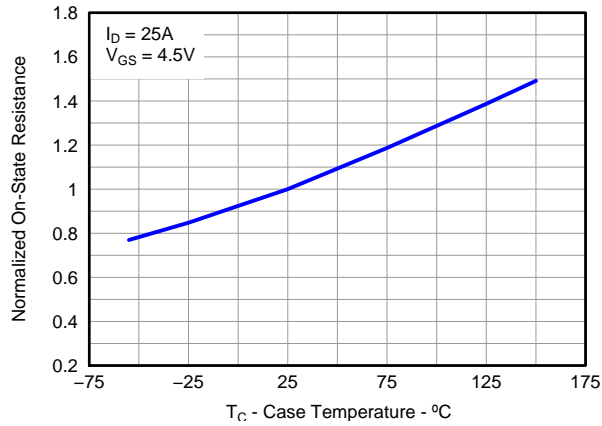


Figure 8. Normalized On-State Resistance vs. Temperature

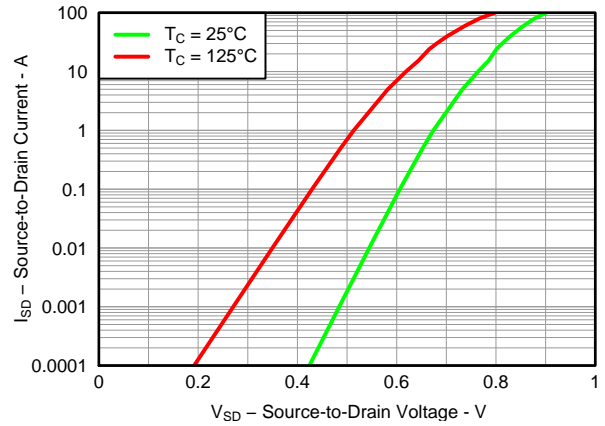


Figure 9. Typical Diode Forward Voltage

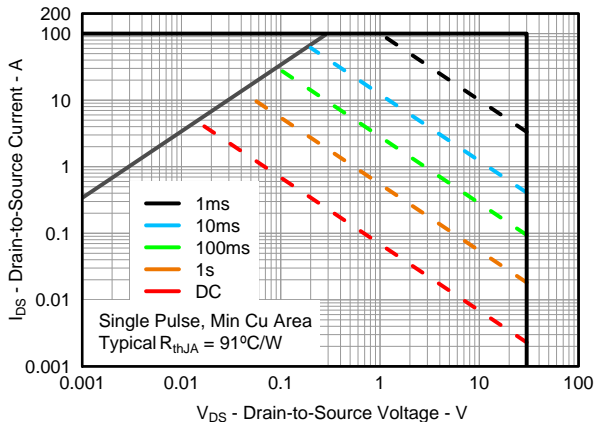


Figure 10. Maximum Safe Operating Area

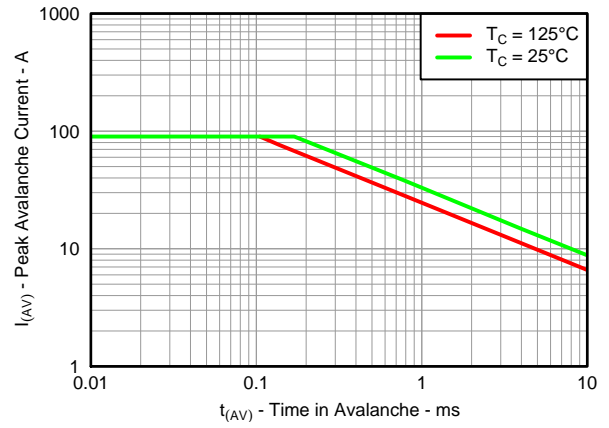


Figure 11. Single Pulse Unclamped Inductive Switching

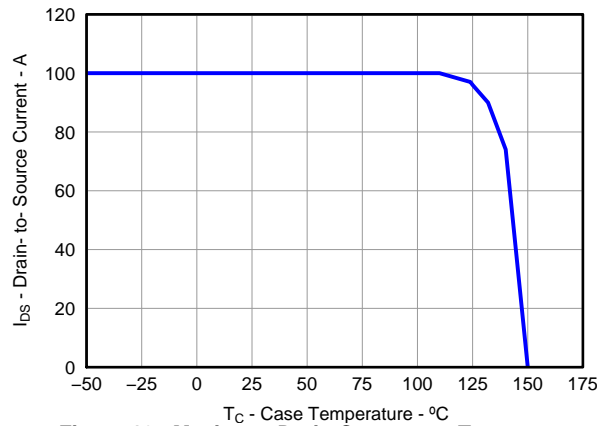


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

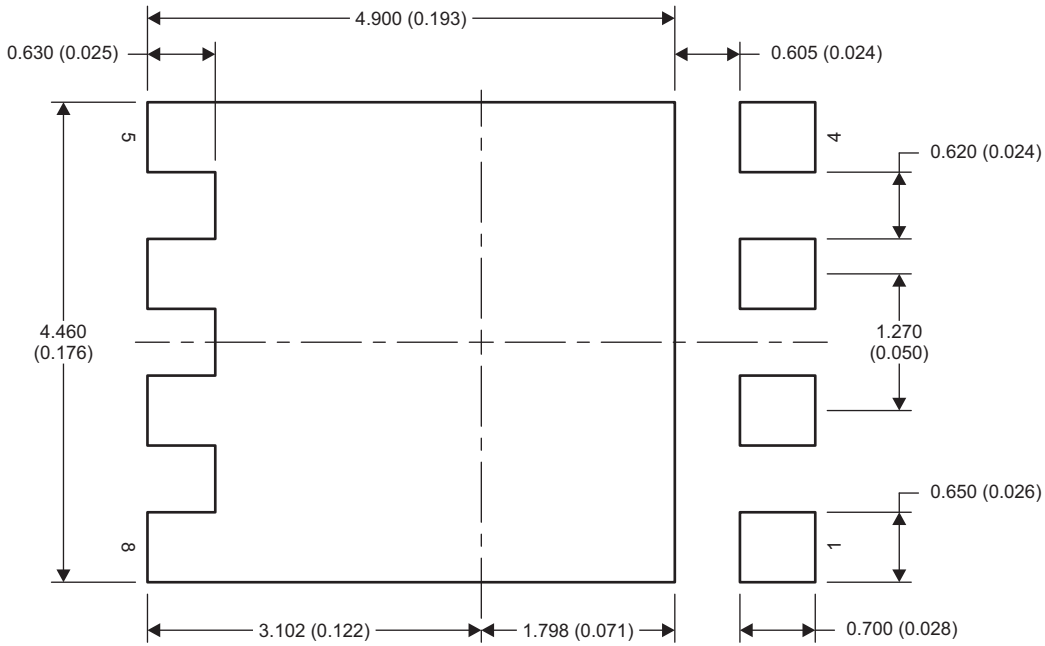
Q5A Package Dimensions



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

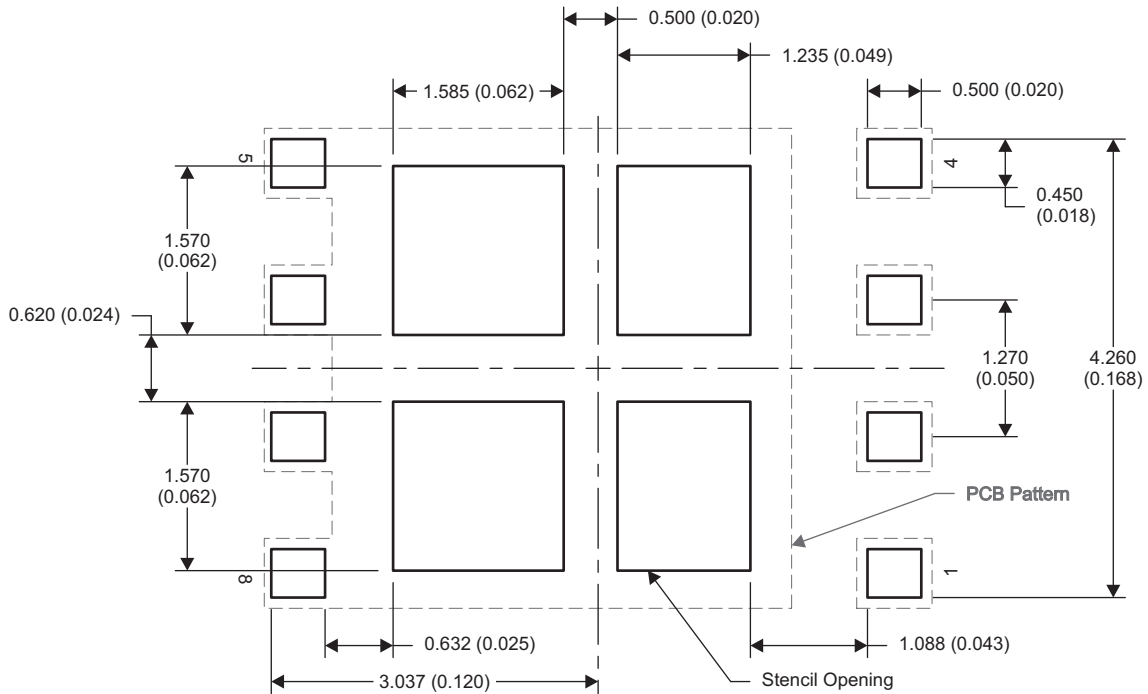
Recommended PCB Pattern



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NOTE: Dimensions are in mm (inches).

Stencil Recommendation

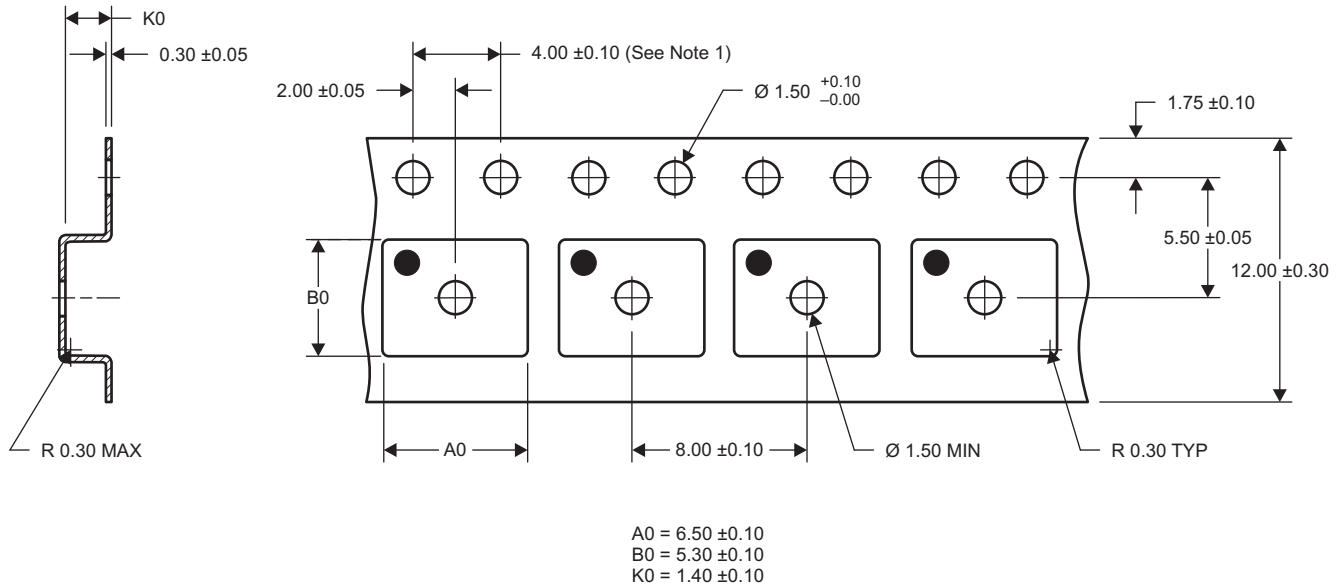


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NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5A Tape and Reel Information



M0138-01

- NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17501Q5A	SON	DQJ	8	2500	330.2	12.4	6.5	5.3	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17501Q5A	SON	DQJ	8	2500	347.0	342.0	55.0

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