

SSC Clock Generator/Buffer

FEATURES

- Part of a Family of Easy to use Clock Generator Devices With Optional SSC
- SSC Capable Clock Generator / Buffer
- SSC Controllable via 3 External Pins
 - $\pm 0\%$ to $\pm 1.5\%$ Center Spread
- 1 External Control Pin for SSC ON / OFF Selection
- 40 MHz to 108 MHz Single-Ended LVCMOS Input
- Single 3.3V Device Power Supply
- Wide Temperature Range – 40°C to 85°C
- Low Space Consumption by 8 Pin TSSOP Package

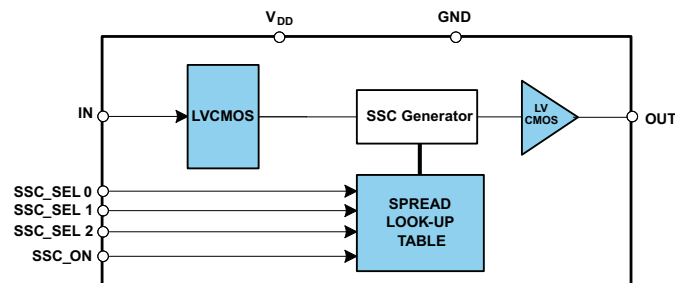
APPLICATIONS

- Consumer and Industrial Applications Requiring EMI Reduction through Spread Spectrum Clocking

PACKAGE

IN	1	8	VDD
SSC_SEL 0	2	7	SSC_SEL 2
SSC_SEL 1	3	6	OUT
GND	4	5	SSC_ON

BLOCK DIAGRAM



DESCRIPTION

The CDCS501 is a spread spectrum capable, LVCMOS Input Clock Buffer for EMI reduction.

The device is designed to counter common EMI problems in modern electronic designs.

It accepts a 3.3V LVCMOS signal at the input and spread this signal by a small amount, centered around the input frequency. The amount of spread can be selected via 3 control pins. The Functional Table contains detailed information on the amount of spread. A 4th control pin can be used to activate or deactivate the Spread Spectrum Clock Generator.

Selecting SSC_ON = off will turn the Spread Spectrum Clock Generator off only. The device will still pass the LVCMOS signal that's presented at its input through to its output. This pin is low active.

The wide operating frequency range covers most commonly used midrange Audio and Video frequencies. The CDCS501 operates in 3.3V environment.

It is characterized for operation from –40°C to 85°C, and available in an 8-pin TSSOP package.



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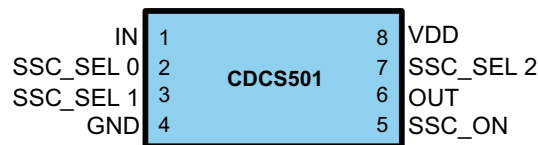
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION TABLE

SSC_ON	SSC_SEL 0	SSC_SEL 1	SSC_SEL 2	SPREAD AMOUNT
1	x	x	X	0.00%
0	0	0	0	1.00%
0	0	0	1	1.50%
0	0	1	0	1.00%
0	0	1	1	1.50%
0	1	0	0	0.50%
0	1	0	1	0.75%
0	1	1	0	0.00%
0	1	1	1	0.50%

DEVICE INFORMATION

PACKAGE



PIN FUNCTIONS

PIN			
NAME	NO.	Type	Description
IN	1	I	LVC MOS Clock Input
OUT	6	O	LVC MOS Clock Output
SSC_SEL 0, 1, 2	2, 3, 7	I	Spread Selection Pins, internal Pull-up
SSC_ON	5	I	SSC on/off Pin, active low; internal Pull-down
VDD	8	Power	3.3V Power Supply
GND	4	Ground	Ground

PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE⁽¹⁾

CDCS501PW 8-PIN TSSOP			THERMAL AIRFLOW (CFM)				UNIT
			0	150	250	500	
R _{θJA}	High K		149	142	138	132	°C / W
	Low K		230	185	170	150	
R _{θJc}	High K	65					°C / W
	Low K	69					

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 4.6	V
V_{IN}	Input voltage range	–0.5 to 4.6	V
V_{out}	Output voltage range	–0.5 to 4.6	V
I_{IN}	Input current ($V_I < 0$, $V_I > V_{DD}$)	20	mA
I_{out}	Continuous output current	50	mA
T_{ST}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.0		3.6	V
f_{IN}	Input Frequency	40		108	MHz
V_{IL}	Low level input voltage LVCMOS			0.3 V_{DD}	V
V_{IH}	High level input voltage LVCMOS	0.7 V_{DD}			V
V_I	Input Voltage threshold LVCMOS		0.5 V_{DD}		V
C_L	Output Load Test LVCMOS			15	pF
I_{OH}/I_{OL}	Output Current			12	mA
T_A	Operating free-air temperature	–40		85	°C

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Device supply current	$f_{IN} = 80 \text{ MHz}$		26		mA
f_{OUT}	Output frequency		40		108	MHz
I_{IH}	LVC MOS input current	$V_I = V_{DD}; V_{DD} = 3.6V$			10	μA
I_{IL}	LVC MOS input current	$V_I = 0 \text{ V}; V_{DD} = 3.6V$			-10	μA
V_{OH}	LVC MOS high-level output voltage	$I_{OH} = -0.1mA$	2.9			V
		$I_{OH} = -8mA$	2.4			
		$I_{OH} = -12mA$	2.2			
V_{OL}	LVC MOS low-level output voltage	$I_{OL} = 0.1mA$			0.1	V
		$I_{OL} = 8mA$			0.5	
		$I_{OL} = 12mA$			0.8	
$t_{JIT(C-C)}$	Cycle to cycle jitter cycles	$f_{out} = 80 \text{ MHz}; SSC = 1\%, 10000 \text{ cycles}$		110		ps
t_r/t_f	Rise and fall time	20%–80%		0.75		ns
O_{dc}	Output duty cycle		45%		55%	
f_{MOD}	Modulation frequency			30		kHz

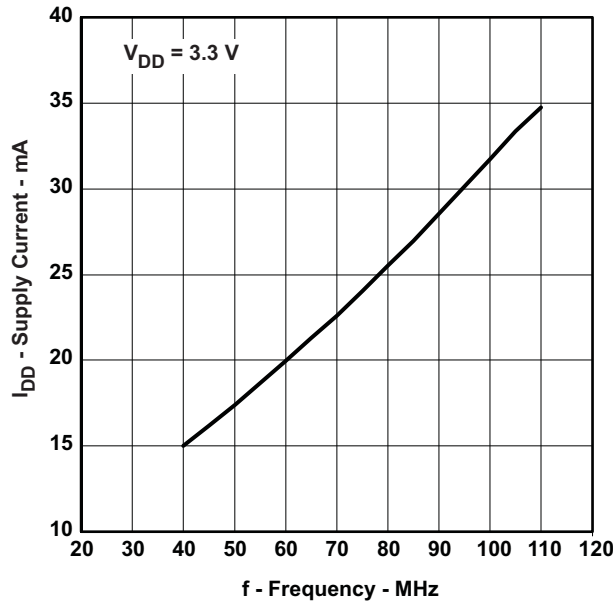


Figure 1. I_{DD} vs. Input Frequency, $V_{DD} = 3.3V$

APPLICATION INFORMATION

SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS501 uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using the below formula.

$$f_{\text{mod}} = f_{\text{IN}} / 2480$$

PARAMETER MEASUREMENT INFORMATION

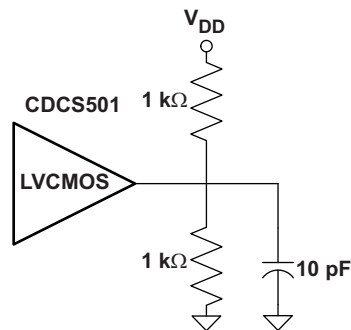


Figure 2. Test Load

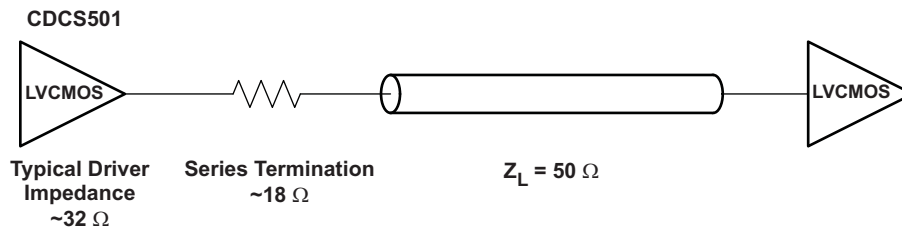


Figure 3. Test Load for 50-Ω Board Environment

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDCS501PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDCS501PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCS501PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCS501PWR	TSSOP	PW	8	2000	346.0	346.0	29.0

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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