

# CD4051B-Q1, CD4052B-Q1, CD4053B-Q1 CMOS ANALOG MULTIPLEXERS/DEMULPLEXERS WITH LOGIC-LEVEL CONVERSION

SCHS354A – AUGUST 2004 – REVISED JANUARY 2008

## Features

- Qualified for Automotive Applications
- Wide Range of Digital and Analog Signal Levels
  - Digital: 3 V to 20 V
  - Analog:  $\leq 20 V_{P-P}$
- Low ON Resistance, 125  $\Omega$  (Typ) Over 15  $V_{P-P}$  Signal Input Range for  $V_{DD} - V_{EE} = 18 V$
- High OFF Resistance, Channel Leakage of  $\pm 100 pA$  (Typ) at  $V_{DD} - V_{EE} = 18 V$
- Logic-Level Conversion for Digital Addressing Signals of 3 V to 20 V ( $V_{DD} - V_{SS} = 3 V$  to 20 V) to Switch Analog Signals to 20  $V_{P-P}$  ( $V_{DD} - V_{EE} = 20 V$ )
- Matched Switching Characteristics,  $r_{on} = 5 \Omega$  (Typ) for  $V_{DD} - V_{EE} = 15 V$

- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2  $\mu W$  (Typ) at  $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10 V$
- Binary Address Decoding on Chip
- 5-V, 10-V, and 15-V Parametric Ratings
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1  $\mu A$  at 18 V Over Full Package Temperature Range, 100 nA at 18 V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

## Applications

- Analog and Digital Multiplexing and Demultiplexing
- Analog-to-Digital (A/D) and Digital-to-Analog (D/A) Conversion
- Signal Gating

## description/ordering information

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches that have low ON impedance and very low OFF leakage current. Control of analog signals up to 20  $V_{P-P}$  can be achieved by digital signal amplitudes of 4.5 V to 20 V (If  $V_{DD} - V_{SS} = 3 V$ , a  $V_{DD} - V_{EE}$  of up to 13 V can be controlled; for  $V_{DD} - V_{EE}$  level differences above 13 V, a  $V_{DD} - V_{SS}$  of at least 4.5 V is required). For example, if  $V_{DD} = 4.5 V$ ,  $V_{SS} = 0 V$ , and  $V_{EE} = -13.5 V$ , analog signals from  $-13.5 V$  to 4.5 V can be controlled by digital inputs of 0 V to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full  $V_{DD} - V_{SS}$  and  $V_{DD} - V_{EE}$  supply-voltage ranges, independent of the logic state of the control signals. When a logic high (H) is present at the inhibit (INH) input, all channels are off.

## ORDERING INFORMATION†

$T_A$	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – M	Reel of 2500	CD4051BQM96Q1	CD4051Q
	TSSOP – PW	Reel of 2000	CD4051BQPWRQ1	CM051BQ
	SOIC – M	Reel of 2500	CD4052BQM96Q1§	CD4052Q
	TSSOP – PW	Reel of 2000	CD4052BQPWRQ1§	CD4052Q
	SOIC – M	Reel of 2500	CD4053BQM96Q1	CD4053Q
	TSSOP – PW	Reel of 2000	CD4053BQPWRQ1§	CD4053Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

§ Product Preview



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 **TEXAS  
INSTRUMENTS**

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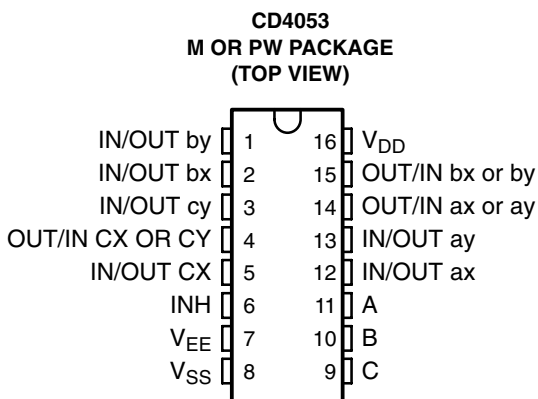
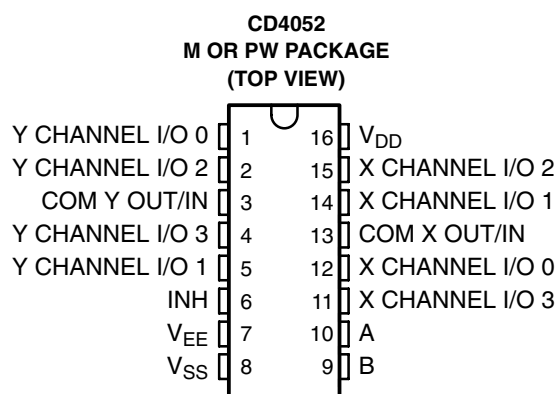
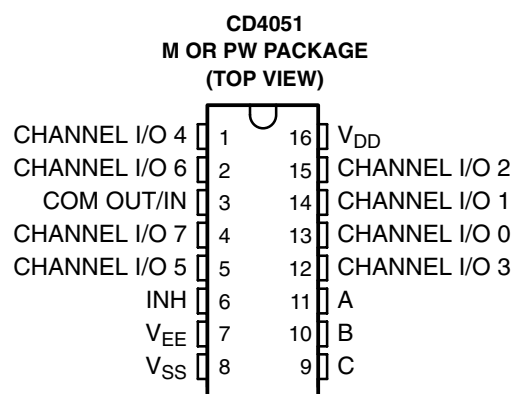
## description/ordering information (continued)

The CD4051B is a single eight-channel multiplexer that has three binary control inputs (A, B, and C) and an inhibit input. The three binary signals select one of eight channels to be turned on and connect one of the eight inputs to the output.

The CD4052B is a differential four-channel multiplexer that has two binary control inputs (A and B) and an inhibit input. The two binary input signals select one of four pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple two-channel multiplexer with three separate digital control inputs (A, B, and C) and an inhibit input. Each control input selects one of a pair of channels, which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs, and the common (COM OUT/IN) terminals are the inputs.



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**Function Tables**

**CD4051**

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	X	X	X	None

X = don't care

**CD4052**

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	0x, 0y
L	L	H	1x, 2y
L	H	L	2x, 2y
L	H	H	3x, 3y
H	X	X	None

X = don't care

**CD4053**

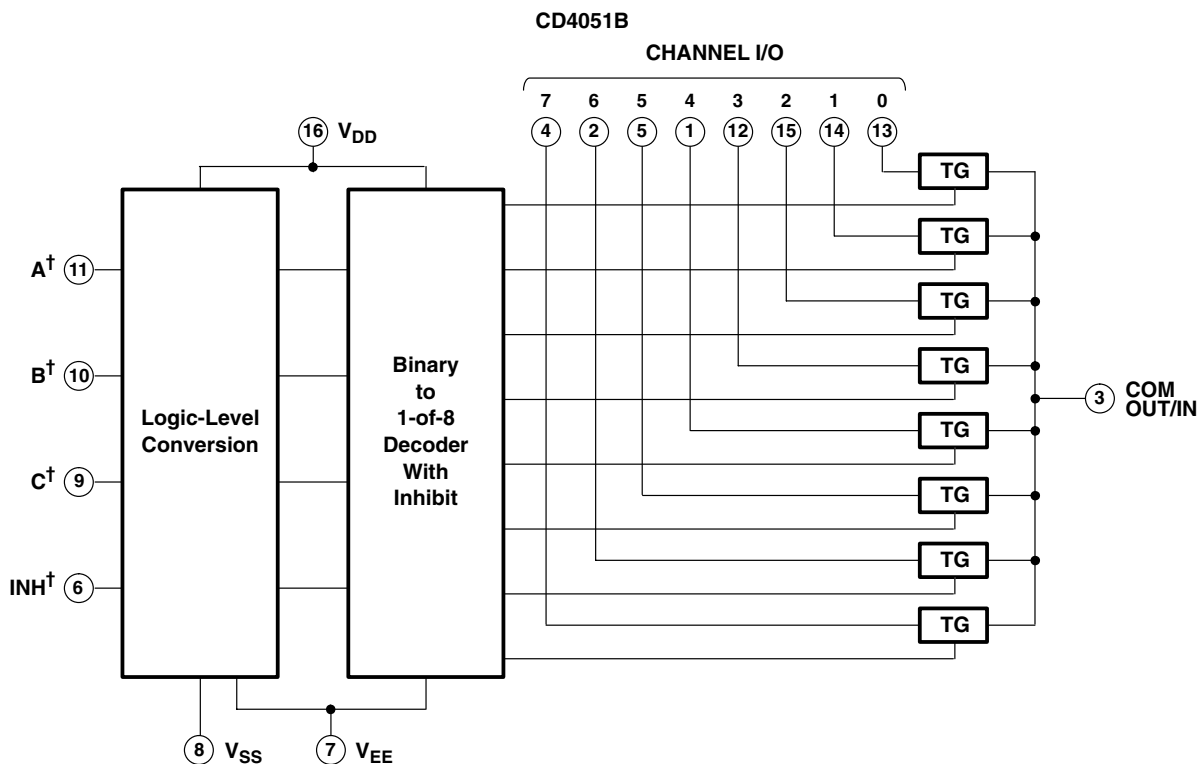
INPUTS		ON CHANNEL
INH	A OR B OR C	
L	L	ax or bx or cx
L	H	ay or by or cy
H	X	None

X = don't care

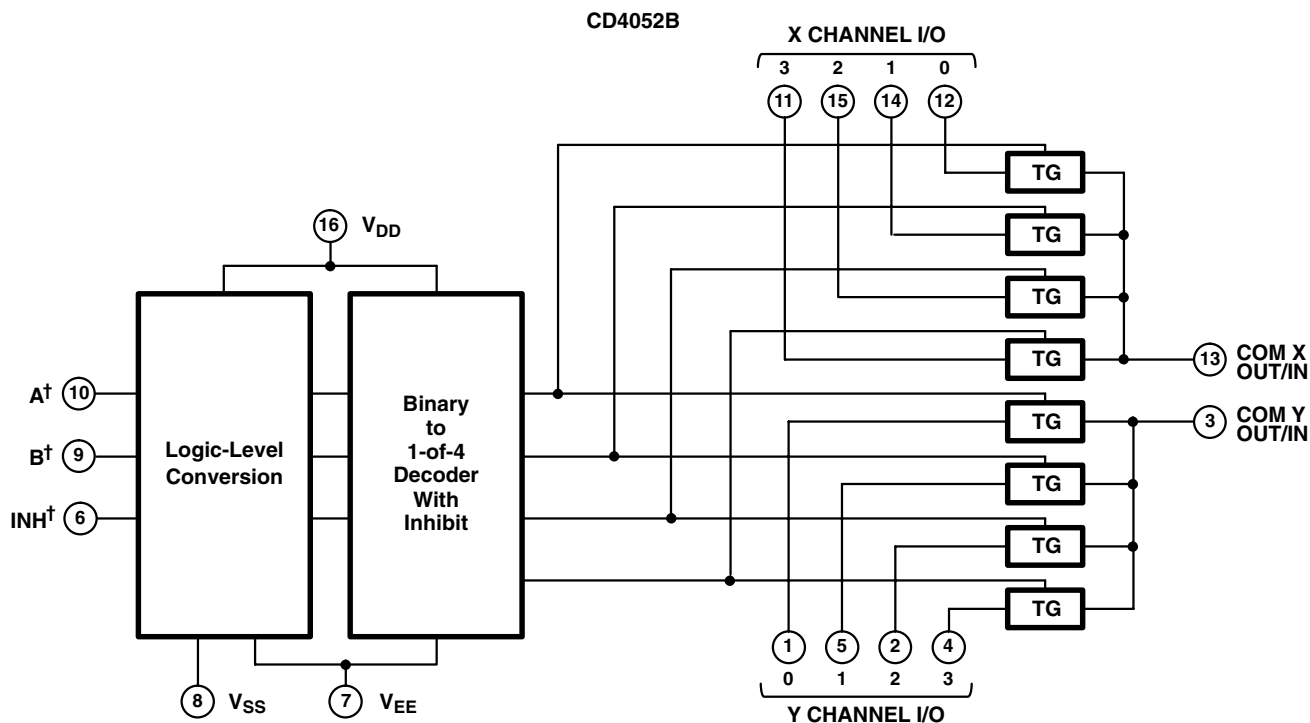
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## logic diagram (positive logic)



† All inputs are protected by CMOS protection network.



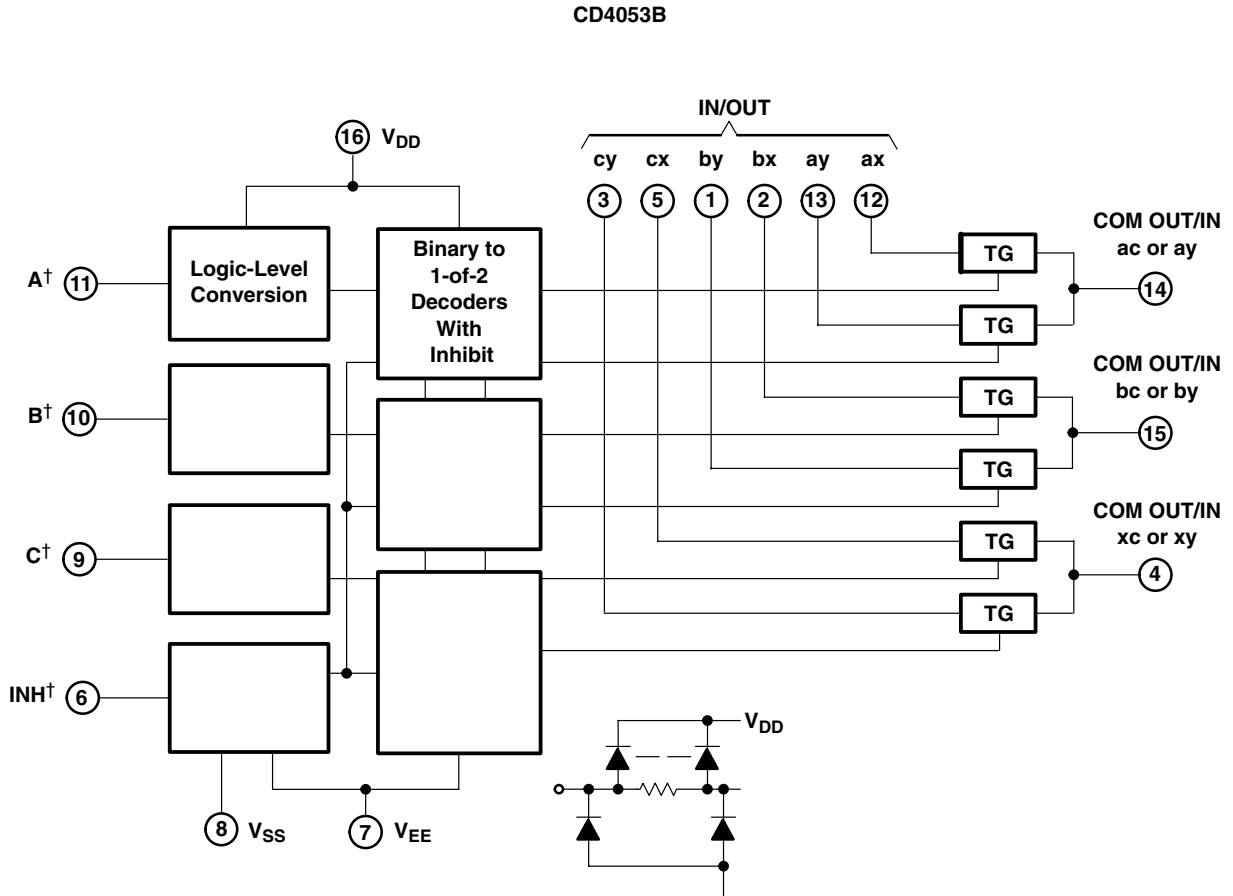
† All inputs are protected by CMOS protection network.



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## logic diagrams (positive logic) (continued)



† All inputs are protected by standard CMOS protection network.

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage range, V <sub>+</sub> to V <sub>-</sub> (voltages referenced to V <sub>SS</sub> terminal)	-0.5 to 20 V
DC input voltage range	-0.5 V to V <sub>DD</sub> + 0.5 V
DC input current, any one input	±10 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 1): M package	73°C/W
PW package	108°C/W
Maximum junction temperature, T <sub>J</sub>	150°C
Lead temperature (during soldering):	
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max	265°C
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions

		MIN	MAX	UNIT
$V_{DD}$	Supply voltage	5	20	V
$T_A$	Operating free-air temperature	-40	125	°C

electrical characteristics,  $V_{SUPPLY} = \pm 5\text{ V}$ ,  $A_V = 1\text{ V}$ ,  $R_L = 100\ \Omega$ , unless otherwise noted (see Note 2)

PARAMETER	TEST CONDITIONS	$V_{DD}$ (V)	LIMITS AT INDICATED TEMPERATURES				UNIT
			-40°C	125°C	25°C		
					MIN	TYP	
$I_{DD}$ Quiescent device current		5	5	150	0.04	5	$\mu\text{A}$
		10	10	300	0.04	10	
		15	20	600	0.04	20	
		20	100	3000	0.08	100	
<b>Signal Input (<math>V_{IS}</math>) and Output (<math>V_{OS}</math>)</b>							
$r_{on}$ Drain-to-source ON-state resistance	$V_{EE} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $V_{IS} = 0\text{ to }V_{DD}$	5	850	1300	470	1050	$\Omega$
		10	330	550	180	400	
		15	210	320	125	240	
$\Delta r_{on}$ ON-state resistance difference between any two switches	$V_{EE} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$	5			15		$\Omega$
		10			10		
		15			5		
Input/output leakage current (switch off)	Any channel OFF (MAX) or all channels OFF (COM OUT/IN) (Max), $V_{EE} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , See Note 3	18	$\pm 0.1$	$\pm 1$	$\pm 10^{-5}$	$\pm 0.1$	$\mu\text{A}$
$C_{is}$ Input capacitance	$V_{EE} = -5\text{ V}$ , $V_{SS} = -5\text{ V}$	5			5		pF
$C_{os}$ Output capacitance	$V_{EE} = -5\text{ V}$ , $V_{SS} = -5\text{ V}$	CD4051			30		pF
		CD4052	5			18	
		CD4053				9	
$C_{ios}$ Feedthrough capacitance	$V_{EE} = -5\text{ V}$ , $V_{SS} = -5\text{ V}$	5			0.2		pF
$t_{pd}$ Propagation delay (signal input to output)	$V_{IS(p-p)} = V_{DD}$ , $R_L = 200\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , $t_r, t_f = 20\text{ ns}$	5			30	60	ns
		10			15	30	
		15			10	20	

NOTES: 2. Peak-to-peak voltage symmetrical about  $\frac{V_{DD} - V_{EE}}{2}$

3. Determined by minimum feasible leakage measurement for automatic testing



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**electrical characteristics,  $V_{SUPPLY} = \pm 5\text{ V}$ ,  $A_V = 1\text{ V}$ ,  $R_L = 100\ \Omega$ , unless otherwise noted**  
**(see Note 2) (continued)**

PARAMETER	TEST CONDITIONS	$V_{EE}$ (V)	$V_{DD}$ (V)	LIMITS AT INDICATED TEMPERATURES					UNIT
				-40°C	125°C	25°C			
						MIN	TYP	MAX	
<b>Control (Address or Inhibit), <math>V_C</math></b>									
$V_{IL}$ Input low voltage	$V_{IL} = V_{DD}$ through $1\text{ k}\Omega$ , $V_{IH} = V_{DD}$ through $1\text{ k}\Omega$ , $R_L = 1\text{ k}\Omega$ to $V_{SS}$ , $I_{IS} < 2\ \mu\text{A}$ on all OFF channels	$V_{SS}$	5	1.5	1.5	1.5		V	
		$V_{SS}$	10	3	3	3			
		$V_{SS}$	15	4	4	4			
$V_{IH}$ Input high voltage	$V_{IL} = V_{DD}$ through $1\text{ k}\Omega$ , $V_{IH} = V_{DD}$ through $1\text{ k}\Omega$ , $R_L = 1\text{ k}\Omega$ to $V_{SS}$ , $I_{IS} < 2\ \mu\text{A}$ on all OFF channels	$V_{SS}$	5	3.5	3.5	3.5		V	
		$V_{SS}$	10	7	7	7			
		$V_{SS}$	15	11	11	11			
$I_{IN}$ Input current	$V_{IN} = 0\text{ V}, 18\text{ V}$		18	$\pm 0.1$	$\pm 1$	$\pm 10^{-5}$	$\pm 0.1$	$\mu\text{A}$	
$t_{pd1}$ Address-to-signal OUT (channels ON or OFF) propagation delay	$t_r, t_f = 20\text{ ns}$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$ , $V_{SS} = 0\text{ V}$ , See Figure 10, Figure 11, and Figure 14	0	5			450	720	ns	
		0	10			160	320		
		0	15			120	240		
		-5	5			225	450		
$t_{pd2}$ Inhibit-to-signal OUT (channel turning ON) propagation delay	$t_r, t_f = 20\text{ ns}$ , $C_L = 50\text{ pF}$ , $R_L = 1\text{ k}\Omega$ , $V_{SS} = 0\text{ V}$ , See Figure 11	0	5			400	720	ns	
		0	10			160	320		
		0	15			120	240		
		-10	5			200	400		
$t_{pd3}$ Inhibit-to-signal OUT (channel turning OFF) propagation delay	$t_r, t_f = 20\text{ ns}$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$ , $V_{SS} = 0\text{ V}$ , See Figure 15	0	5			200	450	ns	
		0	10			90	210		
		0	15			70	160		
		-10	5			130	300		
$C_{IN}$ Input capacitance, any address or inhibit input						5	7.5	pF	

NOTES: 2: Peak-to-peak voltage symmetrical about  $\frac{V_{DD} - V_{EE}}{2}$

3: Determined by minimum feasible leakage measurement for automatic testing

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## electrical specifications

PARAMETER	TEST CONDITIONS		V <sub>IS</sub> (V)	V <sub>DD</sub> (V)	LIMITS AT INDICATED TEMPERATURES			UNIT
					25°C			
					MIN	TYP	MAX	
-3-dB cutoff frequency, channel ON (sine-wave input)	R <sub>L</sub> = 1 kΩ, V <sub>OS</sub> at COM OUT/IN, See Note 2, V <sub>OS</sub> at COM OUT/IN	CD4053	5	10	30			MHz
		CD4052	5	10	25			
		CD4051	5	10	20			
	V <sub>EE</sub> = V <sub>SS</sub> , 20log V <sub>OS</sub> /V <sub>IS</sub> = -3 dB, V <sub>OS</sub> at any channel				60			
THD Total harmonic distortion	R <sub>L</sub> = 10 kΩ, See Note 2		2	5	0.3			%
			3	10	0.2			
			5	15	0.12			
	V <sub>EE</sub> = V <sub>SS</sub> , f <sub>is</sub> = 1-kHz sine wave				0.12			
-40-dB feedthrough frequency (all channels OFF)	R <sub>L</sub> = 1 kΩ, V <sub>OS</sub> at COM OUT/IN, See Note 2	CD4053	5	10	8			MHz
		CD4052	5	10	10			
		CD4051	5	10	12			
	V <sub>EE</sub> = V <sub>SS</sub> , 20log V <sub>OS</sub> /V <sub>IS</sub> = -40 dB, V <sub>OS</sub> at any channel				8			
-40-dB signal crosstalk frequency	R <sub>L</sub> = 1 kΩ, between any two channels, See Note 2		5	10	3			MHz
	V <sub>EE</sub> = V <sub>SS</sub> , 20log V <sub>OS</sub> /V <sub>IS</sub> = -40 dB, Between sections, Measured on common	CD4052			6			
					10			
	V <sub>EE</sub> = V <sub>SS</sub> , 20log V <sub>OS</sub> /V <sub>IS</sub> = -40 dB, Between any two sections, In pin 2, Out pin 14	CD4053			2.5			
					6			
V <sub>EE</sub> = V <sub>SS</sub> , 20log V <sub>OS</sub> /V <sub>IS</sub> = -40 dB, Between any two sections, In pin 15, Out pin 14				6				
Address or inhibit to signal crosstalk	R <sub>L</sub> = 10 kΩ, See Note 4			10	65			mV <sub>PEAK</sub>
	V <sub>EE</sub> = 0 V, V <sub>SS</sub> = 0 V, t <sub>r</sub> , t <sub>f</sub> = 20 ns, V <sub>CC</sub> = V <sub>DD</sub> - V <sub>SS</sub> (square wave)				65			

NOTES: 2. Peak-to-peak voltage symmetrical about  $\frac{V_{DD} - V_{EE}}{2}$

4. Both ends of channel

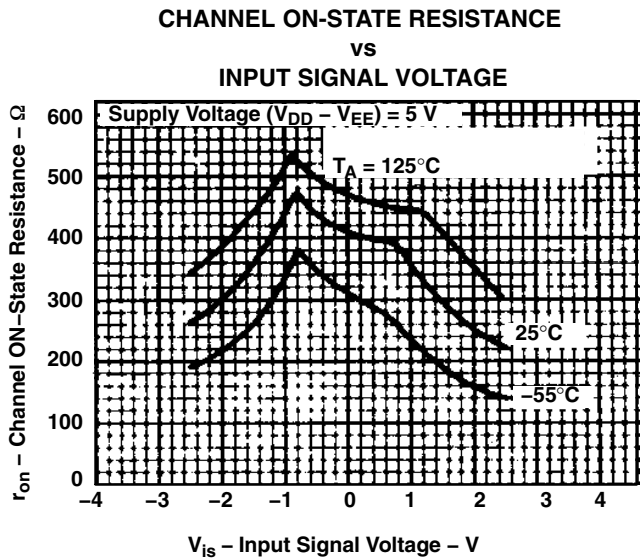




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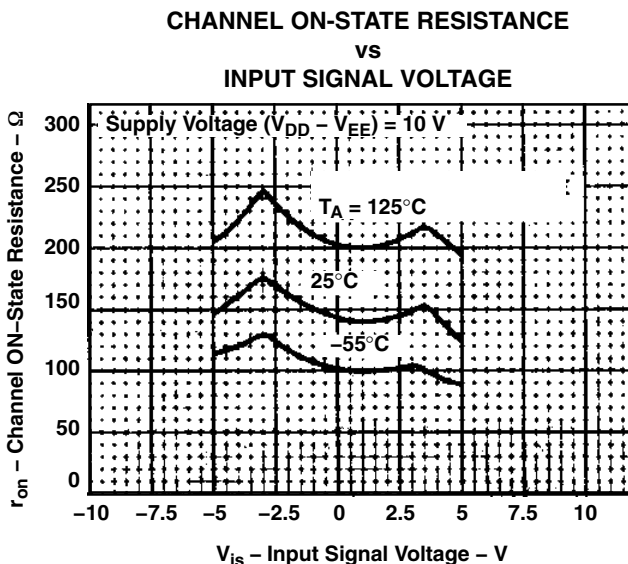
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**TYPICAL CHARACTERISTICS**



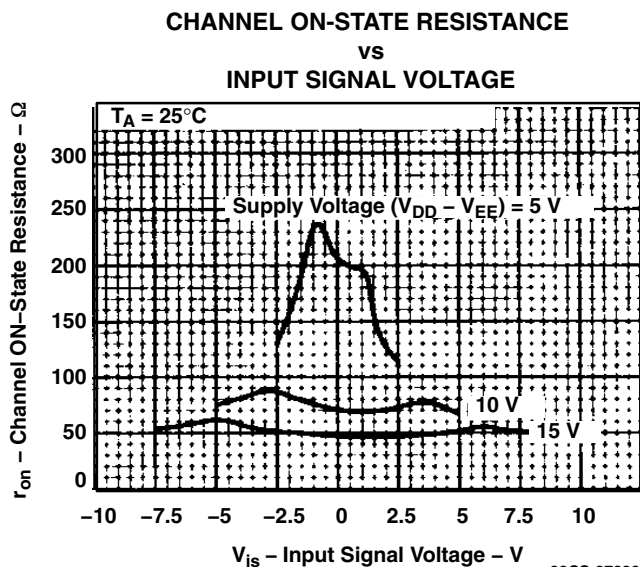
92CS-27326RI

**Figure 1**



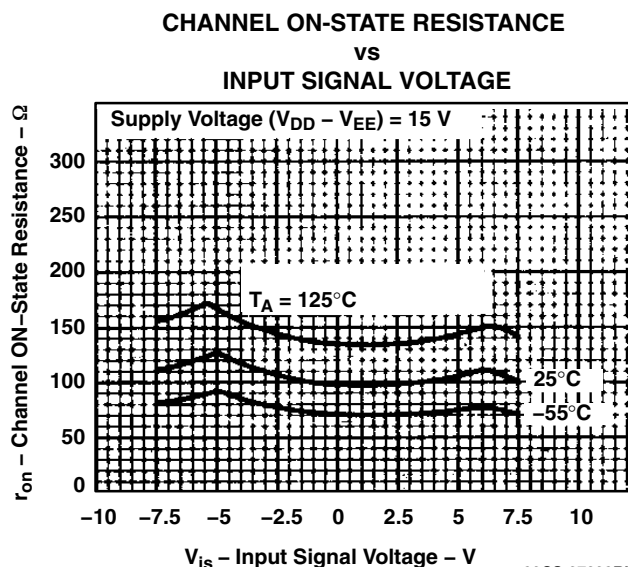
92CS-27327RI

**Figure 2**



92CS-27330RI

**Figure 3**



92CS-27329RI

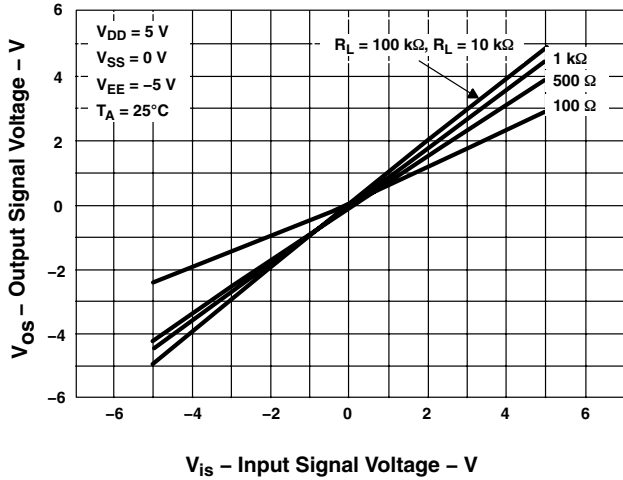
**Figure 4**

**CD4051B-Q1, CD4052B-Q1, CD4053B-Q1**  
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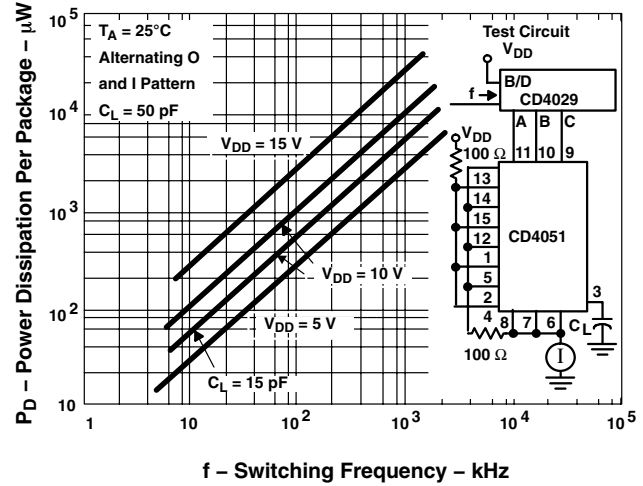
**TYPICAL CHARACTERISTICS**

**ON CHARACTERISTICS FOR  
 1-OF-8 CHANNELS (CD4051B)**



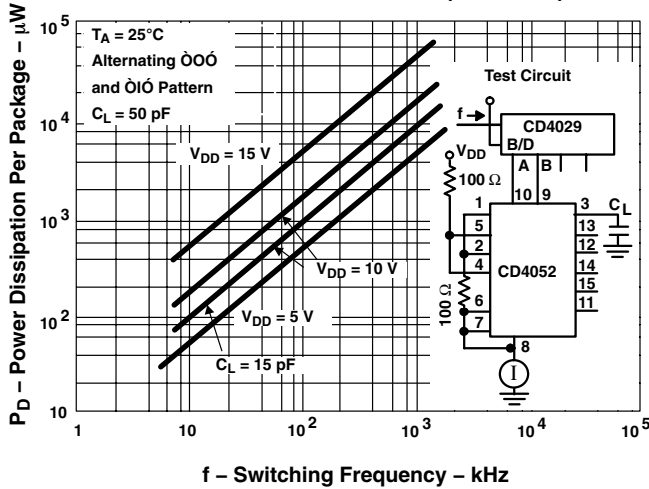
**Figure 5**

**DYNAMIC POWER DISSIPATION  
 VS  
 SWITCHING FREQUENCY (CD4051B)**



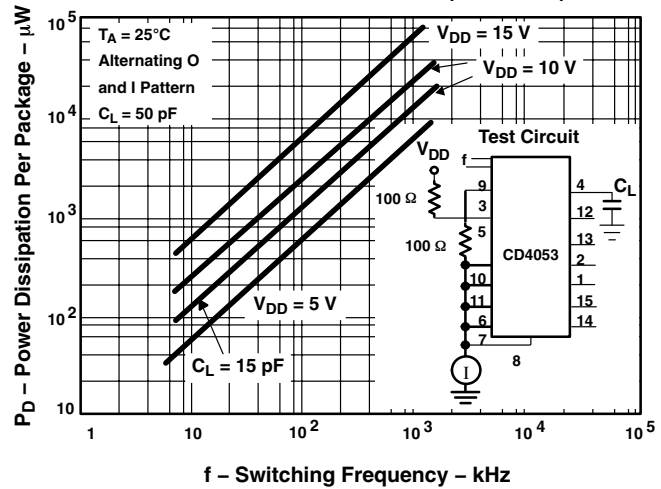
**Figure 6**

**DYNAMIC POWER DISSIPATION  
 VS  
 SWITCHING FREQUENCY (CD4052B)**



**Figure 7**

**DYNAMIC POWER DISSIPATION  
 VS  
 SWITCHING FREQUENCY (CD4053B)**



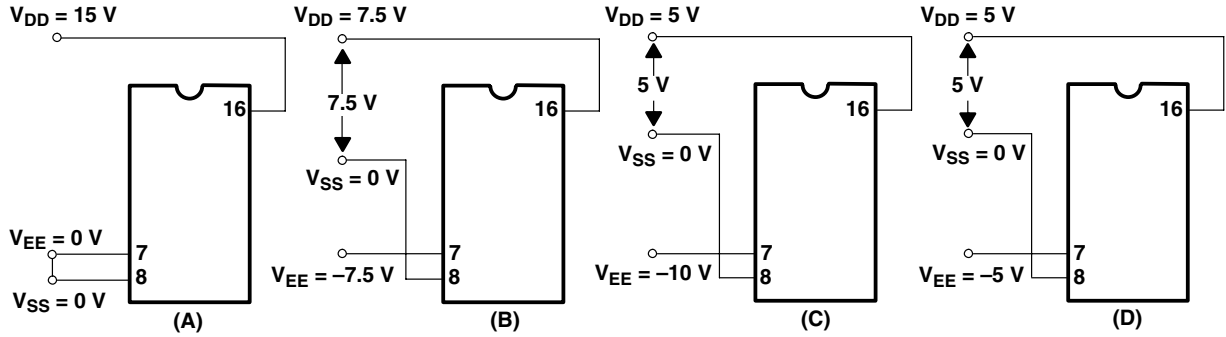
**Figure 8**



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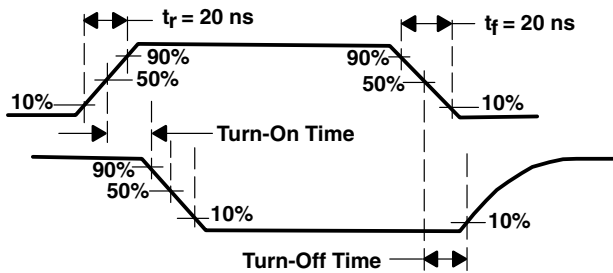
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## PARAMETER MEASUREMENT INFORMATION

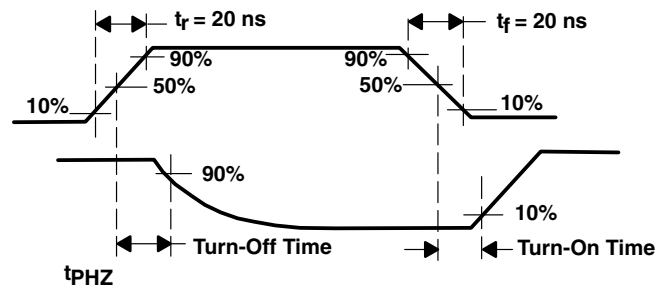


NOTE: The A, B, C, and INH input logic levels are L =  $V_{SS}$  and H =  $V_{DD}$ . The analog signal (through the TG) may swing from  $V_{EE}$  to  $V_{DD}$ .

**Figure 9. Typical Bias-Voltage Test Circuits**



**Figure 10. Channel Turned ON Waveforms  
( $R_L = 1\text{ k}\Omega$ )**

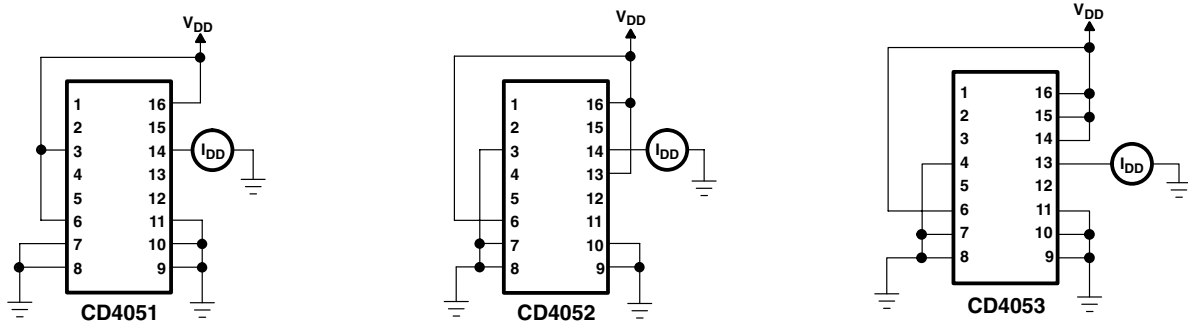


**Figure 11. Channel Turned OFF Waveforms  
( $R_L = 1\text{ k}\Omega$ )**

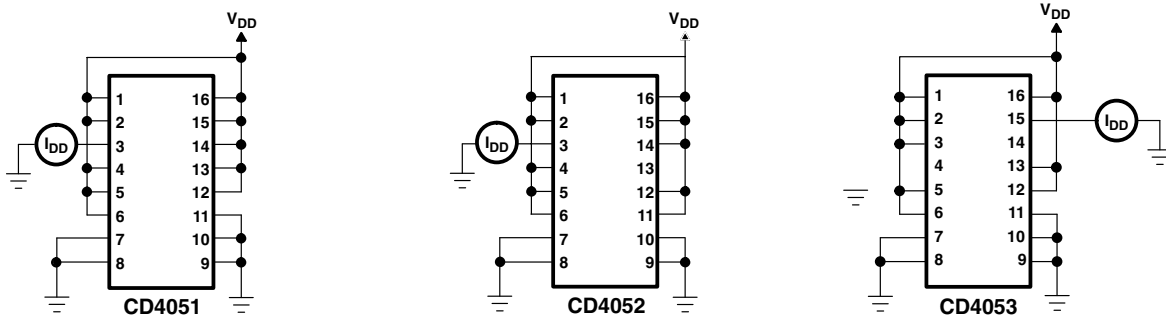
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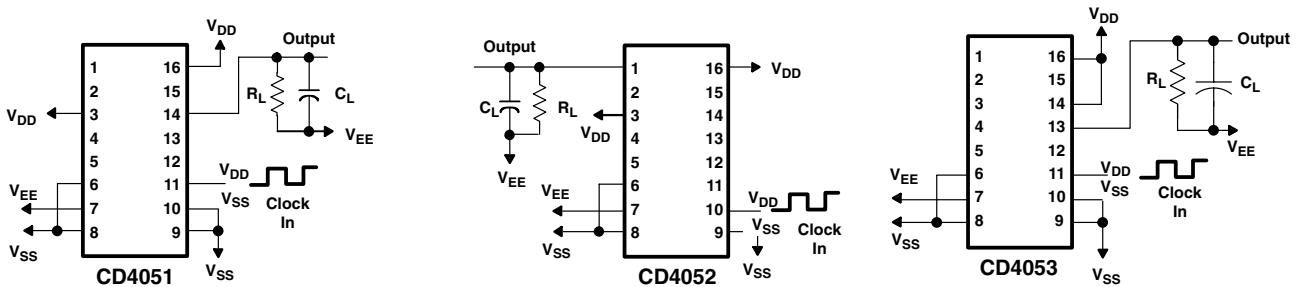
**PARAMETER MEASUREMENT INFORMATION**



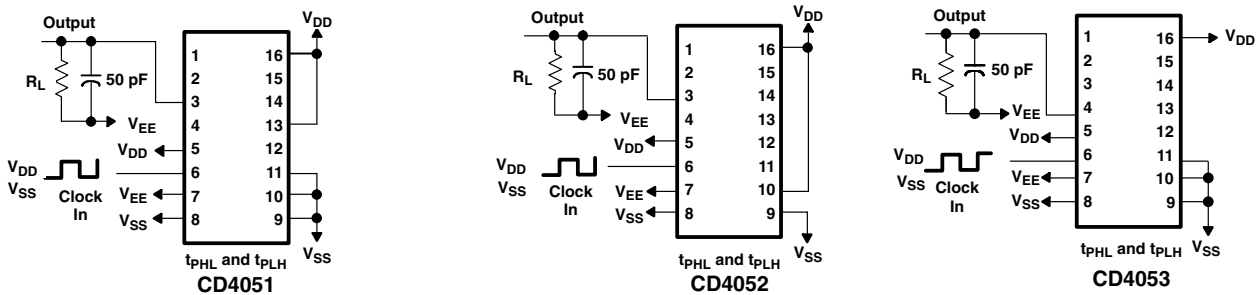
**Figure 12. OFF Channel Leakage Current, Any Channel OFF**



**Figure 13. OFF Channel Leakage Current, All Channels OFF**

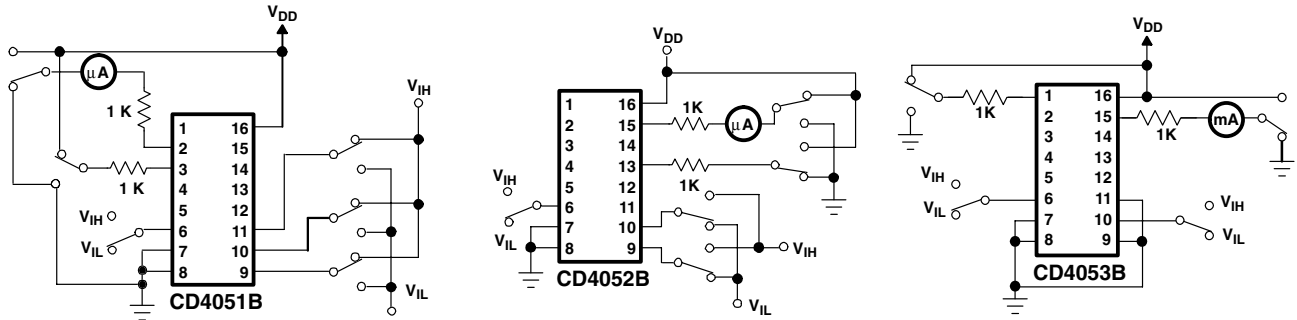


**Figure 14. Propagation Delay, Address Input to Signal Output**



**Figure 15. Propagation Delay, Inhibit Input to Signal Output**

**PARAMETER MEASUREMENT INFORMATION**

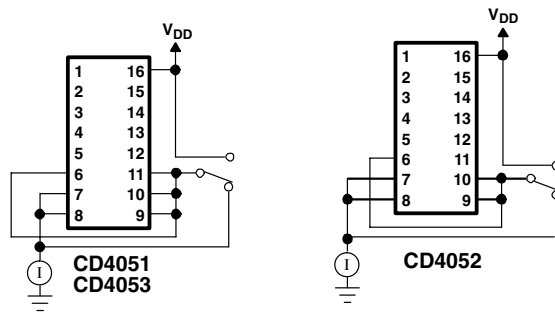


Measure <math>< 2 \mu\text{A}</math> on All OFF Channels (e.g., Channel 6)

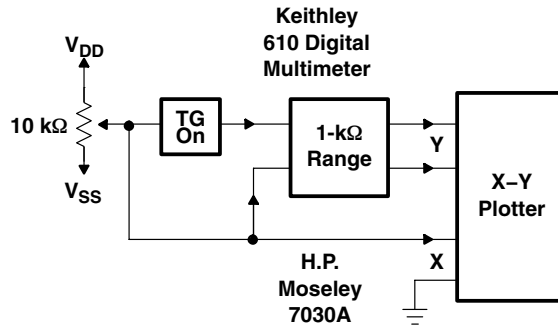
Measure <math>< 2 \mu\text{A}</math> on All OFF Channels (e.g., Channel 2x)

Measure <math>< 2 \mu\text{A}</math> on All OFF Channels (e.g., Channel by)

**Figure 16. Input-Voltage Test Circuit (Noise Immunity)**



**Figure 17. Quiescent Device Current**

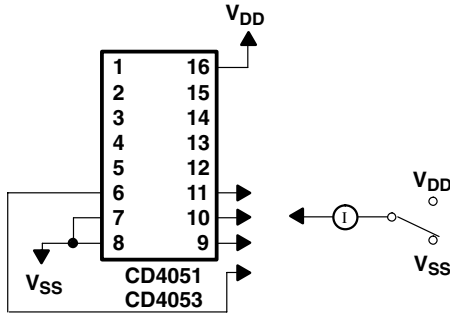


**Figure 18. Channel ON-Resistance Test Circuit**

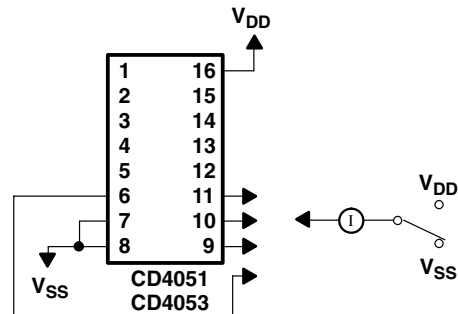
# CD4051B-Q1, CD4052B-Q1, CD4053B-Q1 CMOS ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LOGIC-LEVEL CONVERSION

SCHS354A – AUGUST 2004 – REVISED JANUARY 2008

## PARAMETER MEASUREMENT INFORMATION



NOTE: Measure inputs sequentially to both  $V_{DD}$  and  $V_{SS}$ . Connect all unused inputs to either  $V_{DD}$  or  $V_{SS}$ .



NOTE: Measure inputs sequentially to both  $V_{DD}$  and  $V_{SS}$ . Connect all unused inputs to either  $V_{DD}$  or  $V_{SS}$ .

Figure 19. Input Current

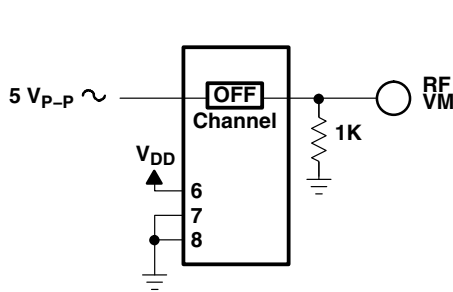


Figure 20. Feedthrough

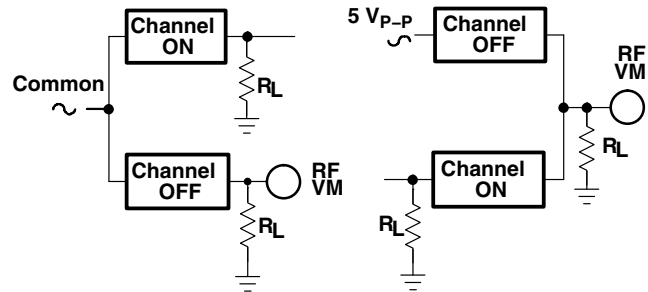


Figure 21. Crosstalk Between Any Two Channels

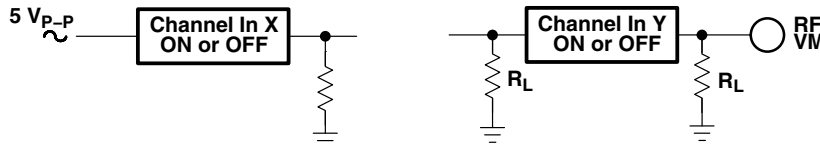


Figure 22. Crosstalk Between Duals or Triplets (CD4052B, CD4053B)

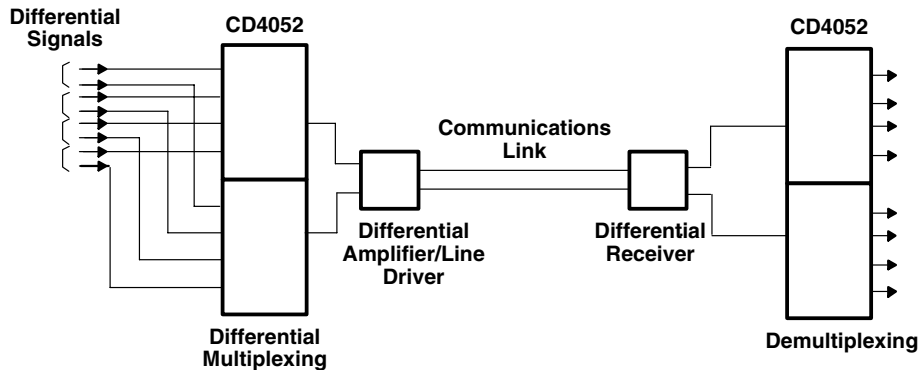


Figure 23. Typical Time-Division Application of the CD4052B

### APPLICATION INFORMATION

In applications where separate power sources drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load). This provision avoids permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the CD4051B, CD4052B, or CD4053B.

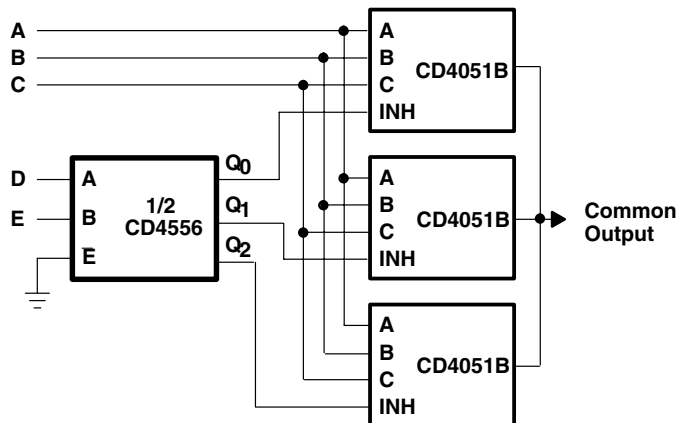


Figure 24. 24-to-1 Multiplexer Addressing

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4051BQPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM051BQ	<a href="#">Samples</a>
CD4051BQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM051BQ	<a href="#">Samples</a>
CD4053BQM96G4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4053Q	<a href="#">Samples</a>
CD4053BQM96Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4053Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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**OTHER QUALIFIED VERSIONS OF CD4051B-Q1, CD4053B-Q1 :**

- Catalog: [CD4051B](#), [CD4053B](#)
  
- Military: [CD4051B-MIL](#), [CD4053B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4051BQPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4051BQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4051BQPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4051BQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE





- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

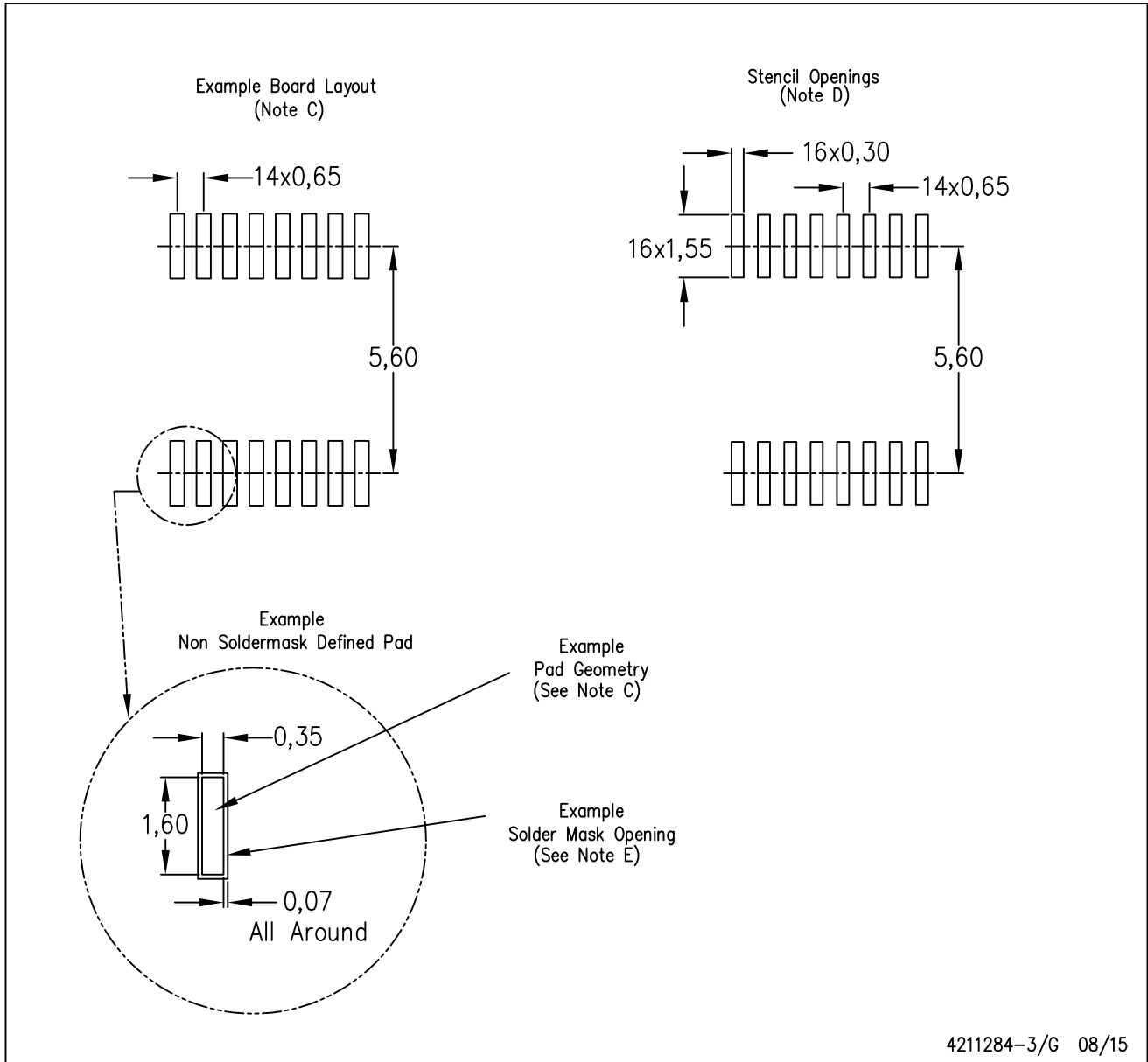
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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