CBTU02044

High-speed two-differential channels 1-to-2 switch

Rev. 1.2 — 21 April 2022 Product data sheet

1 General description

CBTU02044 is a high-speed differential 1-to-2 switching chip optimized to interface with PCIe4.0 for server and client applications. This high performance switch chip could be used for other high-speed interfaces such as PCIe-Gen4, MIPI, DP1.4, and DDR. CBTU02044 also functions as a 2-to-1 MUX by selecting 1 (Port A) as output out of one of the two differential ports (either Port B or C).

Pinouts are optimized for minimum number of layout layers and for achievement of very low crosstalk to meet stringent crosstalk requirements at higher data rate. CBTU02044 is a small package with optimized footprint for smaller real estate occupancy.

CBTU02044 is available in 1.6 mm x 2.4 mm x 0.5 mm HUQFN16 package with 0.4 mm pitch.

2 Features and benefits

- Optimized high-speed signal integrity
- Minimize crosstalk to meet stringent PCIe4.0 requirement
- Two-differential channels 1-to-2 switch/2-to-1 mux
  - Low insertion loss (typ): 0.56 dB at 100 MHz; 1.1 dB at 5 GHz; 1.5 dB at 8 GHz
  - Low off-state isolation: -70 dB at 100 MHz, -23 dB at 5 GHz, -18 dB at 8 GHz
  - Low return loss (typ): 21 dB at 2.5 GHz; 18 dB at 5 GHz; 15 dB at 8 GHz
  - Low ON-state resistance: 10 Ω (typ)
  - 3 dB bandwidth (typ): 17 GHz (typ)
  - DDNEXT < -50 dB @ 8 GHz
  - DDFEXT < -48 dB @ 8 GHz
  - VIC common mode input voltage VIC: 0 V to 2 V
  - Differential input voltage VID <1.6 V
  - Intra-pair skew <4 ps
- VDD power supply voltage range: 1.62 V to 3.63 V
- Low current consumption:
  - For active mode = 200 µA (typ)
  - For power-saving = 3 µA (typ)
- CMOS SEL and XSD pins
- Back current protection on all I/O pins of these switches
- Patent pending high performance analog pass-gate technology
- All channels support rail-to-rail input voltage (up to 2.4 V)
- HUQFN16 1.6 mm × 2.4 mm × 0.5 mm package with 0.4 mm pitch
- ESD: 2000 V HBM; 1000 V CDM
- Operating temperature range: -40 °C to +85 °C

3 Application example

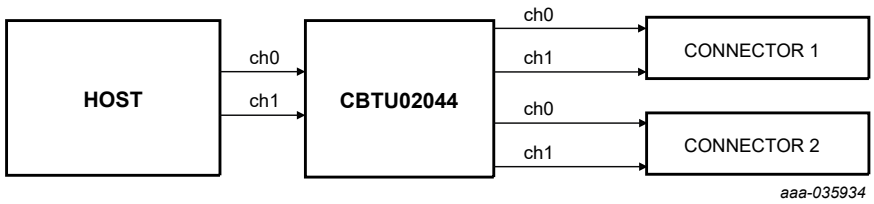


Figure 1. Application example

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
CBTU02044HE	44	HUQFN16	Plastic, super thin quad flat package; no leads; 16 terminals; body 1.6 mm x 2.4 mm x 0.5 mm; 0.4 mm pitch	SOT1832-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
CBTU02044	CBTU02044HEJ	HUQFN16	REEL 13" Q1/T1 *STANDARD MARK SMD	10000	T_{amb} = -40 °C to +85 °C

5 Block diagram

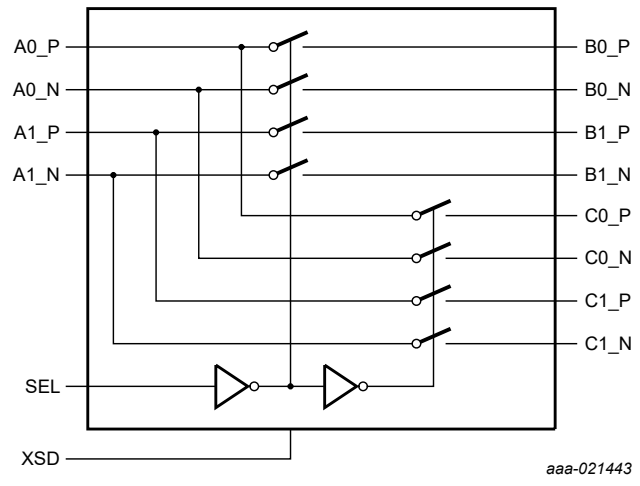


Figure 2. Block diagram

6 Pinning information

6.1 Pinning

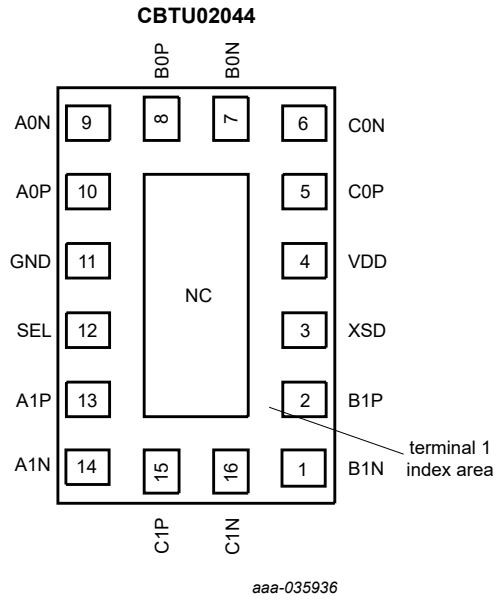


Figure 3. Pin configuration for HUQFN16 (transparent top view)

Refer to Section 11 for package related information.

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
Data path signals			
A0N	9	I/O	Ch0 input
A0P	10	I/O	
B0P	8	I/O	B0 output
B0N	7	I/O	
C0N	6	I/O	C0 output
C0P	5	I/O	
A1P	13	I/O	Ch1 input
A1N	14	I/O	
B1P	2	I/O	B1 output
B1N	1	I/O	
C1N	16	I/O	C1 output
C1P	15	I/O	
Control signal			

Table 3. Pin description...*continued*

Symbol	Pin	Type	Description
SEL	12	GPIO input	Input signal driven by GPIO When SEL = LOW, Port A and Port B are mutually connected When SEL = HIGH, port A and port C are mutually connected
XSD	3	CMOS input	Shutdown pin; should be driven LOW for normal operation. When HIGH, all paths are switched off (high impedance state). And supply current consumption is minimized.
Power supply			
VDD	4	power	Power supply range between 1.62 V and 3.63 V
Ground connection			
GND	11	ground	0 V; must connect to PCB ground
NC	center pad	not connected	Center pad is not connected to the device ground pin inside the package. Recommend to connect center pad to PCB ground

7 Functional description

Refer to Figure 2 of CBTU02044.

The CBTU02044 provides a shutdown function to minimize power consumption when the switch is not active, while the power to CBTU02044 is provided. The XSD pin (power down = HIGH) places all channels in high-impedance state while reducing current consumption to near-zero. When XSD pin is LOW, the device operates normally.

Table 4. ON/OFF control table

XSD	SEL	Function
HIGH	X	A, B and C ports are high-Z
LOW	LOW	A to B ports and vice versa
LOW	HIGH	A to C ports and vice versa

8 Limiting values

Table 5. Limiting values [1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[2]	-0.3	+4.4	V
V_I	input voltage of control pins		[2]	-0.3	+4.4	V
V_{IO}	voltage of I/O pins of switches		[2]	-0.3	+2.6	V
T_{stg}	storage temperature			-65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V
		CDM	[4]	-	1000	V

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values, except differential voltages, are with respect to network ground terminal.

[3] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[4] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9 Recommended operating conditions

Table 6. Operating conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VDD	supply voltage	3.3 V supply option		1.62	-	3.63	V
V_I	input voltage	CMOS inputs		-0.3	-	VDD	V
		switch I/O pins		-0.3	-	+2.4	V
T_{amb}	ambient operating temperature	operating in free air		-40	-	+85	°C

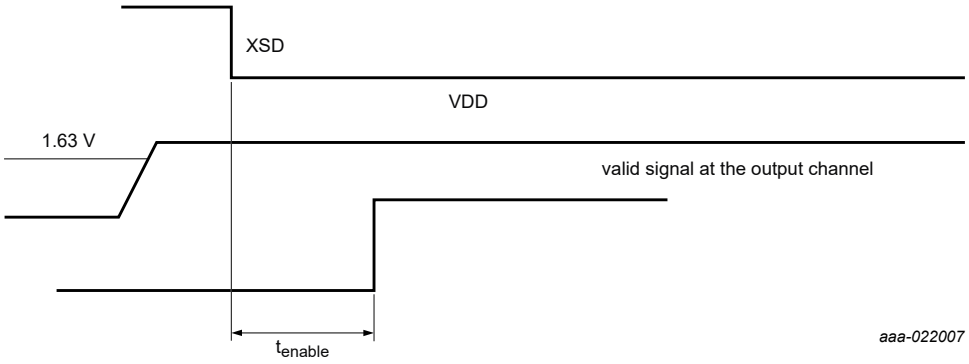
10 Characteristics

10.1 Device general characteristics

Table 7. General characteristics

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	XSD = HIGH (disable)	-	3	10	µA
		XSD = LOW (enable)	-	250	450	µA
$t_{startup}$	start-up time	supply voltage ramping up to valid with XSD = LOW to channel specified operating characteristics	-	-	30	µs
t_{en}	enable time	XSD going LOW to channel specified operating characteristics	-	90	220	µs
t_{rcfg}	reconfiguration time	SEL state changes[2]	-	18	30	ns

[1] Typical values are at VDD = 1.8 V; T_{amb} = 25 °C, and maximum loading
[2] Smooth transition without glitch



Enable time is when valid VDD is available and t = 0 starts when XSD makes transition from HIGH to LOW

Figure 4. Enable time definition

10.2 Switch channel characteristics

Table 8. Dynamic and static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DDIL	differential insertion loss	Channel is OFF					
		f = 5 GHz		-	20	-	dB
		f = 100 MHz		-	40	-	dB
		Channel is ON					
		f = 8 GHz		-	1.5	-	dB
		f = 5 GHz		-	1.1	-	dB
		f = 2.5 GHz		-	0.8	-	dB
		f = 100 MHz		-	0.56	-	dB
B_{-3dB}	bandwidth			-	17	-	GHz
DDRL	differential return loss	f = 8 GHz		-	15	-	dB
		f = 5 GHz		-	18	-	
		f = 2.5 GHz		-	21	-	dB
DDNEXT	High-Speed Differential near-end crosstalk	A0 to A1 or B0 to B1 or C0 to C1 ports					
		f = 8 GHz		-	-	-48	dB
DDFEXT	High-Speed far-end crosstalk	A to B or A to C ports (or vice versa)					
		f = 8 GHz		-	-	-46	dB
V_I	input voltage	Switch I/O pins		-0.3	-	2.4	V
V_{IC}	Common-mode input voltage	for all switch ports		0	-	2.0	V
V_{ID_PP}	Differential input voltage			-	1.2	1.6	V
I_{IH}	HIGH-level input leakage current	High-speed switch I/O; A, B and C ports; XSD = HIGH; V_I = 2.0 V		-	-	1.5	µA
I_{IL}	LOW-level input leakage current	High-speed switch I/O; A, B and C ports; XSD = HIGH; V_I = GND		-	-	1.5	µA
V_{IK}	Input negative clamping voltage	Voltage on high-speed channel pins; II = -18 mA		-	-	-1.2	V
t_{PD}	propagation delay at 8 GHz	From A port to B or C port or vice versa		-	32	35[1]	ps
t_{sk}	Intra-pair skew	Skew between P and N for all the ports		-	3	-	ps
R_{onse}	single-end ON-state resistance	Switch ON resistance with source current is 18 mA		-	10	14	Ω
Z_{input}	DC CM input impedance	XSD = HIGH and V_I > 0 V		-	3000[1]	-	KΩ
C_{in}	input capacitance at 2.5 GHz	VDD = 1.8 V; V_I = 1.4 V or floating		-	622[1]	-	fF

[1] Guaranteed by design

10.3 Control signals characteristics

Table 9. SEL input buffer characteristics

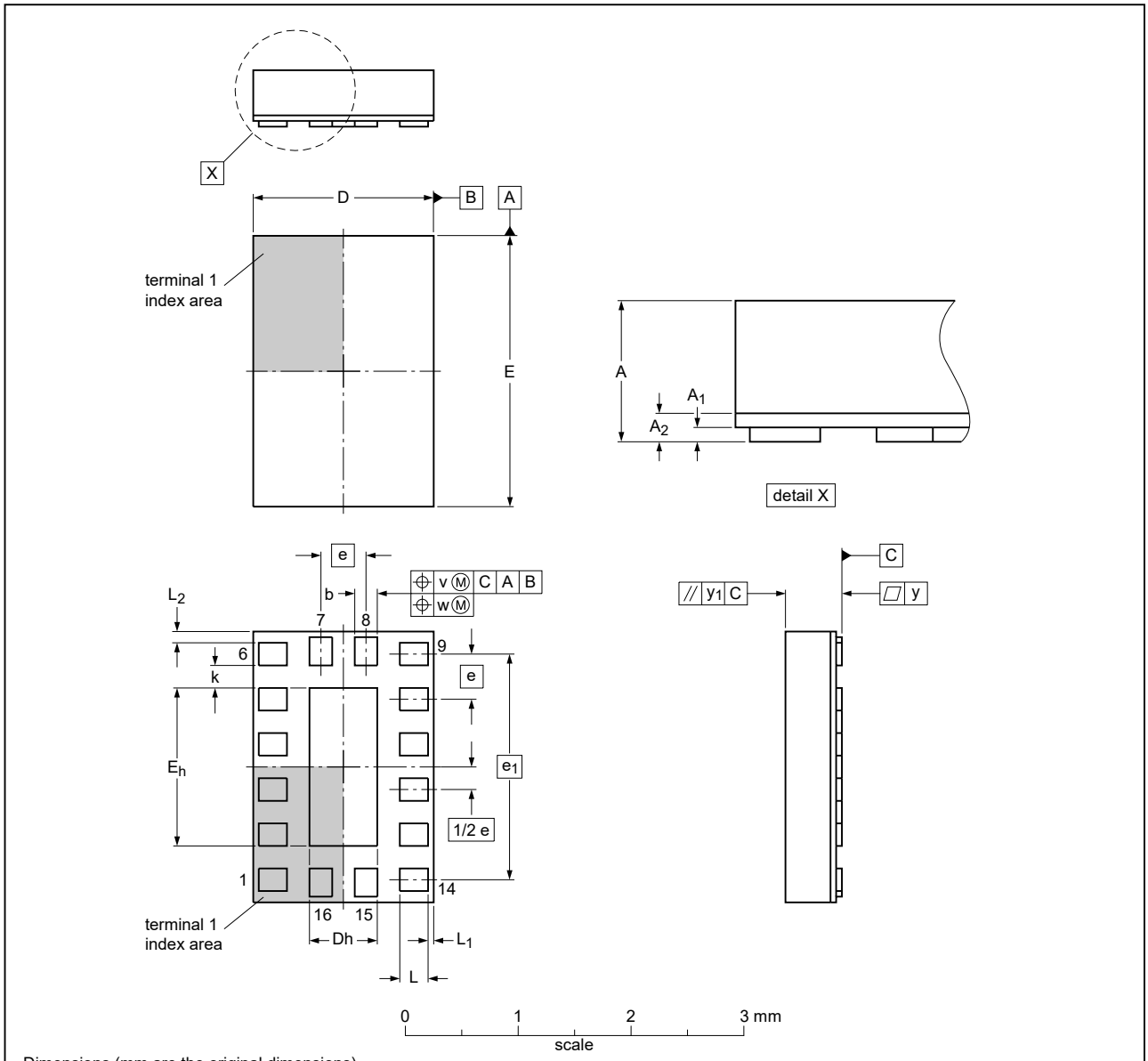
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		1.4	-	-	V
V_{IL}	LOW-level input voltage		-0.3	-	0.4	V
I_{IH}	HIGH-level input leakage current	Measured with input at V_I = VDD	-	-	1.5	µA
I_{IL}	LOW-level input leakage current	Measured with input at V_I = 0 V	-	-	1.5	µA

Table 10. XSD input buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.75 % VDD	-	-	V
V_{IL}	LOW-level input voltage		-0.3	-	0.25 % VDD	V
I_{IH}	HIGH-level input leakage current	Measured with input at V_I = VDD	-	-	1.5	µA
I_{IL}	LOW-level input leakage current	Measured with input at V_I = 0 V	-	-	1.5	µA

11 Package outline

HUQFN16: plastic thermal enhanced Ultra thin quad flat package; no leads; 16 terminals; body 2.4 x 1.6 x 0.5 mm **SOT1832-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	D_h	E	E_h	e	e_1	k	L	L_1	L_2	v	w	y	y_1
	max	0.55	0.05		0.25	1.65	0.65	2.45	1.45			0.25	0.30	0.10	0.15				
mm	nom	0.50	0.03	0.10	0.20	1.60	0.60	2.40	1.40	0.4	2.0	0.20	0.25	0.05	0.10	0.1	0.05	0.05	0.1
	min	0.45	0.00		0.15	1.55	0.55	2.35	1.35			0.15	0.20	0.01	0.05				

sot1832-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1832-1	- - -	- - -	- - -			~~16-01-21~~ 16-02-15

Figure 5. Package outline SOT1832-1 (HUQFN16)

12 Packing information

12.1 SOT1832-1 (HUQFN16); Reel pack, SMD, 13" Q1/T1 standard product orientation; Orderable part number ending ,118 or J; Ordering code (12NC) ending 118

12.1.1 Packing method

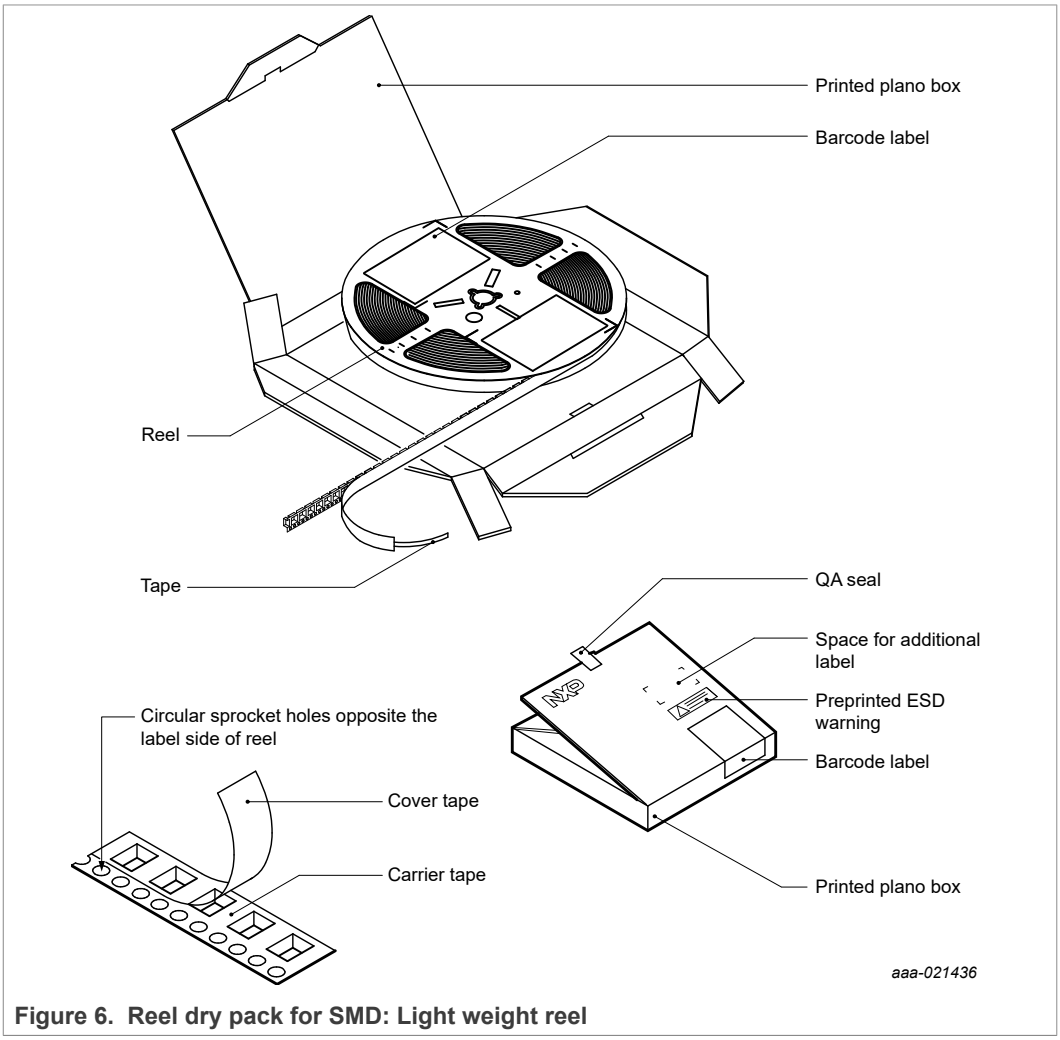


Figure 6. Reel dry pack for SMD: Light weight reel

Table 11. Dimensions and quantities

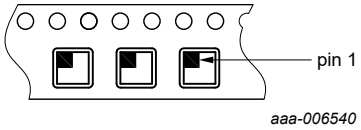
Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
330 × 8	10000	1	342 × 338 × 27

[1] d = reel diameter; w = tape width.
[2] Packing quantity dependent on specific product type.

View ordering and availability details at NXP order portal, or contact your local NXP representative.

12.1.2 Product orientation

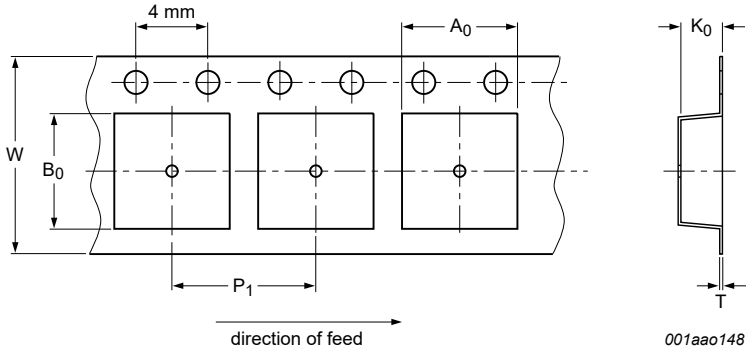
Tape pocket quadrants



Pin 1 is in quadrant Q1/T1

Figure 7. Product orientation in carrier tape

12.1.3 Carrier tape dimensions



Not drawn to scale.

Figure 8. Carrier tape dimensions

Table 12. Carrier tape dimensions

In accordance with IEC 60286-3.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
1.79 ± 0.05	2.50 ± 0.05	0.65 ± 0.05	0.23 ± 0.02	4.0 ± 0.5	8.0 ± 0.3/-0.1

12.1.4 Reel dimensions

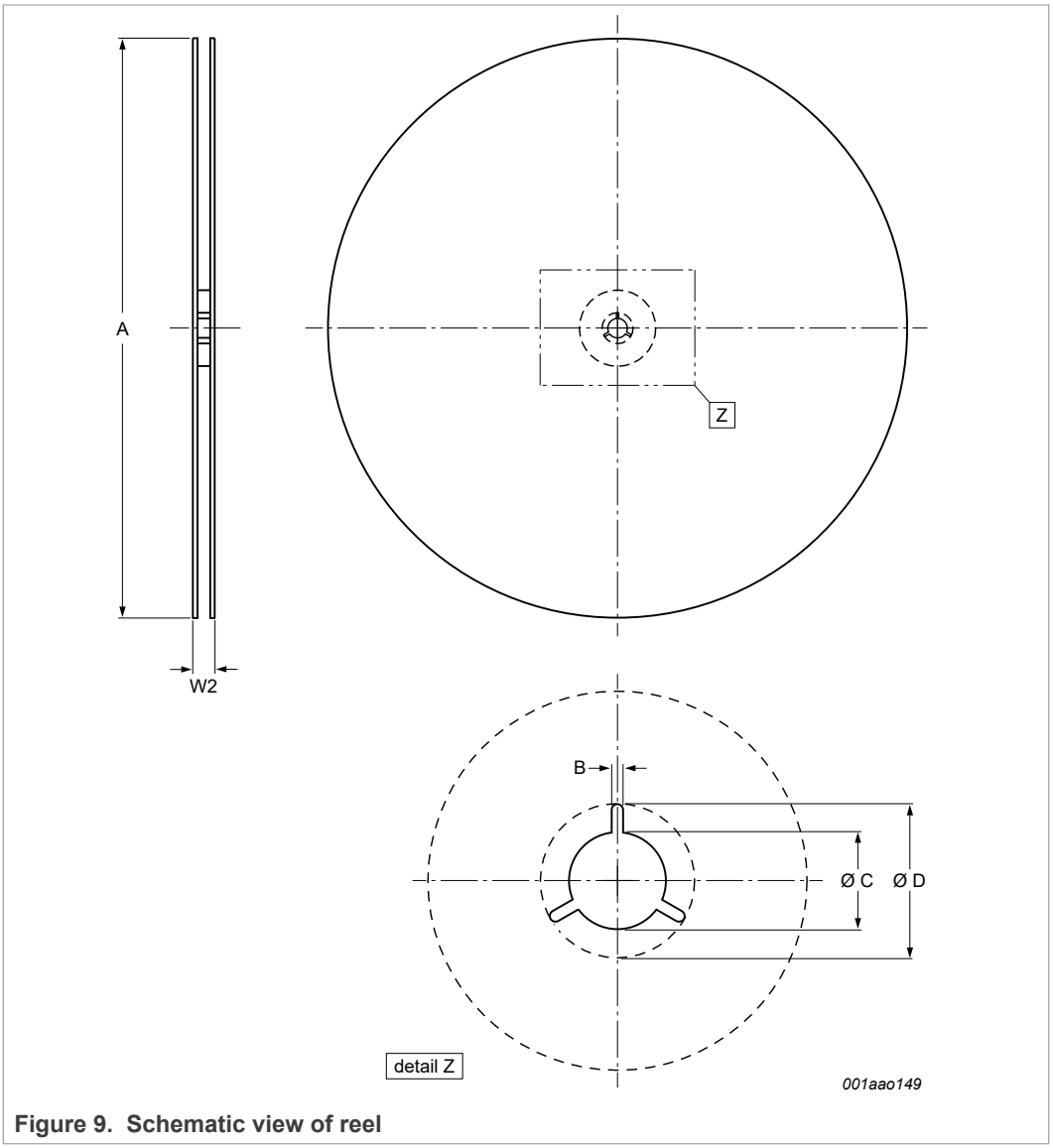


Figure 9. Schematic view of reel

Table 13. Reel dimensions

In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
330	14.4	1.5	12.8	20.2

12.1.5 Barcode label

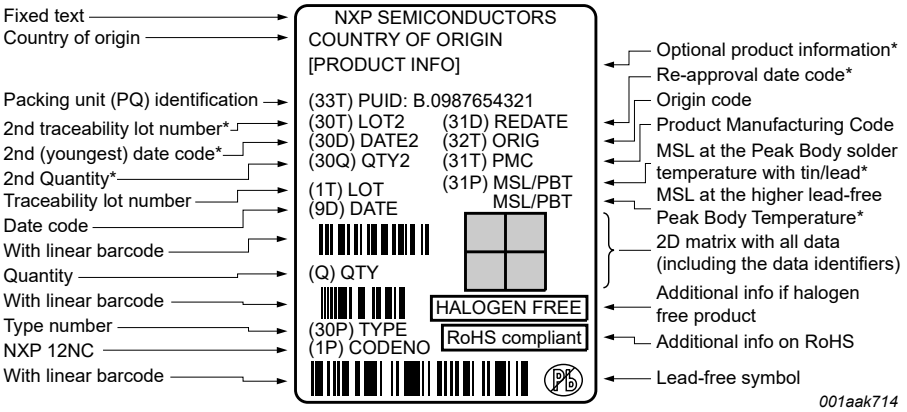


Figure 10. Example of typical box and reel information barcode label

Table 14. Barcode label dimensions

Box barcode label l × w (mm)	Reel barcode label l × w (mm)
100 × 75	36 × 75

13 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15 and Table 16

Table 15. SnPb eutectic process (from J-STD-020D)

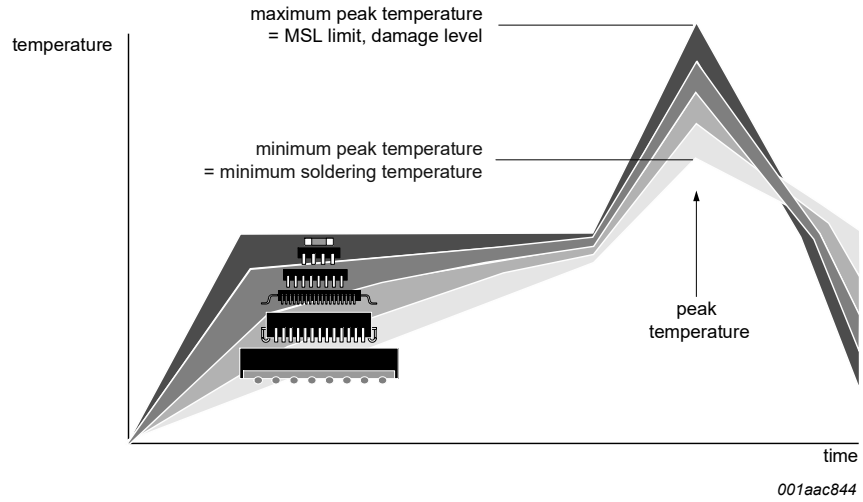
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Figure 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14 Soldering: PCB footprint

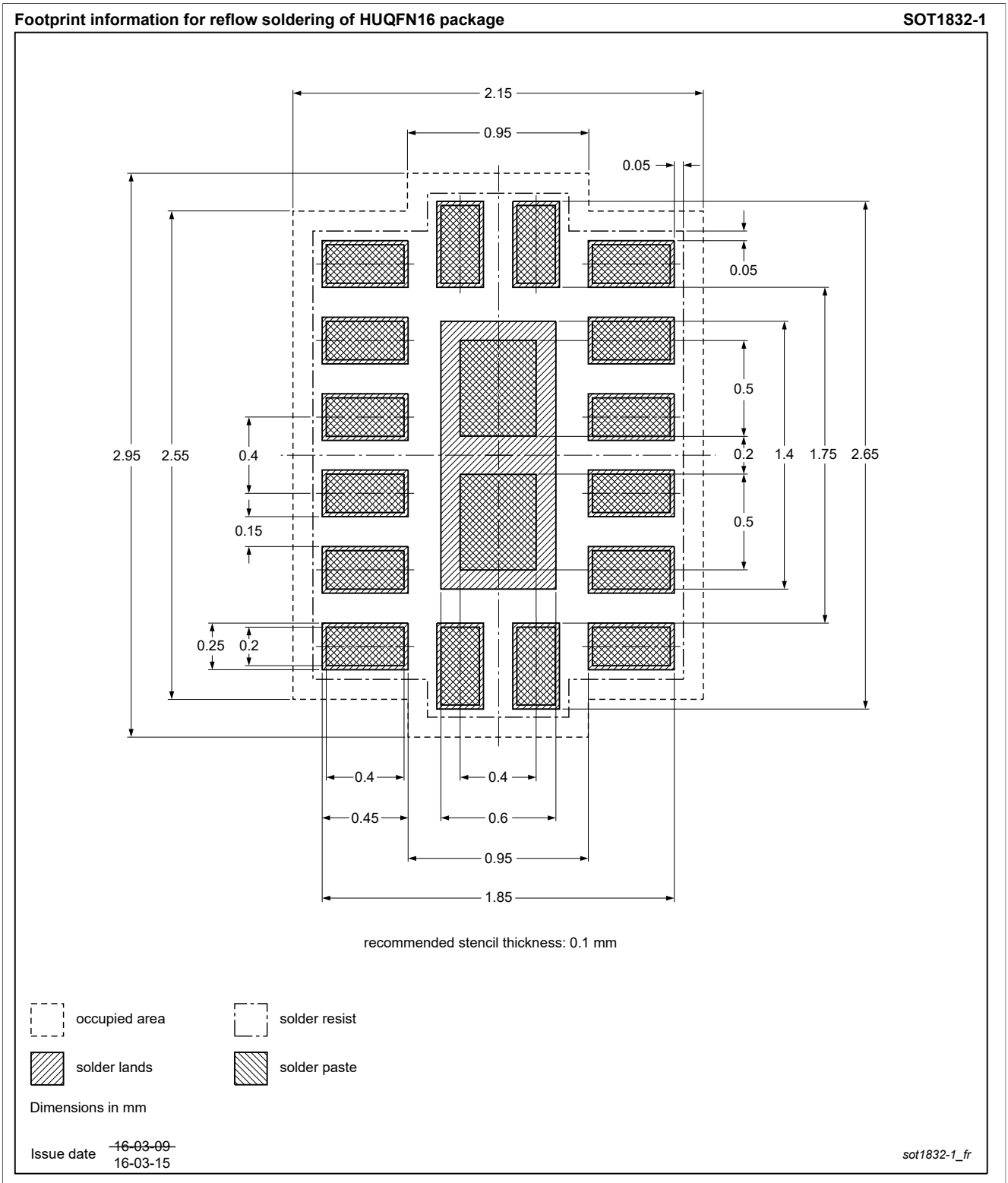


Figure 12. PCB footprint for SOT1832-1 (HUQFN16); reflow soldering

15 Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
HBM	Human Body Model
MIPI	Mobile Industry Processor Interface

16 Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTU02044 v.1.2	20220421	Product data sheet	-	CBTU02044 v.1.1
Modifications:	• Section 10.2: Removed duplicate Table 8 (Dynamic and static characteristics)			
CBTU02044 v.1.1	20210928	Product data sheet	202109024I	-
CBTU02044 v.1.0	20200427	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 21 April 2022
Document identifier: CBTU02044