

# CBTL06GP213

Second-generation high performance general purpose switch

Rev. 3.1 — 13 December 2016

Product data sheet

## 1. General description

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The CBTL06GP213 is a six-channel ('hex') multiplexer for DisplayPort, HDMI and PCI Express applications at Generation 2 ('Gen2') speeds. It provides four differential channels capable of 1 : 2 switching or 2 : 1 multiplexing bidirectional, AC-coupled PCI Express, DisplayPort signals, USB3 SuperSpeed or DC coupled TMDs signals, using high-bandwidth pass-gate technology. It provides support for high common-mode/bias voltage on the high-speed differential channels. Additionally, it provides for switching/multiplexing of the Hot Plug Detect signal as well as the AUX or DDC (Display Data Channel) signals, for a total of six channels on the display side. The AUX and DDC channels provide a four-position multiplexer such that an additional level of multiplexing can be accomplished when AUX and DDC I/Os are on separate pins of the display source device.

The CBTL06GP213 is designed for Gen2 speeds, supporting 5.0 Gbit/s for PCI Express, 5.4 Gbit/s for DisplayPort or 6 Gbit/s for HDMI 2.0. It consumes 490  $\mu$ A current (typical) in operational mode and provides a shutdown function to support battery-powered applications.

A typical application of CBTL06GP213 is on applications where one of two GPU display sources must be selected to connect to a display sink device or connector. A controller chip selects which path to use by setting a select signal HIGH or LOW. Due to the non-directional nature of the signal paths (which use high-bandwidth pass gate technology), the CBTL06GP213 can also be used in the reverse topology, for example, to connect one display source device to one of two display sink devices or connectors.

## 2. Features and benefits

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- 1 : 2 switching or 2 : 1 multiplexing of DisplayPort (v1.2 - 5.4 Gbit/s) PCI Express (v2.0 - 5.0 Gbit/s) signals, USB3 SuperSpeed or HDMI 2.0 (6 Gbit/s) TMDs signals
  - ◆ 4 high-speed differential channels with 2 : 1 muxing/switching for DisplayPort or PCI Express or HDMI signals
  - ◆ 1 channel with 4 : 1 or 4 : 2 muxing/switching for AUX at 1 Mbit/s or DDC signals, USB2 signals
  - ◆ 1 channel with 2 : 1 muxing/switching for single-ended HPD signal
- High-bandwidth analog pass-gate technology
- Supports high-speed signal switching over a wide common-mode range and differential swing
- $R_{ON}$  on DP high-speed channels: 7  $\Omega$



- Low insertion loss:
  - ◆ -0.9 dB at 100 MHz
  - ◆ -1.1 dB at 1.35 GHz
  - ◆ -1.3 dB at 2.7 GHz
- -3 dB bandwidth at 9.5 GHz
- Low crosstalk: -32 dB at 2.7 GHz
- Low off-state isolation: -23 dB at 2.7 GHz
- Low return loss: -19 dB at 2.7 GHz
- Very low intra-pair skew (5 ps typical)
- Very low inter-pair skew (< 80 ps)
- Switch/multiplexer position select CMOS input
- Shutdown mode CMOS input
- Supports backdrive protection
- Single 3.3 V power supply
- Operation current of 490  $\mu$ A typical, shut-down current 10  $\mu$ A maximum
- ESD 2 kV HBM, 500 V CDM
- Available in 5 mm  $\times$  5 mm, 0.5 mm ball pitch TFBGA50 package

### 3. Applications

- Motherboard applications requiring DisplayPort, HDMI, PCI Express, and USB switching/multiplexing
- Docking stations
- Notebook computers
- Chip sets requiring flexible allocation of PCI Express or DisplayPort I/O pins to board connectors

### 4. Ordering information

Table 1. Ordering information

| Type number                  | Topside marking | Solder process                   | Package |   |           |
|------------------------------|-----------------|----------------------------------|---------|---|-----------|
|                              |                 |                                  | Name    | Description   | Version   |
| CBTL06GP213EE <sup>[1]</sup> | GP213           | Pb-free (SnAgCu solder compound) | TFBGA50 | plastic thin fine-pitch ball grid array package; 50 balls; body 5 $\times$ 5 $\times$ 0.8 mm <sup>[2]</sup> | SOT1345-1 |

[1] Industrial temperature range.

[2] Total height including solder balls after printed circuit board mounting = 1.15 mm.

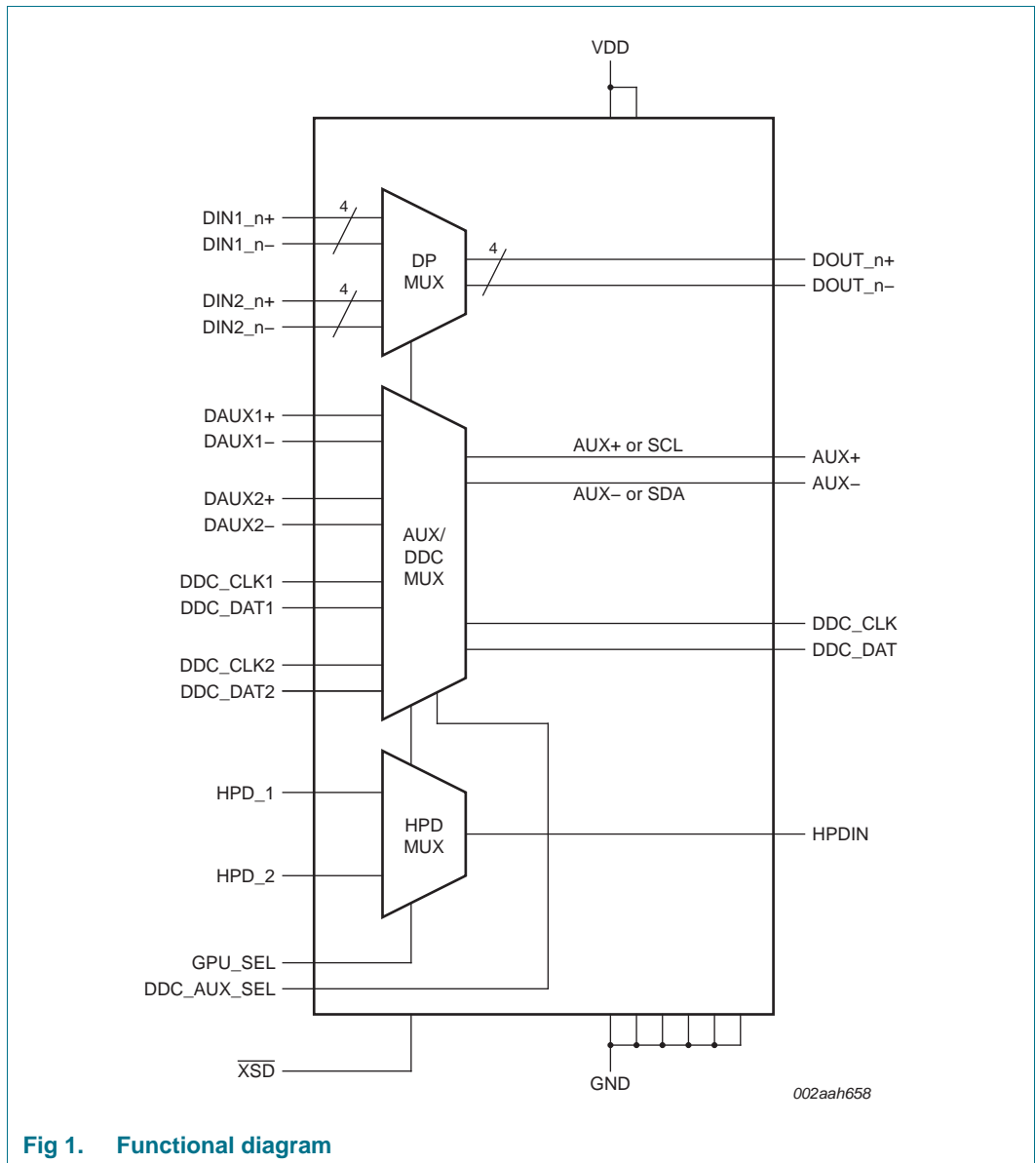
For more information on product marking, refer to [www.nxp.com/products/related/package-markings.html](http://www.nxp.com/products/related/package-markings.html).

**4.1 Ordering options**

**Table 2. Ordering options**

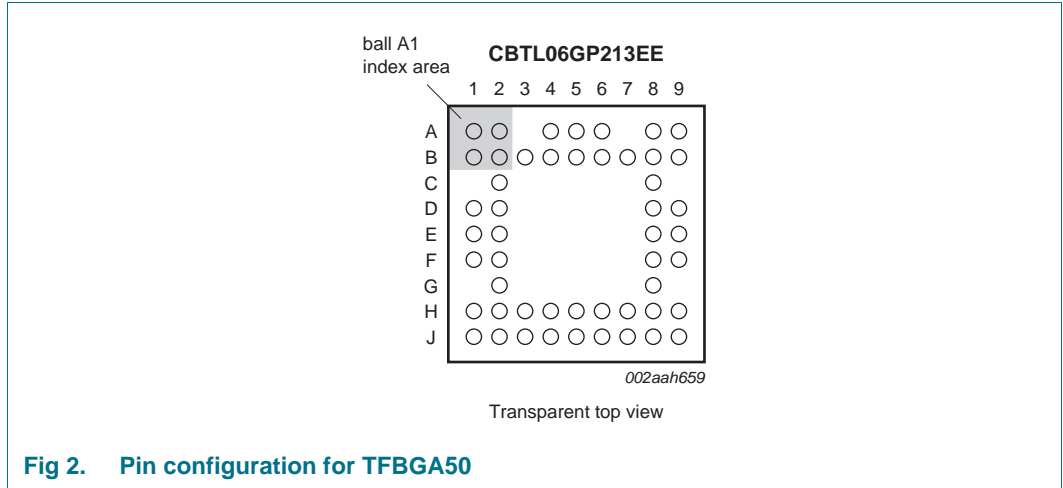
| Type number   | Orderable part number | Package | Packing method                       | Minimum order quantity | Temperature                          |
|---------------|-----------------------|---------|--------------------------------------|------------------------|--------------------------------------|
| CBTL06GP213EE | CBTL06GP213EEJ        | TFBGA50 | Reel 13" Q1/T1<br>*standard mark SMD | 3000                   | T <sub>amb</sub> = -40 °C to +105 °C |

**5. Functional diagram**



**6. Pinning information**

**6.1 Pinning**



|   | 1       | 2           | 3       | 4       | 5        | 6       | 7                       | 8        | 9       |
|---|---------|-------------|---------|---------|----------|---------|-------------------------|----------|---------|
| A | GPU_SEL | VDD         |         | DIN1_0- | DIN1_1-  | DIN1_2- |                         | DIN1_3+  | DIN1_3- |
| B | DOUT_0- | DOUT_0+     | GND     | DIN1_0+ | DIN1_1+  | DIN1_2+ | $\overline{\text{XSD}}$ | DIN2_0+  | DIN2_0- |
| C |         | DDC_AUX_SEL |         |         |          |         |                         | GND      |         |
| D | DOUT_1- | DOUT_1+     |         |         |          |         |                         | DIN2_1+  | DIN2_1- |
| E | DOUT_2- | DOUT_2+     |         |         |          |         |                         | DIN2_2+  | DIN2_2- |
| F | DOUT_3- | DOUT_3+     |         |         |          |         |                         | DIN2_3+  | DIN2_3- |
| G |         | GND         |         |         |          |         |                         | GND      |         |
| H | AUX-    | AUX+        | HPD_2   | GND     | DDC_CLK2 | DAUX2+  | GND                     | DDC_CLK1 | DAUX1+  |
| J | HPDIN   | HPD_1       | DDC_CLK | VDD     | DDC_DAT2 | DAUX2-  | DDC_DAT                 | DDC_DAT1 | DAUX1-  |

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Transparent top view

**Fig 3. Ball mapping**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol                  | Ball | Type                          | Description  |
|-------------------------|------|-------------------------------|--|
| GPU_SEL                 | A1   | 3.3 V CMOS single-ended input | Selects between two multiplexer/switch paths. When HIGH, path 2 left-side is connected to its corresponding right-side I/O. When LOW, path 1 left-side is connected to its corresponding right-side I/O. Refer to <a href="#">Table 6</a> for switch connection details.   |
| DDC_AUX_SEL             | C2   | 3.3 V CMOS single-ended input | Tri-level select pin. Selects between DDC and AUX paths. When HIGH, the AUX+ and AUX- I/Os are connected to appropriate DDC terminals. When LOW, the AUX+ and AUX- I/Os are connected to their appropriate AUX terminals. When MID, AUX and DDC terminals are connected to the AUX+/- and DDC_CLK/DAT I/Os respectively. Refer to <a href="#">Table 6</a> for switch connection details. |
| $\overline{\text{XSD}}$ | B7   | 3.3 V CMOS single-ended input | Shutdown pin. Should be driven HIGH or connected to VDD for normal operation. When LOW, all paths are switched off (non-conducting high-impedance state) and supply current consumption is minimized.  |
| DIN1_0+                 | B4   | differential I/O              | Four high-speed differential pairs for DisplayPort, PCI Express or HDMI, USB3 signals, path 1, left-side.  |
| DIN1_0-                 | A4   | differential I/O              |  |
| DIN1_1+                 | B5   | differential I/O              |  |
| DIN1_1-                 | A5   | differential I/O              |  |
| DIN1_2+                 | B6   | differential I/O              |  |
| DIN1_2-                 | A6   | differential I/O              |  |
| DIN1_3+                 | A8   | differential I/O              |  |
| DIN1_3-                 | A9   | differential I/O              |  |
| DIN2_0+                 | B8   | differential I/O              | Four high-speed differential pairs for DisplayPort, PCI Express or HDMI, USB3 signals, path 2, left-side.  |
| DIN2_0-                 | B9   | differential I/O              |  |
| DIN2_1+                 | D8   | differential I/O              |  |
| DIN2_1-                 | D9   | differential I/O              |  |
| DIN2_2+                 | E8   | differential I/O              |  |
| DIN2_2-                 | E9   | differential I/O              |  |
| DIN2_3+                 | F8   | differential I/O              |  |
| DIN2_3-                 | F9   | differential I/O              |  |
| DOUT_0+                 | B2   | differential I/O              | Four high-speed differential pairs for DisplayPort, PCI Express or HDMI, USB3 signals, right-side.   |
| DOUT_0-                 | B1   | differential I/O              |  |
| DOUT_1+                 | D2   | differential I/O              |  |
| DOUT_1-                 | D1   | differential I/O              |  |
| DOUT_2+                 | E2   | differential I/O              |  |
| DOUT_2-                 | E1   | differential I/O              |  |
| DOUT_3+                 | F2   | differential I/O              |  |
| DOUT_3-                 | F1   | differential I/O              |  |
| DAUX1+                  | H9   | differential I/O              | High-speed differential pair for AUX signals, path 1, left-side.   |
| DAUX1-                  | J9   | differential I/O              |  |

Table 3. Pin description ...continued

| Symbol   | Ball                   | Type             | Description   |
|----------|------------------------|------------------|---|
| DAUX2+   | H6                     | differential I/O | High-speed differential pair for AUX signals, path 2, left-side.                  |
| DAUX2-   | J6                     | differential I/O |   |
| DDC_CLK  | J3                     | differential I/O | Pair of single-ended terminals for DDC clock and data signals, right-side.        |
| DDC_DAT  | J7                     | differential I/O |   |
| DDC_CLK1 | H8                     | differential I/O | Pair of single-ended terminals for DDC clock and data signals, path 1, left-side. |
| DDC_DAT1 | J8                     | differential I/O |   |
| DDC_CLK2 | H5                     | differential I/O | Pair of single-ended terminals for DDC clock and data signals, path 2, left-side. |
| DDC_DAT2 | J5                     | differential I/O |   |
| AUX+     | H2                     | differential I/O | High-speed differential pair for AUX or single-ended DDC signals, right-side.     |
| AUX-     | H1                     | differential I/O |   |
| HPD_1    | J2                     | single-ended I/O | Single ended channel for the HPD signal, path 1, left-side.                       |
| HPD_2    | H3                     | single-ended I/O | Single ended channel for the HPD signal, path 2, left-side.                       |
| HPDIN    | J1                     | single-ended I/O | Single ended channel for the HPD signal, right-side.                              |
| VDD      | A2, J4                 | power supply     | 3.3 V power supply.   |
| GND      | B3, C8, G2, G8, H4, H7 | ground           | Ground.   |

## 7. Functional description

Refer to [Figure 1 “Functional diagram”](#).

The CBTL06GP213 uses a 3.3 V power supply. All main signal paths are implemented using high-bandwidth pass-gate technology and are non-directional. No clock or reset signal is needed for the multiplexer to function.

The switch position for the main channels is selected using the select signal GPU\_SEL. Additionally, the signal DDC\_AUX\_SEL selects between AUX and DDC positions for the DDC / AUX channel. The detailed operation is described in [Section 7.1](#).

### 7.1 Multiplexer/switch select functions

The internal multiplexer switch position is controlled by two logic inputs GPU\_SEL and DDC\_AUX\_SEL as described below.

Table 4. Multiplexer/switch select control for DIN and DOUT channels

| GPU_SEL | DIN1_n                      | DIN2_n                      |
|---------|-----------------------------|-----------------------------|
| 0       | active; connected to DOUT_n | high-impedance              |
| 1       | high-impedance              | active; connected to DOUT_n |

Table 5. Multiplexer/switch select control for HPD channel

| GPU_SEL | HPD1                       | HPD2                       |
|---------|----------------------------|----------------------------|
| 0       | active; connected to HPDIN | high-impedance             |
| 1       | high-impedance             | active; connected to HPDIN |

**Table 6. Multiplexer/switch select control for DDC and AUX channels**

| DDC_AUX_SEL | GPU_SEL | DAUX1                       | DAUX2                       | DDC1                        | DDC2                        |
|-------------|---------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| LOW         | LOW     | active;<br>connected to AUX | high-Z                      | high-Z                      | high-Z                      |
| LOW         | HIGH    | high-Z                      | active;<br>connected to AUX | high-Z                      | high-Z                      |
| HIGH        | LOW     | high-Z                      | high-Z                      | active;<br>connected to AUX | high-Z                      |
| HIGH        | HIGH    | high-Z                      | high-Z                      | high-Z                      | active;<br>connected to AUX |
| MID         | LOW     | active;<br>connected to AUX | high-Z                      | active;<br>connected to DDC | high-Z                      |
| MID         | HIGH    | high-Z                      | active;<br>connected to AUX | high-Z                      | active;<br>connected to DDC |

The voltage thresholds for the different pin settings — LOW, MID and HIGH — are given in [Table 14](#).

## 7.2 Shutdown function

The CBTL06GP213 provides a shutdown function to minimize power consumption when the application is not active but CBTL06GP213 can remain powered. Pin XSD (active LOW) puts all channels in off mode (non-conducting high-impedance state) while reducing current consumption to near-zero.

**Table 7. Shutdown function**

| XSD | State    |
|-----|----------|
| 0   | shutdown |
| 1   | active   |

## 8. Limiting values

**Table 8. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol           | Parameter                       | Conditions                                | Min  | Max  | Unit |
|------------------|---------------------------------|---|------|------|------|
| V <sub>DD</sub>  | supply voltage                  |   | -0.3 | +4.6 | V    |
| V <sub>I</sub>   | input voltage                   | DDC_AUX_SEL, GPU_SEL, XSD, DINx_n, DOUT_n | -0.3 | +4.0 | V    |
|                  |                                 | AUX1, AUX2, AUX, DDC1, DDC2, DDC, HPD     | -0.3 | +6.0 | V    |
| T <sub>stg</sub> | storage temperature             |   | -65  | +150 | °C   |
| V <sub>ESD</sub> | electrostatic discharge voltage | HBM [1]                                   | -    | 2000 | V    |
|                  |                                 | CDM [2]                                   | -    | 500  | V    |

[1] Human Body Model: ANSI/ESDAJEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[2] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

## 9. Recommended operating conditions

**Table 9. Recommended operating conditions**

| Symbol           | Parameter           | Conditions                            | Min  | Typ | Max                   | Unit |
|------------------|---------------------|---------------------------------------|------|-----|-----------------------|------|
| V <sub>DD</sub>  | supply voltage      |                                       | 3.0  | 3.3 | 3.6                   | V    |
| V <sub>I</sub>   | input voltage       | DDC_AUX_SEL, GPU_SEL, XSD             | -0.3 | -   | V <sub>DD</sub> + 0.3 | V    |
|                  |                     | DINx_n, DOUT_n                        | -0.3 | -   | +4.0                  | V    |
|                  |                     | AUX1, AUX2, AUX, DDC1, DDC2, DDC, HPD | -0.3 | -   | +5.5                  | V    |
| T <sub>amb</sub> | ambient temperature | operating in free air                 | -40  | -   | +105                  | °C   |

## 10. Characteristics

### 10.1 General characteristics

**Table 10. General characteristics**

| Symbol               | Parameter            | Conditions   | Min | Typ | Max | Unit |
|----------------------|----------------------|--|-----|-----|-----|------|
| I <sub>DD</sub>      | supply current       | operating mode ( $\overline{XSD} = \text{HIGH}$ )  | -   | 490 | -   | μA   |
|                      |                      | shutdown mode ( $\overline{XSD} = \text{LOW}$ )  | -   | -   | 15  | μA   |
| P <sub>cons</sub>    | power consumption    | operating mode ( $\overline{XSD} = \text{HIGH}$ )  | -   | 1.6 | -   | mW   |
| t <sub>startup</sub> | start-up time        | supply voltage valid or $\overline{XSD}$ going HIGH to channel specified operating characteristics | -   | -   | 5   | ms   |
| t <sub>rcfg</sub>    | reconfiguration time | GPU_SEL or DDC_AUX_SEL state change to channel specified operating characteristics                 | -   | -   | 10  | μs   |



## 10.2 DisplayPort channel characteristics

Table 11. DisplayPort channel characteristics

| Symbol        | Parameter                        | Conditions   | Min  | Typ  | Max  | Unit          |
|---------------|----------------------------------|--|------|------|------|---------------|
| $V_I$         | input voltage                    |  | -0.3 | -    | +4.0 | V             |
| $V_{IC}$      | common-mode input voltage        |  | 0    | -    | 3.6  | V             |
| $V_{ID}$      | differential input voltage       | peak-to-peak   | -    | -    | +1.4 | V             |
| $R_{ON}$      | ON resistance                    | $V_{DD} = 3.3\text{ V}; I_I = 20\text{ mA}$          |      |      |      |               |
|               |                                  | $V_{IC} = 0\text{ V to } 2\text{ V}$                 | -    | 7    | 10   | $\Omega$      |
|               |                                  | $V_{IC} = 2\text{ V to } 3.6\text{ V}$               | -    | 8    | 10   | $\Omega$      |
| DDIL          | differential insertion loss      | channel is ON; $f \leq 100\text{ MHz}$               | -    | -0.9 | -    | dB            |
|               |                                  | channel is ON; $f = 1.35\text{ GHz}$                 | -    | -1.1 | -    | dB            |
|               |                                  | channel is ON; $f = 2.7\text{ GHz}$                  | -    | -1.3 | -    | dB            |
|               |                                  | channel is OFF; $f = 2.7\text{ GHz}$                 | -    | -23  | -    | dB            |
| DDRL          | differential return loss         | $f = 100\text{ MHz}$                                 | -    | -22  | -    | dB            |
|               |                                  | $f = 1.35\text{ GHz}$                                | -    | -21  | -    | dB            |
|               |                                  | $f = 2.7\text{ GHz}$                                 | -    | -19  | -    | dB            |
| DDNEXT        | differential near-end crosstalk  | adjacent channels are ON                             |      |      |      |               |
|               |                                  | $f = 100\text{ MHz}$                                 | -    | -50  | -    | dB            |
|               |                                  | $f = 2.7\text{ GHz}$                                 | -    | -32  | -    | dB            |
| B             | bandwidth                        | -3.0 dB intercept                                    | -    | 9.5  | -    | GHz           |
| $t_{PD}$      | propagation delay                | from left-side port to right-side port or vice versa | -    | 80   | -    | ps            |
| $t_{sk(dif)}$ | differential skew time           | intra-pair   | -    | 5    | 8    | ps            |
| $t_{sk}$      | skew time                        | inter-pair   | -    | -    | 80   | ps            |
| $I_{LIH}$     | HIGH-level input leakage current | $V_{DD} = 3.3\text{ V}; V_I = 4.0\text{ V}$          | -    | -    | 10   | $\mu\text{A}$ |
|               |                                  | $V_{DD} = 0\text{ V}; V_I = 4.0\text{ V}$            | -    | -    | 10   | $\mu\text{A}$ |
| $I_{LIL}$     | LOW-level input leakage current  | $V_{DD} = 3.3\text{ V}; V_I = \text{GND}$            | -    | -    | 10   | $\mu\text{A}$ |

All S-parameter measurements are with respect to 100  $\Omega$  differential impedance reference, 50  $\Omega$  single-ended impedance reference. DDIL and DDRL measurements are with Common-mode voltage of 3 V.

10.3 AUX and DDC ports

Table 12. AUX and DDC port characteristics

| Symbol         | Parameter                        | Conditions  | Min  | Typ  | Max  | Unit          |
|----------------|----------------------------------|---|------|------|------|---------------|
| $V_I$          | input voltage                    |   | -0.3 | -    | +5.5 | V             |
| $V_{bias(DC)}$ | bias voltage (DC)                | AUX   | 0    | -    | 3.3  | V             |
| $V_{i(dif)}$   | differential input voltage       | AUX; single-ended swing   | -    | -    | 0.7  | V             |
| $R_{ON}$       | ON resistance                    | AUX path; $V_{DD} = 3.3\text{ V}$ ; $I_I = 20\text{ mA}$            |      |      |      |               |
|                |                                  | $V_{IC} = 0\text{ V to }3.3\text{ V}$                               | -    | 4.7  | -    | $\Omega$      |
|                |                                  | $V_{IC} = 3.3\text{ V to }5.25\text{ V}$                            | -    | 6.5  | -    | $\Omega$      |
|                |                                  | DDC path; $V_{DD} = 3.3\text{ V}$ ; $I_I = 20\text{ mA}$            |      |      |      |               |
|                |                                  | $V_{IC} = 0\text{ V to }3.3\text{ V}$                               | -    | 6.5  | -    | $\Omega$      |
| DDIL           | differential insertion loss      | on AUX/DDC ports  |      |      |      |               |
|                |                                  | channel is ON; $f \leq 100\text{ MHz}$                              | -    | -0.7 | -    | dB            |
|                |                                  | channel is ON; $f = 240\text{ MHz}$                                 | -    | -1.0 | -    | dB            |
|                |                                  | channel is ON; $f = 720\text{ MHz}$                                 | -    | -1.2 | -    | dB            |
| DDRL           | differential return loss         | on AUX/DDC ports  |      |      |      |               |
|                |                                  | $f = 100\text{ MHz}$  | -    | -21  | -    | dB            |
|                |                                  | $f = 240\text{ MHz}$  | -    | -16  | -    | dB            |
|                |                                  | $f = 720\text{ MHz}$  | -    | -12  | -    | dB            |
| $t_{PD}$       | propagation delay                | from left-side port to right-side port or vice versa <sup>[1]</sup> | -    | 80   | -    | ps            |
| $t_{sk(dif)}$  | differential skew time           | intra-pair skew on AUX  | -    | 10   | -    | ps            |
| $I_{LIH}$      | HIGH-level input leakage current | $V_{DD} = 3.3\text{ V}$ ; $V_I = 4.0\text{ V}$                      | -    | -    | -10  | $\mu\text{A}$ |
| $I_{LIL}$      | LOW-level input leakage current  | $V_{DD} = 3.3\text{ V}$ ; $V_I = \text{GND}$                        | -    | -    | +10  | $\mu\text{A}$ |

[1] Time from DDC/AUX input changing state to AUX output changing state. Includes DDC/AUX rise/fall time.

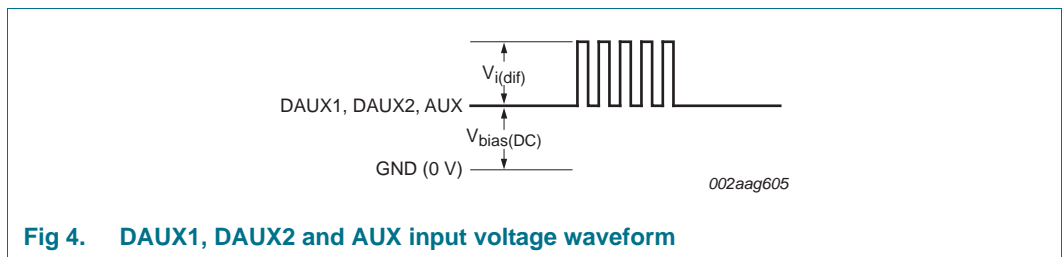


Fig 4. DAUX1, DAUX2 and AUX input voltage waveform

All S-parameter measurements are with respect to 100  $\Omega$  differential impedance reference and 50  $\Omega$  single-ended impedance reference.

### 10.4 HPDIN input, HPD\_x outputs

**Table 13. HPD input and output characteristics**

| Symbol           | Parameter                        | Conditions                                      | Min  | Typ | Max  | Unit |
|------------------|----------------------------------|---|------|-----|------|------|
| V <sub>I</sub>   | input voltage                    |   | -0.3 | -   | +5.5 | V    |
| R <sub>ON</sub>  | ON resistance                    | V <sub>DD</sub> = 3.3 V; I <sub>I</sub> = 20 mA |      |     |      |      |
|                  |                                  | V <sub>IC</sub> = 0 V to 3.3 V                  | -    | 5   | -    | Ω    |
|                  |                                  | V <sub>IC</sub> = 3.3 V to 5.5 V                | -    | 6.5 | -    | Ω    |
| I <sub>LIH</sub> | HIGH-level input leakage current | V <sub>DD</sub> = 3.3 V; V <sub>I</sub> = 4.0 V | -    | -   | -10  | μA   |
| I <sub>LIL</sub> | LOW-level input leakage current  | V <sub>DD</sub> = 3.3 V; V <sub>I</sub> = GND   | -    | -   | +10  | μA   |
| t <sub>PD</sub>  | propagation delay                | from HPDIN to HPD_x or vice versa               | [1]  | 100 | -    | ps   |

[1] Time from HPDIN changing state to HPD\_x changing state. Includes HPD rise/fall time.

### 10.5 GPU\_SEL, DDC\_AUX\_SEL, $\overline{XSD}$ inputs

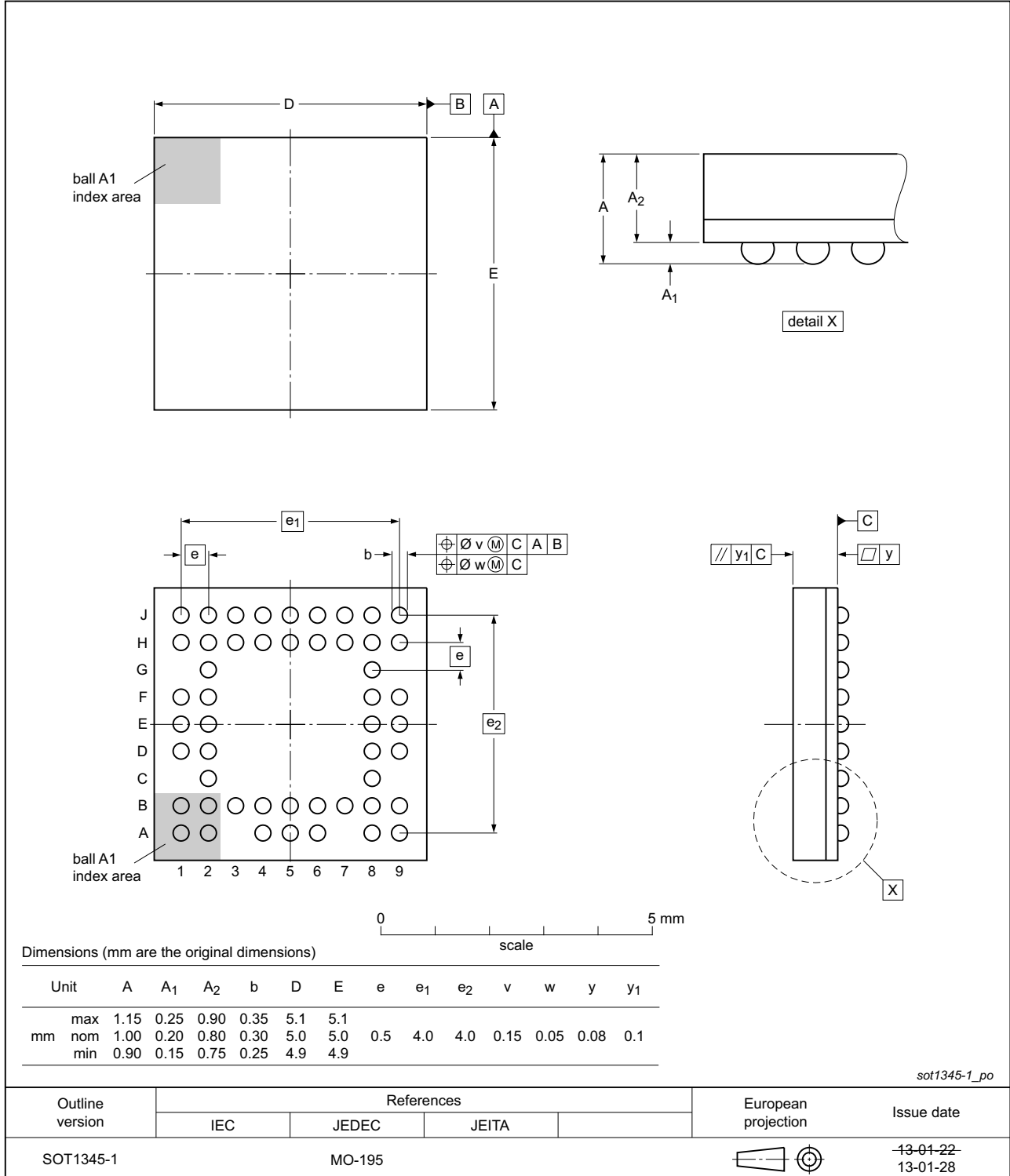
**Table 14. GPU\_SEL, DDC\_AUX\_SEL,  $\overline{XSD}$  input characteristics**

| Symbol          | Parameter             | Conditions   | Min                    | Typ | Max                    | Unit |
|-----------------|-----------------------|--|------------------------|-----|------------------------|------|
| V <sub>I</sub>  | input voltage         | HIGH-level;<br>GPU_SEL, DDC_AUX_SEL, $\overline{XSD}$                                    | 0.7 × V <sub>DD</sub>  | -   | -                      | V    |
|                 |                       | MID-level;<br>DDC_AUX_SEL  | 0.45 × V <sub>DD</sub> | -   | 0.55 × V <sub>DD</sub> | V    |
|                 |                       | LOW-level;<br>GPU_SEL, DDC_AUX_SEL, $\overline{XSD}$                                     | -                      | -   | 0.2 × V <sub>DD</sub>  | V    |
| I <sub>LI</sub> | input leakage current | HIGH-level;<br>V <sub>DD</sub> = 3.3 V; HIGH-level V <sub>I</sub> = 3.6 V                | -                      | -   | -10                    | μA   |
|                 |                       | MID-level;<br>V <sub>DD</sub> = 3.3 V; MID-level V <sub>I</sub> = 0.55 × V <sub>DD</sub> | -                      | -   | -10                    | μA   |
|                 |                       | LOW-level;<br>V <sub>DD</sub> = 3.3 V; LOW-level V <sub>I</sub> = GND                    | -                      | -   | +10                    | μA   |

**11. Package outline**

TFBGA50: plastic thin fine-pitch ball grid array package; 50 balls;

SOT1345-1



**Fig 5. Package outline TFBGA50 (SOT1345-1)**

## 12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

**12.4 Reflow soldering**

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 6](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 15](#) and [16](#)

**Table 15. SnPb eutectic process (from J-STD-020D)**

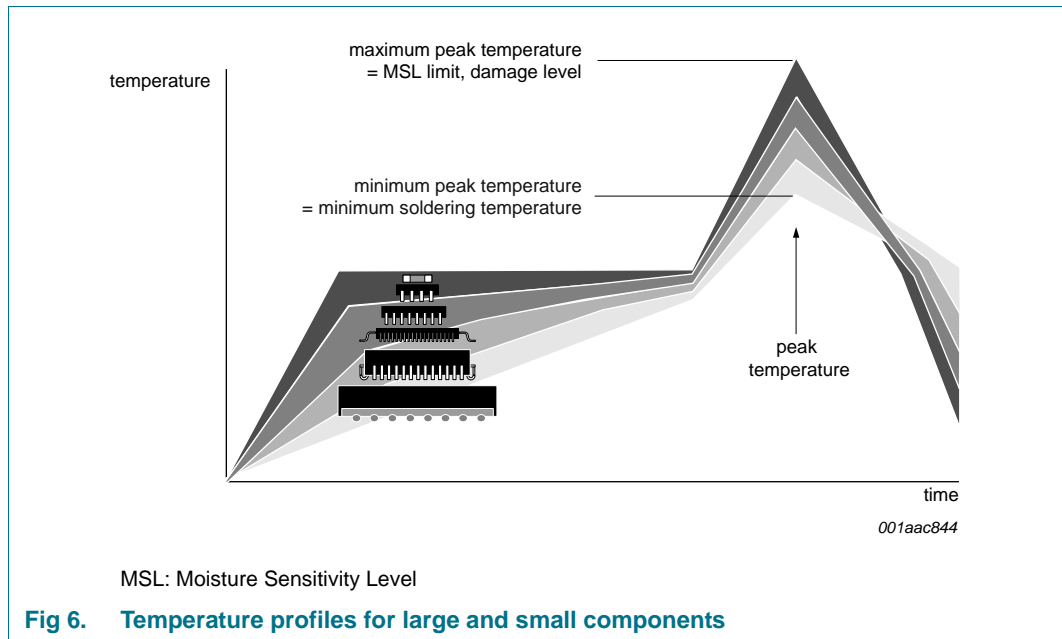
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 16. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 6](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

### 13. Abbreviations

**Table 17. Abbreviations**

| Acronym | Description                                   |
|---------|---|
| AUX     | Auxiliary channel (in DisplayPort definition) |
| DDC     | Display Data Channel                          |
| DVI     | Digital Video Interface                       |
| GPU     | Graphics Processor Unit                       |
| HDMI    | High-Definition Multimedia Interface          |
| HPD     | Hot Plug Detect                               |
| PCB     | Printed-Circuit Board                         |
| PCIe    | PCI Express                                   |

## 14. Revision history

Table 18. Revision history

| Document ID       | Release date   | Data sheet status  | Change notice | Supersedes      |
|-------------------|--|--------------------|---------------|-----------------|
| CBTL06GP213 v.3.1 | 20161213   | Product data sheet | -             | CBTL06GP213 v.3 |
| Modifications:    | • <a href="#">Section 1</a> and <a href="#">Section 2</a> : Updated HDMI spec from 1.4b to 2.0 |                    |               |                 |
| CBTL06GP213 v.3   | 20140627   | Product data sheet | -             | CBTL06GP213 v.2 |
| CBTL06GP213 v.2   | 20140217   | Product data sheet | -             | CBTL06GP213 v.1 |
| CBTL06GP213 v.1   | 20130830   | Product data sheet | -             | -               |



## 15. Legal information

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| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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