256-Kb I²C CMOS Serial EEPROM

FEATURES

- **Supports Standard and Fast I²C Protocol**
- **1.8 V to 5.5 V Supply Voltage Range**
- **64-Byte Page Write Buffer**
- **Hardware Write Protection for entire memory**
- **Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA).**
- **Low power CMOS technology**
- **1,000,000 program/erase cycles**
- **100 year data retention**
- **Industrial temperature range**
- **RoHS-compliant 8-pin PDIP and SOIC packages**

For Ordering Information details, see page 13.

DEVICE DESCRIPTION

The CAT24C256 is a 256-Kb Serial CMOS EEPROM, internally organized as 512 pages of 64 bytes each, for a total of 32,768 bytes of 8 bits each.

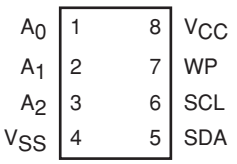
It features a 64-byte page write buffer and supports both the Standard (100 kHz) as well as Fast (400 kHz) I²C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

External address pins make it possible to address up to eight CAT24C256 devices on the same bus.

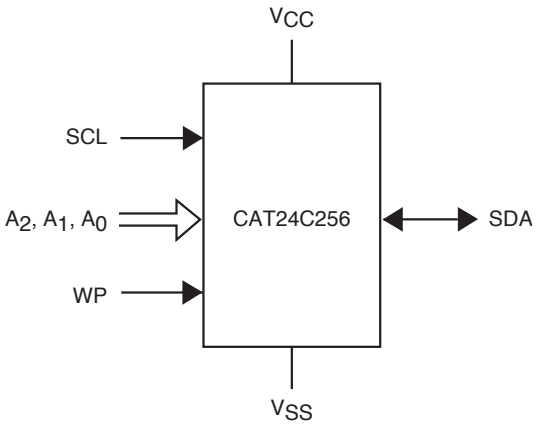
PIN CONFIGURATION

PDIP (L)
SOIC (W, X)



For the location of Pin 1, please consult the corresponding package drawing.

FUNCTIONAL SYMBOL



PIN FUNCTIONS

A_0, A_1, A_2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

* Catalyst carries the I²C protocol under a license from the Philips Corporation.

ABSOLUTE MAXIMUM RATINGS(1)

Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground(2)	-0.5 V to +6.5 V

RELIABILITY CHARACTERISTICS(3)

Symbol	Parameter	Min	Units
N_{END}(4)	Endurance	1,000,000	Program/ Erase Cycles
T_{DR}	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	Supply Current	Read or Write at 400 kHz		1	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		1	µA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		1	µA
V_{IL}	Input Low Voltage		-0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} > 2.5 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	V_{CC} > 1.8 V, I_{OL} = 1.0 mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

T_A = 25°C, f = 400 kHz, V_{CC} = 5 V

Symbol	Parameter	Conditions	Min	Max	Units
C_{IN}(3)	SDA I/O Pin Capacitance	V_{IN} = 0 V		8	pF
C_{IN}(3)	Input Capacitance (other pins)	V_{IN} = 0 V		6	pF

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Page Mode, V_{CC} = 5 V, 25°C

A.C. CHARACTERISTICS[1]

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	1.8 V - 5.5 V		2.5 V - 5.5 V		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
T_I[2]	Noise Suppression Time Constant at SCL, SDA Inputs		0.1		0.1	µs
t_{AA}	SCL Low to SDA Data Out		3.5		0.9	µs
t_{BUF}[2]	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.3		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		µs
$t_{SU:DAT}$	Data In Setup Time	0.25		0.1		µs
t_R[2]	SDA and SCL Rise Time		1		0.3	µs
t_F[2]	SDA and SCL Fall Time		0.3		0.3	µs
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	0.1		0.1		µs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU}[2], [3]	Power-up to Ready Mode		1		1	ms

Notes:

(1) Test conditions according to “A.C. Test Conditions” table.

(2) Tested initially and after a design or process change that affects this parameter.

(3) t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_{OL} = 3 mA (V_{CC} ≥ 2.5 V); I_{OL} = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

PIN DESCRIPTION

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address pins accept the device address. These pins have on-chip pull-down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on-chip pull-down resistor.

FUNCTIONAL DESCRIPTION

The CAT24C256 supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C256 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A_0, A_1, and A_2.

I^2C BUS PROTOCOL

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 1).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 2). The next 3 bits, A_2, A_1 and A_0, select one of 8 possible Slave devices. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9^{th} clock cycle (Figure 3). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9^{th} clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 4.

Figure 1. Start/Stop Timing

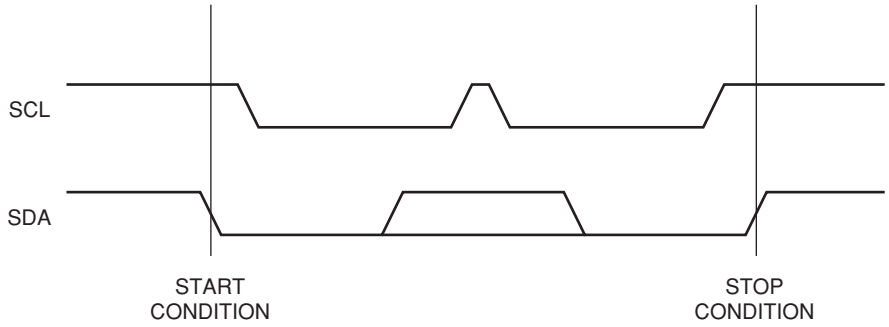


Figure 2. Slave Address Bits

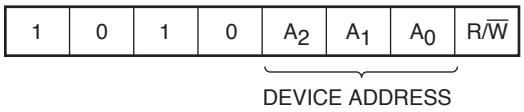


Figure 3. Acknowledge Timing

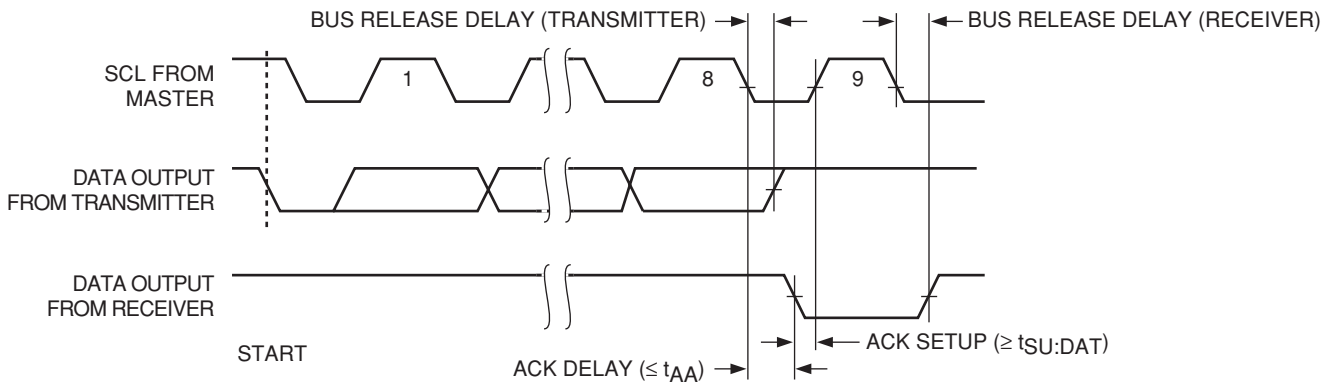
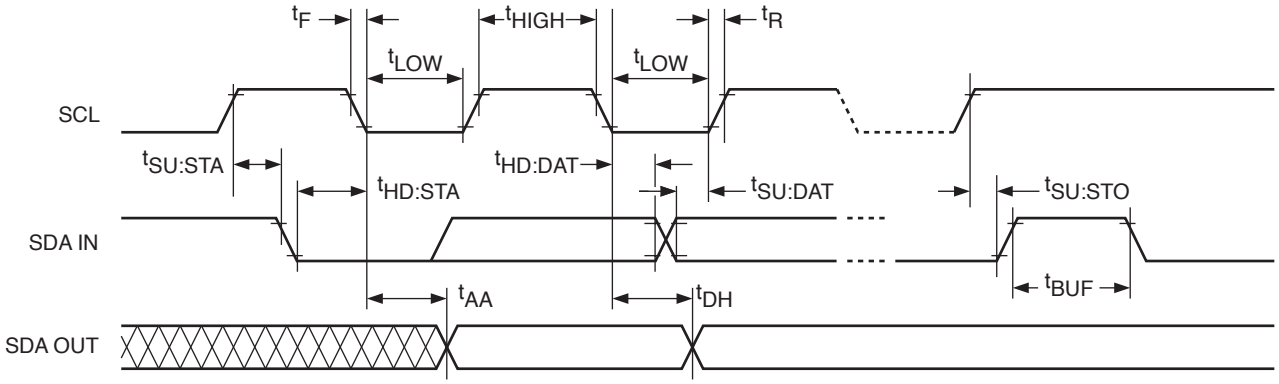


Figure 4. Bus Timing



WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 5). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 6). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The CAT24C256 contains 32,768 bytes of data, arranged in 512 pages of 64 bytes each. A two byte address word, following the Slave address, points to the first byte to be written. The most significant bit of the address word is 'don't care', the next 9 bits identify the page and the last 6 bits identify the byte within the page. Up to 64 bytes can be written in one Write cycle (Figure 7).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 64 data bytes, then earlier bytes will be overwritten by later bytes in a 'wrap-around' fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT24C256 is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a 'Selective Read' command (see READ OPERATIONS).

The CAT24C256 will not acknowledge the Slave address, as long as internal Write is in progress.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C256.

Figure 5. Byte Write Timing

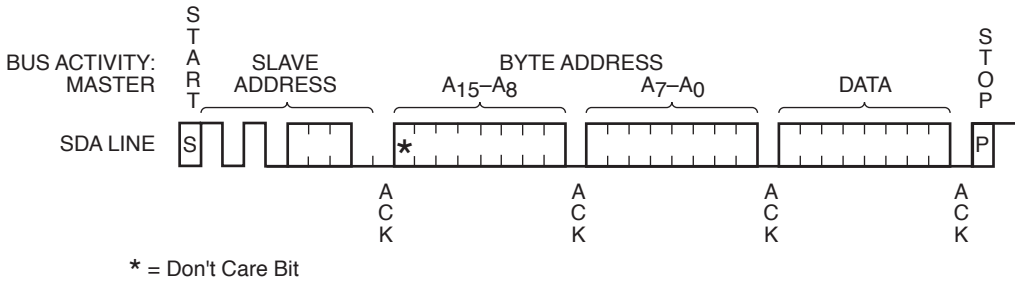


Figure 6. Write Cycle Timing

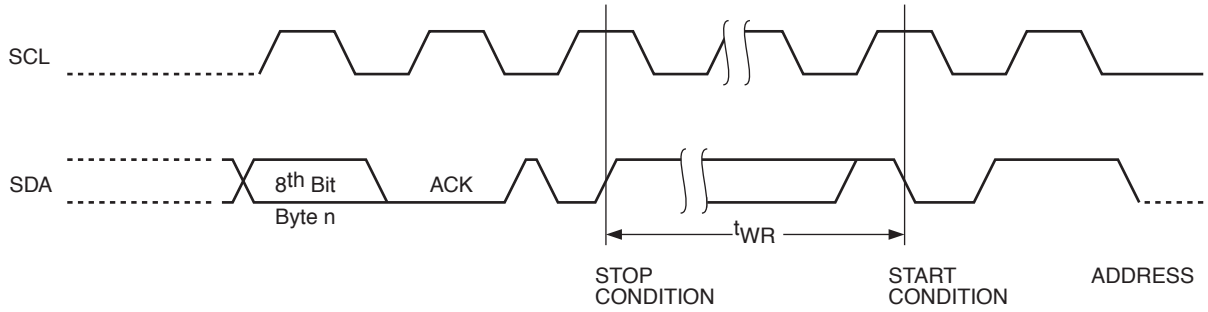
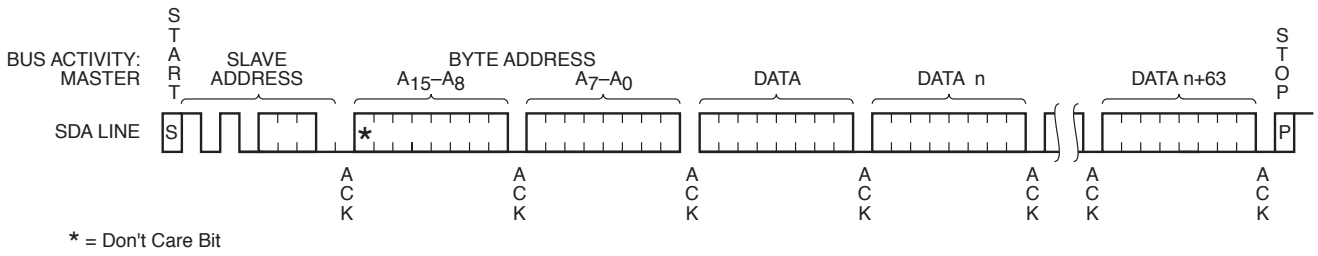


Figure 7. Page Write Timing



READ OPERATIONS

Immediate Address Read

In standby mode, the CAT24C256 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that 'previous' byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the CAT24C256 is presented with a Slave address containing a '1' in the R/W bit position (Figure 8), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a 'dummy' Write operation (Figure 9). Here the START is followed by the Slave address (with the R/W bit set to '0') and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the 'Immediate Address Read' sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the CAT24C256, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 10). If the end of memory is reached during sequential Read, then the address counter will 'wrap-around' to the beginning of memory, etc. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

Figure 8. Immediate Address Read Timing

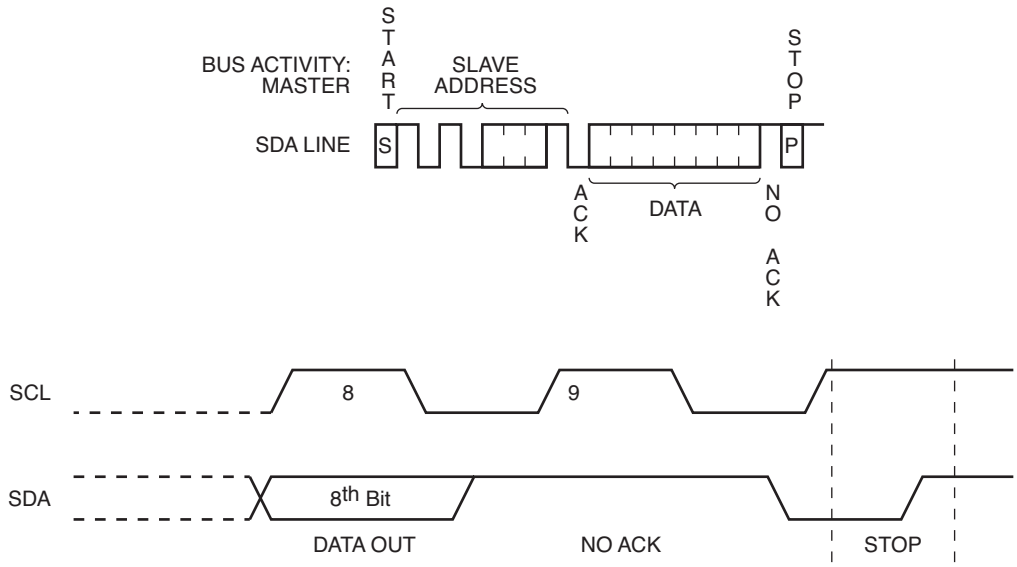


Figure 9. Selective Read Timing

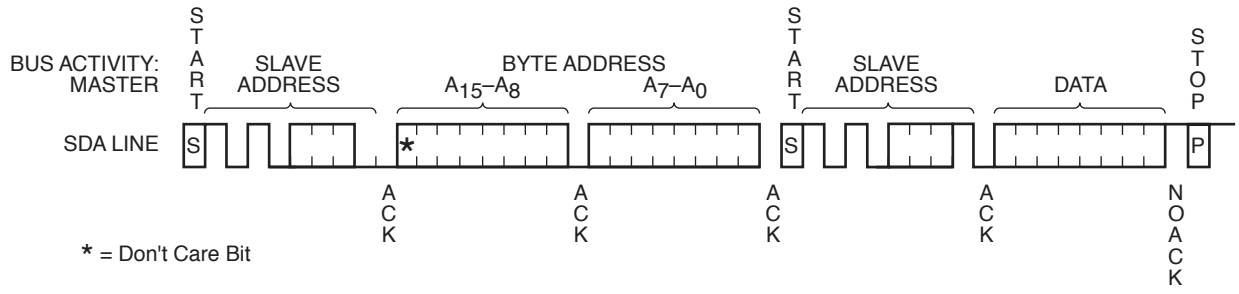
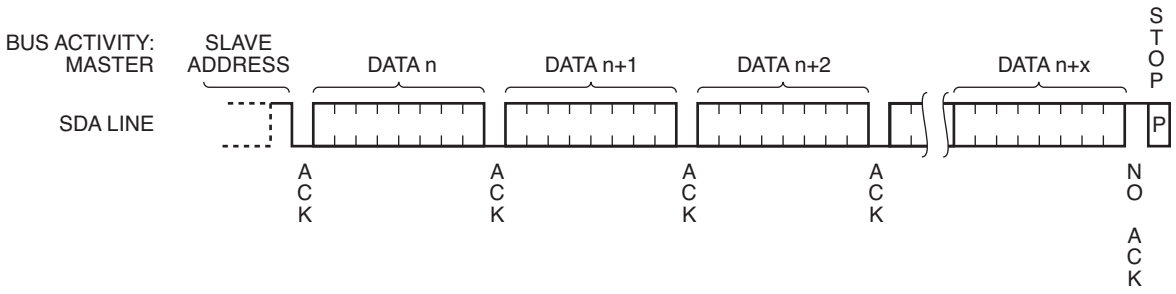
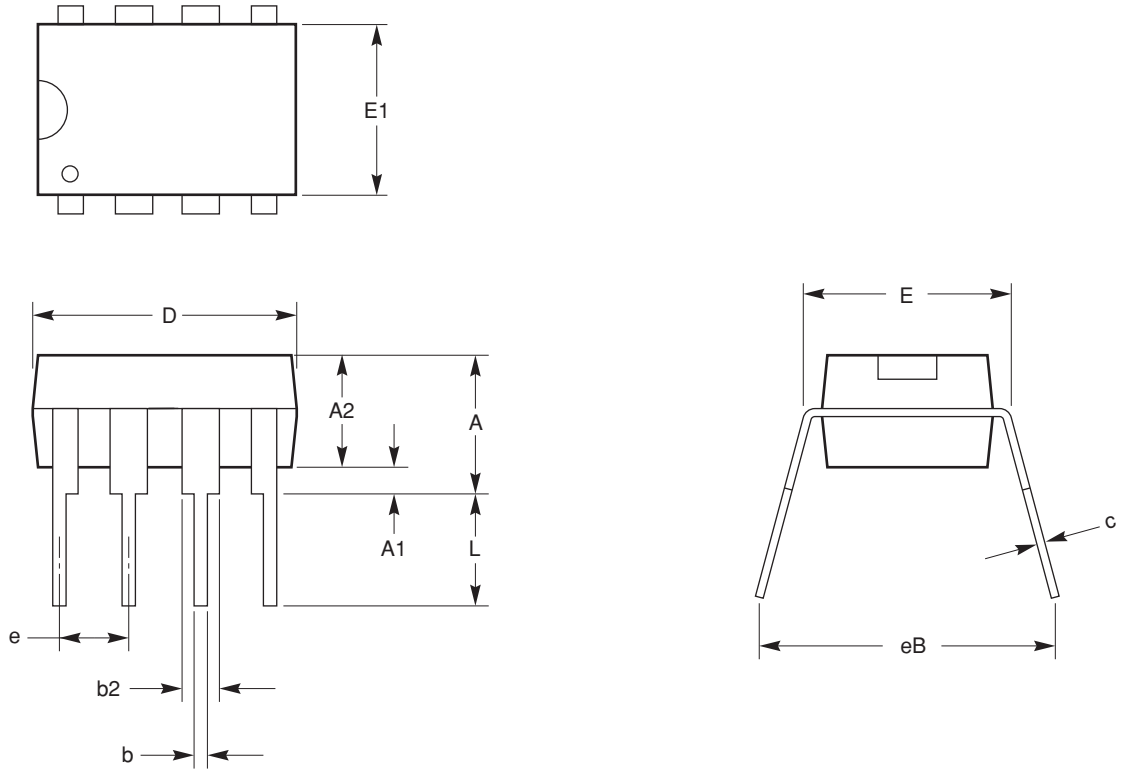


Figure 10. Sequential Read Timing



PACKAGE OUTLINES

8-LEAD 300 MIL WIDE PLASTIC DIP (L)

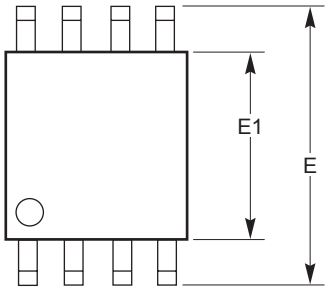


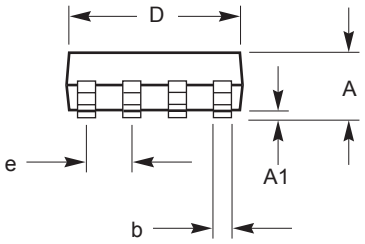
SYMBOL	MIN	NOM	MAX
A			4.57
A1	0.38		
A2	3.05		3.81
b	0.36	0.46	0.56
b2	1.14		1.77
c	0.21	0.26	0.35
D	9.02		10.16
E	7.62	7.87	8.25
E1	6.09	6.35	7.11
e		2.54 BSC	
eB	7.87		9.65
L	2.92		3.81

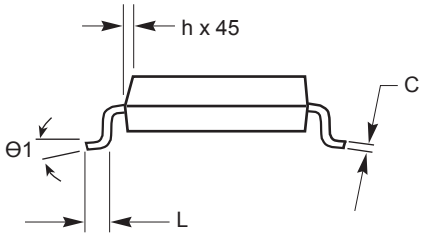
For current Tape and Reel information, download the PDF file from:
http://www.catsemi.com/documents/tapeandreel.pdf

Notes:
(1) Complies with JEDEC Standard MS001.
(2) All dimensions are in millimeters.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982

8-LEAD 150 MIL WIDE SOIC (W)





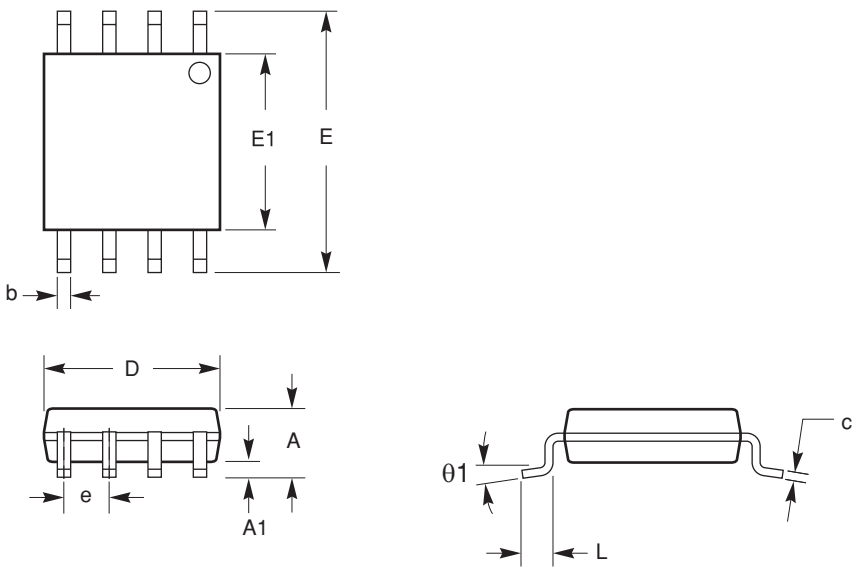


SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
Θ1	0°		8°

For current Tape and Reel information, download the PDF file from:
http://www.catsemi.com/documents/tapeandreel.pdf

Notes:
(1) Complies with JEDEC specification MS-012 dimensions.
(2) All linear dimensions are in millimeters.

8-LEAD 208 MIL WIDE SOIC, EIAJ (X)

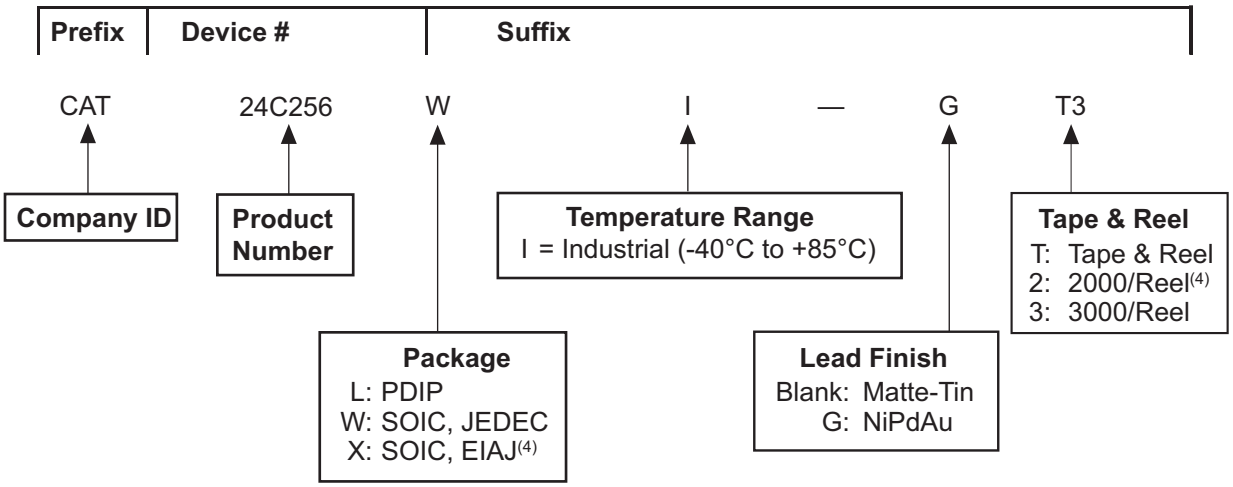


SYMBOL	MIN	NOM	MAX
A1	0.05		0.25
A			2.03
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e		1.27 BSC	
L	0.51		0.76
θ1	0°		8°

For current Tape and Reel information, download the PDF file from:
http://www.catsemi.com/documents/tapeandreel.pdf

Notes:
(1) Complies with EIAJ specification.
(2) All linear dimensions are in millimeters.

ORDERING INFORMATION



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu.

(3) The device used in the above example is a CAT24C256WI-GT3 (SOIC-JEDEC, Industrial Temperature, NiPdAu, Tape & Reel).

(4) For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2000 pcs/reel, i.e. CAT24C256XI-T2.

(5) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

REVISION HISTORY

Date	Revision	Comments
10/07/05	A	Initial Issue
11/16/05	B	Update Ordering Information Add Tape and Reel Specifications
02/02/06	C	Update Ordering Information
01/12/07	D	Update Package Outlines. Add SOIC, EIAJ Package Outlines Update A.C. Characteristics. Add A.C. Test Conditions Update Figures 1, 3 and 4 Delete Package Marking. Deleted Tape and Reel Updated Ordering Information

Catalyst Semiconductor, Inc.
Corporate Headquarters
2975 Stender Way
Santa Clara, CA 95054
Phone: 408.542.1000
Fax: 408.542.1200
www.catsemi.com

Publication #: 1104
Revison: D
Issue date: 01/12/07