



# BUK9Y104-100B

## N-channel TrenchMOS logic level FET

Rev. 04 — 7 April 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive systems
- DC-to-DC converters
- General purpose power switching
- Solenoid drivers

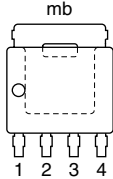
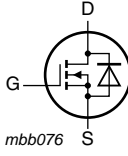
### 1.4 Quick reference data

Table 1. Quick reference data

| Symbol                         | Parameter                                    | Conditions   | Min | Typ | Max  | Unit       |
|--------------------------------|--|--|-----|-----|------|------------|
| $V_{DS}$                       | drain-source voltage                         | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$   | -   | -   | 100  | V          |
| $I_D$                          | drain current                                | $V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ;<br>see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>   | -   | -   | 14.8 | A          |
| $P_{tot}$                      | total power dissipation                      | $T_{mb} = 25\text{ °C}$  | -   | -   | 59   | W          |
| <b>Static characteristics</b>  |  |  |     |     |      |            |
| $R_{DS(on)}$                   | drain-source on-state resistance             | $V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$   | -   | 86  | 99   | m $\Omega$ |
|                                |  | $V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ;<br>see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>                       | -   | 91  | 104  | m $\Omega$ |
| <b>Avalanche ruggedness</b>    |  |  |     |     |      |            |
| $E_{DS(AL)S}$                  | non-repetitive drain-source avalanche energy | $I_D = 14.8\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ;<br>$R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ;<br>$T_{j(init)} = 25\text{ °C}$ ; unclamped | -   | -   | 35   | mJ         |
| <b>Dynamic characteristics</b> |  |  |     |     |      |            |
| $Q_{GD}$                       | gate-drain charge                            | $V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ;<br>$V_{DS} = 80\text{ V}$ ; see <a href="#">Figure 13</a>   | -   | 4.7 | -    | nC         |

## 2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                       | Simplified outline  | Graphic symbol  |
|-----|--------|-----------------------------------|---|---|
| 1   | S      | source                            |  |  |
| 2   | S      | source                            |   |   |
| 3   | S      | source                            |   |   |
| 4   | G      | gate                              |   |   |
| mb  | D      | mounting base; connected to drain |   |   |

**SOT669 (LFPAK)**

## 3. Ordering information

Table 3. Ordering information

| Type number   | Package |   |         |
|---------------|---------|---|---------|
|               | Name    | Description   | Version |
| BUK9Y104-100B | LFPAK   | plastic single-ended surface-mounted package (LFPAK); 4 leads | SOT669  |

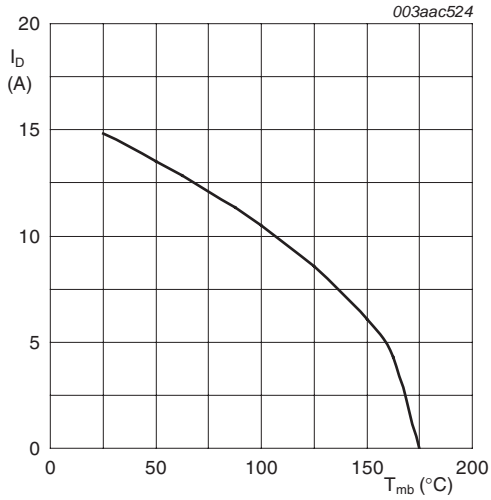
## 4. Limiting values

**Table 4. Limiting values**

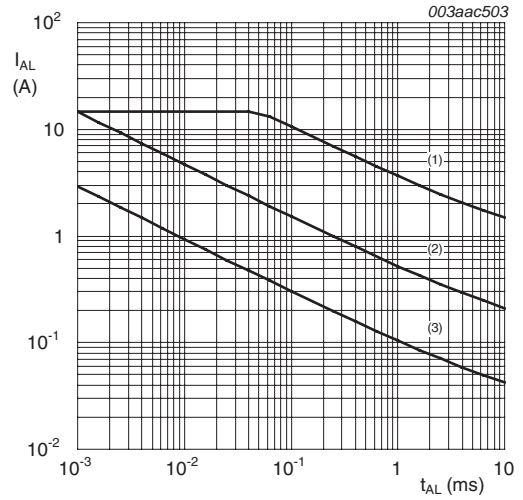
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions  | Min   | Typ | Max   | Unit |
|-----------------------------|--|---|---|-----|-------|------|
| $V_{DS}$                    | drain-source voltage                         | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$  | -   | -   | 100   | V    |
| $V_{DGR}$                   | drain-gate voltage                           | $R_{GS} = 20\text{ k}\Omega$  | -   | -   | 100   | V    |
| $V_{GS}$                    | gate-source voltage                          |   | -15   | -   | 15    | V    |
| $I_D$                       | drain current                                | $T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a> ;<br>see <a href="#">Figure 3</a>  | -   | -   | 14.8  | A    |
|                             |  | $T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a>   | -   | -   | 10.48 | A    |
| $I_{DM}$                    | peak drain current                           | $T_{mb} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed;<br>see <a href="#">Figure 3</a>  | -   | -   | 59    | A    |
| $P_{tot}$                   | total power dissipation                      | $T_{mb} = 25\text{ °C}$   | -   | -   | 59    | W    |
| $T_{stg}$                   | storage temperature                          |   | -55   | -   | 175   | °C   |
| $T_j$                       | junction temperature                         |   | -55   | -   | 175   | °C   |
| <b>Source-drain diode</b>   |  |   |   |     |       |      |
| $I_S$                       | source current                               | $T_{mb} = 25\text{ °C}$   | -   | -   | 14.8  | A    |
| $I_{SM}$                    | peak source current                          | $t_p \leq 10\text{ ms}$ ; pulsed; $T_{mb} = 25\text{ °C}$   | -   | -   | 59    | A    |
| <b>Avalanche ruggedness</b> |  |   |   |     |       |      |
| $E_{DS(AL)S}$               | non-repetitive drain-source avalanche energy | $I_D = 14.8\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ;<br>$V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped | -   | -   | 35    | mJ   |
| $E_{DS(AL)R}$               | repetitive drain-source avalanche energy     | see <a href="#">Figure 2</a>  | <a href="#">[1]</a> <a href="#">[2]</a> <a href="#">[3]</a> | -   | -     | J    |
|                             |  |   | <a href="#">[4]</a>   |     |       |      |

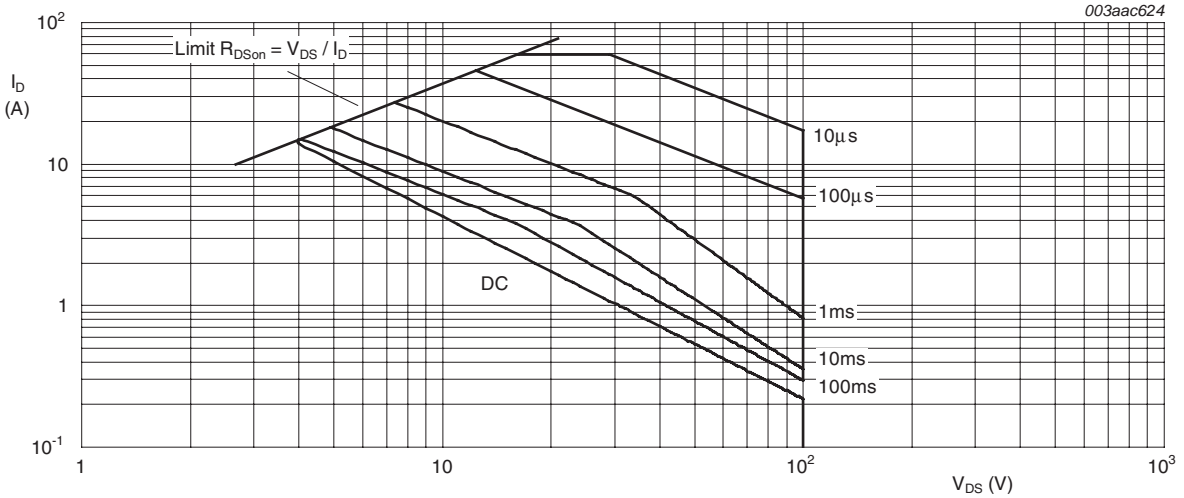
- [1] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.  
 [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.  
 [3] Repetitive avalanche rating limited by an average junction temperature of 170 °C.  
 [4] Refer to application note AN10273 for further information.



**Fig 1. Continuous drain current as a function of mounting base temperature**



**Fig 2. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time**



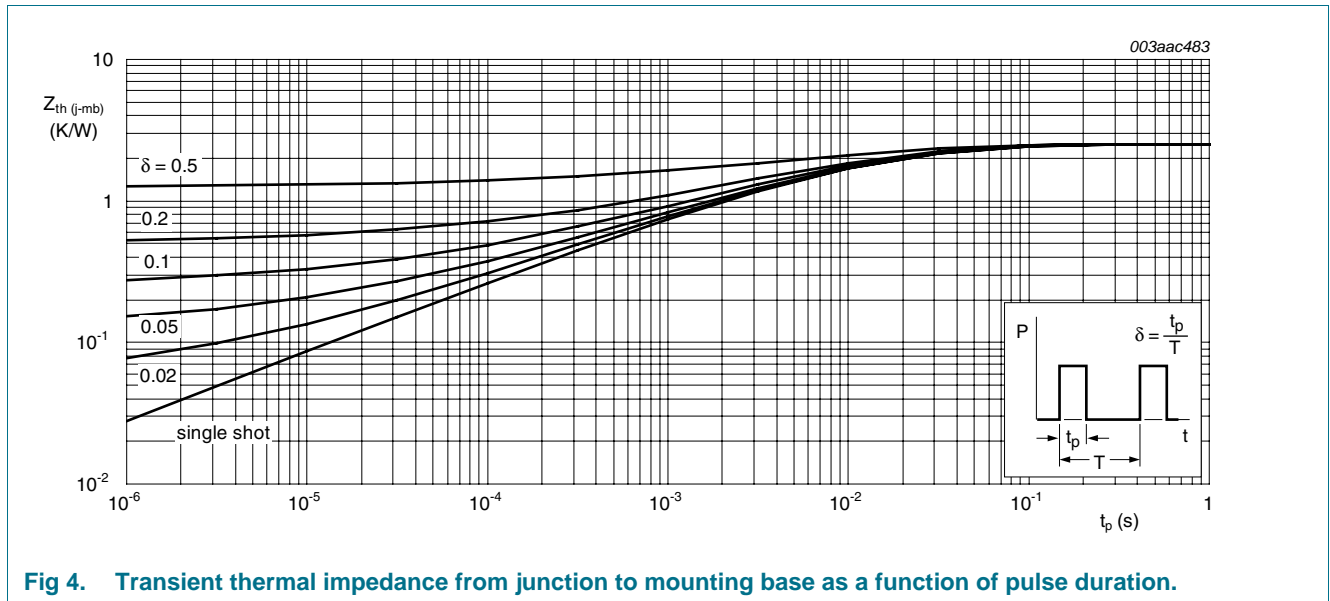
$T_{mb} = 25^\circ\text{C}; I_{DM}$  is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

**5. Thermal characteristics**

**Table 5. Thermal characteristics**

| Symbol         | Parameter   | Conditions                   | Min | Typ | Max  | Unit |
|----------------|---|------------------------------|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see <a href="#">Figure 4</a> | -   | -   | 2.53 | K/W  |

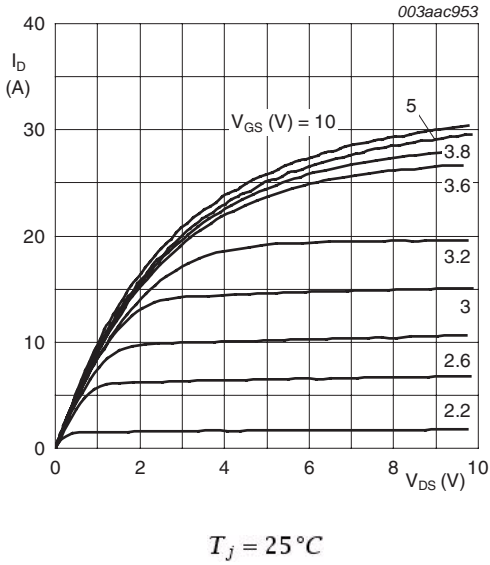


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

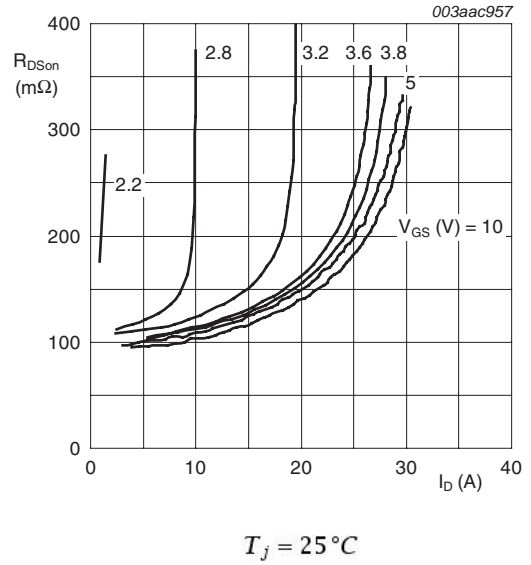
## 6. Characteristics

Table 6. Characteristics

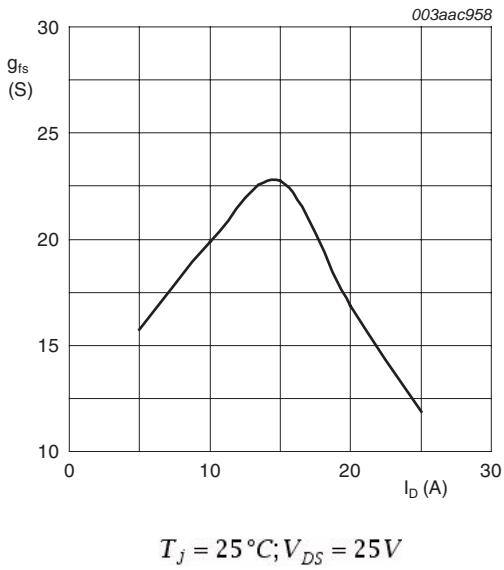
| Symbol                         | Parameter                        | Conditions   | Min  | Typ  | Max  | Unit          |
|--------------------------------|----------------------------------|--|------|------|------|---------------|
| <b>Static characteristics</b>  |                                  |  |      |      |      |               |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage   | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | 100  | -    | -    | V             |
|                                |                                  | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$  | 90   | -    | -    | V             |
| $V_{GS(th)}$                   | gate-source threshold voltage    | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>      | 1.25 | 1.65 | 2.15 | V             |
| $V_{GSth}$                     | gate-source threshold voltage    | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>     | 0.5  | -    | -    | V             |
|                                |                                  | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>     | -    | -    | 2.45 | V             |
| $I_{DSS}$                      | drain leakage current            | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -    | 0.02 | 1    | $\mu\text{A}$ |
| $I_{GSS}$                      | gate leakage current             | $V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | -    | 2    | 100  | nA            |
|                                |                                  | $V_{DS} = 0 \text{ V}; V_{GS} = -15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -    | 2    | 100  | nA            |
| $R_{DS(on)}$                   | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$  | -    | 86   | 99   | m $\Omega$    |
|                                |                                  | $V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 11</a>                                | -    | -    | 270  | m $\Omega$    |
|                                |                                  | $V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$   | -    | -    | 107  | m $\Omega$    |
|                                |                                  | $V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a> | -    | 91   | 104  | m $\Omega$    |
| $I_{DSS}$                      | drain leakage current            | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$   | -    | -    | 500  | $\mu\text{A}$ |
| <b>Dynamic characteristics</b> |                                  |  |      |      |      |               |
| $Q_{G(tot)}$                   | total gate charge                | $I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V};$<br>see <a href="#">Figure 13</a>   | -    | 11   | -    | nC            |
| $Q_{GS}$                       | gate-source charge               |  | -    | 1.7  | -    | nC            |
| $Q_{GD}$                       | gate-drain charge                |  | -    | 4.7  | -    | nC            |
| $C_{iss}$                      | input capacitance                | $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$<br>$T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>        | -    | 854  | 1139 | pF            |
| $C_{oss}$                      | output capacitance               |  | -    | 87   | 105  | pF            |
| $C_{rss}$                      | reverse transfer capacitance     |  | -    | 42   | 58   | pF            |
| $t_{d(on)}$                    | turn-on delay time               | $V_{DS} = 30 \text{ V}; R_L = 6 \text{ } \Omega; V_{GS} = 5 \text{ V};$<br>$R_{G(ext)} = 10 \text{ } \Omega$                                 | -    | 15   | -    | ns            |
| $t_r$                          | rise time                        |  | -    | 8    | -    | ns            |
| $t_{d(off)}$                   | turn-off delay time              |  | -    | 36   | -    | ns            |
| $t_f$                          | fall time                        |  | -    | 6    | -    | ns            |
| <b>Source-drain diode</b>      |                                  |  |      |      |      |               |
| $V_{SD}$                       | source-drain voltage             | $I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 15</a>                                 | -    | 0.85 | 1.2  | V             |
| $t_{rr}$                       | reverse recovery time            | $I_S = 20 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$  | -    | 79   | -    | ns            |
| $Q_r$                          | recovered charge                 | $V_{DS} = 30 \text{ V}$  | -    | 190  | -    | nC            |



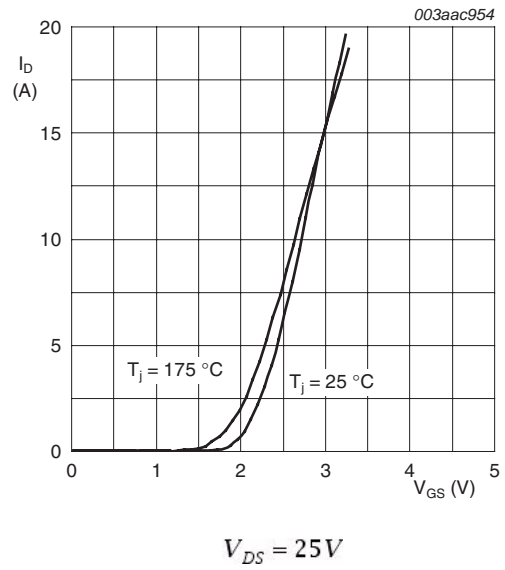
**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



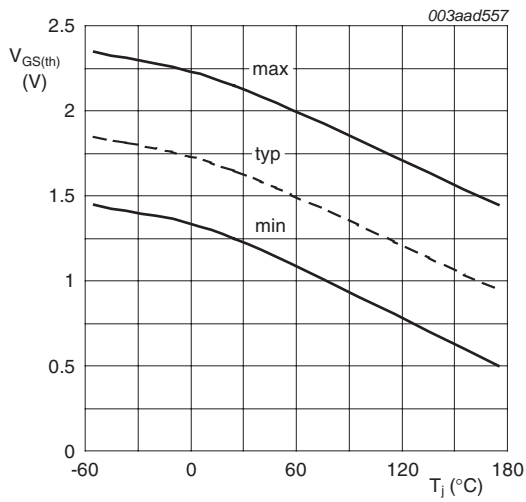
**Fig 6. Drain-source on-state resistance as a function of drain current; typical values.**



**Fig 7. Forward transconductance as a function of drain current; typical values.**

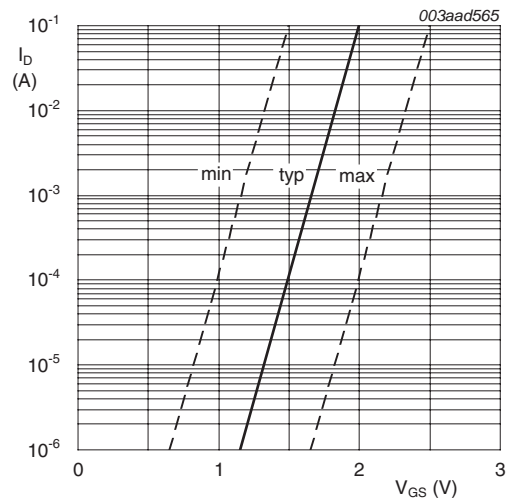


**Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



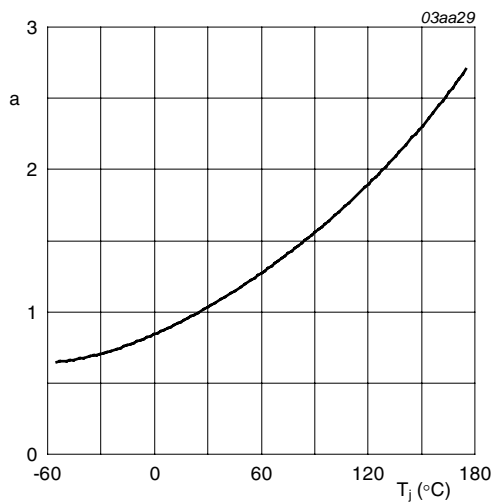
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



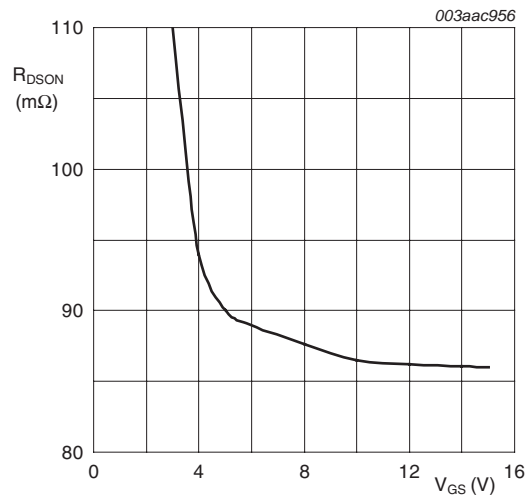
$$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

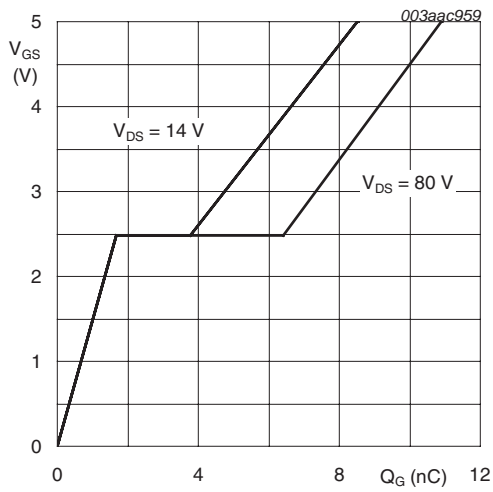
**Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature**



$$T_j = 25^\circ\text{C}; I_D = 5\text{A}$$

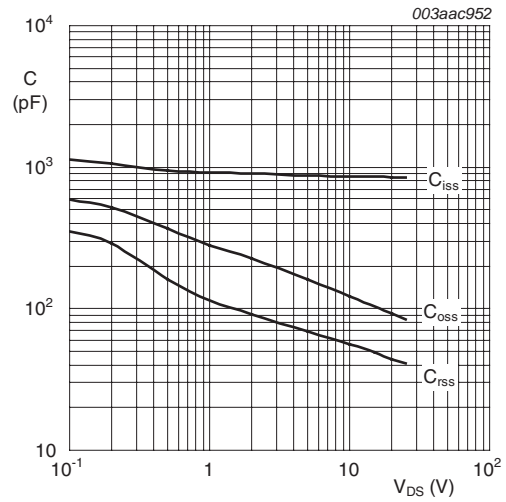
**Fig 12. Drain-source on-state resistance as a function of gate-source voltage; typical values.**





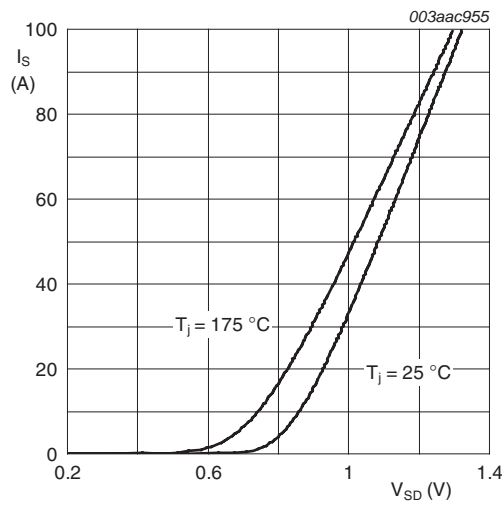
$T_j = 25\text{ }^\circ\text{C}; I_D = 5\text{ A}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



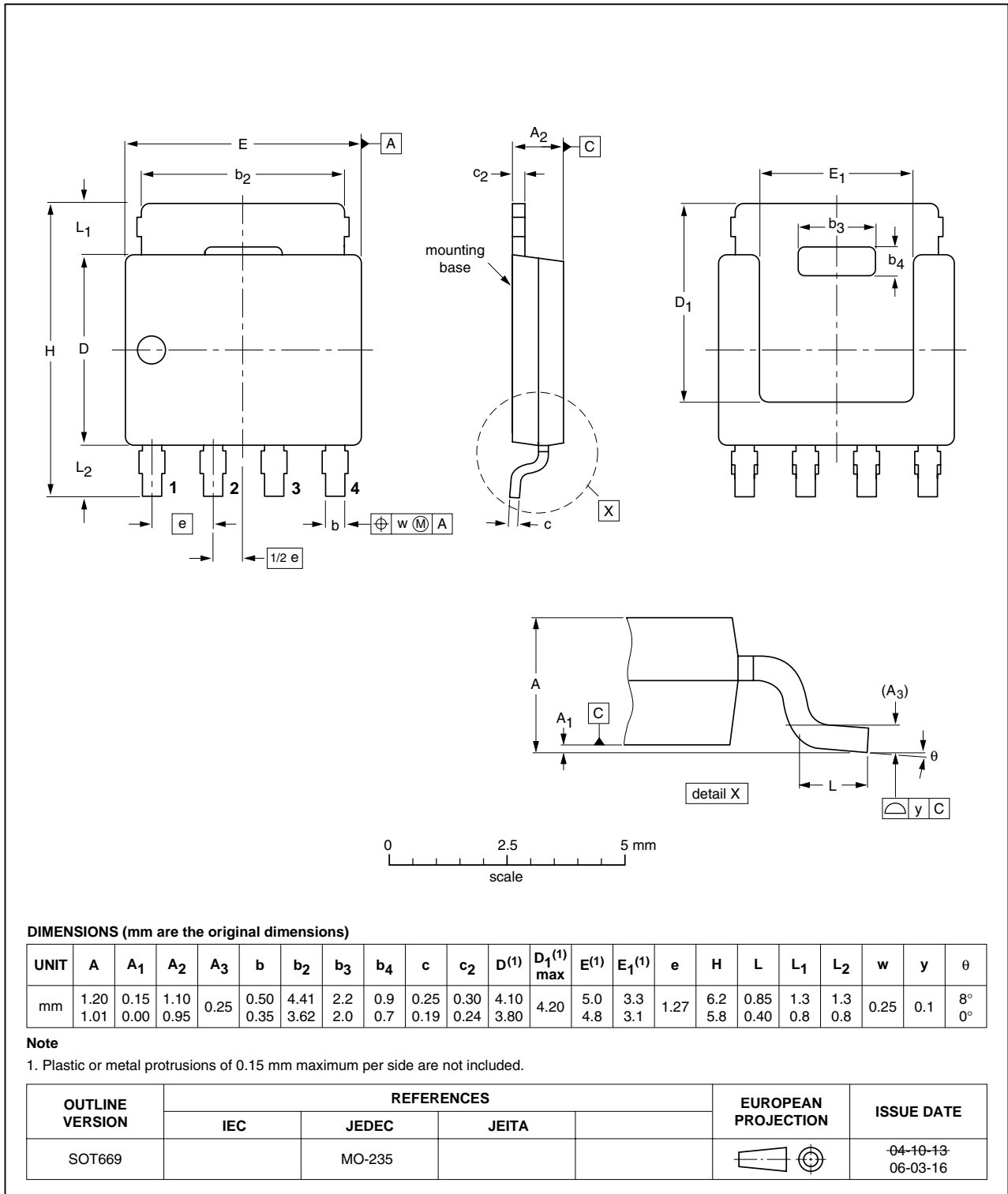
$V_{GS} = 0\text{ V}$

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**

**7. Package outline**

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669



**Fig 16. Package outline SOT669 (LFPAK)**

## 8. Revision history

Table 7. Revision history

| Document ID     | Release date                                | Data sheet status    | Change notice | Supersedes      |
|-----------------|---|----------------------|---------------|-----------------|
| BUK9Y104-100B_4 | 20100407                                    | Product data sheet   | -             | BUK9Y104-100B_3 |
| Modifications:  | • Status changed from objective to product. |                      |               |                 |
| BUK9Y104-100B_3 | 20100211                                    | Objective data sheet | -             | BUK9Y104-100B_2 |

## 9. Legal information

### 9.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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