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Kind regards,

Team Nexperia



# BUK9840-55

## N-channel TrenchMOS logic level FET

16 March 2016

Product data sheet

### 1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 2. Features and benefits

- AEC Q101 compliant
- Electrostatically robust due to integrated protection diodes
- Low conduction losses due to low on-state resistance

### 3. Applications

- Automotive and general purpose power switching

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	55	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$	-	-	10.7	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C};$ <a href="#">Fig. 4</a>	-	-	8.3	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}$	-	30	40	m $\Omega$
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 3.6\text{ A}; V_{sup} \leq 25\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 5\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	-	60	mJ

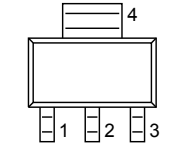
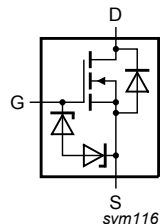


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## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SC-73 (SOT223)</p>	
2	D	drain		
3	S	source		
4	D	drain		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK9840-55	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223
BUK9840-55/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
BUK9840-55	94055
BUK9840-55/CU	xxYWW 94055

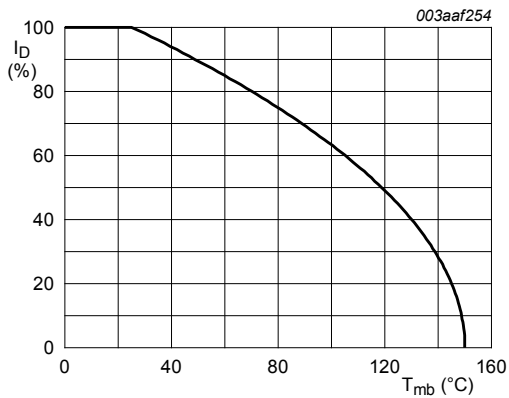
## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	55	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage		-10	10	V
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}; \text{Fig. 4}$	-	8.3	W
$I_D$	drain current	$T_{sp} = 25\text{ °C}$	-	10.7	A
		$T_{sp} = 100\text{ °C}$	-	6.8	A

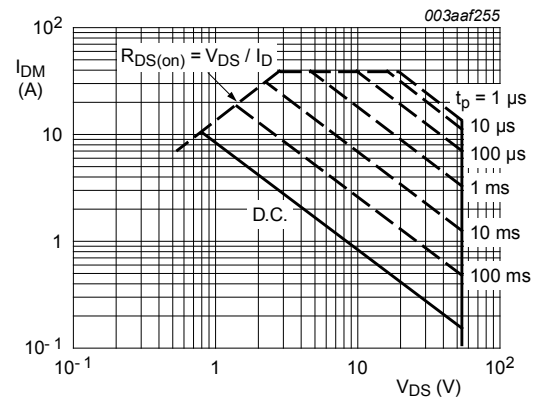
Symbol	Parameter	Conditions	Min	Max	Unit
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$ ; pulsed	-	40	A
$T_{stg}$	storage temperature		-55	150	$^{\circ}\text{C}$
$T_j$	junction temperature		-55	150	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	10.7	A
$I_{SM}$	peak source current	pulsed; $T_{sp} = 25\text{ }^{\circ}\text{C}$	-	40	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 3.6\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; unclamped	-	60	mJ
<b>Electrostatic discharge</b>					
$V_{esd}$	electrostatic discharge voltage	HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$	-	2	kV



$V_{GS} \geq 10\text{ V}$

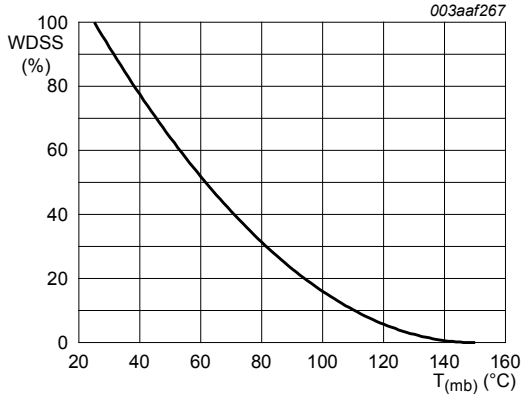
**Fig. 1. Normalized continuous drain current as a function of solder point temperature**

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$



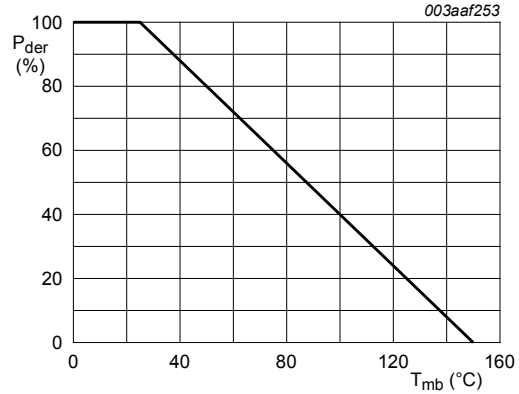
$T_{sp} = 25\text{ }^{\circ}\text{C}$ ;  $I_{DM}$  is single pulse

**Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**



$I_D = 3.6 \text{ A}$

**Fig. 3. Normalised drain-source non-repetitive avalanche energy rating; avalanche energy as a function of mounting base temperature**



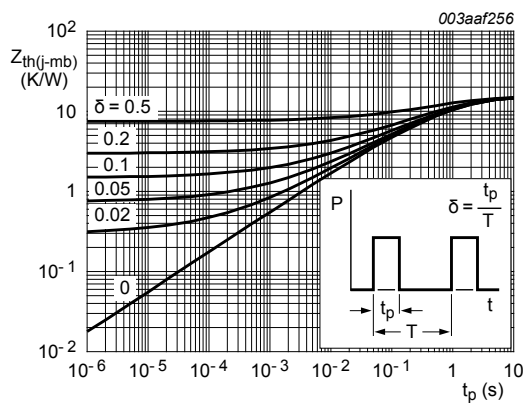
**Fig. 4. Normalized total power dissipation as a function of solder point temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Mounted on any printed-circuit board	-	12	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Mounted on a printed-circuit	-	120	-	K/W

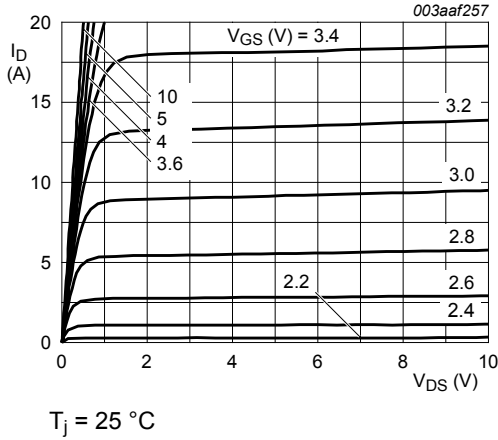


**Fig. 5. Transient thermal impedance from junction to solder point as a function of pulse duration**

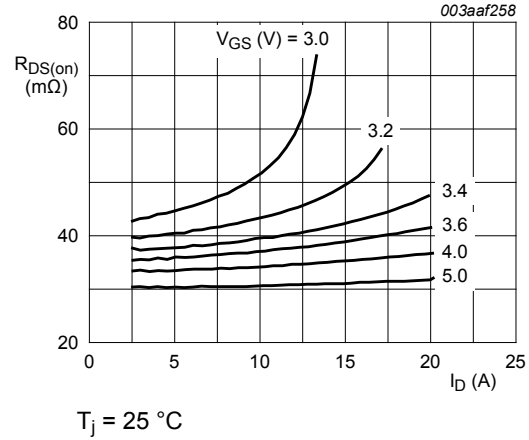
## 10. Characteristics

Table 7. Characteristics

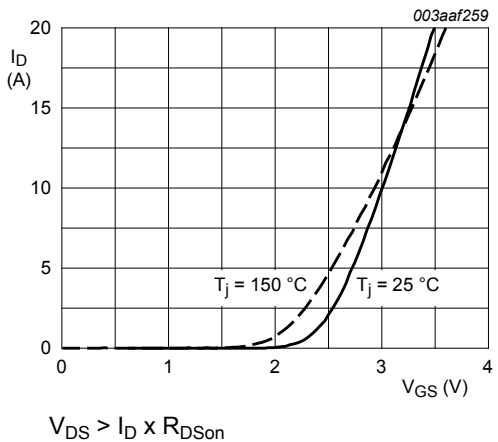
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$	0.6	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
		$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	5	$\mu\text{A}$
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	5	$\mu\text{A}$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	-	74	$\text{m}\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	30	40	$\text{m}\Omega$
$V_{(BR)GSS}$	gate-source breakdown voltage	$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = 1 \text{ mA}$	10	-	-	V
		$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = -1 \text{ mA}$	10	-	-	V
<b>Dynamic characteristics</b>						
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	1050	1400	pF
$C_{oss}$	output capacitance		-	205	245	pF
$C_{rss}$	reverse transfer capacitance		-	110	150	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 3.3 \text{ }\Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 10 \text{ }\Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 9 \text{ A}$	-	17	25	ns
$t_r$	rise time		-	65	100	ns
$t_{d(off)}$	turn-off delay time		-	70	105	ns
$t_f$	fall time		-	70	105	ns
$g_{fs}$	transfer conductance	$V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	11	19	-	S
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.85	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 5 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s};$	-	45	-	ns
$Q_r$	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.3	-	$\mu\text{C}$



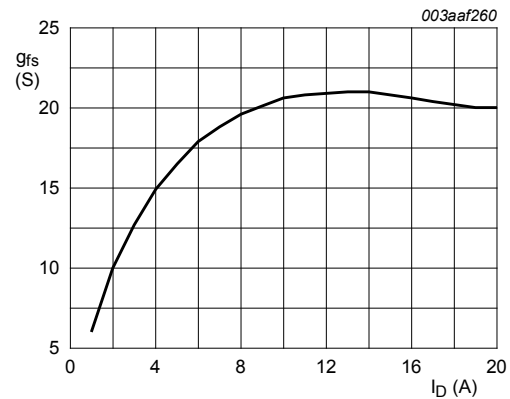
**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



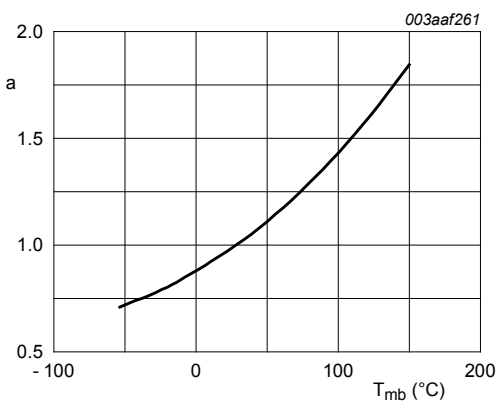
**Fig. 7. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

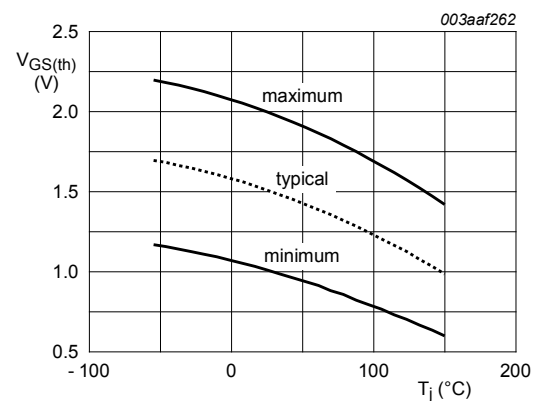


**Fig. 9. Forward transconductance as a function of drain current; typical values**

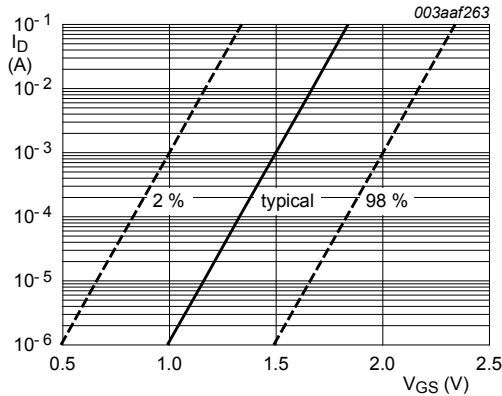


**Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

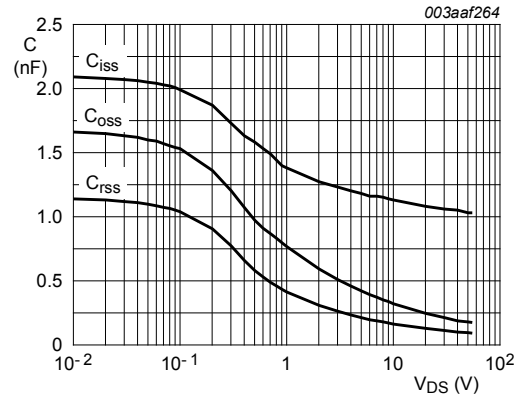


**Fig. 11. Gate-source threshold voltage as a function of junction temperature**



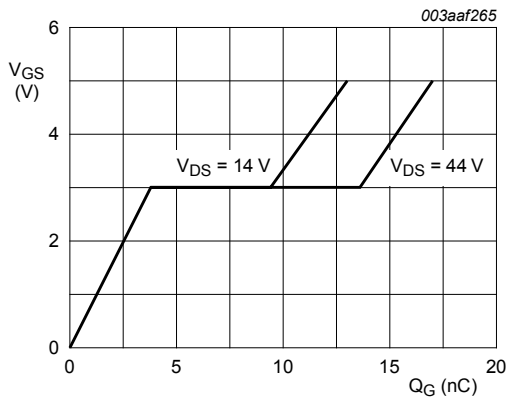
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$

**Fig. 12. Sub-threshold drain current as a function of gate-source voltage**



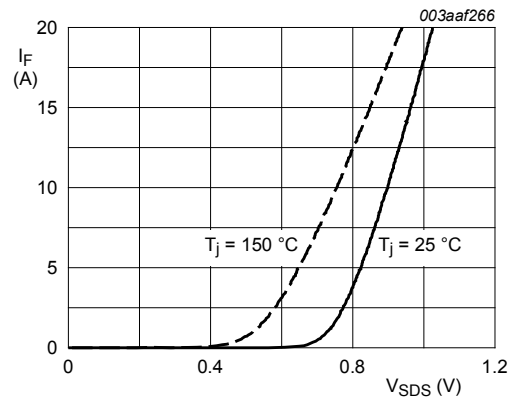
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$T_j = 25\text{ }^\circ\text{C}; I_D = 9\text{ A}$

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{ V}$

**Fig. 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



### 11. Package outline

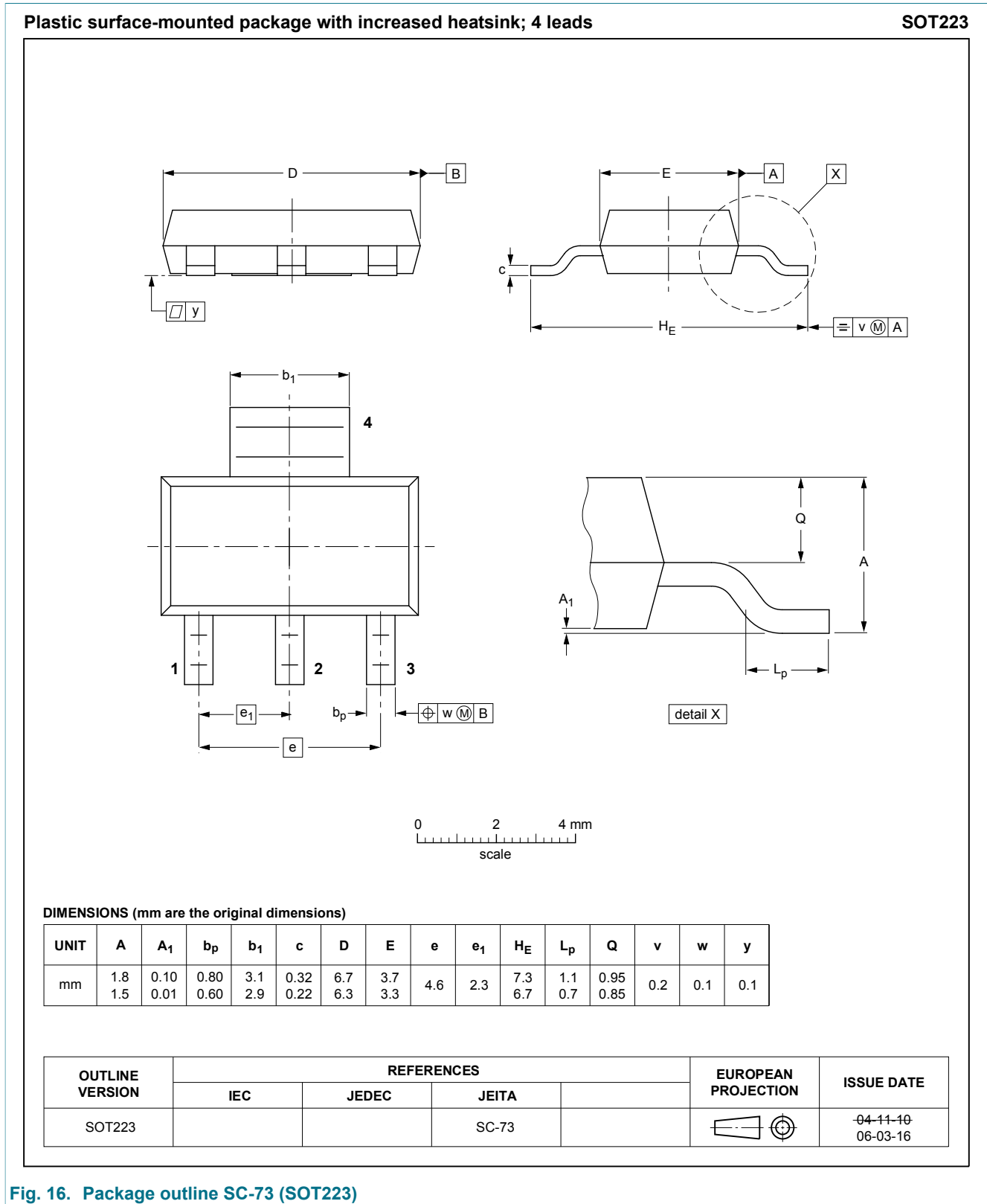


Fig. 16. Package outline SC-73 (SOT223)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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