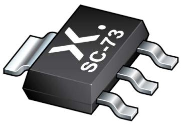

BUK98180-100A

N-channel TrenchMOS logic level FET

16 March 2016 **Product data sheet**

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources

3. Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 150 °C		-	-	100	V
I_D	drain current	V_{GS} = 5 V; T_{sp} = 25 °C; Fig. 2; Fig. 3		-	-	4.6	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Fig. 1		-	-	8	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C		-	147	173	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C		-	-	201	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; Fig. 12; Fig. 13		-	153	180	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 4 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	16	mJ

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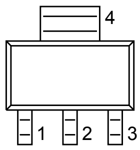
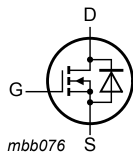
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **SC-73 (SOT223)**	
2	D	drain		
3	S	source		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK98180-100A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223
BUK98180-100A/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK98180-100A	918010
BUK98180-100A/CU	918010

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ		-	100	V
V_{GS}	gate-source voltage			-10	10	V
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; Fig. 1		-	8	W
I_D	drain current	$T_{sp} = 25$ °C; $V_{GS} = 5$ V; Fig. 2; Fig. 3		-	4.6	A
		$T_{sp} = 100$ °C; $V_{GS} = 5$ V; Fig. 2		-	3	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs; Fig. 3		-	18	A

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
V_{GSM}	peak gate-source voltage	pulsed; $t_p \leq 50$ µs		-15	15	V
Source-drain diode						
I_S	source current	$T_{sp} = 25$ °C		-	4.6	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; $T_{sp} = 25$ °C		-	18	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 4$ A; $V_{sup} \leq 100$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped		-	16	mJ

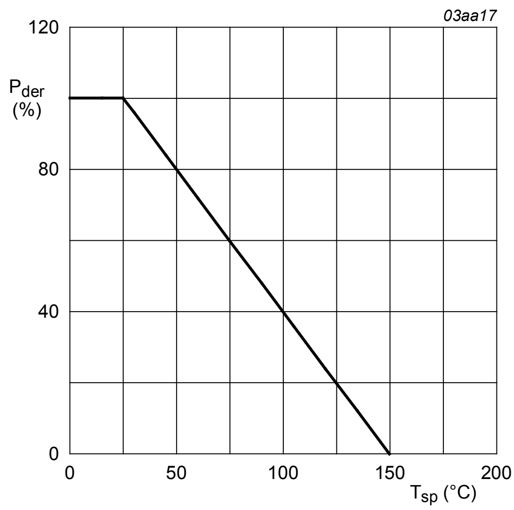


Fig. 1. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

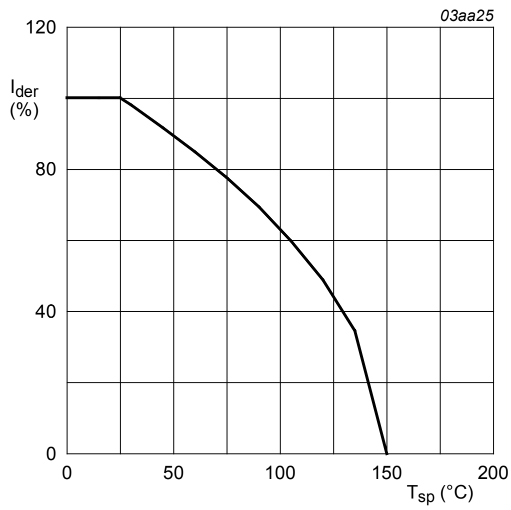


Fig. 2. Normalized continuous drain current as a function of solder point temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

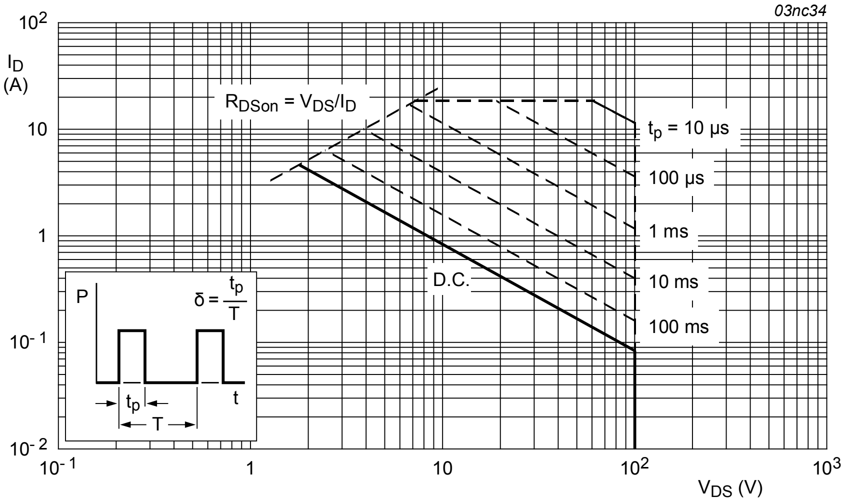


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{amb} = 25°C$; I_{DM} is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 4		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient			-	120	-	K/W

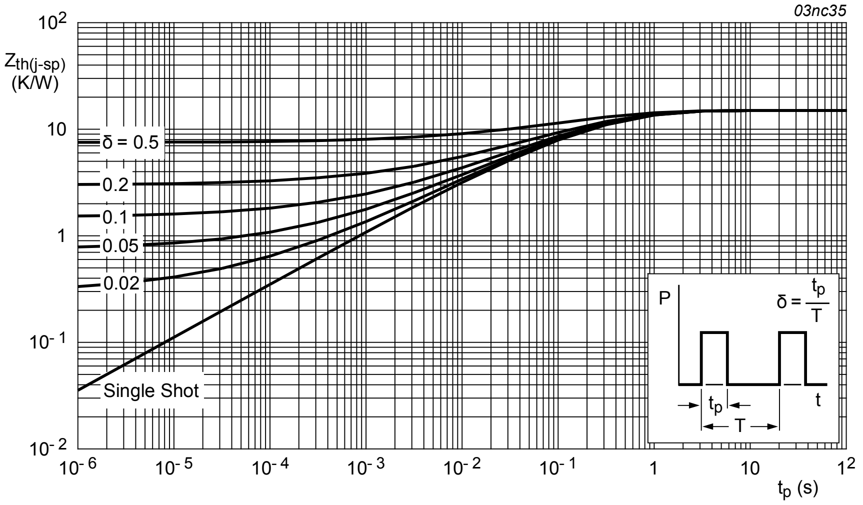


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C		89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 11		1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 11		-	-	2.3	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; Fig. 11		0.6	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 150 °C		-	-	500	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.05	10	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C		-	147	173	mΩ
		V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C		-	-	201	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; Fig. 12; Fig. 13		-	153	180	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 150 °C; Fig. 12; Fig. 13		-	-	389	mΩ
Dynamic characteristics							
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	464	619	pF
C_{oss}	output capacitance			-	60	72	pF
C_{rss}	reverse transfer capacitance			-	36	50	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C		-	7	-	ns
t_r	rise time			-	89	-	ns
$t_{d(off)}$	turn-off delay time			-	18	-	ns
t_f	fall time			-	25	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C		-	49	-	ns
Q_r	recovered charge			-	130	-	nC

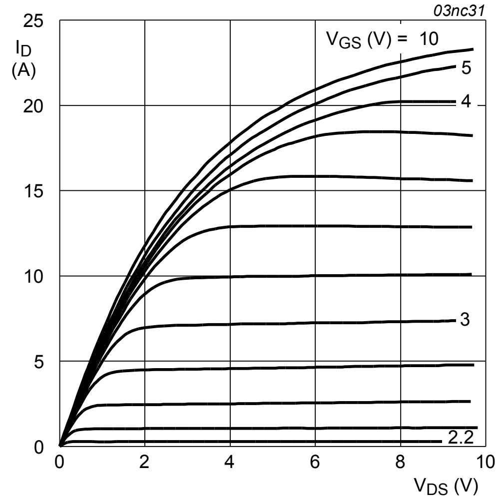


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

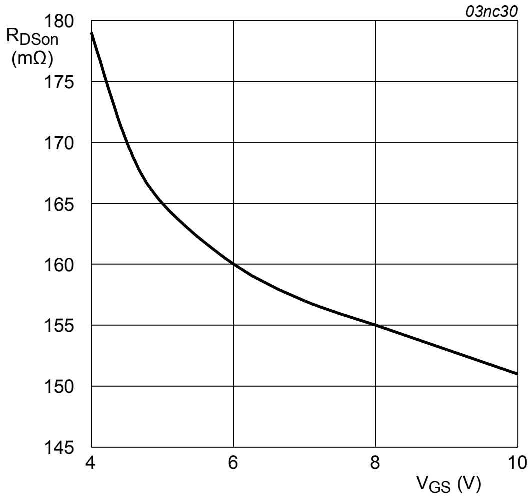
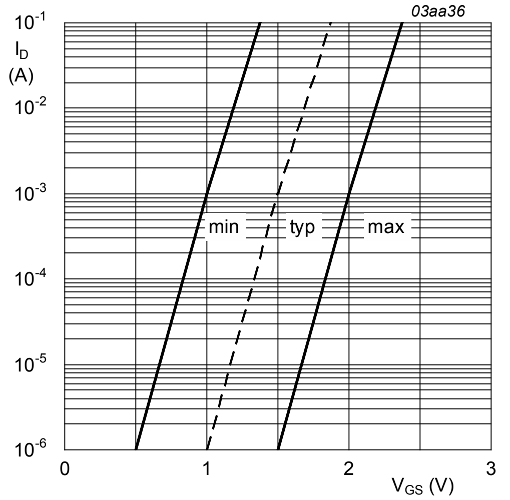


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C; I_D = 5A$



T_j = 25 °C; V_{DS} = 5 V

Fig. 7. Sub-threshold drain current as a function of gate-source voltage

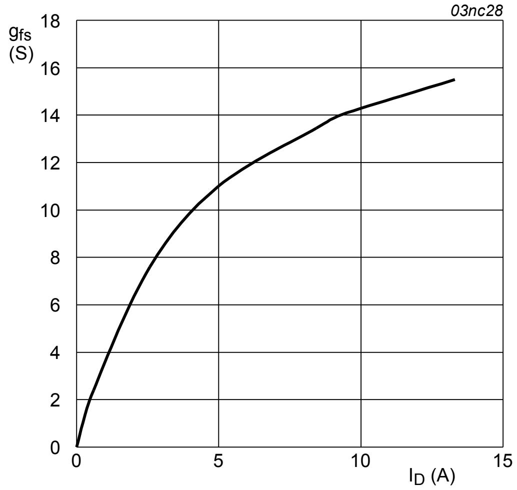


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25°C; V_{DS} = 25V$

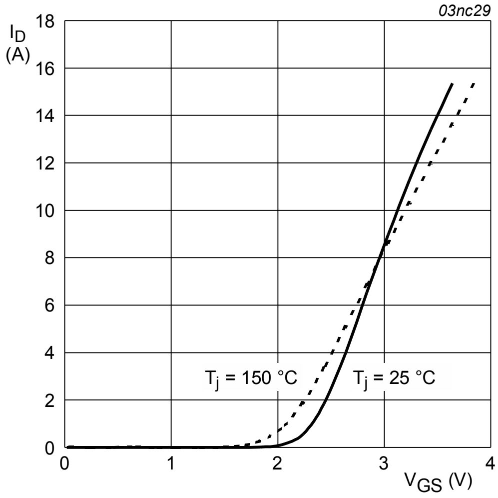


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 25V$

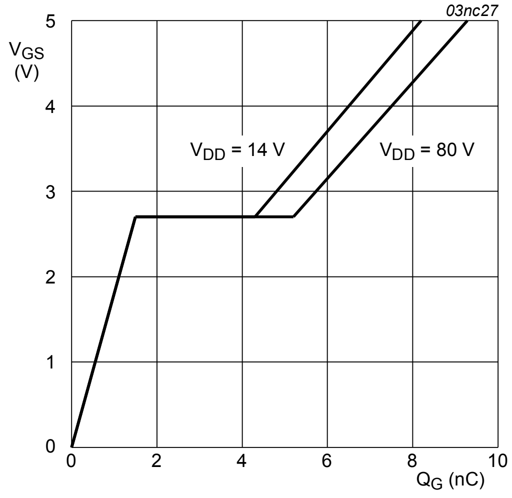


Fig. 10. Gate-source voltage as a function of turn-on gate charge; typical values

$T_j = 25°C; I_D = 5A$

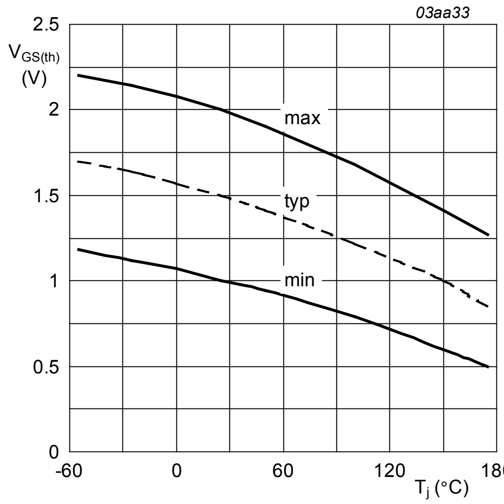


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$I_D = 1mA; V_{DS} = V_{GS}$

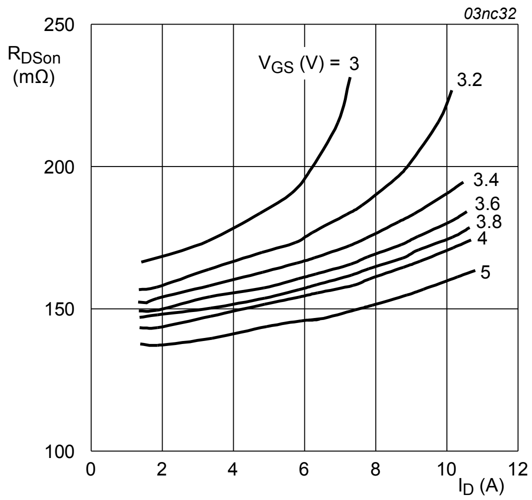


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

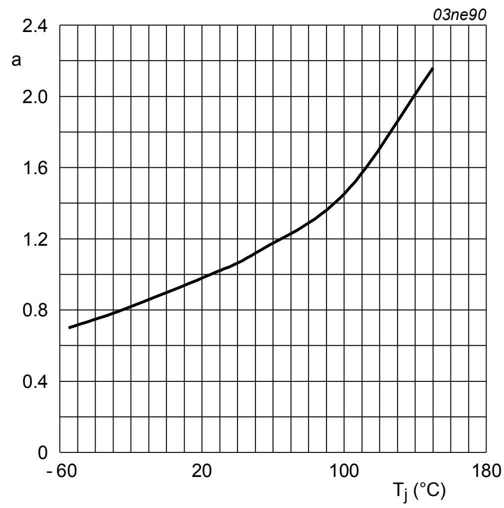


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

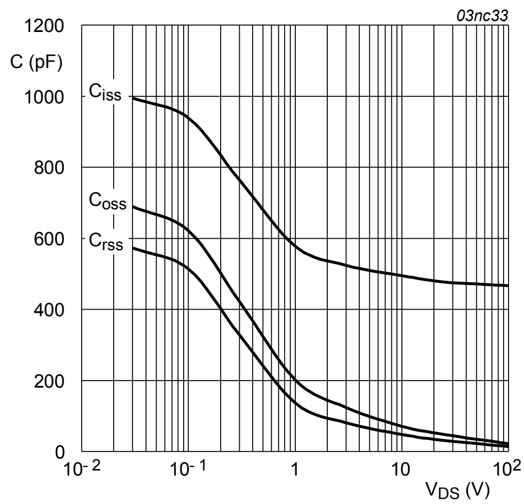


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

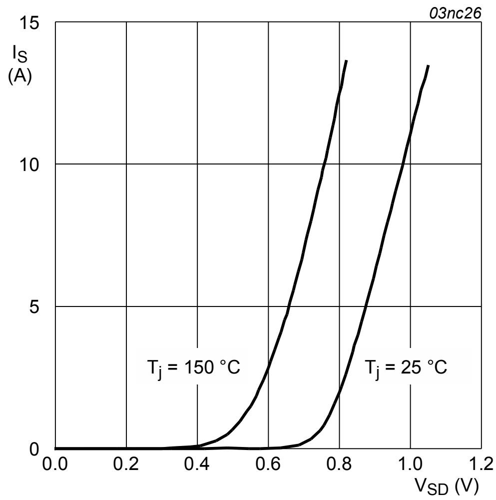
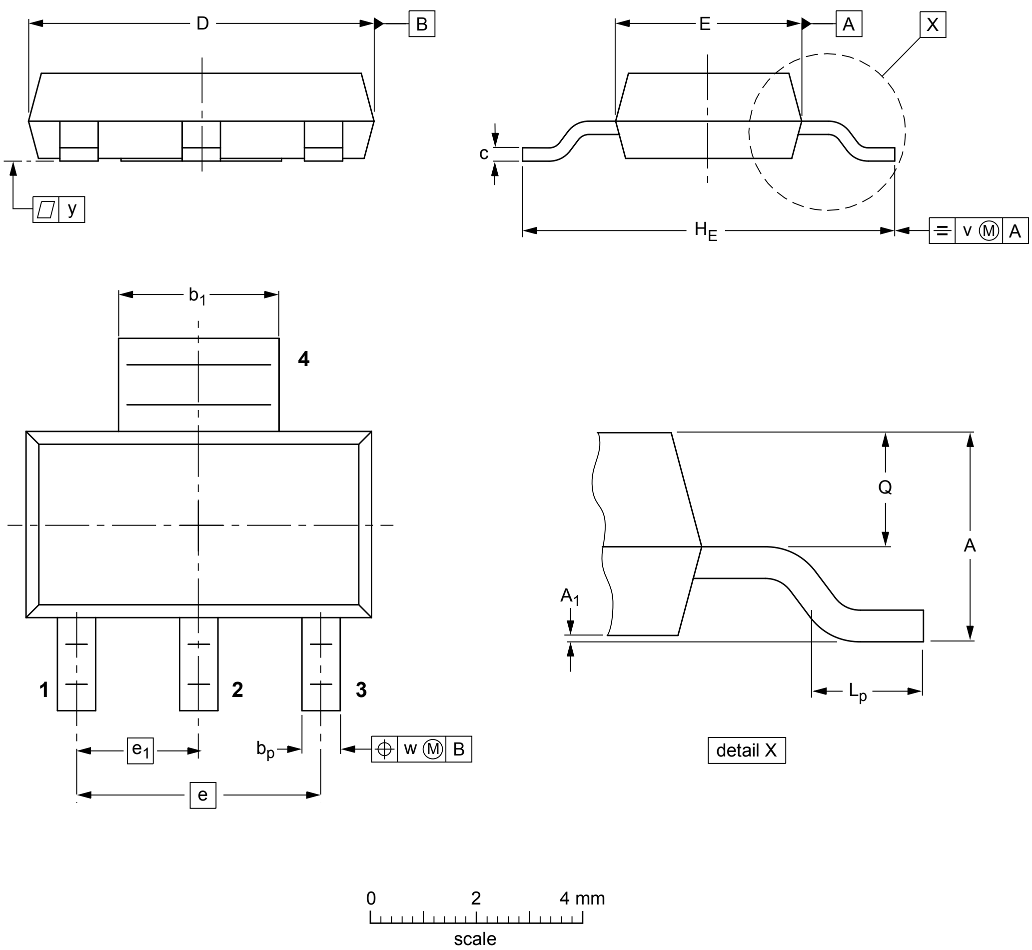


Fig. 15. Reverse diode current as a function of reverse diode voltage; typical value

$$V_{GS} = 0V$$

11. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig. 16. Package outline SC-73 (SOT223)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents