



BUK9675-100A

N-channel TrenchMOS logic level FET

18 August 2015

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance

3. Applications

- Automotive and general purpose power switching

4. Quick reference data

Table 1. Quick reference data

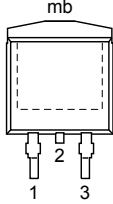
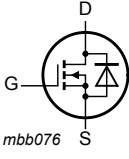
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|--|------------------------|-----|-----|------------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$ | - | - | 100 | V |
| I_D | drain current | $V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 | - | - | 23 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | - | 98 | W |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | - | 55 | 72 | m Ω |
| | | $V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | - | 60 | 75 | m Ω |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 23\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4 | [1][2] | - | 100 | mJ |

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[2] Refer to application note AN10273 for further information.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|---|---|
| 1 | G | gate |  <p>D2PAK (SOT404)</p> |  |
| 2 | D | drain | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|---------|--|---------|
| | Name | Description | Version |
| BUK9675-100A | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|--------------|--------------|
| BUK9675-100A | BUK9675-100A |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$ | - | 100 | V |
| V_{DGR} | drain-gate voltage | $R_{GS} = 20\text{ k}\Omega$ | - | 100 | V |
| V_{GS} | gate-source voltage | | -15 | 15 | V |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | 98 | W |
| I_D | drain current | $T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2 | - | 16 | A |
| | | $T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2 | - | 23 | A |
| I_{DM} | peak drain current | $T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3 | - | 92 | A |
| T_{stg} | storage temperature | | -55 | 175 | °C |
| T_j | junction temperature | | -55 | 175 | °C |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|---|--------|-----|--------|
| Source-drain diode | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | - | 23 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\ \mu\text{s}$; $T_{mb} = 25\text{ °C}$ | - | 92 | A |
| Avalanche ruggedness | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 23\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped; Fig. 4 | [1][2] | - | 100 mJ |

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.

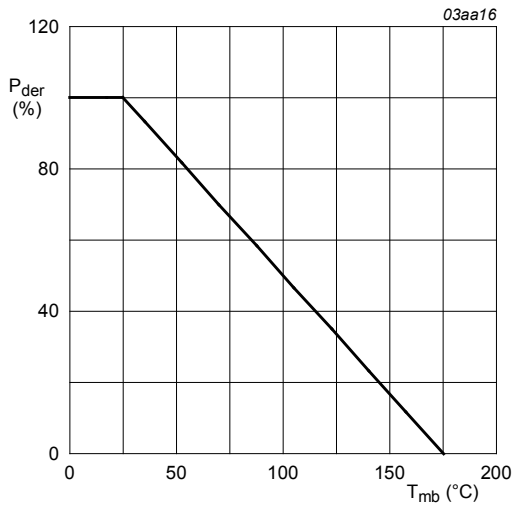
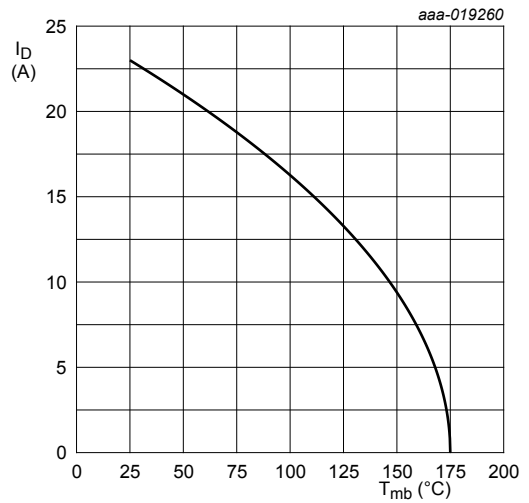


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$



$V_{GS} \geq 5\text{ V}$

Fig. 2. Continuous drain current as a function of mounting base temperature

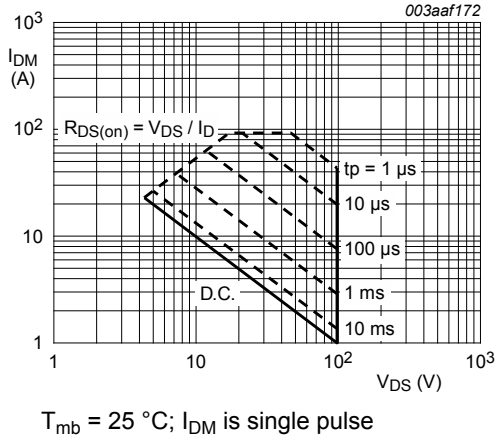


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

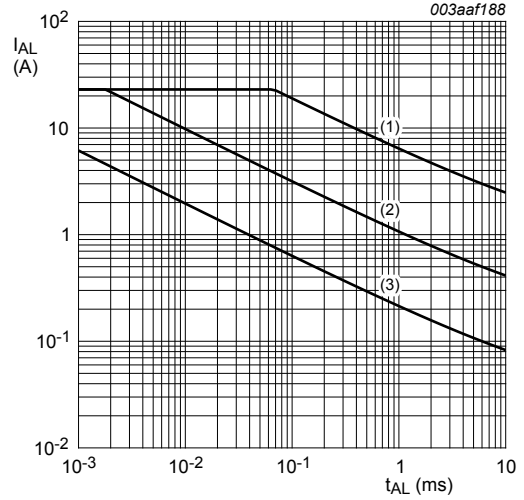


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------------------------|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | | - | - | 1.5 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Minimum footprint; FR4 board | - | 50 | - | K/W |

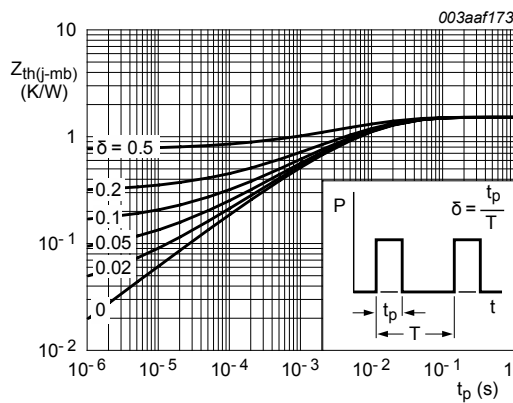


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|------|------|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | 100 | - | - | V |
| | | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ | 89 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 10 | 0.5 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10 ; Fig. 11 | 1 | 1.5 | 2 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 10 | - | - | 2.3 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$ | - | - | 500 | μA |
| | | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 0.05 | 10 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 2 | 100 | nA |
| | | $V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 2 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 12 | - | 55 | 72 | m Ω |
| | | $V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 13 | - | - | 188 | m Ω |
| | | $V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 12 | - | 61 | 84 | m Ω |
| | | $V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 12 | - | 60 | 75 | m Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 10 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V};$ Fig. 14 ; Fig. 15 | - | 24.3 | - | nC |
| Q_{GS} | gate-source charge | | - | 3 | - | nC |
| Q_{GD} | gate-drain charge | | - | 12.2 | - | nC |
| C_{iss} | input capacitance | $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 16 | - | 1278 | 1704 | pF |
| C_{oss} | output capacitance | | - | 129 | 155 | pF |
| C_{rss} | reverse transfer capacitance | | - | 88 | 120 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ }^\circ\Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ }^\circ\Omega; T_j = 25 \text{ }^\circ\text{C}$ | - | 13 | 20 | ns |
| t_r | rise time | | - | 120 | 168 | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 58 | 87 | ns |
| t_f | fall time | | - | 57 | 86 | ns |
| L_D | internal drain inductance | from drain lead 6 mm from package to centre of die; $T_j = 25 \text{ }^\circ\text{C}$ | - | 4.5 | - | nH |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|----------------------------|--|-----|------|-----|------|
| | | from upper edge of drain tab to centre of die; $T_j = 25\text{ }^\circ\text{C}$ | - | 2.5 | - | nH |
| L_S | internal source inductance | from source lead to source bond pad; $T_j = 25\text{ }^\circ\text{C}$ | - | 7.5 | - | nH |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 17 | - | 0.85 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; | - | 53.7 | - | ns |
| Q_r | recovered charge | $V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$ | - | 126 | - | nC |

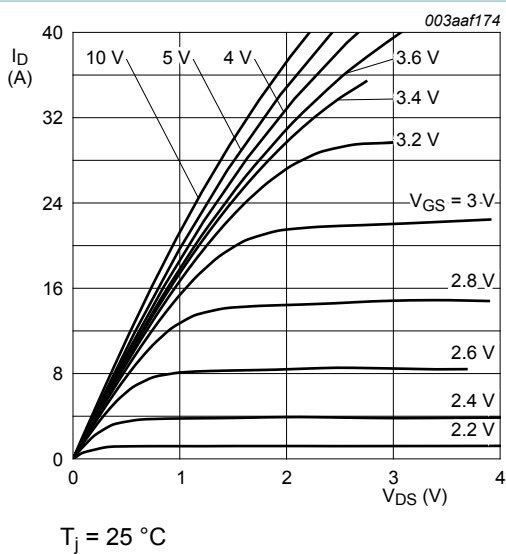


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

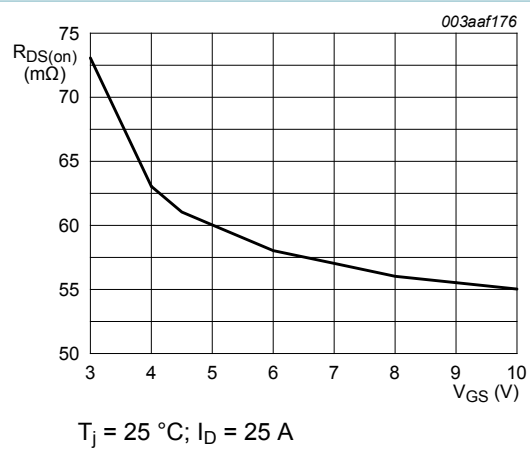


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

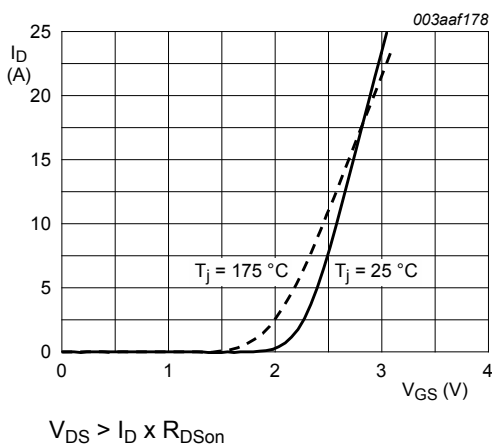


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

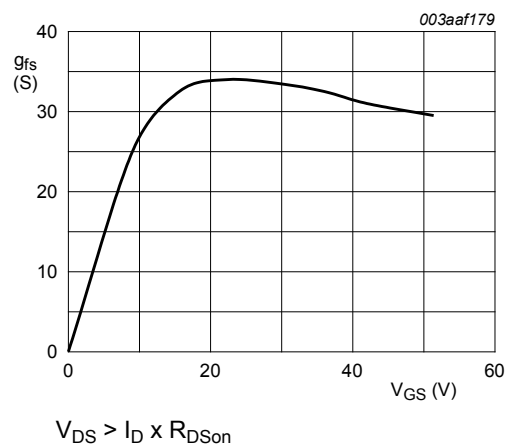


Fig. 9. Forward transconductance as a function of drain current; typical values

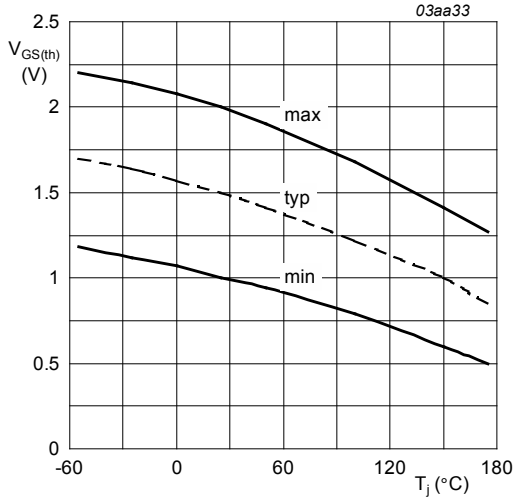
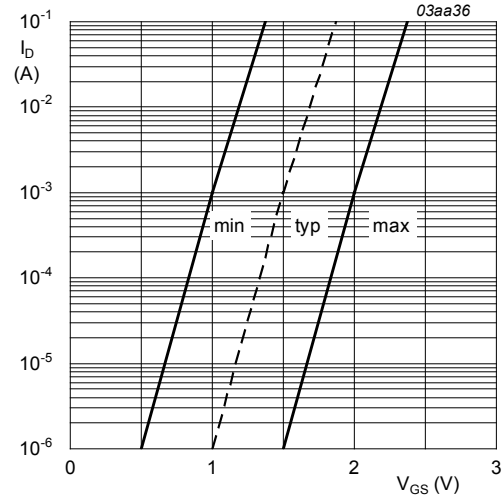


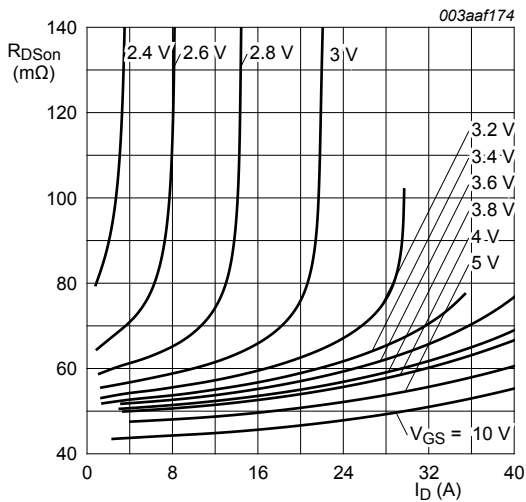
Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$



$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$$

Fig. 11. Sub-threshold drain current as a function of gate-source voltage



$$T_j = 25\text{ }^\circ\text{C}$$

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

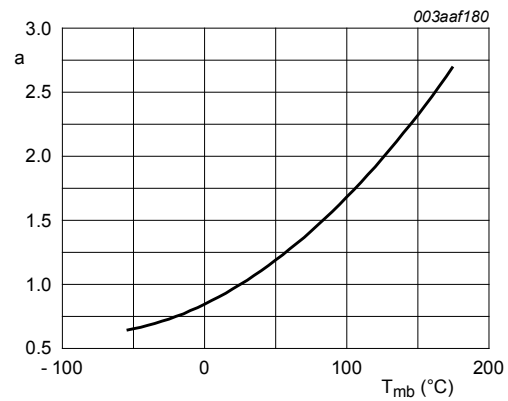


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

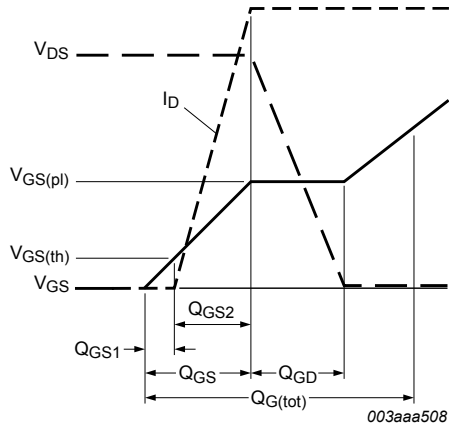
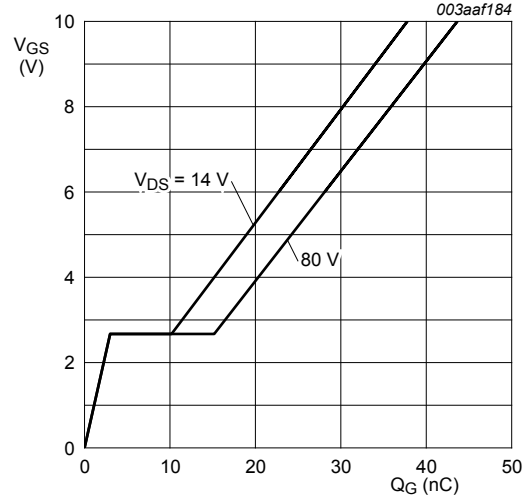
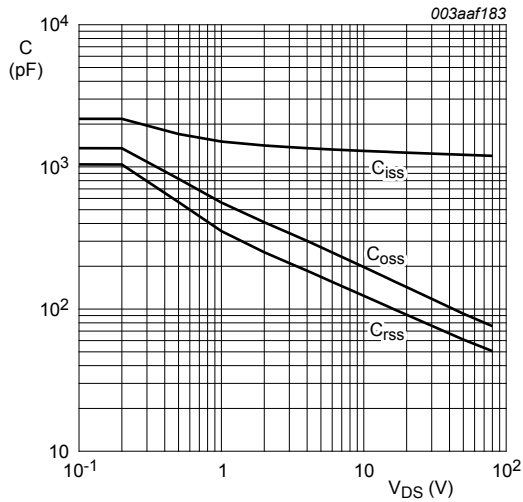


Fig. 14. Gate charge waveform definitions



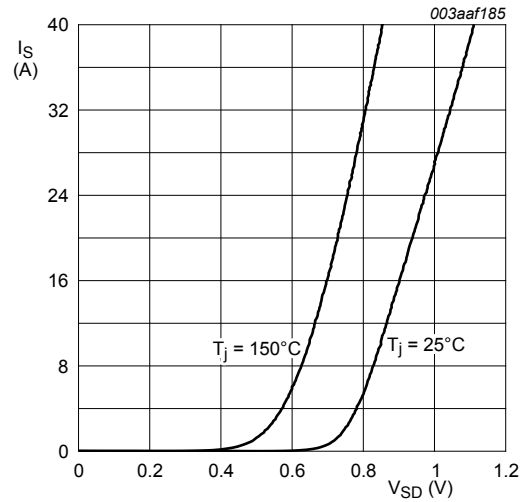
$T_j = 25^\circ\text{C}$; $I_D = 10$ A

Fig. 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0$ V; $f = 1$ MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

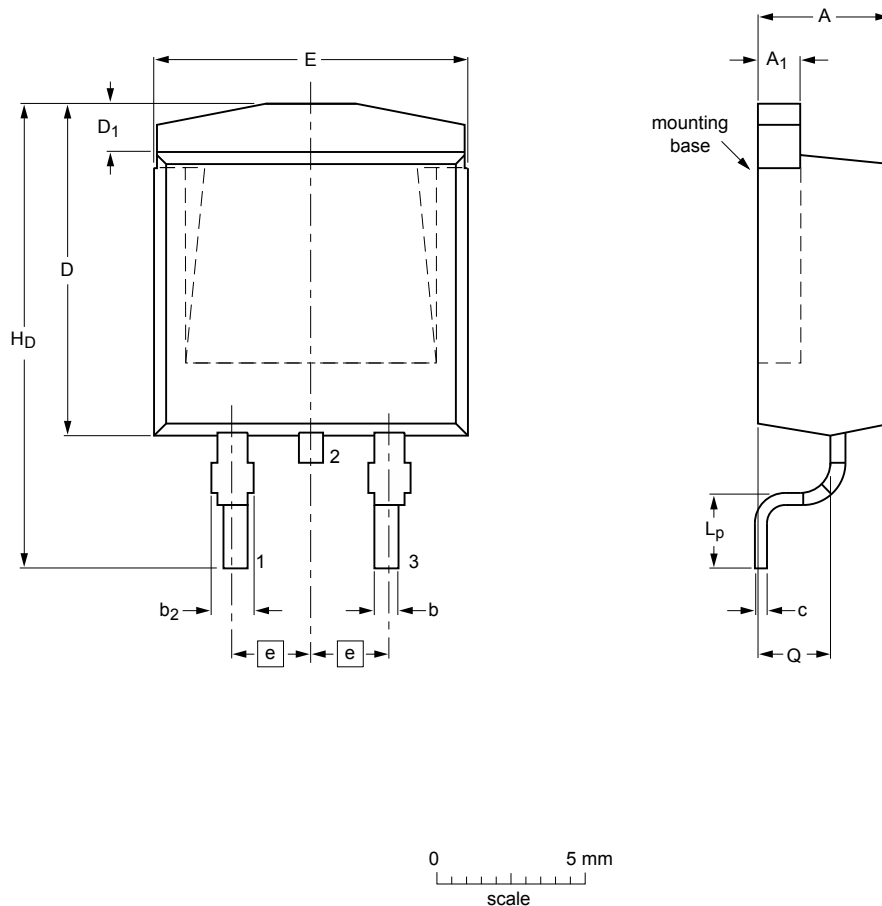


$V_{GS} = 0$ V

Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

| Unit | A | A ₁ | b | b ₂ | c | D | D ₁ | E | e | H _D | L _p | Q |
|------|-----|----------------|------|----------------|------|----|----------------|------|------|----------------|----------------|-----|
| max | 4.5 | 1.40 | 0.85 | 1.45 | 0.64 | 11 | 1.6 | 10.3 | | 15.8 | 2.9 | 2.6 |
| nom | | | | | | | | | 2.54 | | | |
| min | 4.1 | 1.27 | 0.60 | 1.05 | 0.46 | | 1.2 | 9.7 | | 14.8 | 2.1 | 2.2 |

sot404_po

| Outline version | References | | | European projection | Issue date |
|-----------------|------------|-------|-------|---------------------|------------------------|
| | IEC | JEDEC | JEITA | | |
| SOT404 | | | | | -06-03-16- 13-02-25 |

Fig. 18. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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