



# BUK7Y3R5-40E

N-channel 40 V, 3.5 mΩ standard level MOSFET in LFPAK56

19 June 2015

Product data sheet

## 1. General description

Standard level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with  $V_{GS(th)}$  rating of greater than 1 V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	[1]	-	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>		-	-	167	W
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a>		-	2.5	3.5	mΩ
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 32\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	16.2	-	nC

[1] Continuous current is limited by package.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y3R5-40E	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y3R5-40E	73E540

## 8. Limiting values

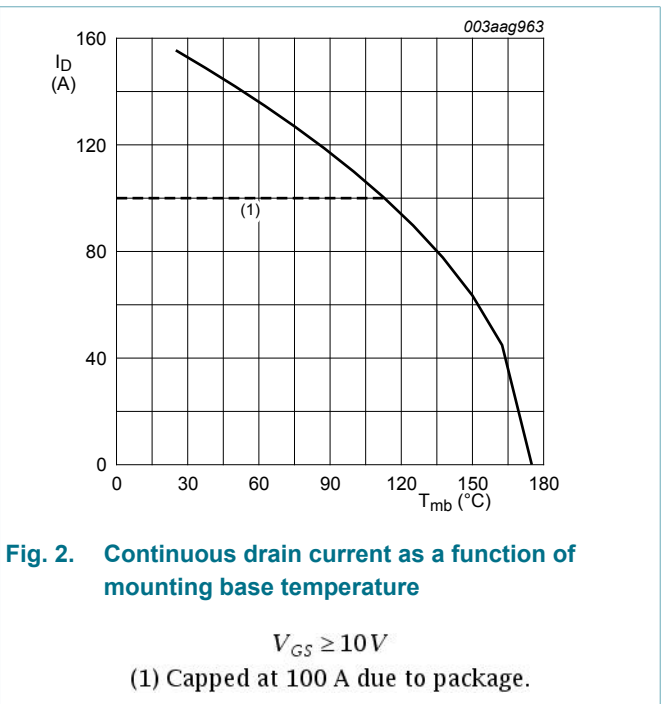
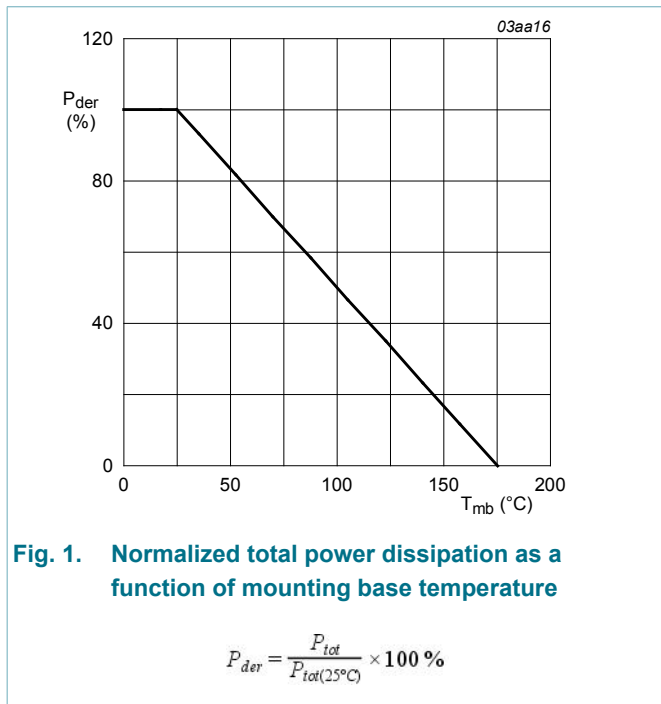
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$		-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	40	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	167	W
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 2</a>	[1]	-	100	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 2</a>	[1]	-	100	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Fig. 3</a>		-	622	A
$T_{stg}$	storage temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	622	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; <a href="#">Fig. 4</a>	[2][3]	-	135	mJ

- [1] Continuous current is limited by package.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.



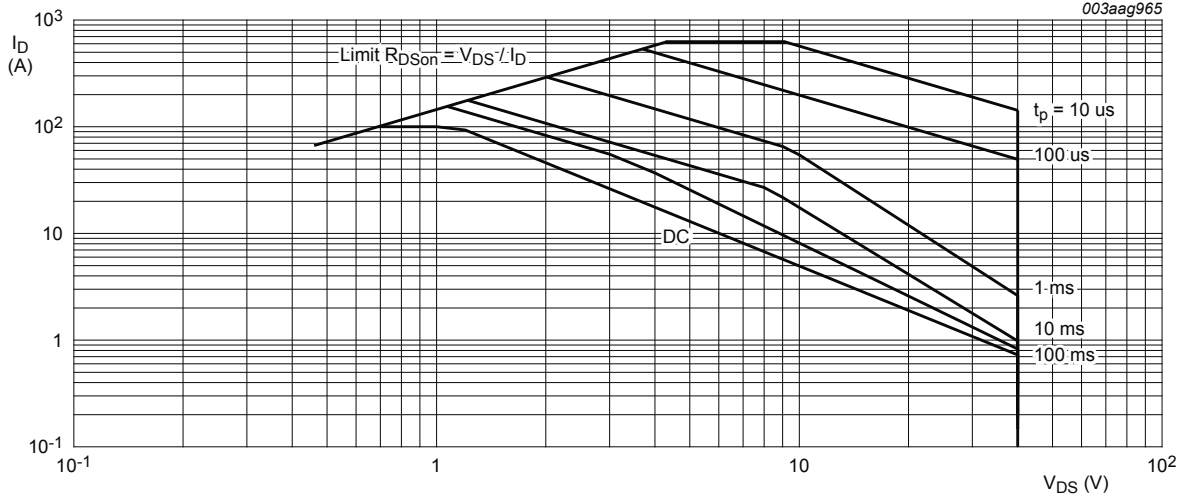


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$ ;  $I_{DM}$  is a single pulse

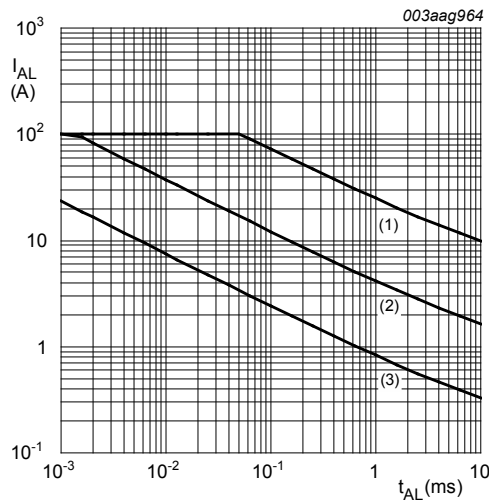


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^\circ C$ ; (2)  $T_{j (init)} = 150^\circ C$ ; (3) Repetitive Avalanche

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.9	K/W

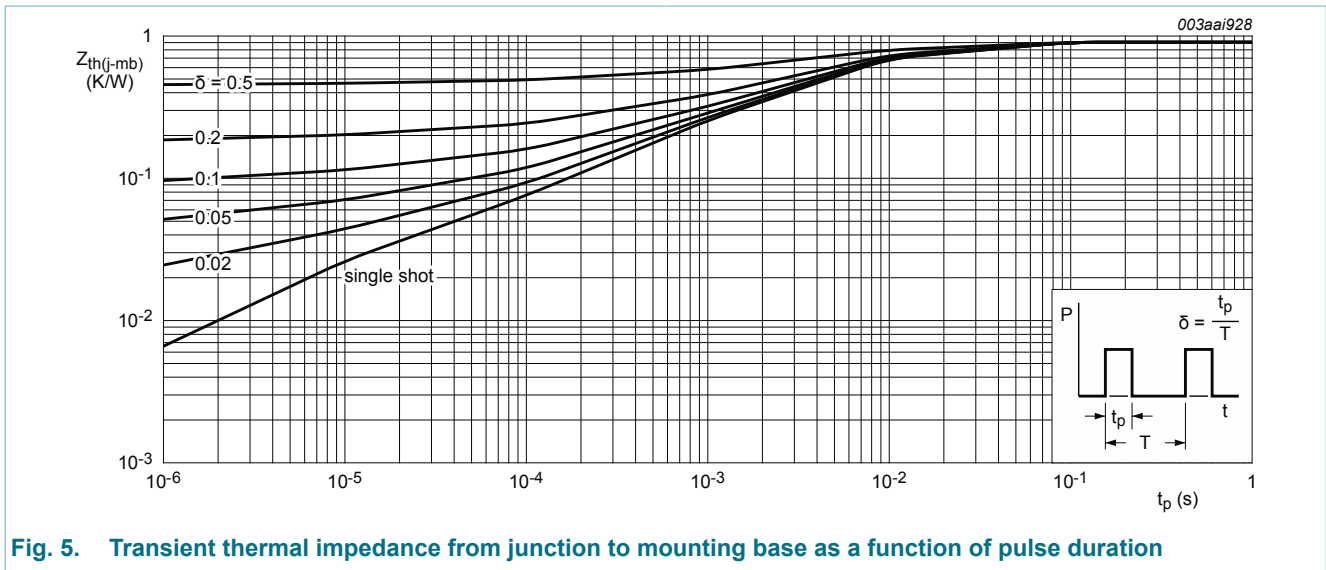


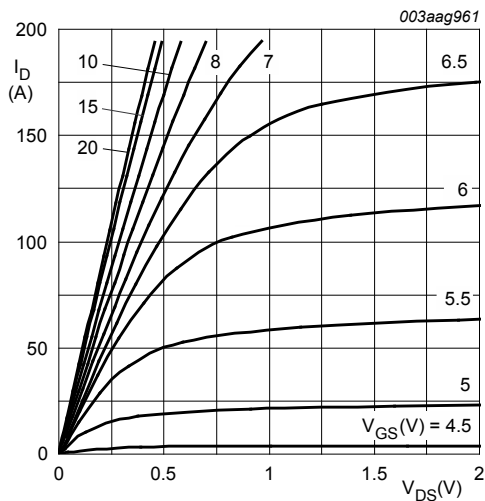
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

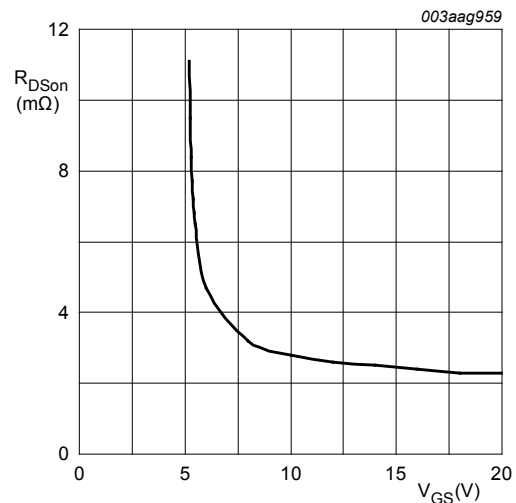
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	-	-	4.5	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.13	10	$\mu A$
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	2.5	3.5	mΩ
		$V_{GS} = 10 V; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 11; Fig. 12</a>	-	-	6.9	mΩ
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13; Fig. 14</a>	-	49.4	-	nC
$Q_{GS}$	gate-source charge		-	13.5	-	nC
$Q_{GD}$	gate-drain charge		-	16.2	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$	-	2688	3583	pF
$C_{oss}$	output capacitance	$T_j = 25\text{ °C};$ <a href="#">Fig. 15</a>	-	514	617	pF
$C_{rss}$	reverse transfer capacitance		-	313	429	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega; V_{GS} = 10\text{ V};$	-	13.6	-	ns
$t_r$	rise time	$R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ °C}$	-	24.9	-	ns
$t_{d(off)}$	turn-off delay time		-	30	-	ns
$t_f$	fall time		-	20.4	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C};$ <a href="#">Fig. 16</a>	-	0.83	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	29.6	-	ns
$Q_r$	recovered charge	$V_{DS} = 25\text{ V}; T_j = 25\text{ °C}$	-	25.4	-	nC



$T_j = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$

**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25\text{ °C}; I_D = 25\text{ A}$

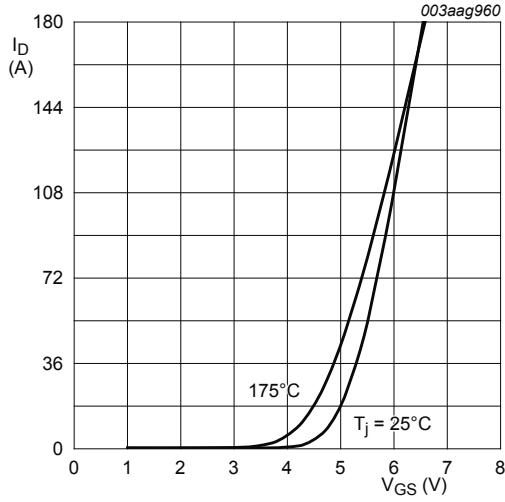


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10\text{ V}$$

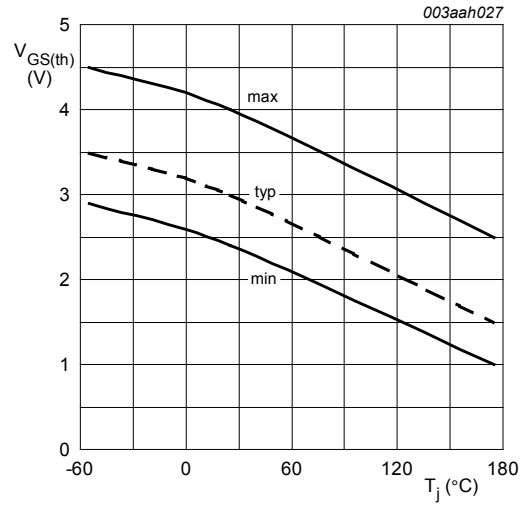


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

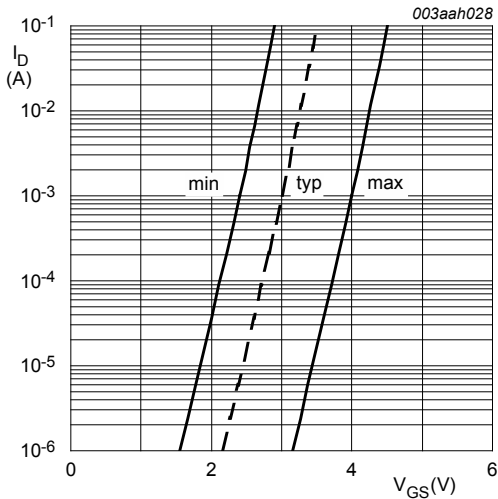


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$$

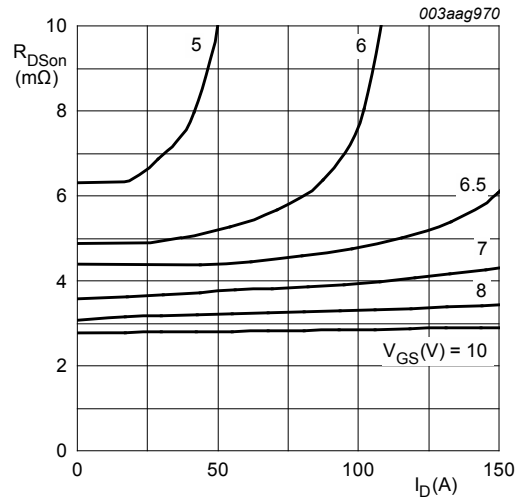


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$$

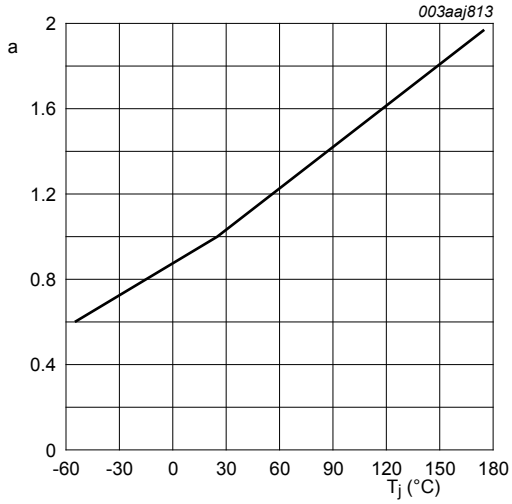
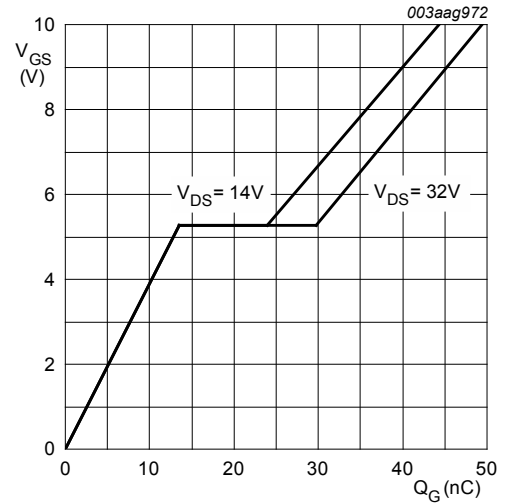


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



$T_j = 25^\circ C$ ;  $I_D = 25 A$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

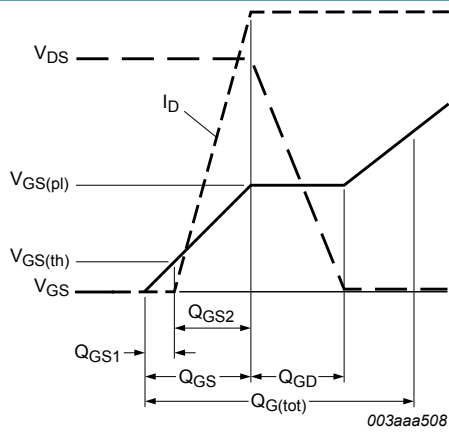
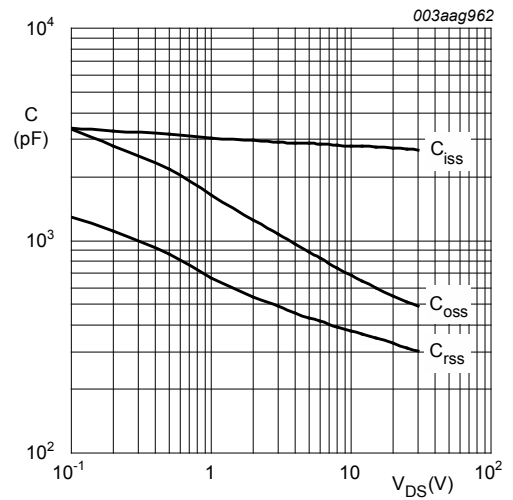


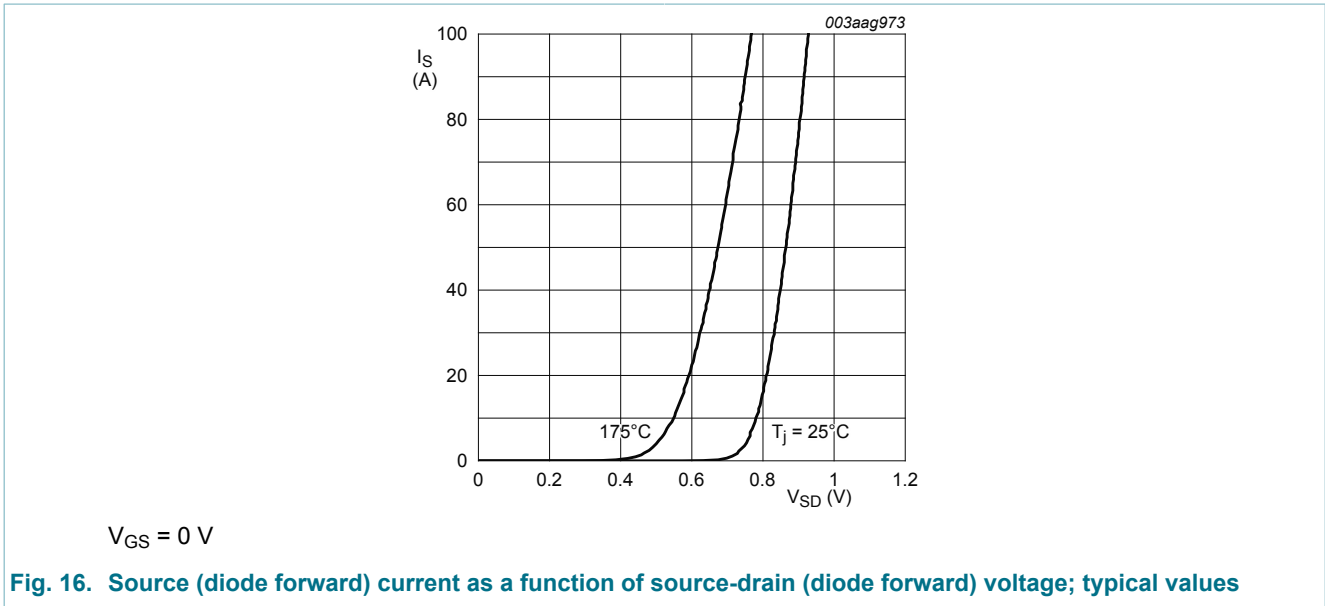
Fig. 14. Gate charge waveform definitions



$V_{GS} = 0 V$ ;  $f = 1 MHz$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





### 11. Package outline



Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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