MOSFET N-channel enhancement switching transistor — BSS83

DESCRIPTION

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type. The transistor is sealed in a SOT143 envelope and features a low ON resistance and low capacitances. The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

APPLICATIONS

- analog and/or digital switch
- switch driver

PINNING

1 = substrate (b)
2 = source
3 = drain
4 = gate

Note

1. Drain and source are interchangeable.

Marking code:

BSS83 = M74

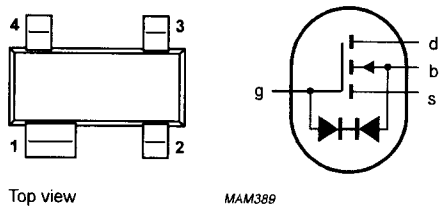

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (DC)	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230 mW
Gate-source threshold voltage			
$V_{DS} = V_{GS}$; V_{SB} = 0;	$V_{GS(th)}$	>	0.1 V
I_D = 1 μA		<	2.0 V
Drain-source ON-resistance			
V_{GS} = 10 V; V_{SB} = 0; I_D = 0.1 mA	R_{DSon}	<	45 Ω
Feed-back capacitance			
$V_{GS} = V_{BS}$ = −15 V;			
V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6 pF

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10	V
Source-drain voltage	V_{SD}	max.	10	V
Drain-substrate voltage	V_{DB}	max.	15	V
Source-substrate voltage	V_{SB}	max.	15	V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C[1]	P_{tot}	max.	230	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air[1]	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage			
$V_{GS} = V_{BS} = -5$ V; I_D = 10 nA	$V_{(BR)DSX}$	>	10 V
Source-drain breakdown voltage			
$V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10 V
Drain-substrate breakdown voltage			
V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15 V
Source-substrate breakdown voltage			
V_{GB} = 0; I_D = 10 nA; open drain	$V_{(BR)SBO}$	>	15 V
Drain-source leakage current			
$V_{GS} = V_{BS} = -2$ V; V_{DS} = 6,6 V	I_{DSoff}	<	10 nA
Source-drain leakage current			
$V_{GD} = V_{BD} = -2$ V; V_{SD} = 6,6 V	I_{SDoff}	<	10 nA
Forward transconductance at f = 1 kHz			
V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	>	10 mS
		typ.	15 mS
Gate-source threshold voltage			
$V_{DS} = V_{GS}$; V_{SB} = 0; I_D = 1 μA	$V_{GS(th)}$	>	0,1 V
		<	2,0 V
Drain-source ON-resistance			
I_D = 0,1 mA;			
V_{GS} = 5 V; V_{SB} = 0	R_{DSon}	<	70 Ω
V_{GS} = 10 V; V_{SB} = 0	R_{DSon}	<	45 Ω
V_{GS} = 3,2 V; V_{SB} = 6,8 V (see Fig.4)	R_{DSon}	typ.	80 Ω
		<	120 Ω
Gate-substrate zener voltages			
$V_{DB} = V_{SB}$ = 0; $-I_G$ = 10 μA	$V_{Z(1)}$	>	12,5 V
$V_{DB} = V_{SB}$ = 0; $+I_G$ = 10 μA	$V_{Z(2)}$	>	12,5 V
Capacitances at f = 1 MHz			
$V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	1,5 pF
Output capacitance	C_{oss}	typ.	1,0 pF
Switching times (see Fig.2)			
V_{DD} = 10 V; V_i = 5 V	t_{on}	typ.	1,0 ns
	t_{off}	typ.	5,0 ns

Note

1. Device mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.

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Pulse generator:

R_i	=	50 Ω
t_r	<	0,5 ns
t_f	<	1,0 ns
t_p	=	20 ns
δ	<	0,01

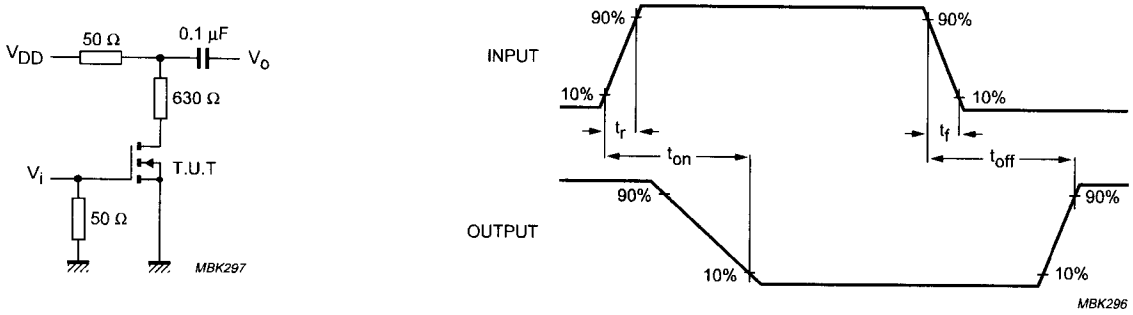
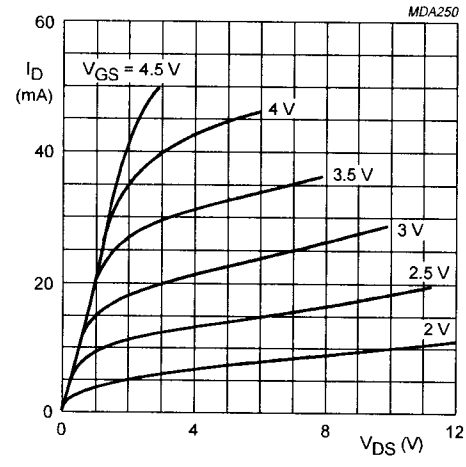
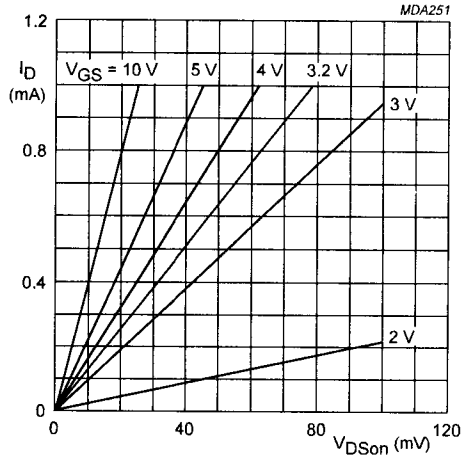


Fig.2 Switching times test circuit and input and output waveforms.



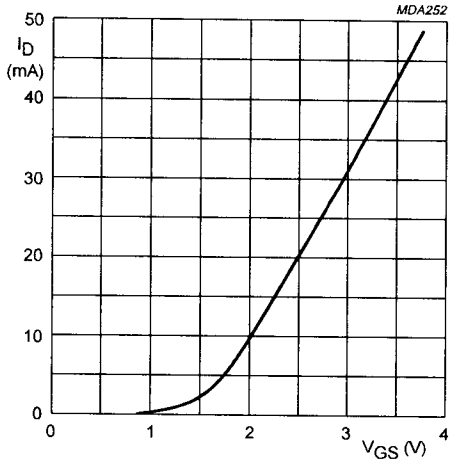
T_j = 25 °C.

Fig.3 V_{SB} = 0; typical values.



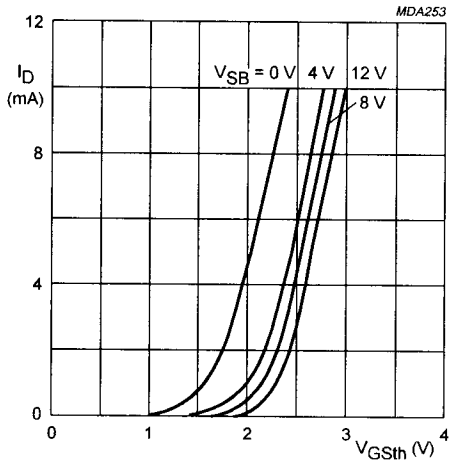
T_j = 25 °C.

Fig.4 V_{SB} = 6,8 V; typical values.



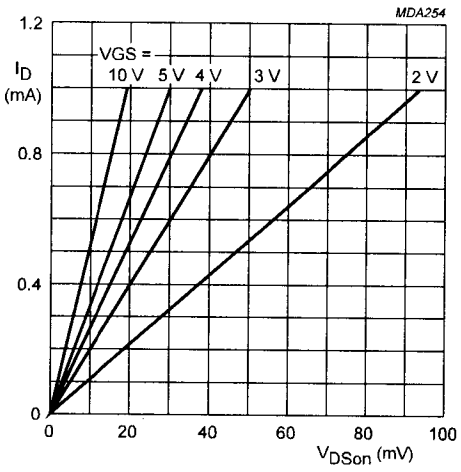
T_j = 25 °C.

Fig.5 V_{DS} = 10 V; V_{BS} = 0; typical values.



T_j = 25 °C.

Fig.6 V_{DS} = V_{GS} = $V_{GS(th)}$.

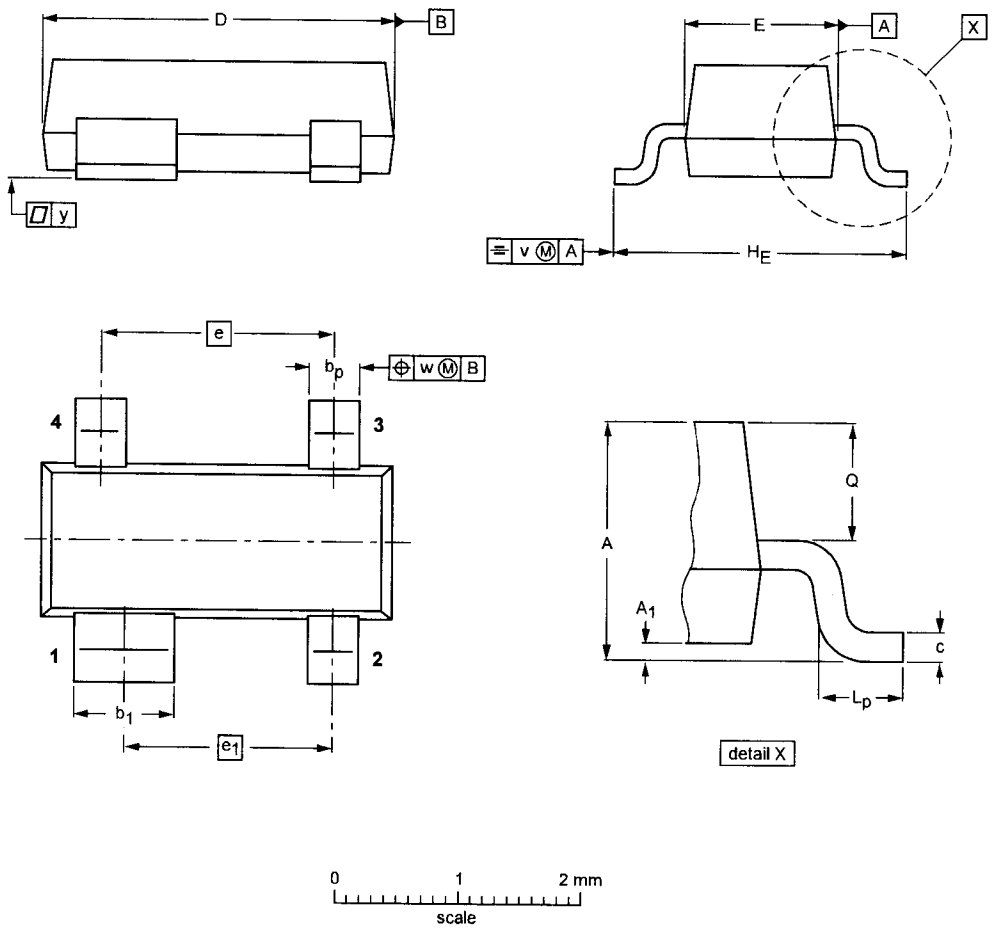


T_j = 25 °C.

Fig.7 V_{SB} = 0; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; 4 leads **SOT143B**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28