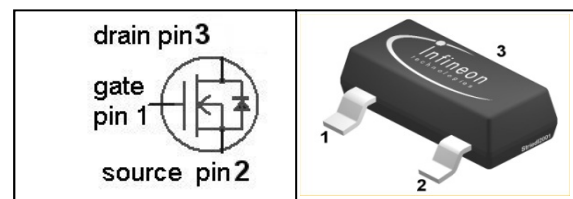


SIPMOS[®] Small-Signal-Transistor
Feature

- N-Channel
- Enhancement mode
- Logic level
- dv/dt rated
- Pb-free lead-plating; RoHS compliant
- Qualified according to AEC Q101
- Halogen-free according to IEC61249-2-21


Product Summary

V_{DS}	240	V
$R_{DS(on),max}$	14	Ω
I_D	0.1	A

PG-SOT-23


Type	Package	Pb-free	Tape and Reel Information	Marking
BSS131	PG-SOT23	Yes	H6327	SRs

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_A=25\text{ °C}$	0.11	A
		$T_A=70\text{ °C}$	0.09	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	0.4	
Reverse diode dv/dt	dv/dt	$I_D=0.1\text{ A}$, $V_{DS}=192\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V
ESD Class		JESD22-A114-HBM	Class 0	
Power dissipation	P_{tot}	$T_A=25\text{ °C}$	0.36	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - minimal footprint	R_{thJA}		-	-	350	K/W
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Electrical characteristics, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	240	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=0\text{ V}, I_D=56\text{ }\mu\text{A}$	0.8	1.4	1.8	
Drain-source leakage current	$I_{D(off)}$	$V_{DS}=240\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	0.01	μA
		$V_{DS}=240\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	-	5	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	10	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=0.09\text{ A}$	-	9.07	20	Ω
		$V_{GS}=10\text{ V}, I_D=0.1\text{ A}$	-	7.7	14	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=0.08\text{ A}$	0.06	0.13	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	58	77	pF
Output capacitance	C_{oss}		-	7.3	10	
Reverse transfer capacitance	C_{rss}		-	2.8	4.2	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=120\text{ V},$ $V_{GS}=10\text{ V}, I_D=0.1\text{ A},$ $R_G=6\ \Omega$	-	3.3	5.0	ns
Rise time	t_r		-	3.1	4.6	
Turn-off delay time	$t_{d(off)}$		-	13.7	20	
Fall time	t_f		-	64.5	97	

Gate Charge Characteristics

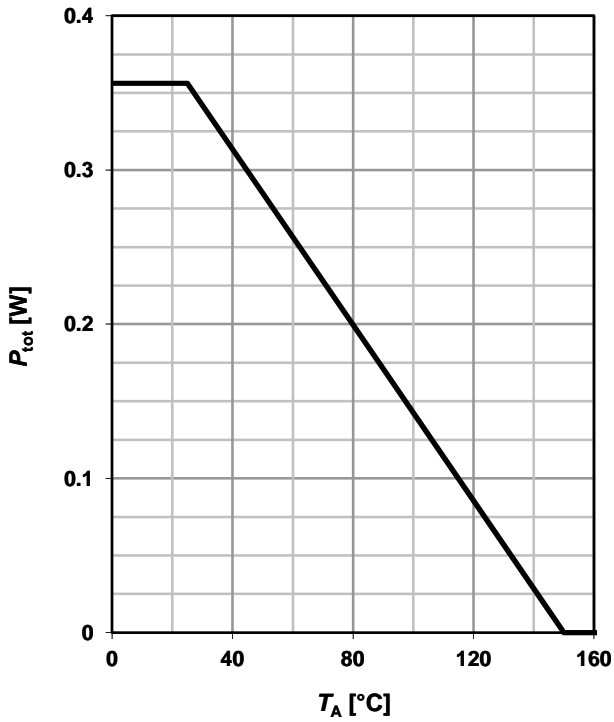
Gate to source charge	Q_{gs}	$V_{DD}=192\text{ V}, I_D=0.1\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	0.16	0.22	nC
Gate to drain charge	Q_{gd}		-	0.8	1.2	
Gate charge total	Q_g		-	2.1	3.1	
Gate plateau voltage	$V_{plateau}$		-	2.90	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_A=25\text{ }^\circ\text{C}$	-	-	0.11	A
Diode pulse current	$I_{S,pulse}$		-	-	0.43	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=0.1\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.81	1.2	V
Reverse recovery time	t_{rr}	$V_R=120\text{ V}, I_F=0.1\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	42.9	64.3	ns
Reverse recovery charge	Q_{rr}		-	22.6	34	nC

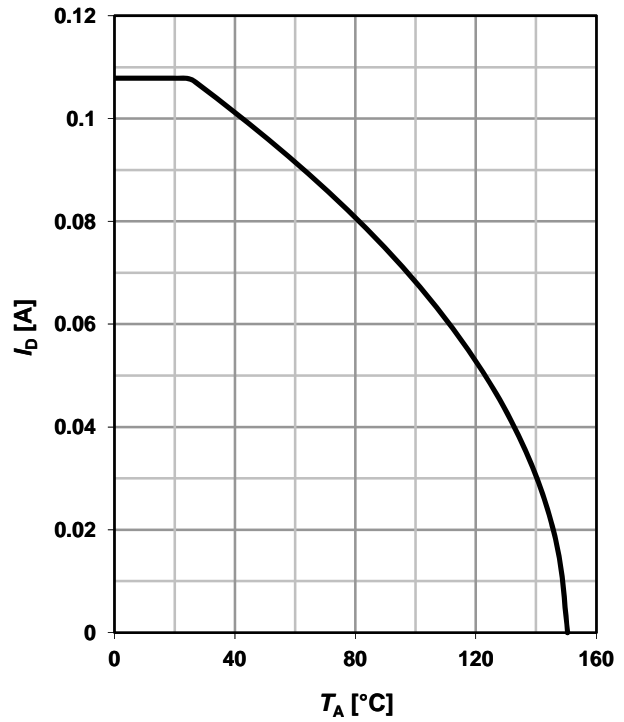
1 Power dissipation

$P_{tot}=f(T_A)$



2 Drain current

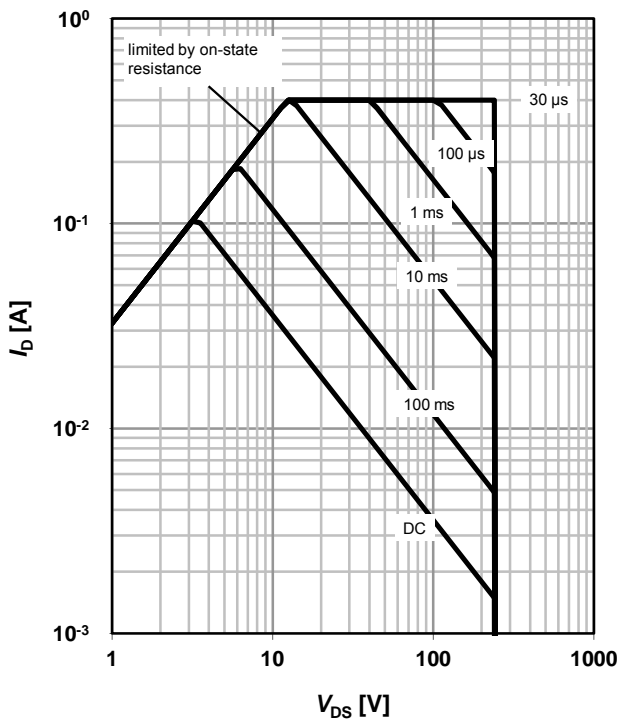
$I_D=f(T_A); V_{GS} \geq 10\text{ V}$



3 Safe operating area

$I_D=f(V_{DS}); T_A=25\text{ °C}; D=0$

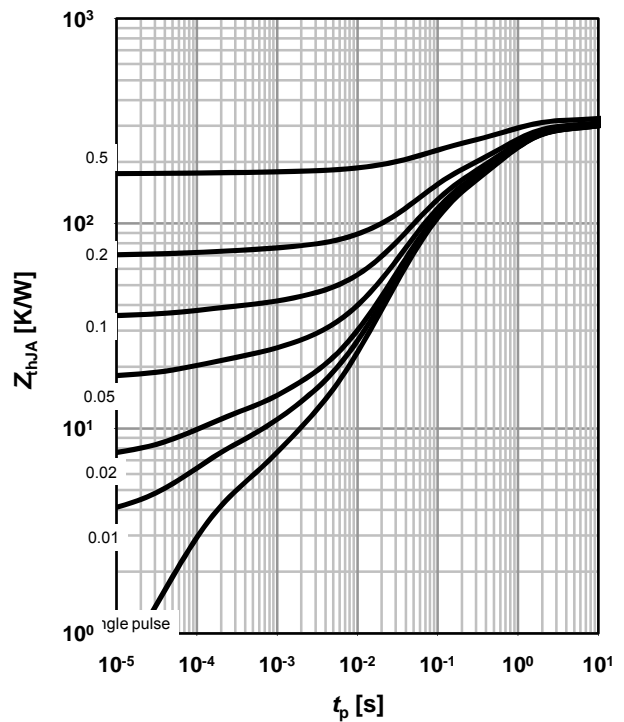
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJA}=f(t_p)$

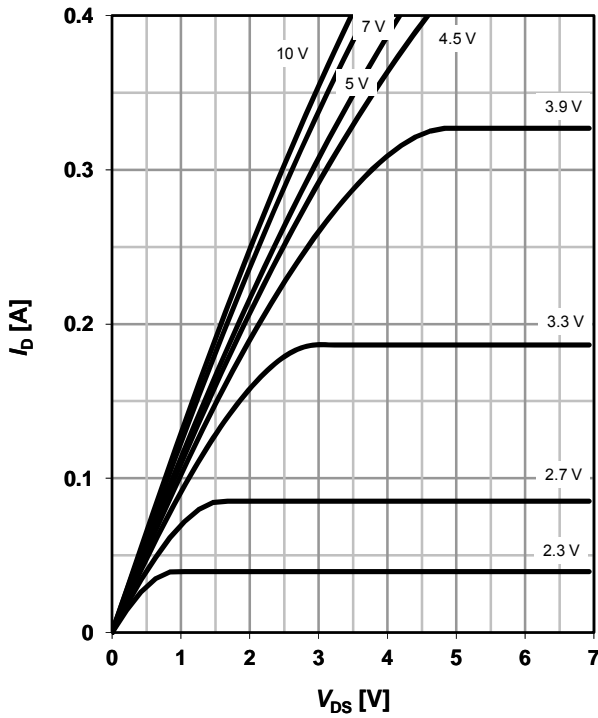
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

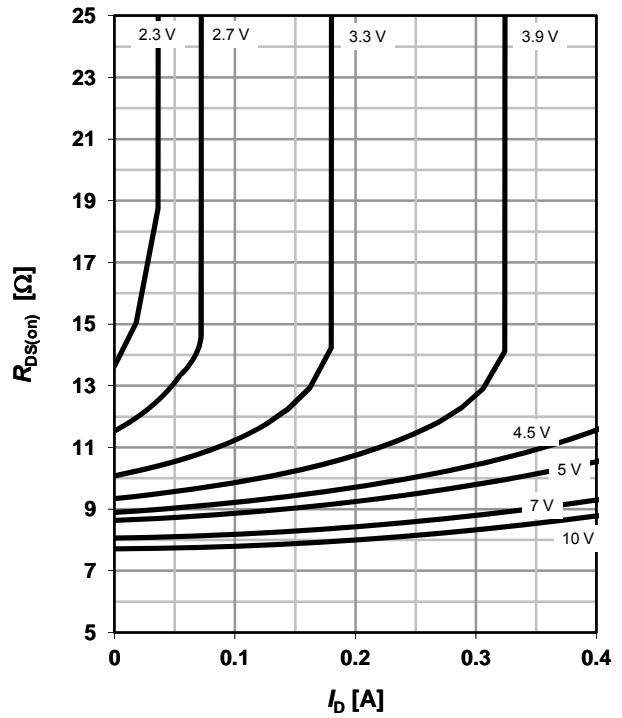
parameter: V_{GS}



6 Typ. drain-source on resistance

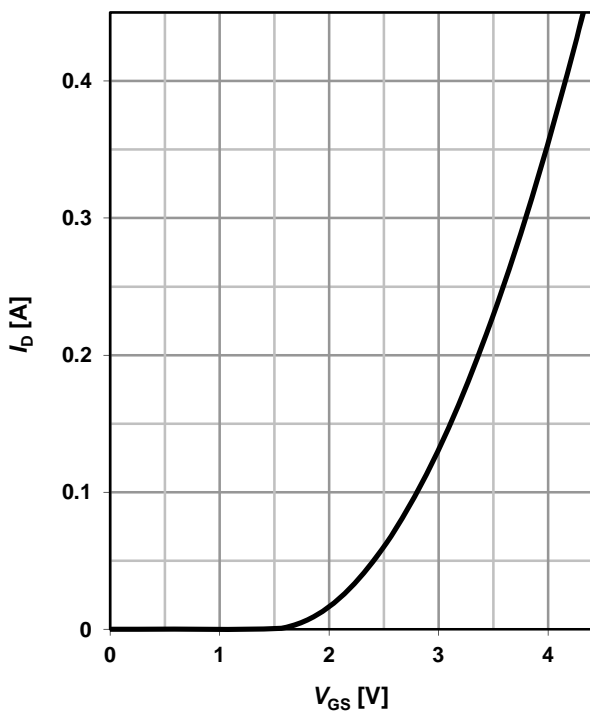
$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

parameter: V_{GS}



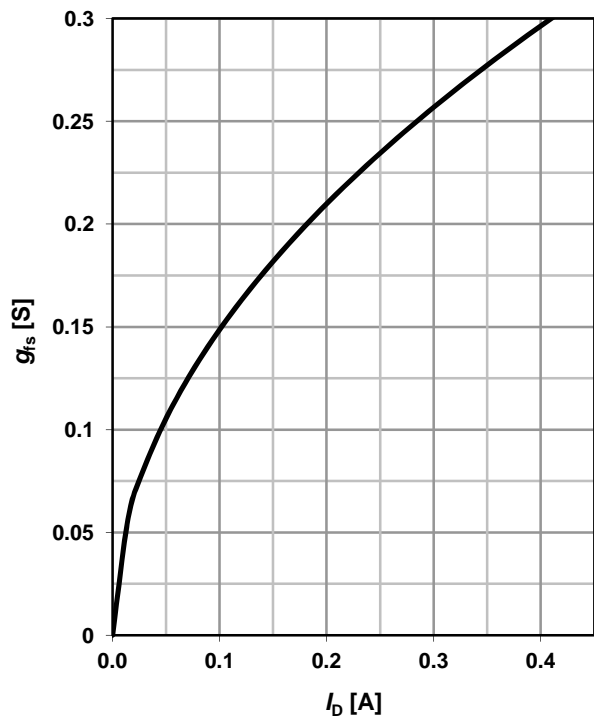
7 Typ. transfer characteristics

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$



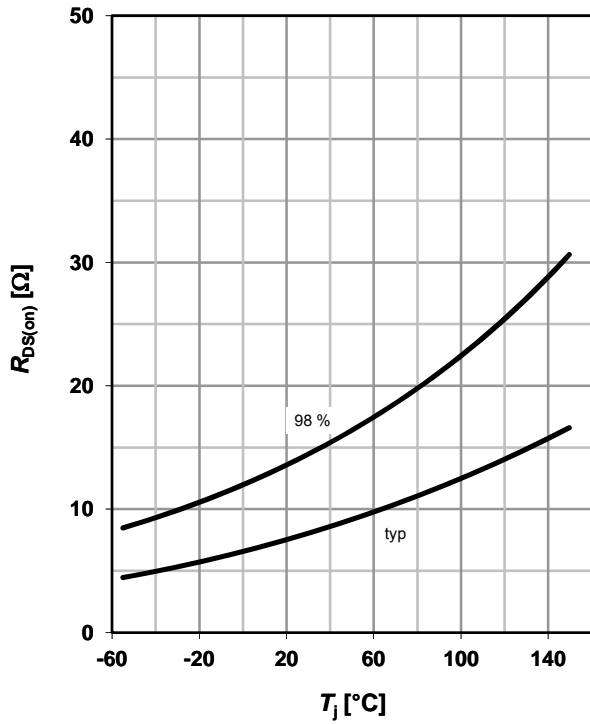
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

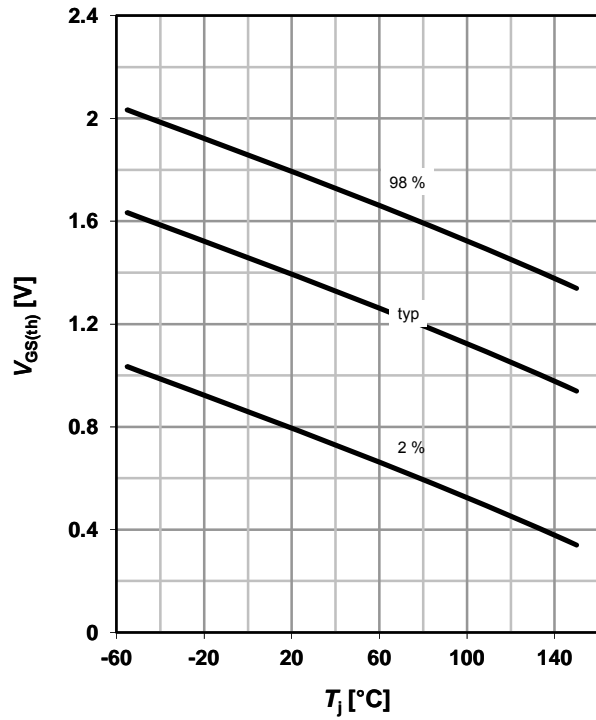
$R_{DS(on)}=f(T_j); I_D=0.1\text{ A}; V_{GS}=10\text{ V}$



10 Typ. gate threshold voltage

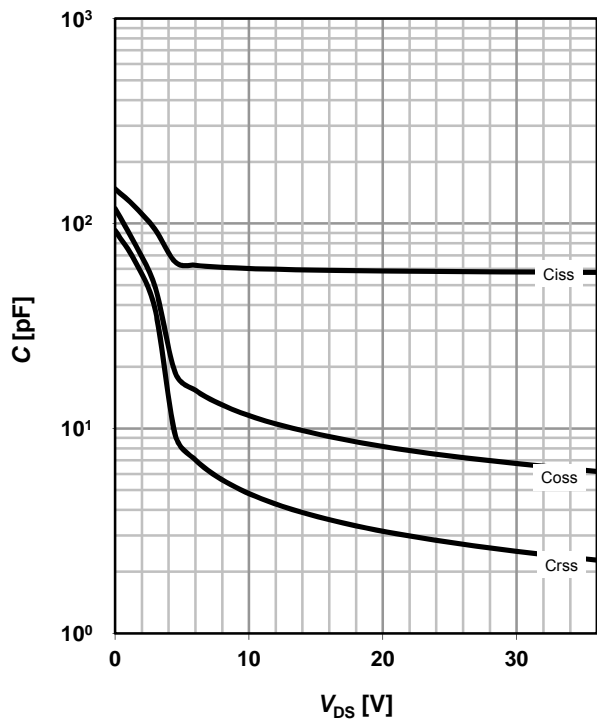
$V_{GS(th)}=f(T_j); V_{DS}=V_{GS}; I_D=56\ \mu\text{A}$

parameter: I_D



11 Typ. capacitances

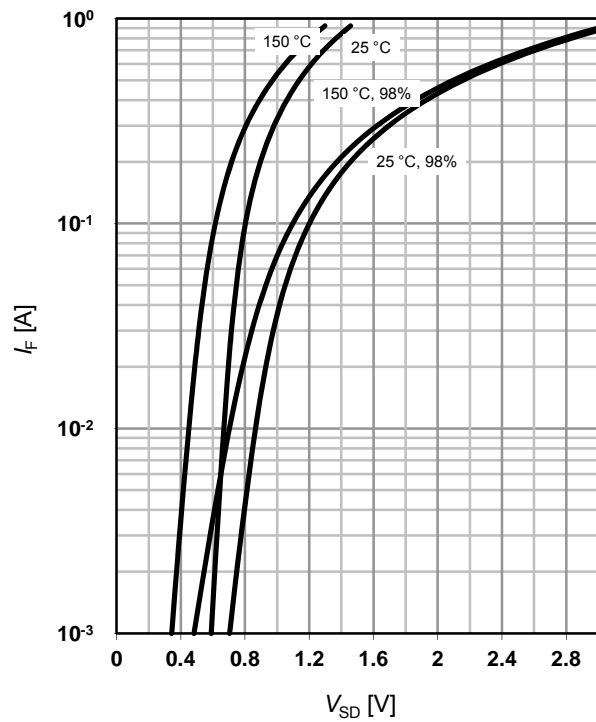
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}; T_j=25^\circ\text{C}$



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

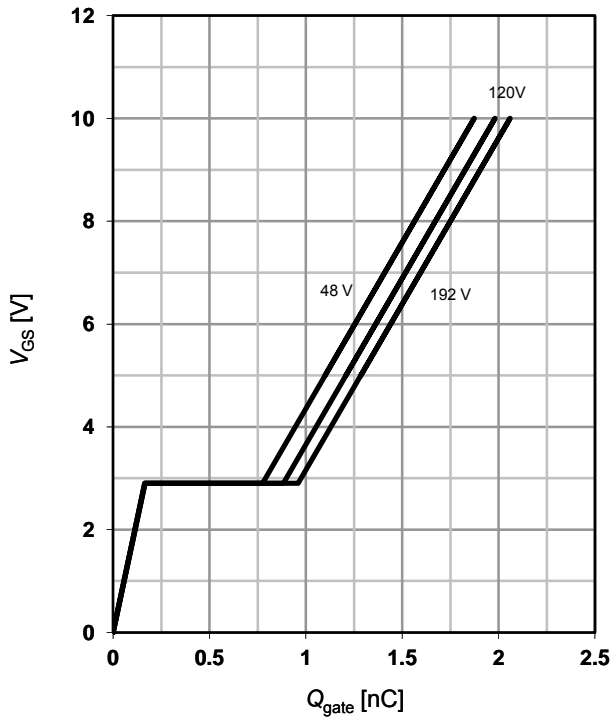
parameter: T_j



13 Typ. gate charge

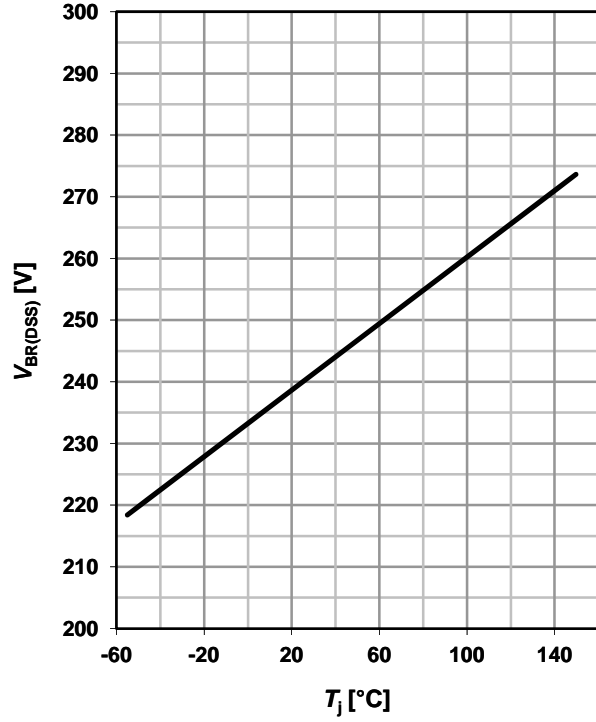
$V_{GS}=f(Q_{gate}); I_D=0.1\text{ A pulsed}$

parameter: V_{DD}

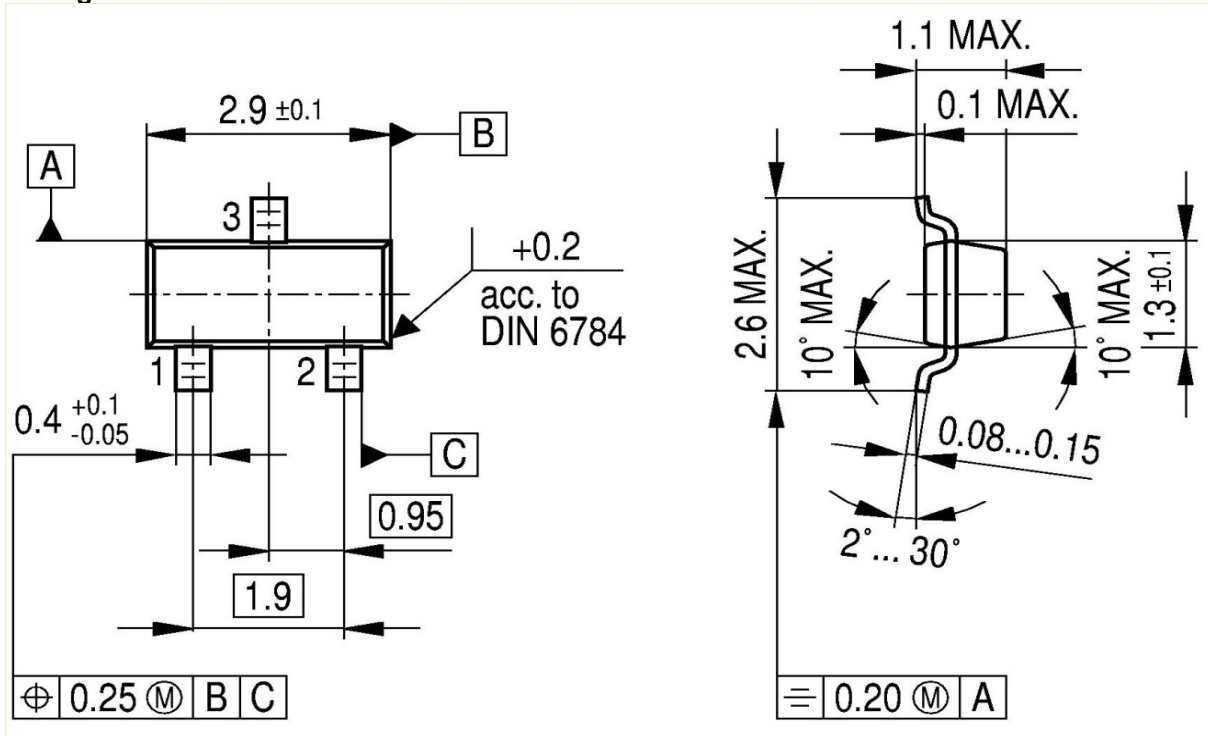


14 Drain-source breakdown voltage

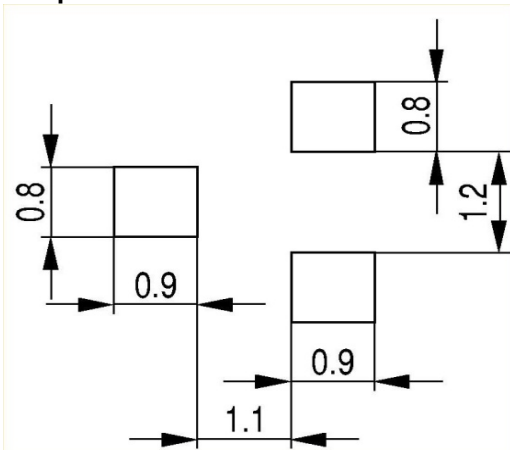
$V_{BR(DSS)}=f(T_j); I_D=250\ \mu\text{A}$



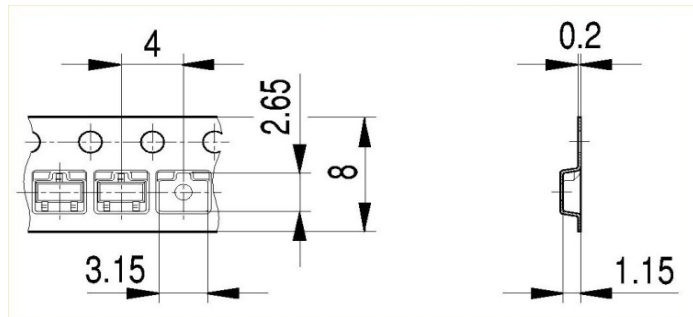
Package Outline:



Footprint:



Packaging:



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