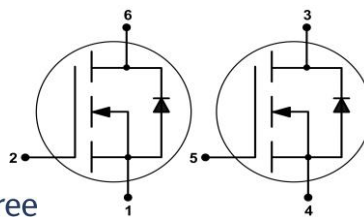
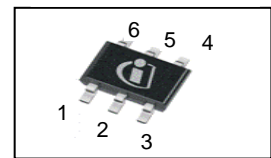


OptiMOS™ 2 Small-Signal-Transistor
Features

- Dual N-channel
- Enhancement mode
- Super Logic level (2.5V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen-free according to IEC61249-2-21


PG-SOT-363

Product Summary

V_{DS}	20	V
$R_{DS(on),max}$	$V_{GS}=4.5\text{ V}$	350
	$V_{GS}=2.5\text{ V}$	600
I_D	0.95	A

Type	Package	Tape and Reel Information	Marking	Lead Free	Packing
BSD235N	PG-SOT-363	H6327: 3000 pcs/ reel	X6s	Yes	Non dry

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter ¹⁾	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_A=25\text{ °C}$	0.95	A
		$T_A=70\text{ °C}$	0.76	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	3.8	
Avalanche energy, single pulse	E_{AS}	$I_D=0.95\text{ A}$, $R_{GS}=16\ \Omega$	1.6	mJ
Reverse diode dv/dt	dv/dt	$I_D=0.95\text{ A}$, $V_{DS}=16\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 12	V
Power dissipation	P_{tot}	$T_A=25\text{ °C}$	0.5	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	°C
ESD Class		JESD22-A114 -HBM	0 (<250V)	
Soldering Temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/150/56	

⁽¹⁾ Remark: only one of both transistors in operation.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - ambient	R_{thJA}	minimal footprint ⁽²⁾	-	-	250	K/W
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Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	20	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=1.6\text{ }\mu\text{A}$	0.7	0.95	1.2	
Drain-source leakage current	I_{DSS}	$V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	-	1	μA
		$V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=12\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=2.5\text{ V}$, $I_D=0.29\text{ A}$	-	415	600	$\text{m}\Omega$
		$V_{GS}=4.5\text{ V}$, $I_D=0.95\text{ A}$	-	266	350	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=0.76\text{ A}$		2	-	S

²⁾ Performed on 40 mm² FR4 PCB. The traces are 1mm wide, 70 μm thick and 20mm long; they are present on both sides of the PCB

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=10\text{ V},$ $f=1\text{ MHz}$	-	49	63	pF
Output capacitance	C_{oss}		-	23	32	
Reverse transfer capacitance	C_{rss}		-	3.2	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=10\text{ V}, V_{GS}=4.5\text{ V},$ $I_D=0.95\text{ A}, R_{G,ext}=6\ \Omega$	-	3.8	-	ns
Rise time	t_r		-	3.6	-	
Turn-off delay time	$t_{d(off)}$		-	4.5	-	
Fall time	t_f		-	1.2	-	

Gate Charge Characteristics

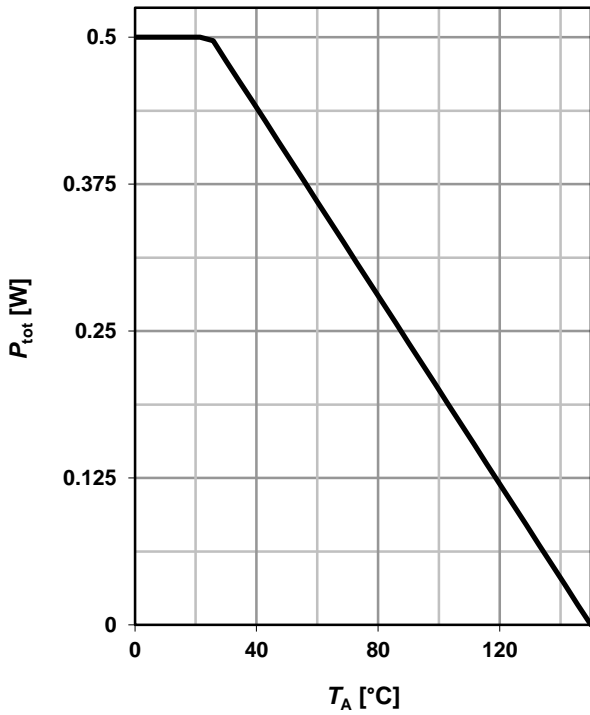
Gate to source charge	Q_{gs}	$V_{DD}=10\text{ V}, I_D=0.95\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	0.11	-	nC
Gate to drain charge	Q_{gd}		-	0.07	-	
Gate charge total	Q_g		-	0.32	-	
Gate plateau voltage	$V_{plateau}$		-	2.4	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_A=25\text{ }^\circ\text{C}$	-	-	0.5	A
Diode pulse current	$I_{S,pulse}$		-	-	3.8	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=0.95\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.2	V
Reverse recovery time	t_{rr}	$V_R=10\text{ V}, I_F=0.95\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	5.2	-	ns
Reverse recovery charge	Q_{rr}		-	0.97	-	nC

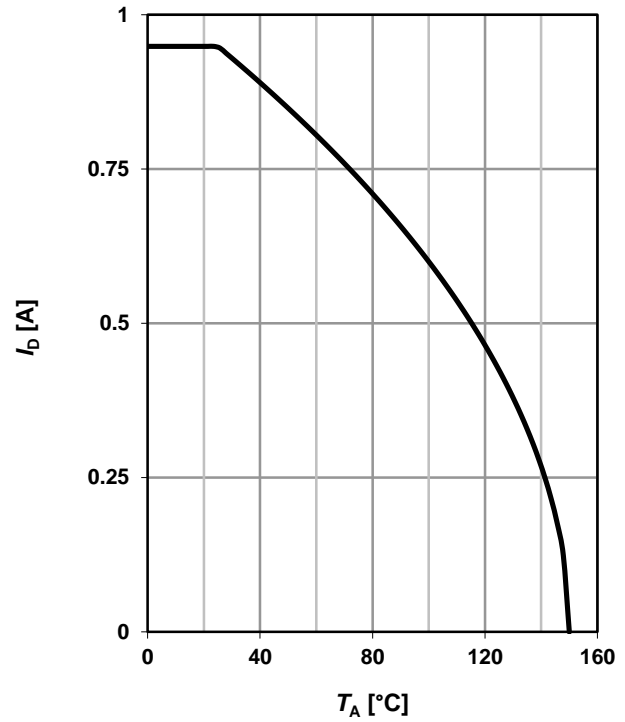
1 Power dissipation

$P_{tot}=f(T_A)$



2 Drain current

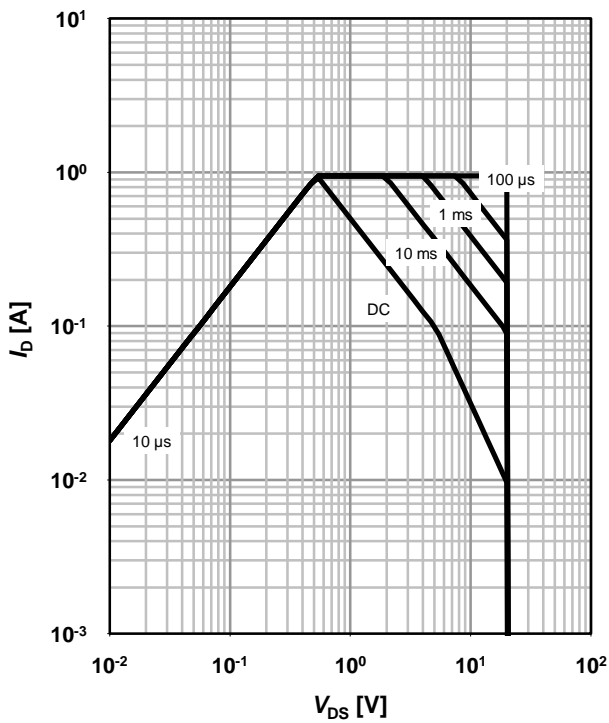
$I_D=f(T_A); V_{GS} \geq 4.5 V$



3 Safe operating area

$I_D=f(V_{DS}); T_A=25\text{ °C}; D=0$

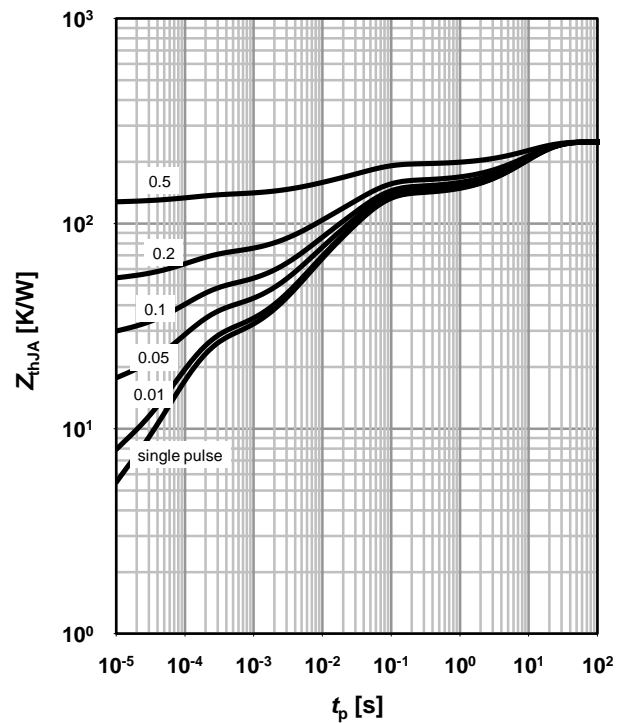
parameter: t_p



4 Max. transient thermal impedance

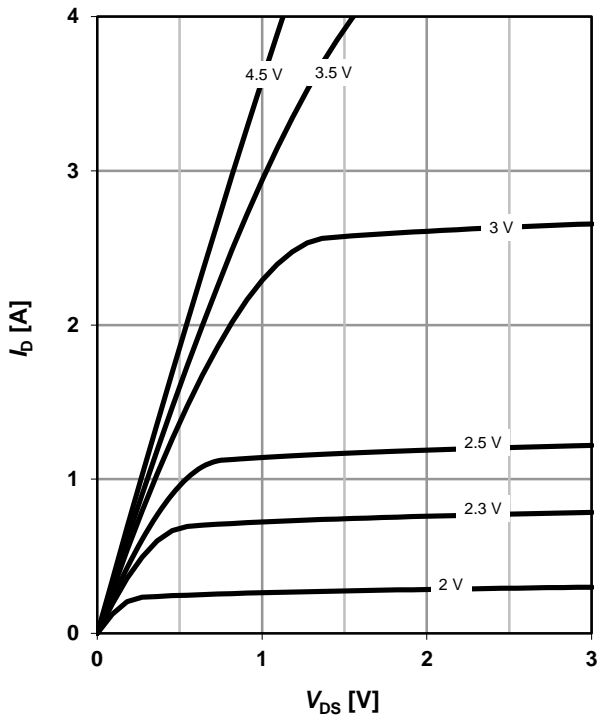
$Z_{thJA}=f(t_p)$

parameter: $D=t_p/T$

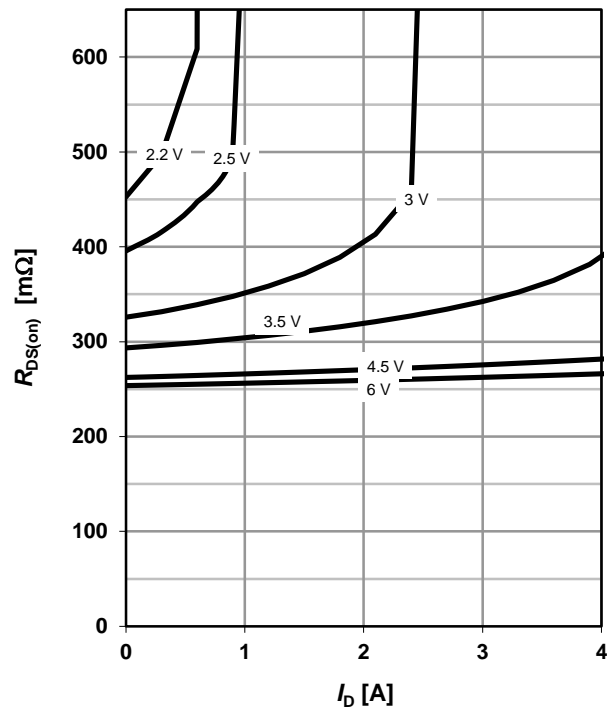


5 Typ. output characteristics

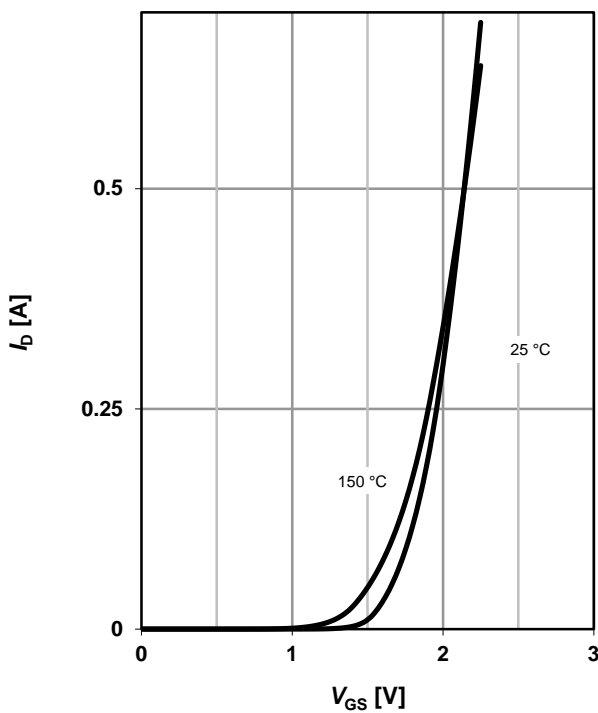
$$I_D = f(V_{DS}); T_j = 25\text{ °C}$$

 parameter: V_{GS}

6 Typ. drain-source on resistance

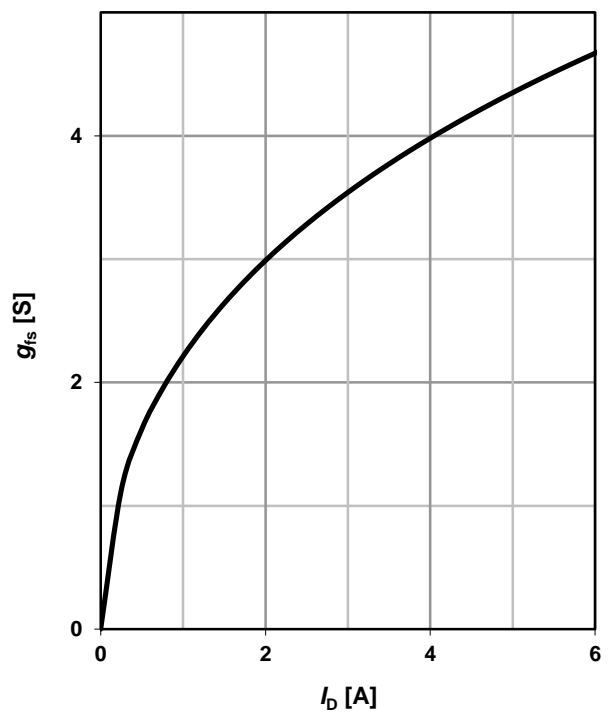
$$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$$

 parameter: V_{GS}

7 Typ. transfer characteristics

$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

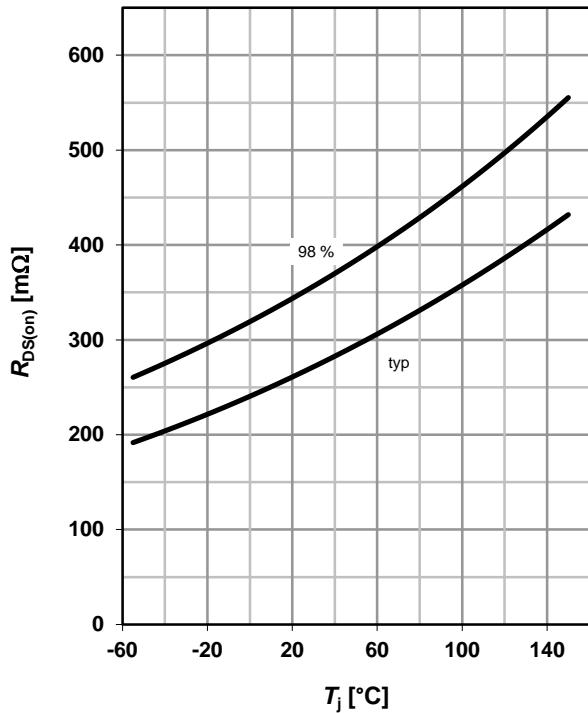

8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25\text{ °C}$$



9 Drain-source on-state resistance

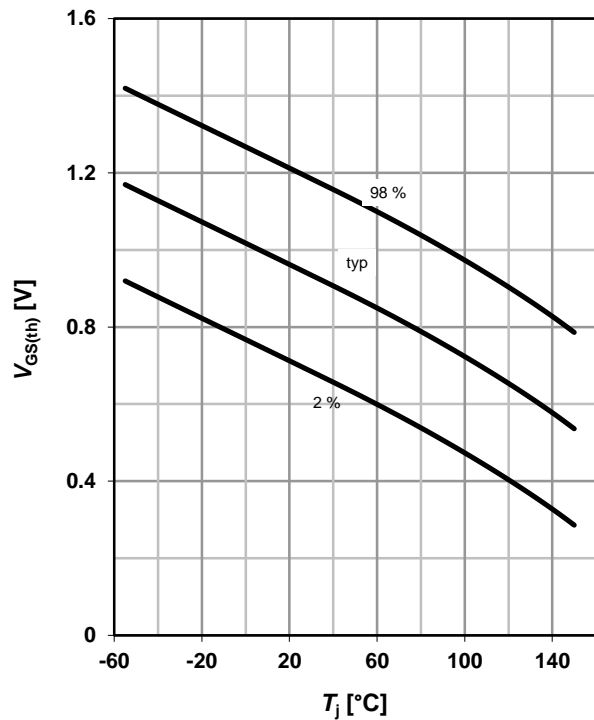
$R_{DS(on)}=f(T_j); I_D=0.95\text{ A}; V_{GS}=4.5\text{ V}$



10 Typ. gate threshold voltage

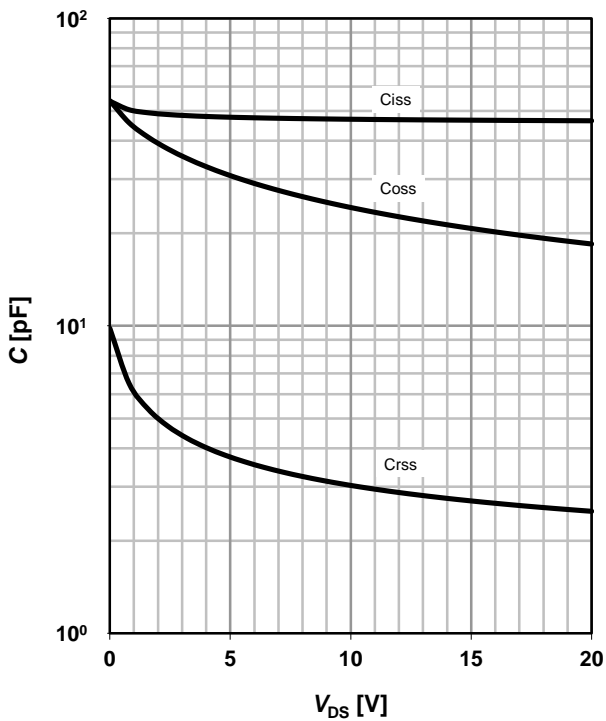
$V_{GS(th)}=f(T_j); V_{DS}=V_{GS}; I_D=1.6\ \mu\text{A}$

parameter: I_D



11 Typ. capacitances

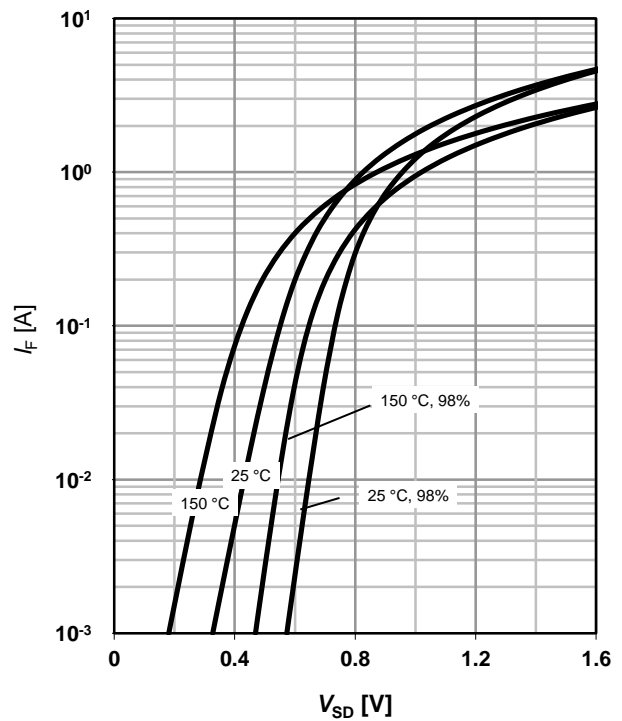
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}; T_j=25^\circ\text{C}$



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

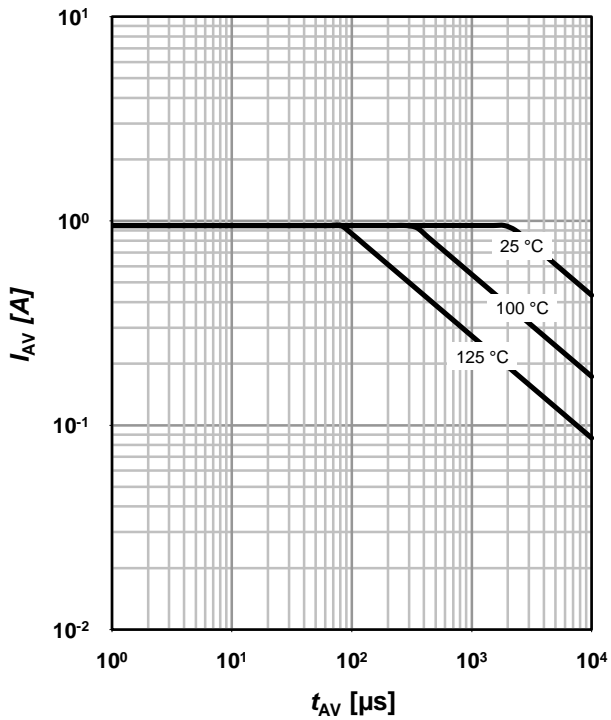
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=16 \Omega$

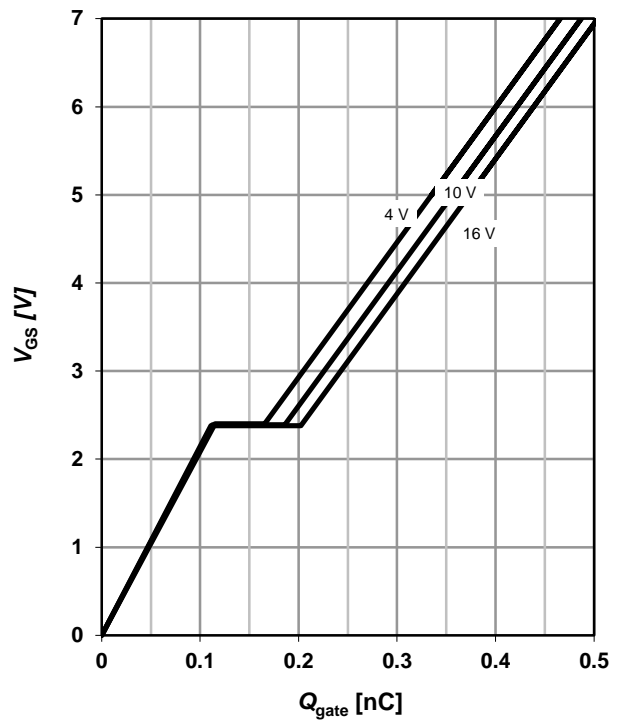
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

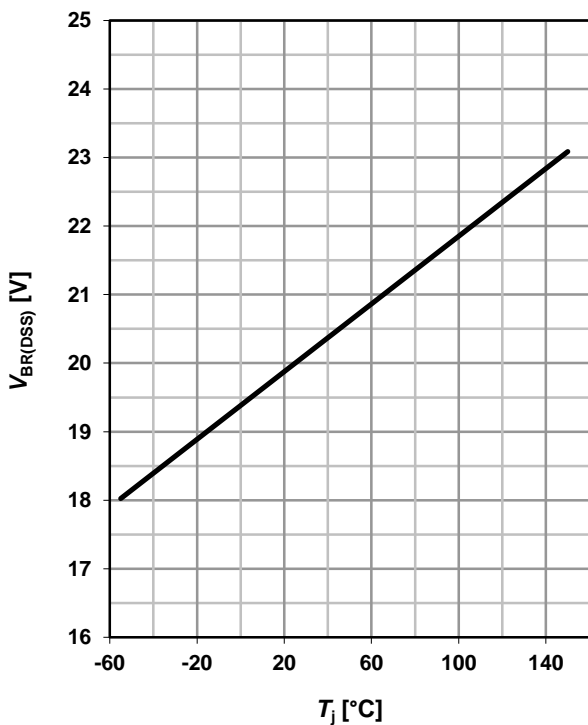
$V_{GS}=f(Q_{\text{gate}}); I_D=0.95 \text{ A pulsed}$

parameter: V_{DD}

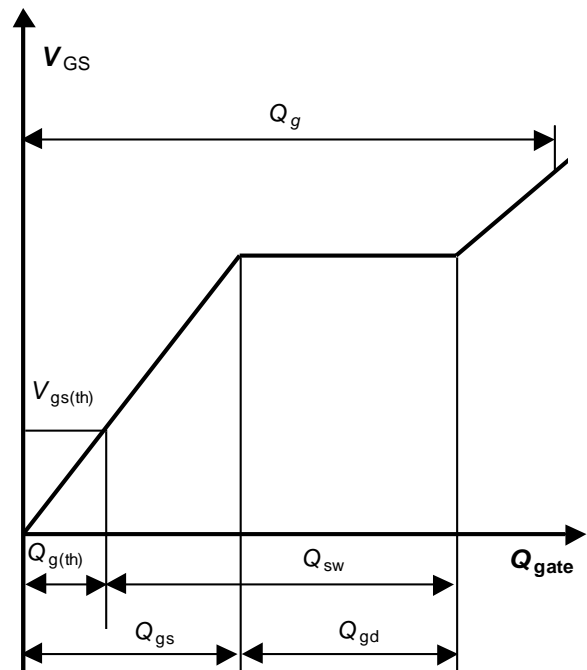


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=250 \mu\text{A}$

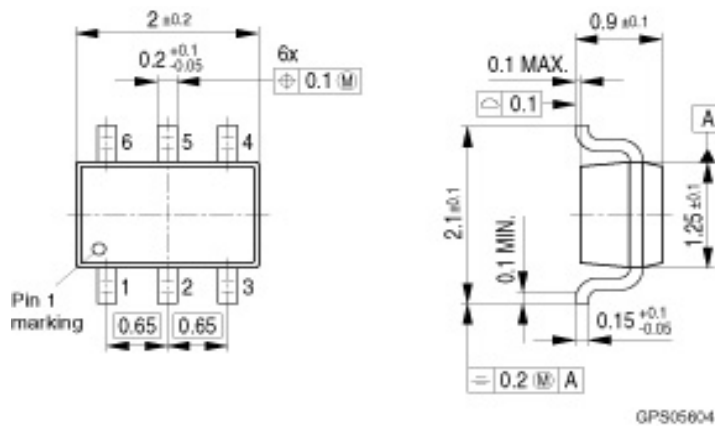


16 Gate charge waveforms

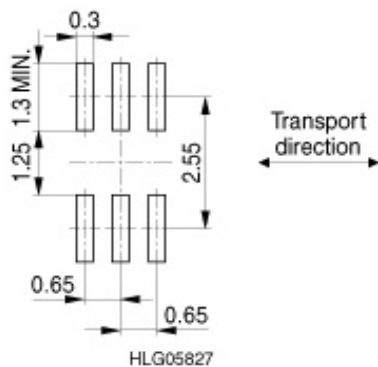


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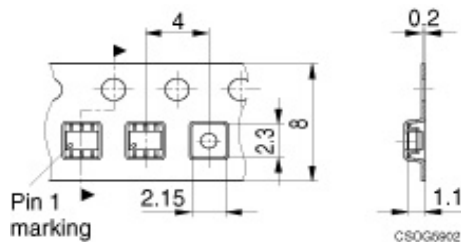
Package Outline:



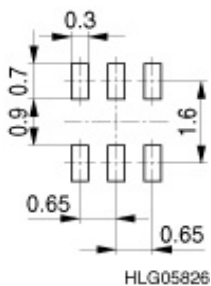
Footprint:



Packing:



Reflow soldering:



Note: For symmetric types there is no defined Pin 1 orientation in the reel.

Dimensions in mm

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