Wide Range Fuel Gauge with Impedance Track™ for Lead-Acid Batteries

Check for Samples: bq34z110

FEATURES

- Supports Lead-Acid Chemistries
- Capacity Estimation Using Patented Impedance Track™ Technology for Batteries from 4 V to 64 V
  - Aging Compensation
  - Self-Discharge Compensation
- Supports Battery Capacities Above 65 Ahr
- Supports Charge and Discharge Currents Above 32 A
- External NTC Thermistor Support
- Supports Two-Wire I^{2}C and HDQ Single Wire Communication Interfaces with Host System
- SHA-1/HMAC Authentication
- One- or Four-LED Direct Display Control
- Five-LED and Higher Display Through Port Expander
- Reduced Power Modes (Typical Battery Pack Operating Range Conditions)
  - Normal Operation: < 140 µA Average
  - Sleep: < 64 µA Average
  - Full Sleep: < 19 µA Average
- Package: 14-Pin TSSOP

APPLICATIONS

- Light Electric Vehicles
- Power Tools
- Medical Instrumentation
- Uninterruptable Power Supplies (UPS)
- Mobile Radios

PRODUCT PREVIEW

DESCRIPTION

The Texas Instruments bq34z110 is a fuel gauge solution that works independently of battery series-cell configurations, and supports Lead-Acid battery chemistries. Batteries from 4 V to 64 V can be supported through an external voltage translation circuit that can be controlled automatically to reduce system power consumption.

The bq34z110 device provides several interface options, including an I^{2}C™ slave, an HDQ slave, one or four direct LEDs, and an Alert output pin. Additionally, the bq34z110 provides support for an external port expander for more than four LEDs.

ORDERING INFORMATION

T_A	PART NUMBER	PACKAGE (TSSOP)	TUBE	TAPE AND REEL
–40°C to 85°C	bq34z110PW or bq34z110PWR	14-Pin	PW	PWR

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DETAILS

PIN-OUT DIAGRAM

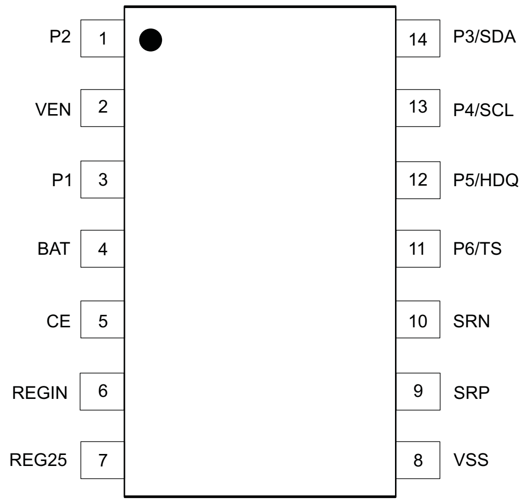

Figure 1. bq34z110 Pin-Out Diagram

Table 1. bq34z110 External Pin Functions

PIN NAME	PIN NUMBER	TYPE (1)	DESCRIPTION
P2	1	O	LED 2 or Not Used (connect to Vss)
VEN	2	O	Active High Voltage Translation Enable. This signal is optionally used to switch the input voltage divider on/off to reduce the power consumption (typ 45 uA) of the divider network.
P1	3	O	LED 1 or Not Used (connect to Vss). This pin is also used to drive an LED for single-LED mode. Use a small signal N-FET (Q1) in series with the LED as shown on Figure 9.
BAT	4	I	Translated Battery Voltage Input
CE	5	I	Chip Enable. Internal LDO is disconnected from REGIN when driven low.
REGIN	6	P	Internal integrated LDO input. Decouple with a 0.1-µF ceramic capacitor to Vss.
REG25	7	P	2.5-V Output voltage of the internal integrated LDO. Decouple with 1-µF ceramic capacitor to Vss
VSS	8	P	Device ground
SRP	9	I	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is nearest the BAT– connection.
SRN	10	I	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRN is nearest the PACK– connection.
P6/TS	11	I	Pack thermistor voltage sense (use 103AT-type thermistor)
P5/HDQ	12	I/O	Open drain HDQ Serial communication line (slave)
P4/SCL	13	I	Slave I^{2}C serial communication clock input. Use with a 10-K pull-up resistor (typical). Also used for LED 4 in the four-LED mode.
P3/SDA	14	I/O	Open drain slave I^{2}C serial communication data line. Use with a 10-kΩ pull-up resistor (typical). Also used for LED 3 in the four-LED mode.

(1) I = Input, O = Output, P = Power, I/O = Digital input/output

PRODUCT PREVIEW

TYPICAL IMPLEMENTATION

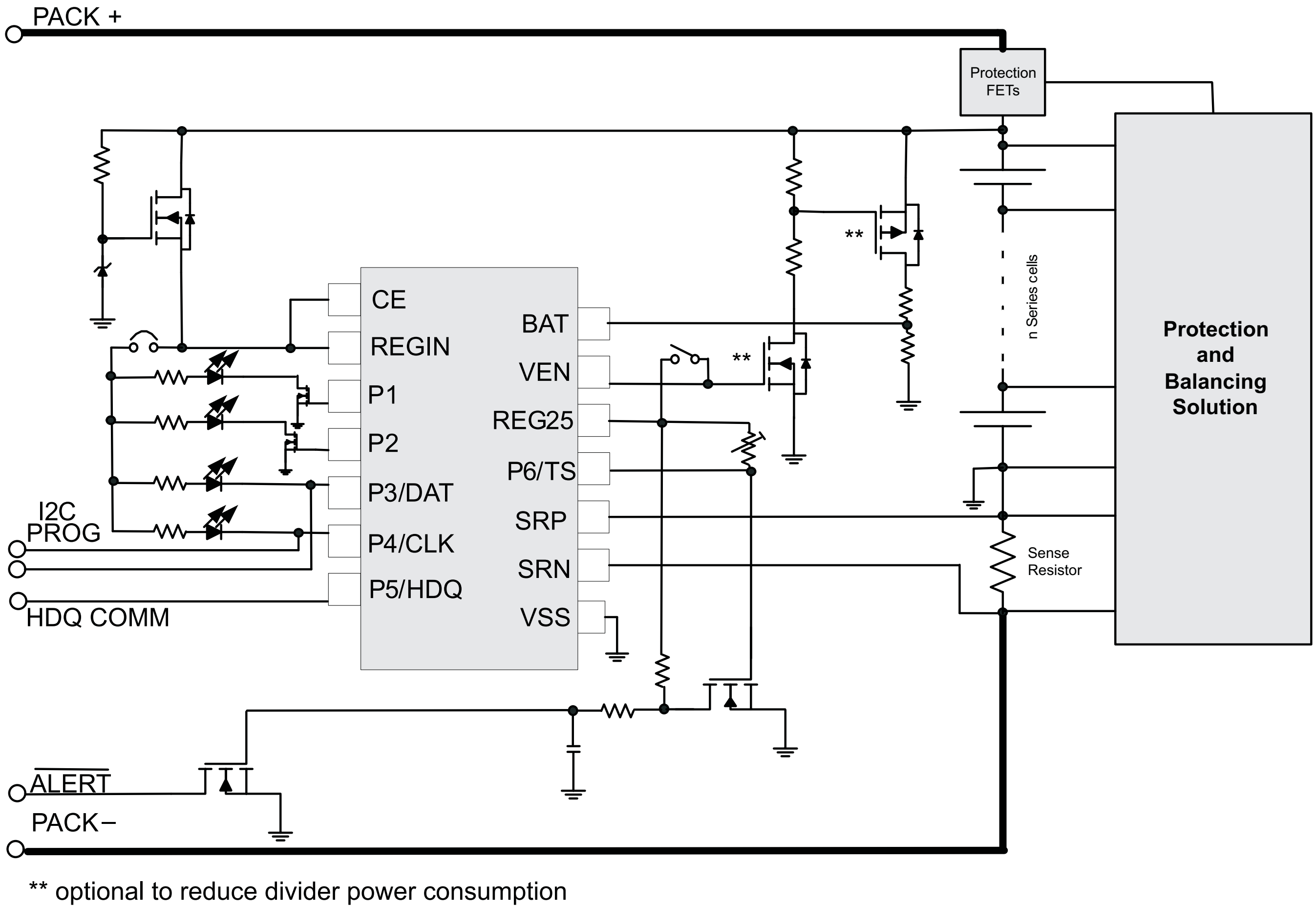

Figure 2. bq34z110 Typical Implementation

THERMAL INFORMATION

THERMAL METRIC(1)		bq34z110 TSSOP (14-Pins)	UNITS
$θ_{JA, High K}$	Junction-to-ambient thermal resistance	103.8	°C/W
$θ_{JC(top)}$	Junction-to-case(top) thermal resistance	31.9	
$θ_{JB}$	Junction-to-board thermal resistance	46.6	
$ψ_{JT}$	Junction-to-top characterization parameter	2.0	
$ψ_{JB}$	Junction-to-board characterization parameter	45.9	
$θ_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		VALUE		UNIT
		MIN	MAX	
V_{REGIN}	Regulator Input Range	–0.3	5.5	V
V_{CC}	Supply Voltage Range	–0.3	2.75	V
V_{IOD}	Open-drain I/O pins (SDA, SCL, HDQ)	–0.3	5.5	V
V_{BAT}	Bat Input pin	–0.3	5.5	V
V_I	Input Voltage range to all other pins (P1, P2, SRP, SRN)	–0.3	VCC + 0.3	V
ESD	Human-body model (HBM), BAT pin		1.5	kV
	Human-body model (HBM), all other pins		2	kV
T_A	Operating free-air temperature range	–40	85	°C
T_F	Functional temperature range	–40	100	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 25ºC, C_{LDO25} = 1 µF, and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{REGIN}	Supply Voltage	No operating restrictions	2.7		4.5	V
		No FLASH writes	2.45		2.7	V
C_{REGIN}	External input capacitor for internal LDO between REGIN and VSS	Nominal capacitor values specified. Recommend a 10% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{LDO25}	External output capacitor for internal LDO between VCC and VSS		0.47	1		µF
I_{CC}	Normal operating-mode current	Gas Gauge in NORMAL mode, I_{LOAD} > ***Sleep Current***		140		µA
I_{SLP}	SLEEP operating-mode current	Gas Gauge in SLEEP mode, I_{LOAD} < Sleep Current		64		µA
I_{SLP+}	FULL SLEEP operating-mode current	Gas Gauge in FULL SLEEP mode, I_{LOAD} < ***Sleep Current***		19		µA
V_{OL}	Output voltage, low (SCL, SDA, HDQ)	I_{OL} = 3 mA			0.4	V
$V_{OH(PP)}$	Output voltage, high	I_{OH} = –1 mA	V_{CC} – 0.5			V
$V_{OH(OD)}$	Output voltage, high (SDA, SCL, HDQ)	External pull-up resistor connected to V_{CC}	V_{CC} – 0.5			V
V_{IL}	Input voltage, low		–0.3		0.6	V
$V_{IH(OD)}$	Input voltage, high (SDA, SCL, HDQ)		1.2		6	V
V_{A1}	Input voltage range (TS)		VSS – 0.05		1	V
V_{A2}	Input voltage range (BAT)		VSS – 0.125		5	V
V_{A3}	Input voltage range (SRP, SRN)		VSS – 0.125		0.125	V
I_{LKG}	Input leakage current (I/O pins)				0.3	µA
t_{PUCD}	Power-up communication delay			250		ms

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POWER-ON RESET

T_A = –40°C to 85°C; Typical Values at TA = 25°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going battery voltage input at REG25		2.05	2.20	2.31	V
V_{HYS}	Power-on reset hysteresis		45	115	185	mV

LDO REGULATOR

T_A = 25°C, C_{LDO25} = 1 µF, V_{REGIN} = 3.6 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITION		MIN	NOM	MAX	UNIT
V_{REG25}	Regulator output voltage	2.7 V ≤ V_{REGIN} ≤ 4.5 V, I_{OUT} ≤ 16 mA	T_A= –40°C to 85°C	2.3	2.5	2.7	V
		2.45 V ≤ V_{REGIN} < 2.7 V (low battery), I_{OUT} ≤ 3 mA	T_A = –40°C to 85°C	2.3			
I_{SHORT} (2)	Short Circuit Current Limit	V_{REG25} = 0 V	T_A = –40°C to 85°C			250	mA

(1) LDO output current, I_{OUT}, is the sum of internal and external load currents.
(2) Assured by design. Not production tested.

INTERNAL TEMPERATURE SENSOR CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{TEMP}	Temperature sensor voltage gain			–2		mV/°C

LOW-FREQUENCY OSCILLATOR

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(1)(2)	T_A = 0°C to 60°C	–1.5%	0.25%	1.5%	
		T_A = –20°C to 70°C	–2.5%	0.25%	2.5%	
		T_A = –40°C to 85°C	–4%	0.25%	4%	
$t_{(LSXO)}$	Start-up time(3)			500		µs

(1) The frequency drift is included and measured from the trimmed frequency at VCC = 2.5 V, T_A = 25°C.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

HIGH-FREQUENCY OSCILLATOR

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency			8.389		MHz
$f_{(EIO)}$	Frequency error(1)(2)	T_A = 0°C to 60°C	–2%	0.38%	2%	
		T_A = –20°C to 70°C	–3%	0.38%	3%	
		T_A = –40°C to 85°C	–4.5%	0.38%	4.5%	
$t_{(SXO)}$	Start-up time(3)			2.5	5	ms

(1) The frequency error is measured from 2.097 MHz.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

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INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SR)}$	Input voltage range, $V_{(SRN)}$ and $V_{(SRP)}$	$V_{(SR)} = V_{(SRN)} – V_{(SRP)}$	–0.125		0.125	V
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
$V_{OS(SR)}$	Input offset			10		µV
I_{NL}	Integral nonlinearity error			±0.007	±0.034	% FSR
$Z_{IN(SR)}$	Effective input resistance (1)		2.5			MΩ
$I_{lkg(SR)}$	Input leakage current[1]				0.3	µA

(1) Assured by design. Not tested in production.

ADC (TEMPERATURE AND CELL MEASUREMENT) CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(ADC)}$	Input voltage range		0.05		1	V
t_{ADC_CONV}	Conversion time				125	ms
	Resolution		14		15	bits
$V_{OS(ADC)}$	Input offset			1		mV
Z_{ADC1}	Effective input resistance (TS) (1)		8			MΩ
Z_{ADC2}	Effective input resistance (BAT)(1)	bq34z110 not measuring cell voltage	8			MΩ
		bq34z110 measuring cell voltage		100		KΩ
$I_{lkg(ADC)}$	Input leakage current (1)				0.3	µA

DATA FLASH MEMORY CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention[1]		10			Years
	Flash-programming write cycles[1]		20,000			Cycles
$t_{WORDPROG}$	Word programming time[1]				2	ms
I_{CCPROG}	Flash-write supply current[1]			5	10	mA

(1) Assured by design. Not tested in production.

HDQ COMMUNICATION TIMING CHARACTERISTICS

T_A = –40°C to 85°C, C_{REG} = 0.47 µF, 2.45 V < V_{REGIN} = V_{BAT} < 5.5 V; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CYCH)}$	Cycle time, host to bq34z110		190			µs
$t_{(CYCD)}$	Cycle time, bq34z110 to host		190	205	250	µs
$t_{(HW1)}$	Host sends 1 to bq34z110		0.5		50	µs
$t_{(DW1)}$	bq34z110 sends 1 to host		32		50	µs
$t_{(HW0)}$	Host sends 0 to bq34z110		86		145	µs
$t_{(DW0)}$	bq34z110 sends 0 to host		80		145	µs
$t_{(RSPS)}$	Response time, bq34z110 to host		190		950	µs
$t_{(B)}$	Break time		190			µs
$t_{(BR)}$	Break recovery time		40			µs
$t_{(RISE)}$	HDQ line rising time to logic 1 (1.2 V)				950	ns
$t_{(RST)}$	HDQ Reset		1.8		2.2	s

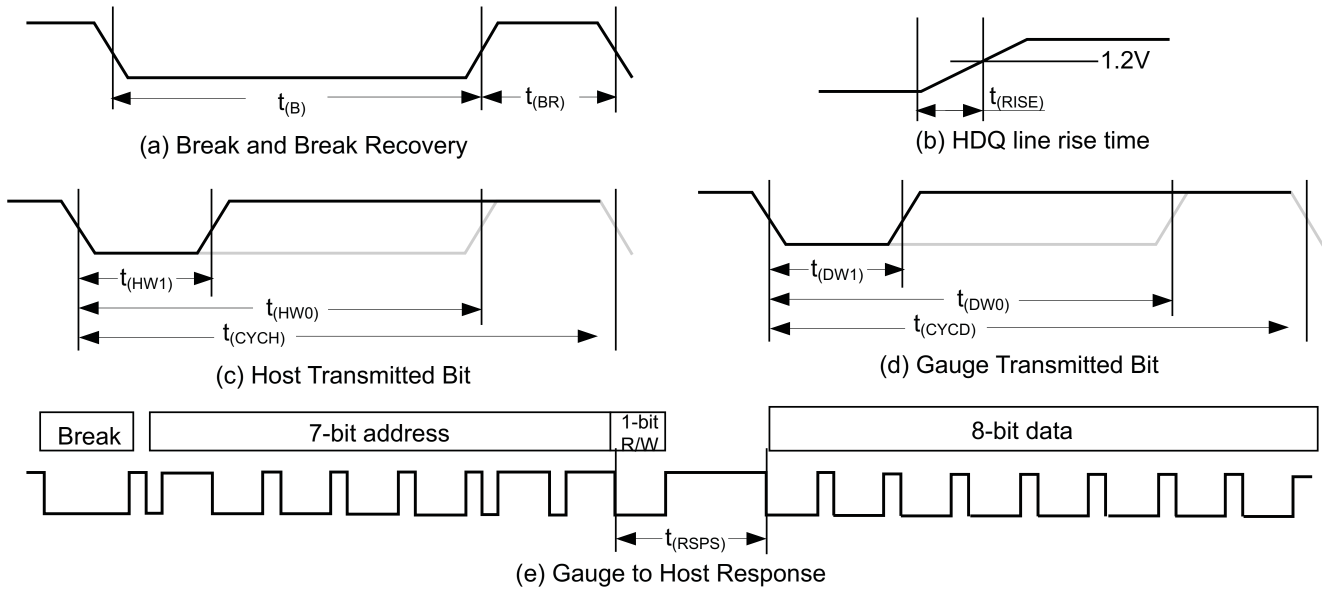

Figure 3. Timing Diagrams

PRODUCT PREVIEW

I²C-COMPATIBLE INTERFACE TIMING CHARACTERISTICS

T_A = –40°C to 85°C, C_{REG} = 0.47 μF, 2.45 V < V_{REGIN} = V_{BAT} < 5.5 V; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	SCL/SDA rise time				300	ns
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse width (high)		600			ns
$t_{w(L)}$	SCL pulse width (low)		1.3			μs
$t_{su(STA)}$	Setup for repeated start		600			ns
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{su(DAT)}$	Data setup time		100			ns
$t_{h(DAT)}$	Data hold time		0			ns
$t_{su(STOP)}$	Setup time for stop		600			ns
t_{BUF}	Bus free time between stop and start		66			μs
f_{SCL}	Clock frequency				400	kHz

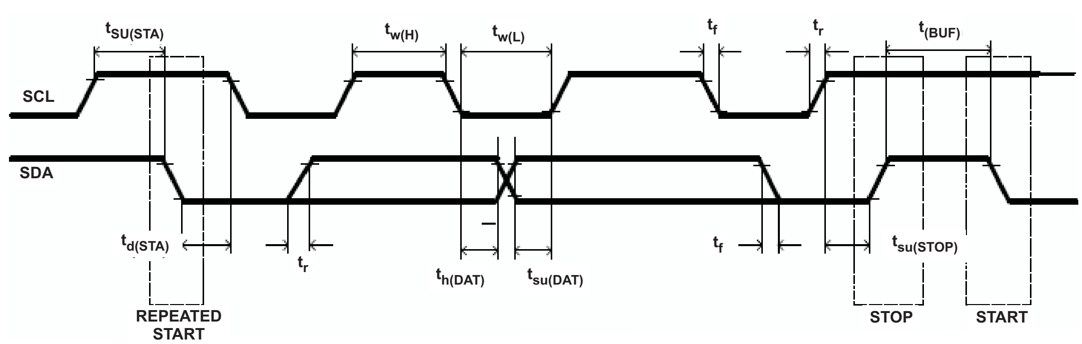

Figure 4. I²C-Compatible Interface Timing Diagrams

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
BQ34Z110PW	PREVIEW	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ34Z110PWR	PREVIEW	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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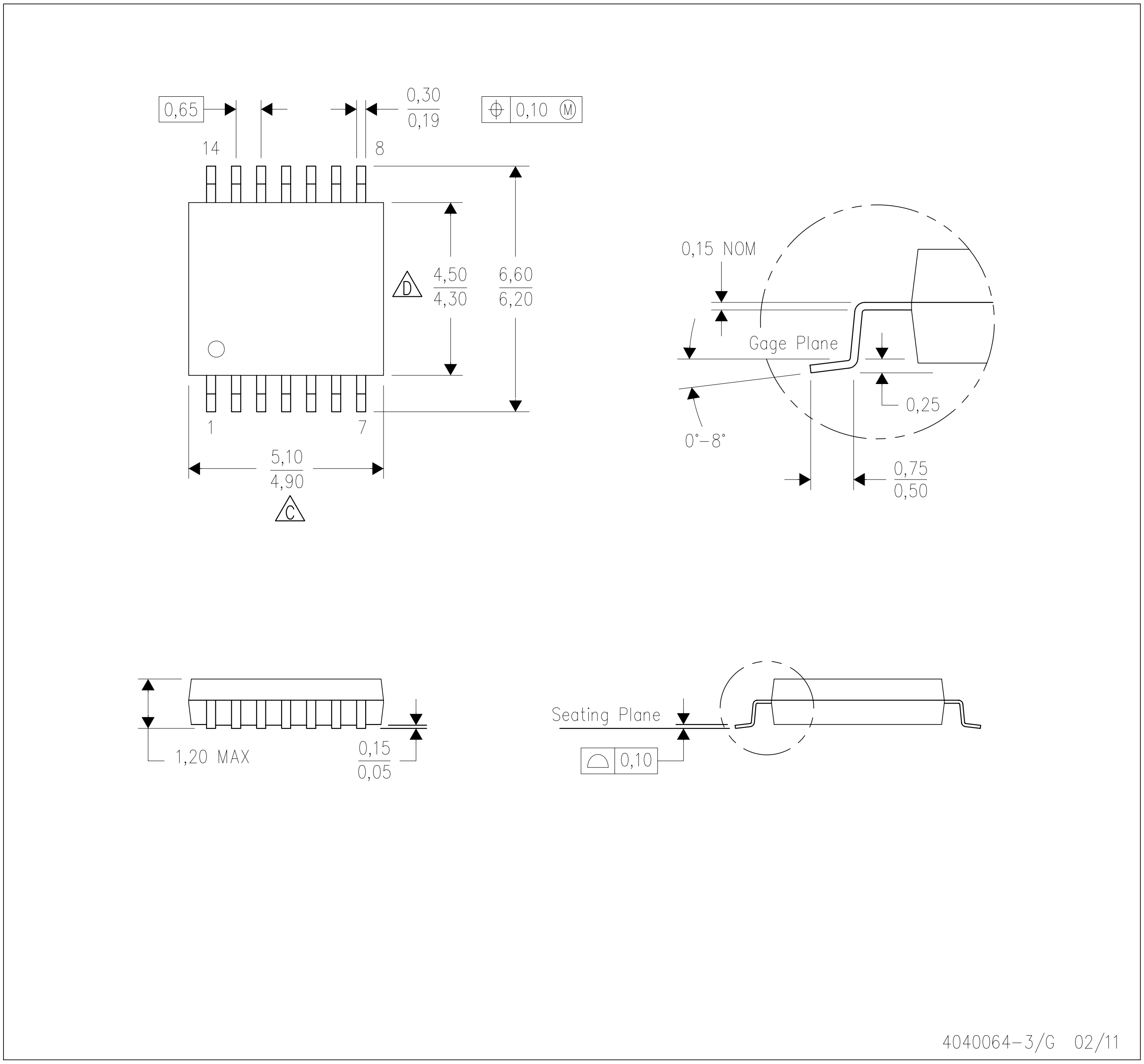
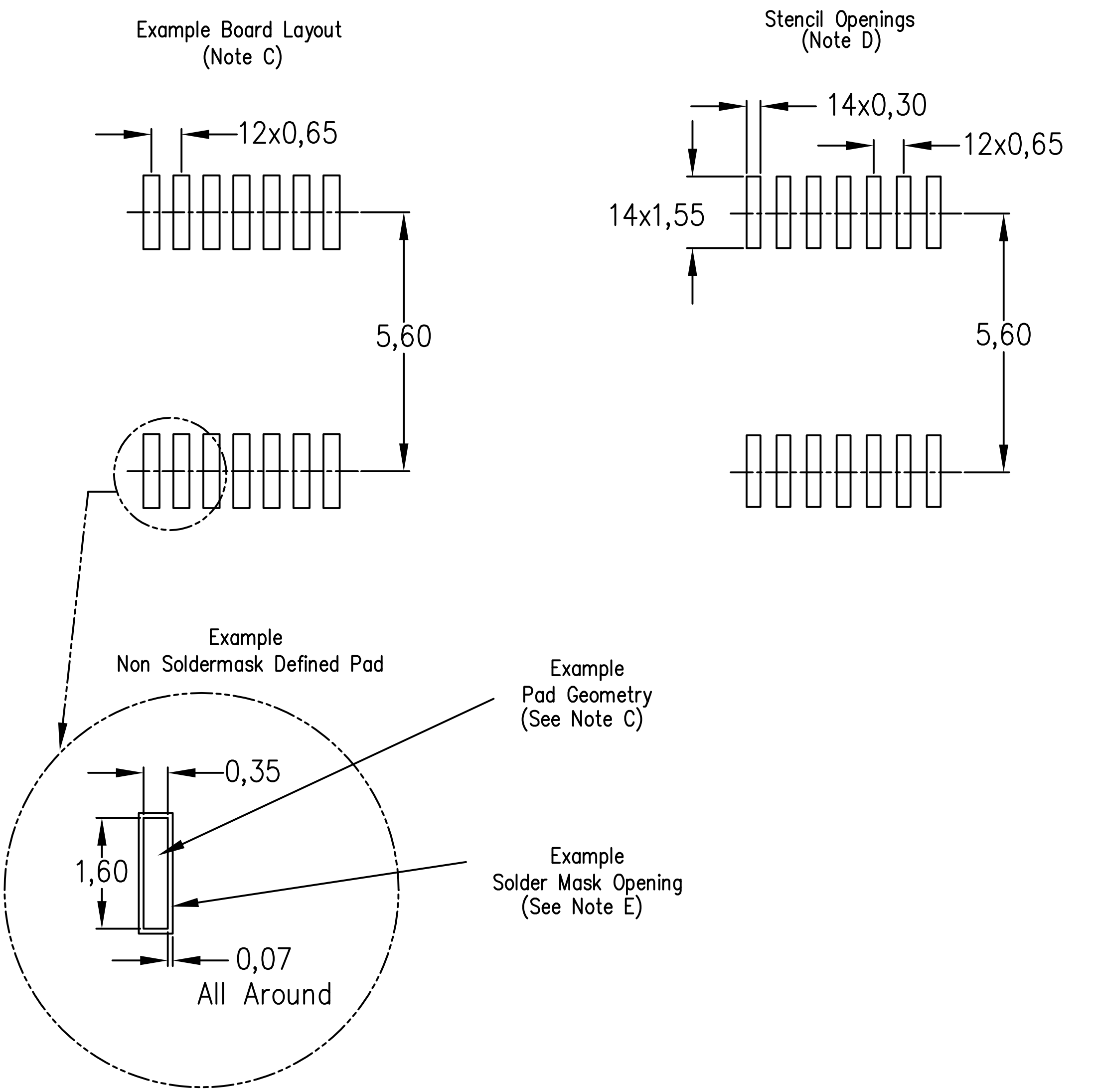
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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