System-Side Impedance Track™ Fuel Gauge

Check for Samples: bq27441-G1

FEATURES

- **Single Series Cell Li-Ion Battery Fuel Gauge**
  - **Resides on System Board**
  - **Supports Embedded or Removable Batteries**
  - **Powered Directly from Battery with Integrated LDO**
  - **Supports a Low-Value External Sense Resistor (10mΩ)**
- **Easy to Configure Fuel Gauging Based on Patented Impedance Track™ Technology**
  - **Reports Remaining Capacity and State of Charge (SOC) with Smoothing Filter**
  - **Automatically Adjusts for Battery Aging, Self-discharge, Temperature, and Rate Changes**
  - **Battery State of Health (Aging) Estimation**
- **Microcontroller Peripheral Supports:**
  - **400-kHz I²C™ Serial Interface**
  - **Configurable SOC Interrupt, or Battery Low Digital Output Warning**
  - **Internal Temperature Sensor, or Host Reported Temperature**
- **Small 12-pin 2.5 mm × 4 mm SON Package**

APPLICATIONS

- **Smartphones, Feature Phones and Tablets**
- **Digital Still and Video Cameras**
- **Handheld Terminals**
- **MP3 or Multimedia Players**

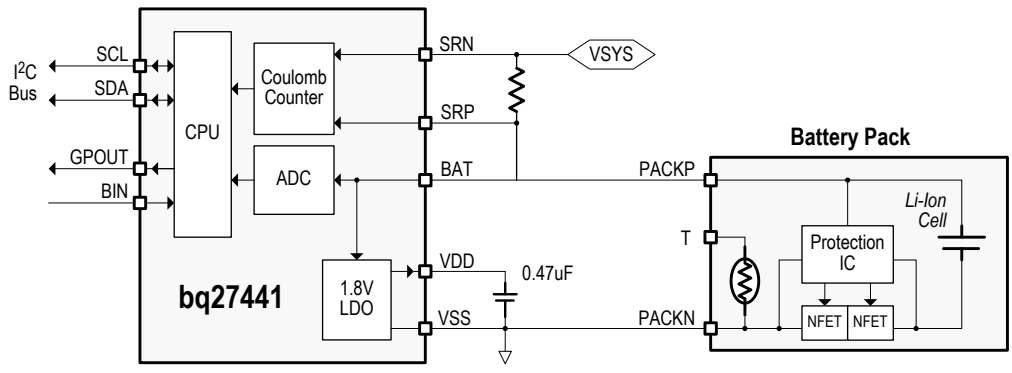
DESCRIPTION

The Texas Instruments bq27441-G1 is an easy to configure microcontroller peripheral that provides system-side fuel gauging for single-cell Li-Ion batteries. The device requires minimal user configuration and system microcontroller firmware development.

The bq27441-G1 uses the patented Impedance Track™ algorithm for fuel gauging, and provides information such as remaining battery capacity (mAh), state-of-charge (%), and battery voltage (mV).

Battery fuel gauging with the bq27441-G1 requires connections only to PACK+ (P+) and PACK– (P–) for a removable battery pack or embedded battery circuit. The tiny 12-pin 2.5 mm × 4 mm SON package is ideal for space constrained applications.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

AVAILABLE OPTIONS

PART NUMBER	BATTERY TYPE	CHEM_ID (1)	DM_CODE (2)	FIRMWARE VERSION (3)	PACKAGE (4)
bq27441DRZR-G1A	$LiCoO_2$ (4.2 V max charge)	0x0128	0x48	1.09 (0x0109)	12-pin, 2.5 × 4 mm SON
bq27441DRZT-G1A					
bq27441DRZR-G1B	$LiMn_2O_4$ (4.3 - 4.35 V max charge)	0x0312	0x58		
bq27441DRZT-G1B					

(1) See the CHEM_ID subcommand to confirm the battery chemistry type.
(2) See the DM_CODE subcommand to confirm the Data Memory code.
(3) See the FW_VERSION subcommand to confirm the firmware version.
(4) For the most current package and ordering information see the Package Option Addendum at the end of this document; or, see the TI website at www.ti.com.

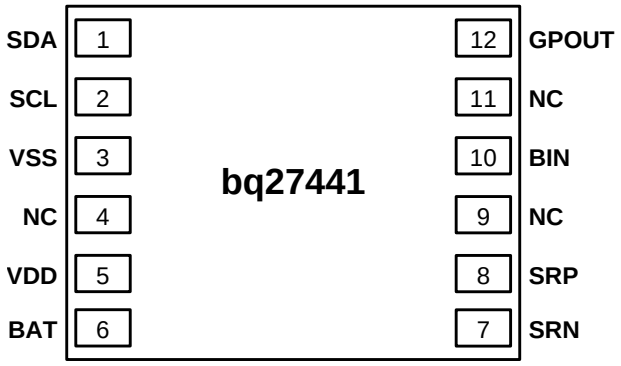
THERMAL INFORMATION

THERMAL METRIC (1)		bq27441-G1 DRZ (12-PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	64.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	59.8	
θ_{JB}	Junction-to-board thermal resistance	52.7	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	28.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN DIAGRAM AND PACKAGE DIMENSIONS

PIN DIAGRAM
(TOP VIEW)



12-pin VSON, 2.5 x 4mmm 0.4mm pitch

PIN FUNCTIONS

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BAT	6	PI, AI	LDO regulator input, battery voltage input, and coulomb counter input typically connected to the PACK+ terminal.
VDD	5	PO	1.8V Regulator Output. Decouple with 0.47µF ceramic capacitor to Vss. This pin is not intended to provide power for other devices in the system.
VSS	3	PI	Ground pin.
SRP	8	AI	Coulomb counter differential inputs expecting an external 10mΩ, 1% sense resistor. Connect SRP to BAT (CELLP) and connect SRN to PACKP. Refer to application diagram.
SRN	7	AI	
GPOUT	12	DO	General Purpose open-drain output. May be configured as a Battery Low indicator or perform SOC interrupt (SOC_INT) function.
SDA	1	DIO	Slave I^2C serial bus for communication with system (Master). Open-drain pins. Use with external 10kΩ pull-up resistors (typical) for each pin. If the external pull-up resistors will be disconnected from these pins during normal operation, recommend using external 1MΩ pull-down resistors to VSS at each pin to avoid floating inputs.
SCL	2	DIO	
BIN	10	DI	Battery-insertion detection input. A logic high to low transition is detected as a battery insertion event. Recommend using a pull-up resistor >1MΩ (1.8 MΩ typical) to VDD for reduced power consumption. An internal pull-up resistor option is also available.
NC	4, 8, 11	--	No internal connection. May be left floating or tied to VSS.

(1) I/O = Digital input/output, IA = Analog input, P = Power connection

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
V_{BAT}	BAT pin input voltage range	–0.3	6	V
V_{SR}	SRP and SRN pins input voltage range	-0.3	[V_{BAT} + 0.3]	V
	Differential voltage across SRP and SRN. ABS(SRP - SRN).		2	V
V_{DD}	VDD pin supply voltage range (LDO ouptut)	–0.3	2	V
V_{IOD}	Open-drain I/O pins (SDA, SCL)	–0.3	6	V
V_{IOPP}	Push-Pull I/O pins (BIN)	–0.3	[V_{DD} + 0.3]	V
T_A	Operating free-air temperature range	–40	85	°C
T_{STG}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 30°C and V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{BAT}(1)	External input capacitor for internal LDO between BAT and V_{SS}	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{LDO18} (1)	External output capacitor for internal LDO between V_{DD} and V_{SS}			0.47		µF
V_{PU} (1)	External pull-up voltage for open-drain pins (SDA, SCL, GPOUT)		1.62		3.6	V

(1) Specified by design. Not production tested.

SUPPLY CURRENT

T_A = 30°C and V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} (1)	NORMAL mode current	I_{LOAD} > ***Sleep Current*** (2)		93		µA
I_{SLP} (1)	SLEEP mode current	I_{LOAD} < ***Sleep Current*** (2)		21		µA
I_{HIB} (1)	HIBERNATE mode current	I_{LOAD} < ***Hibernate Current*** (2)		9		µA
I_{SD} (1)	SHUTDOWN mode current	Fuel gauge in host commanded SHUTDOWN mode. (LDO Regulator Output Disabled.)		0.6		µA

(1) Specified by design. Not production tested.
(2) Wake Comparator Disabled.

DIGITAL INPUT AND OUTPUT DC CHARACTERISTICS

T_A = –40°C to 85°C, typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH(OD)}$	Input voltage, high (2)	External pullup resistor to V_{PU}	V_{PU} x 0.7			V
$V_{IH(PP)}$	Input voltage, high (3)		1.4			V
V_{IL}	Input voltage, low (2) (3)				0.6	V
V_{OL}	Output voltage, low (2)				0.6	V
I_{OH}	Output source current, high (2)				0.5	mA
$I_{OL(OD)}$	Output sink current, low (2)				-3	mA
C_{IN} (1)	Input capacitance (2) (3)				5	pF
I_{lkg}	Input leakage current (I/O pins) (2) (3)				1	µA

(1) Specified by design. Not production tested.
(2) Open Drain pins: (SCL, SDA, GPOUT)
(3) Push Pull pin: (BIN)

LDO REGULATOR, WAKE-UP AND AUTO-SHUTDOWN DC CHARACTERISTICS

T_A = –40°C to 85°C, typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	BAT pin regulator input		2.45		4.5	V
V_{DD}	Regulator output voltage			1.8		V
$UVLO_{IT+}$	V_{BAT} Under Voltage Lock Out LDO Wake-Up Rising Threshold			2		V
$UVLO_{IT-}$	V_{BAT} Under Voltage Lock Out LDO Auto-Shutdown Falling Threshold			1.95		V
V_{WU+} (1)	GPOUT (input) LDO Wake-Up rising edge threshold (2)	LDO Wake-up from SHUTDOWN mode	1.2			V

(1) Specified by design. Not production tested.
(2) If the device is commanded to SHUTDOWN via I2C with V_{BAT} > $UVLO_{IT+}$, a wake-up rising edge trigger is required on GPOUT .

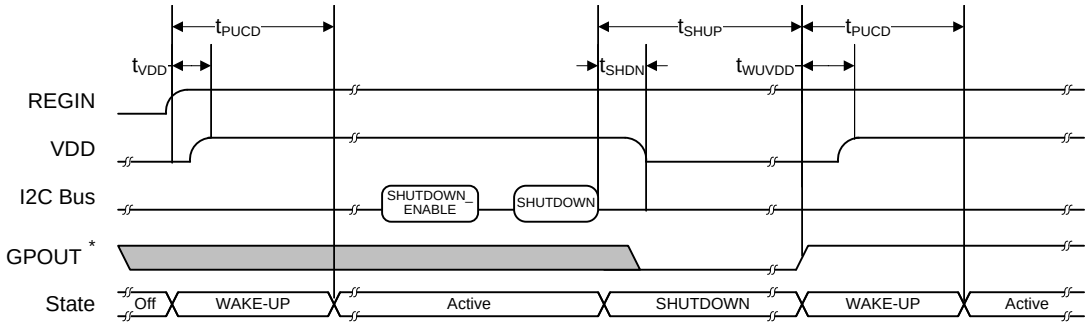
LDO REGULATOR, WAKE-UP AND AUTO-SHUTDOWN AC CHARACTERISTICS

T_A = –40°C to 85°C, typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SHDN} (1)	SHUTDOWN Entry Time	Time delay from SHUTDOWN command to LDO output disable.			250	ms
t_{SHUP} (1)	SHUTDOWN GPOUT Low time	Minimum low time of GPOUT (input) in SHUTDOWN before WAKEUP	10			µs
t_{VDD} (1)	Initial V_{DD} Output delay			13		ms
t_{WUVDD} (1)	Wake-up V_{DD} Output delay	Time delay from rising edge of GPOUT (input) to nominal VDD output.		8		ms
t_{PUCD}	Power-up communication delay	Time delay from rising edge of REGIN to the Active state. Includes firmware initialization time.		250		ms

(1) Specified by design. Not production tested.

SHUTDOWN and WAKE-UP Timing



* GPOUT is configured as an input for wake-up signaling.

Figure 1. SHUTDOWN and WAKE-UP Timing Diagram

ADC (TEMPERATURE AND CELL MEASUREMENT) CHARACTERISTICS

T_A = –40°C to 85°C; typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(BAT)}$	BAT pin voltage measurement range.	Voltage divider enabled.	2.45		4.5	V
t_{ADC_CONV}	Conversion time			125		ms
	Effective Resolution			15		bits

(1) Specified by design. Not tested in production.

INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

T_A = –40°C to 85°C; typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SR}	Input voltage range from BAT to SRX pins			BAT ± 25		mV
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Effective Resolution	Single conversion		16		bits

(1) Assured by design. Not tested in production.

I²C-COMPATIBLE INTERFACE COMMUNICATION TIMING CHARACTERISTICS

T_A = –40°C to 85°C; typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standard Mode (100 kHz)						
$t_{d(STA)}$	Start to first falling edge of SCL		4			µs
$t_{w(L)}$	SCL pulse duration (low)		4.7			µs
$t_{w(H)}$	SCL pulse duration (high)		4			µs
$t_{su(STA)}$	Setup for repeated start		4.7			µs
$t_{su(DAT)}$	Data setup time	Host drives SDA	250			ns
$t_{h(DAT)}$	Data hold time	Host drives SDA	0			ns
$t_{su(STOP)}$	Setup time for stop		4			µs
$t_{(BUF)}$	Bus free time between stop and start	Includes Command Waiting Time	66			µs
t_f	SCL/SDA fall time (1)				300	ns
t_r	SCL/SDA rise time (1)				300	ns
f_{SCL}	Clock frequency(2)				100	kHz
Fast Mode (400 kHz)						
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{w(L)}$	SCL pulse duration (low)		1300			ns
$t_{w(H)}$	SCL pulse duration (high)		600			ns
$t_{su(STA)}$	Setup for repeated start		600			ns
$t_{su(DAT)}$	Data setup time	Host drives SDA	100			ns
$t_{h(DAT)}$	Data hold time	Host drives SDA	0			ns
$t_{su(STOP)}$	Setup time for stop		600			ns
$t_{(BUF)}$	Bus free time between stop and start	Includes Command Waiting Time	66			µs
t_f	SCL/SDA fall time (1)				300	ns
t_r	SCL/SDA rise time (1)				300	ns
f_{SCL}	Clock frequency(2)				400	kHz

(1) Specified by design. Not production tested.
(2) If the clock frequency (f_{SCL}) is > 100 kHz, use 1-byte write commands for proper operation. All other transactions types are supported at 400 kHz. (Refer to I²C INTERFACE and I²C Command Waiting Time)

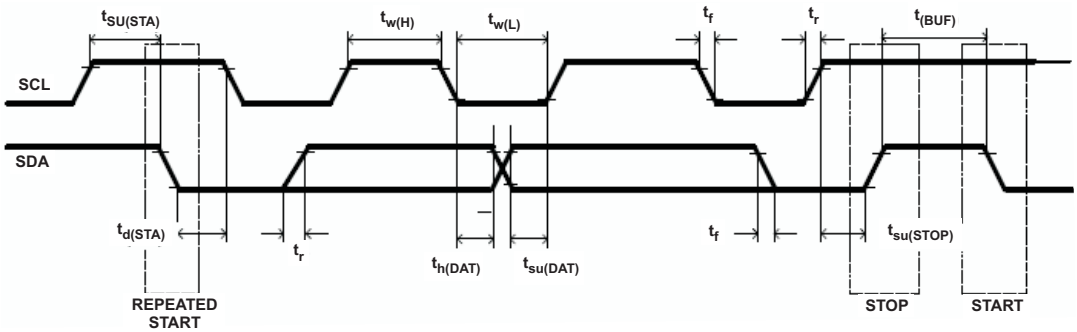


Figure 2. I²C-Compatible Interface Timing Diagrams

GENERAL DESCRIPTION

The bq27441-G1 accurately predicts the battery capacity and other operational characteristics of a single Li-based rechargeable cell. It can be interrogated by a system processor to provide cell information, such as state-of-charge (SOC).

Information is accessed through a series of commands, called *Standard Commands*. Further capabilities are provided by the additional *Extended Commands* set. Both sets of commands, indicated by the general format *Command( )*, are used to read and write information contained within the bq27441-G1 control and status registers, as well as its data locations. Commands are sent from system to gauge using the bq27441-G1's I^2C serial communications engine, and can be executed during application development, system manufacture, or end-equipment operation.

The key to the bq27441-G1's high-accuracy gas gauging prediction is Texas Instrument's proprietary Impedance Track™ algorithm. This algorithm uses cell measurements, characteristics, and properties to create state-of-charge predictions that can achieve high accuracy across a wide variety of operating conditions and over the lifetime of the battery.

The bq27441-G1 measures charge/discharge activity by monitoring the voltage across a small-value sense resistor. When a cell is attached to the bq27441-G1, cell impedance is computed, based on cell current, cell open-circuit voltage (OCV), and cell voltage under loading conditions.

The bq27441-G1 uses an integrated temperature sensor for estimating cell temperature. Alternatively, the host processor can provide temperature data for the bq27441-G1.

To minimize power consumption, the bq27441-G1 has several power modes: INITIALIZATION, NORMAL, SLEEP, and HIBERNATE. The bq27441-G1 passes automatically between these modes, depending upon the occurrence of specific events, though a system processor can initiate some of these modes directly. More details are found in the *bq27441-G1 Technical Reference Manual (SLUUAC9)*.

NOTE

Formatting Conventions in this Document:

Commands: *italics* with parentheses( ) and no breaking spaces, for example, *RemainingCapacity( ).*

Data Flash: *italics*, **bold**, and breaking spaces, for example, ***Design Capacity***.

Register bits and flags: *italics* with brackets [ ], for example, *[TDA]*

Data flash bits: *italics*, **bold**, and brackets [ ], for example, ***[LED1]***

Modes and states: ALL CAPITALS, for example, UNSEALED mode.

DATA COMMANDS

STANDARD DATA COMMANDS

The bq27441-G1 uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in . Because each command consists of two bytes of data, two consecutive I^2C transmissions must be executed both to initiate the command function, and to read or write the corresponding two bytes of data. Additional details are found in the *bq27441-G1 Technical Reference Manual (SLUUAC9)*.

Table 1. Standard Commands

NAME		COMMAND CODE	UNITS	SEALED ACCESS
Control( )	CNTL	0x00 / 0x01	N/A	R/W
Temperature( )	TEMP	0x02 / 0x03	0.1°K	R/W
Voltage( )	VOLT	0x04 / 0x05	mV	R
Flags( )	FLAGS	0x06 / 0x07	N/A	R
NominalAvailableCapacity( )		0x08 / 0x09	mAh	R
FullAvailableCapacity( )		0x0a / 0x0b	mAh	R
RemainingCapacity( )	RM	0x0c / 0x0d	mAh	R
FullChargeCapacity( )	FCC	0x0e / 0x0f	mAh	R
AverageCurrent( )		0x10 / 0x11	mA	R
StandbyCurrent( )		0x12 / 0x13	mA	R
MaxLoadCurrent( )		0x14 / 0x15	mA	R
AveragePower( )		0x18 / 0x19	mW	R
StateOfCharge( )	SOC	0x1c / 0x1d	%	R
IntTemperature( )		0x1e / 0x1f	0.1°K	R
StateOfHealth( )	SOH	0x20 / 0x21	num / %	R

Control( ): 0x00/0x01

Issuing a *Control( )* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control( )* command allows the system to control specific features of the bq27441-G1 during normal operation and additional features when the device is in different access modes, as described in . Additional details are found in the *bq27441-G1 Technical Reference Manual (SLUUAC9)*.

Table 2. *Control( )* Subcommands

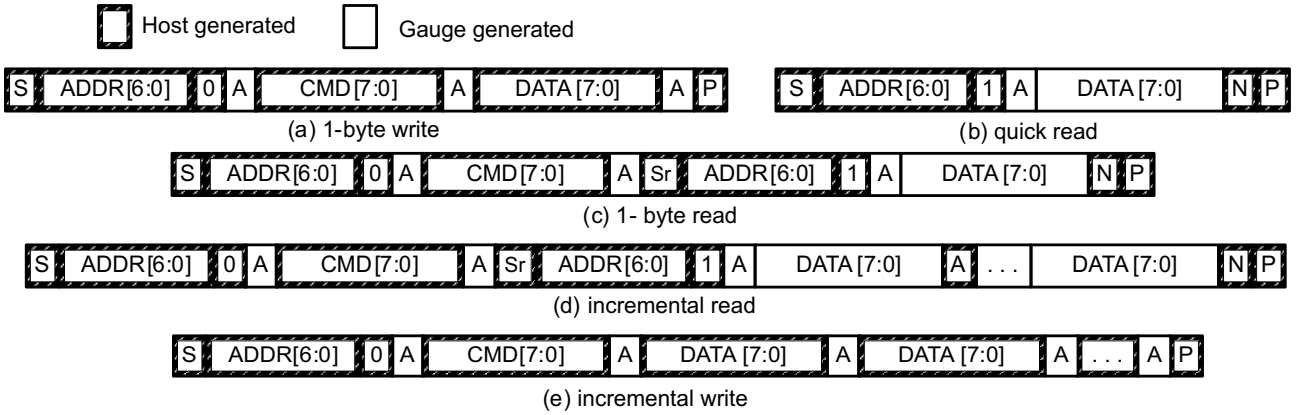
CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
CONTROL_STATUS	0x0000	Yes	Reports the status of device.
DEVICE_TYPE	0x0001	Yes	Reports the device type (0x0421).
FW_VERSION	0x0002	Yes	Reports the firmware version of the device.
DM_CODE	0x0004	Yes	Reports the Data Memory Code number stored in NVM.
PREV_MACWRITE	0x0007	Yes	Returns previous MAC command code.
CHEM_ID	0x0008	Yes	Reports the chemical identifier of the Impedance Track™ configuration
BAT_INSERT	0x000c	Yes	Forces the *[BAT_DET]* bit set when the *[BIE]* bit is 0.
BAT_REMOVE	0x000d	Yes	Forces the *[BAT_DET]* bit clear when the *[BIE]* bit is 0.
SET_HIBERNATE	0x0011	Yes	Forces CONTROL_STATUS [*HIBERNATE*] to 1.
CLEAR_HIBERNATE	0x0012	Yes	Forces CONTROL_STATUS [*HIBERNATE*] to 0.
SET_CFGUPDATE	0x0013	No	Force CONTROL_STATUS [*CFGUPMODE*] to 1 and gauge enters CONFIG UPDATE mode.
SHUTDOWN_ENABLE	0x001b	No	Enables device SHUTDOWN mode.
SHUTDOWN	0x001c	No	Commands the device to enter SHUTDOWN mode.
SEALED	0x0020	No	Places the device in SEALED access mode.
TOGGLE_GPOUT	0x0023	Yes	Commands the device to toggle the GPOUT pin for 1ms.
RESET	0x0041	No	Performs a full device reset.
SOFT_RESET	0x0042	No	Gauge exits CONFIG UPDATE mode.

See the bq27441-G1 Technical Reference Manual for detailed descriptions for the Standard Data Commands and *Control( )* subcommands.

FUNCTIONAL DESCRIPTION

I²C INTERFACE

The bq27441-G1 supports the standard I²C read, incremental read, quick read, one-byte write, and incremental write functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The first 8 bits of the I²C protocol are, therefore, 0xAA or 0xAB for write or read, respectively.

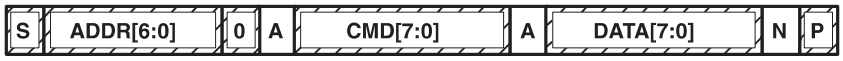


(S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The quick read returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, increments whenever data is acknowledged by the bq27441-G1 or the I²C master. “Quick writes” function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data).

The following command sequences are not supported:

Attempt to write a read-only address (NACK after data sent by master):



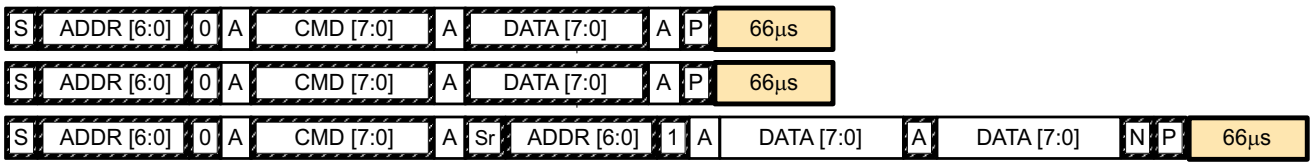
Attempt to read an address above 0x6B (NACK command):

I²C Time Out

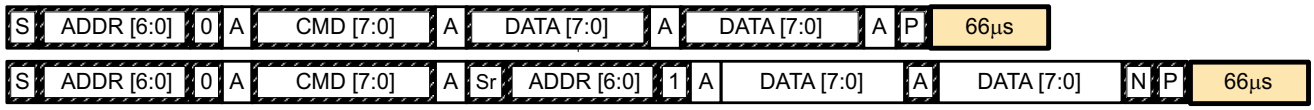
The I²C engine releases both SDA and SCL if the I²C bus is held low for 2 seconds. If the bq27441-G1 is holding the lines, releasing them frees them for the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine enters the low-power sleep mode.

I²C Command Waiting Time

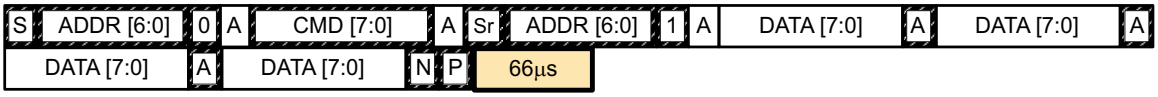
To ensure proper operation at 400 kHz, a $t_{(BUF)}$ ≥ 66 µs bus-free waiting time must be inserted between all packets addressed to the bq27441-G1. In addition, if the SCL clock frequency (f_{SCL}) is > 100 kHz, use individual 1-byte write commands for proper data flow control. The following diagram shows the standard waiting time required between issuing the control subcommand the reading the status result. For read-write standard command, a minimum of 2 seconds is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host must not issue any standard command more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.



Waiting time inserted between two 1-byte write packets for a subcommand and reading results
(required for 100 kHz < f_{SCL} ≤ 400 kHz)



Waiting time inserted between incremental 2-byte write packet for a subcommand and reading results
(acceptable for f_{SCL} ≤ 100 kHz)

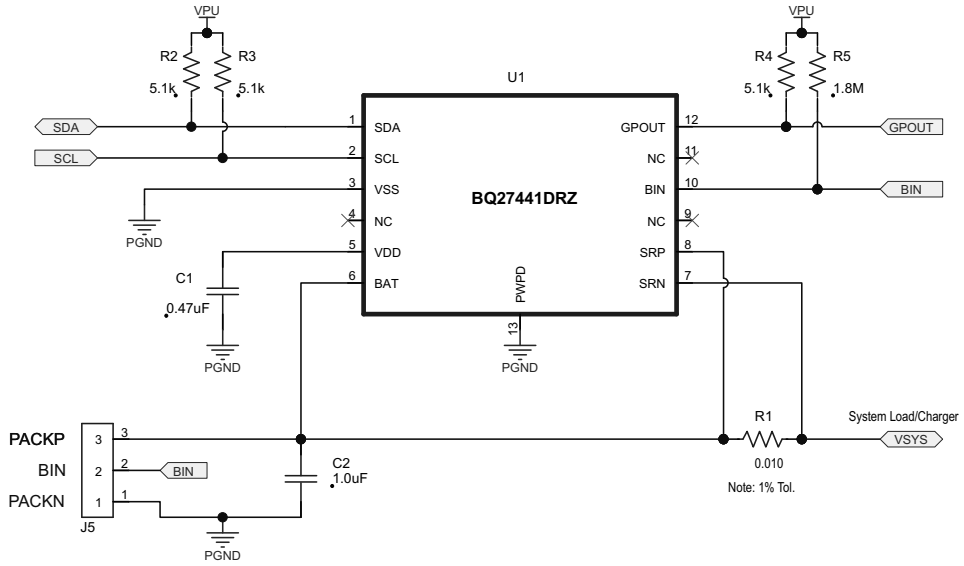


Waiting time inserted after incremental read

I²C Clock Stretching

A clock stretch can occur during all modes of fuel gauge operation. In SLEEP and HIBERNATE modes, a short ≤ 100 µs clock stretch occurs on all I²C traffic as the device must wake-up to process the packet. In the other modes (INITIALIZATION , NORMAL) a ≤ 4 ms clock stretching period may occur within packets addressed for the fuel gauge as the I²C interface performs normal data flow control.

REFERENCE SCHEMATIC



REVISION HISTORY

Changes from Original (November 2013) to Revision A	Page
• Changed the device status From Product Preview To: Production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ27441DRZR-G1A	ACTIVE	SON	DRZ	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ27 441A	Samples
BQ27441DRZR-G1B	ACTIVE	SON	DRZ	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ27 441B	Samples
BQ27441DRZT-G1A	ACTIVE	SON	DRZ	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ27 441A	Samples
BQ27441DRZT-G1B	ACTIVE	SON	DRZ	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ27 441B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

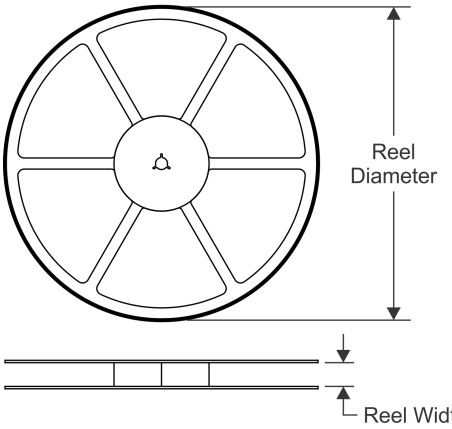
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

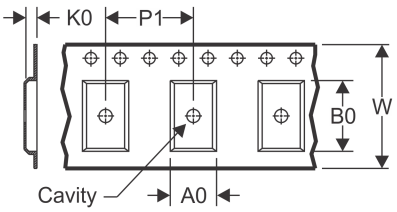
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

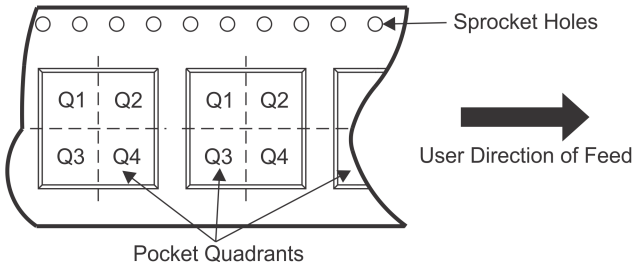


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

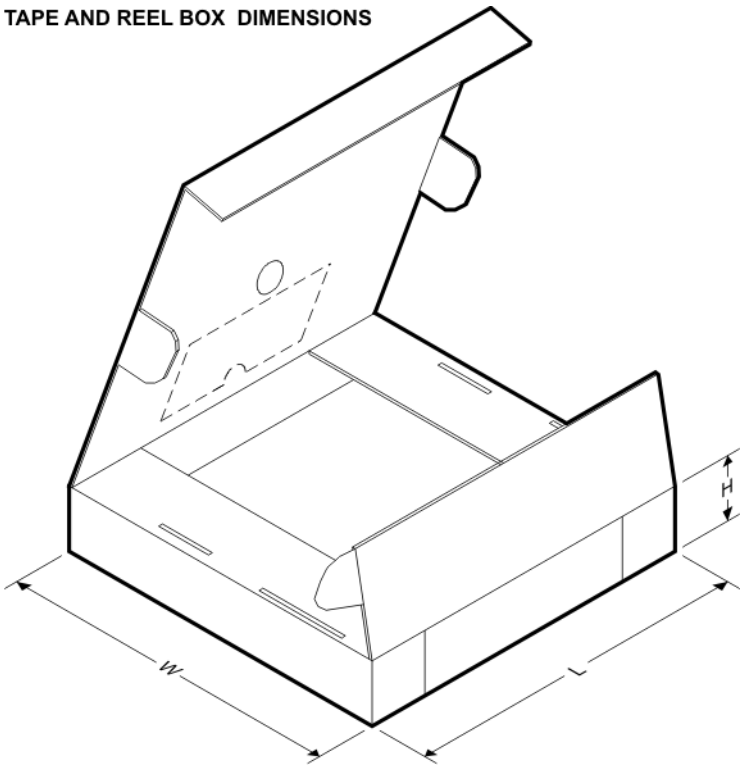
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27441DRZR-G1A	SON	DRZ	12	3000	330.0	12.4	2.8	4.3	1.2	4.0	12.0	Q2
BQ27441DRZR-G1B	SON	DRZ	12	3000	330.0	12.4	2.8	4.3	1.2	4.0	12.0	Q2
BQ27441DRZT-G1A	SON	DRZ	12	250	180.0	12.4	2.8	4.3	1.2	4.0	12.0	Q2
BQ27441DRZT-G1B	SON	DRZ	12	250	180.0	12.4	2.8	4.3	1.2	4.0	12.0	Q2

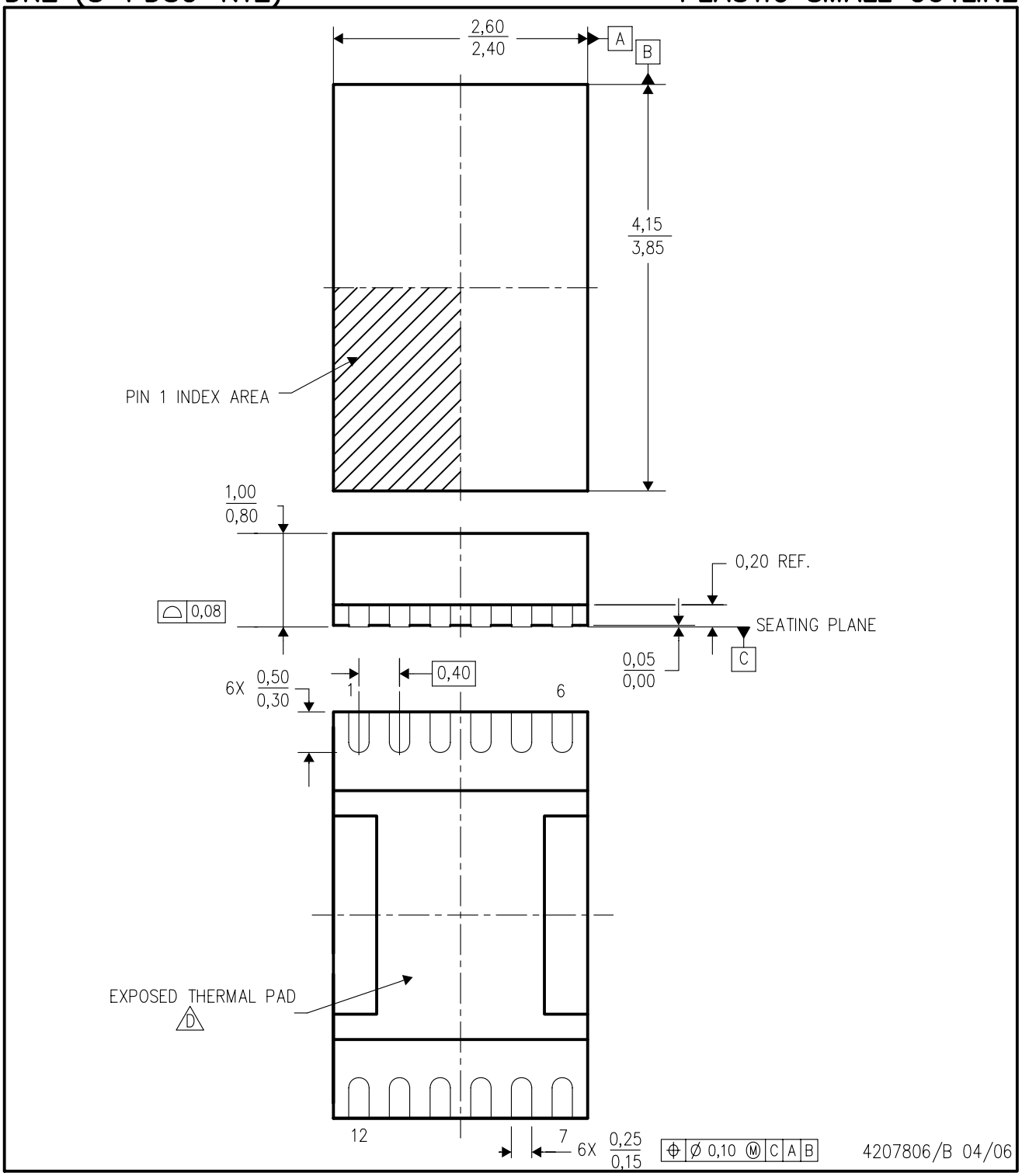
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27441DRZR-G1A	SON	DRZ	12	3000	367.0	367.0	35.0
BQ27441DRZR-G1B	SON	DRZ	12	3000	367.0	367.0	35.0
BQ27441DRZT-G1A	SON	DRZ	12	250	210.0	185.0	35.0
BQ27441DRZT-G1B	SON	DRZ	12	250	210.0	185.0	35.0

DRZ (S–PDSO–N12) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. This package is lead–free.

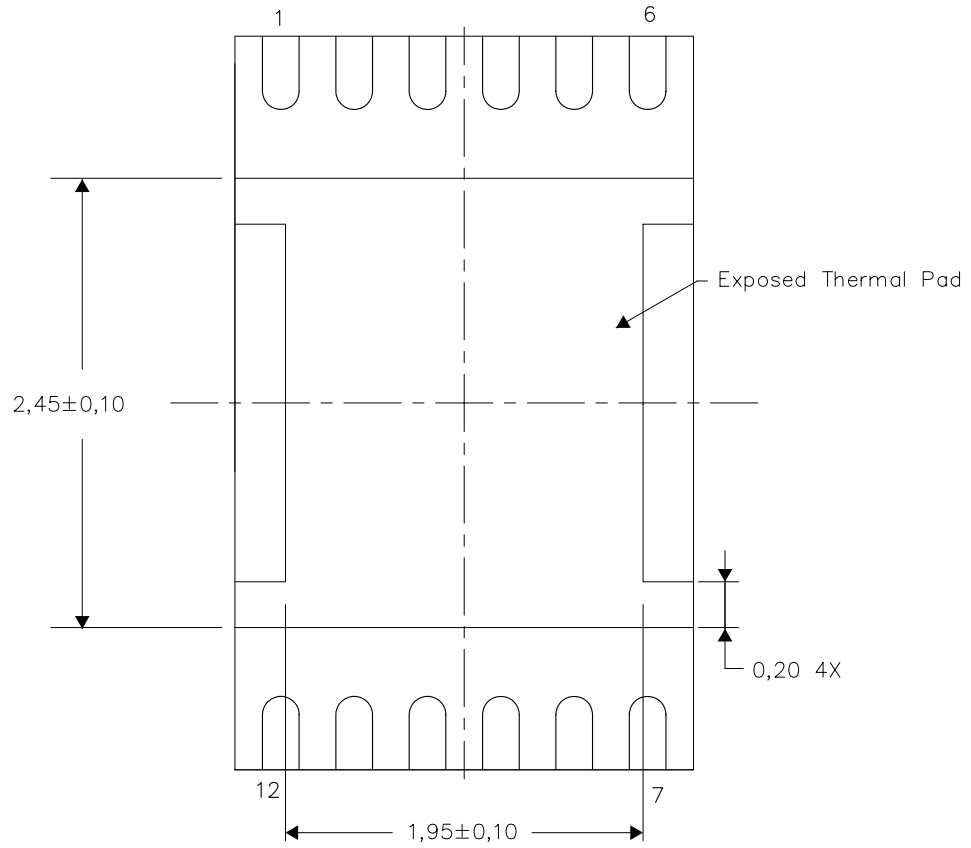
DRZ (R–PDSO–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

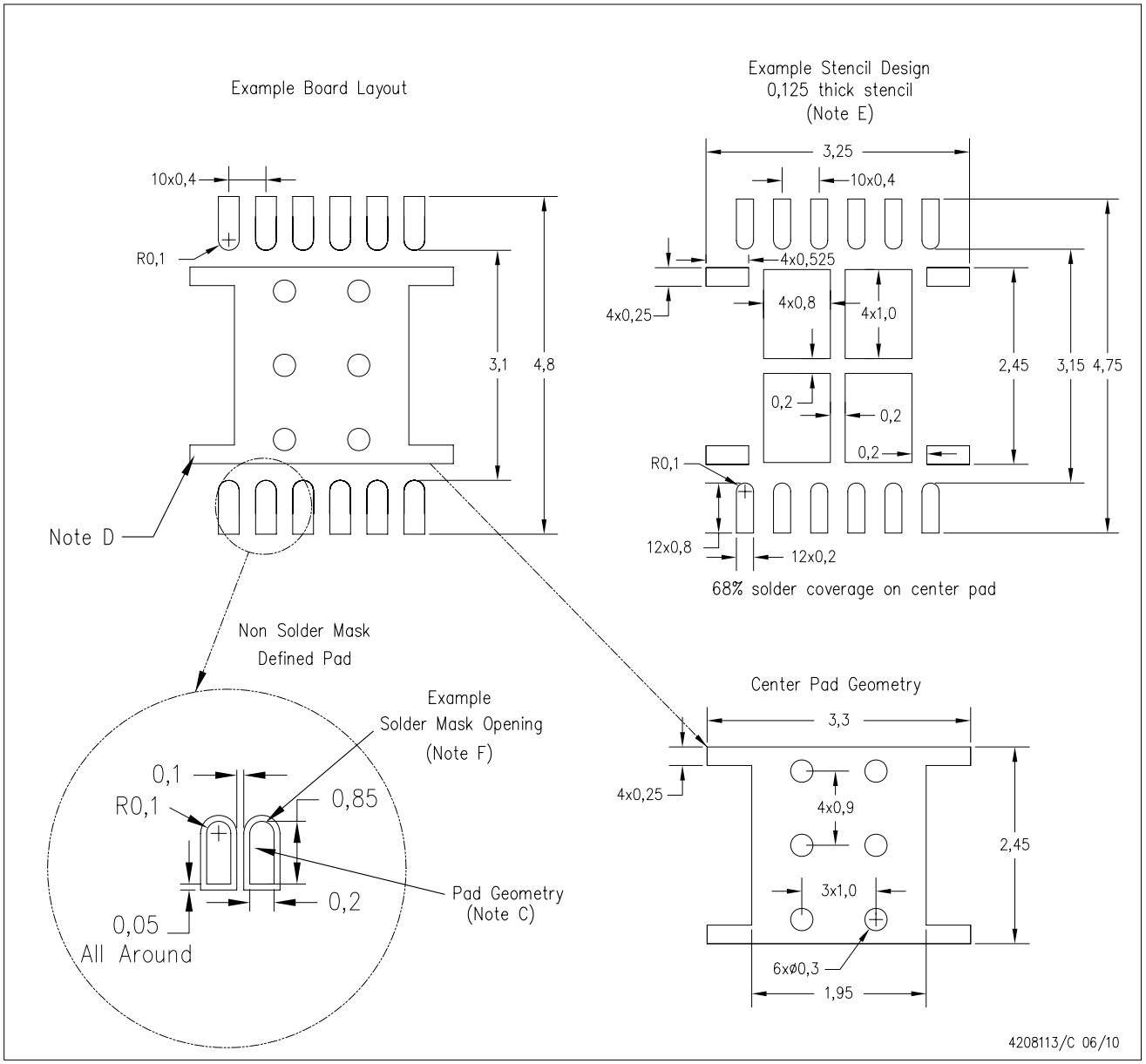


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRZ (S–PDSO–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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