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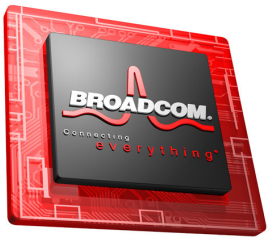
BCM8220 PRODUCT Brief



2.488/2.667 GBPS ULTRA LOW POWER SONET/SDH TRANSCEIVER

FEATURES

- OC-48/STM-16 SONET/SDH transceiver
- Selectable full-duplex transmission between standard rate of 2.488 Gbps or Forward Error Correction rate of 2.667 Gbps.
- Single-chip, integrated solution containing multiplexer (Mux), clock multiplication unit (CMU), demultiplexer (Demux), and clock data recovery (CDR) functions.
- 4-bit, 622.08/666.84-MHz, LVDS system interface
- Both line and system loopback modes
- Additional diagnostic features include lock detect and loss of signal.
- Meets SONET/SDH jitter requirements
- Low power dissipation of 550 mW typical
- Operates at 1.8V
- 1.8V or 3.3V CMOS I/O interface
- Standard CMOS fabrication process
- Two packages offered:
  - 100-pin QFP package, 14 mm ∞ 14 mm ∞ 1.4 mm
  - 100-pin BGA package, 11 mm ∞ 11 mm ∞ 1.71 mm

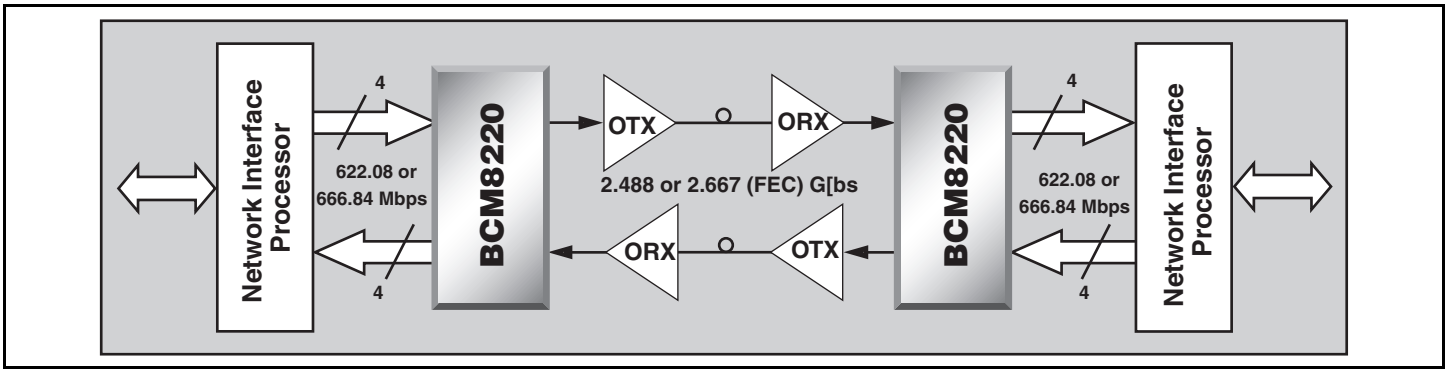
SUMMARY OF BENEFITS

- Ultra low power consumption eliminates external heat sinks, fans for system airflow, and expensive high current power supplies.
- High integration reduces design cycle and time to market.
- Features increased port density per board and system.
- Selectable standard OC-48/STM-16 rate of 2.488 Gbps or Forward Error Correction rate of 2.667 Gbps, allowing for easy system configuration to maximize transmission bandwidth and data availability.
- Extensive diagnostic features provide easy system troubleshooting.
- Compliant with industry standards to reduce design cycle and time to market.
- CMOS-based device takes advantage of the most effective silicon economy of scale.

APPLICATIONS

- OC-48/STM-16 transmission Equipment
- SONET/SDH optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbones
- Terabit and edge routers
- DWDM systems

BCM8220 Application Block Diagram



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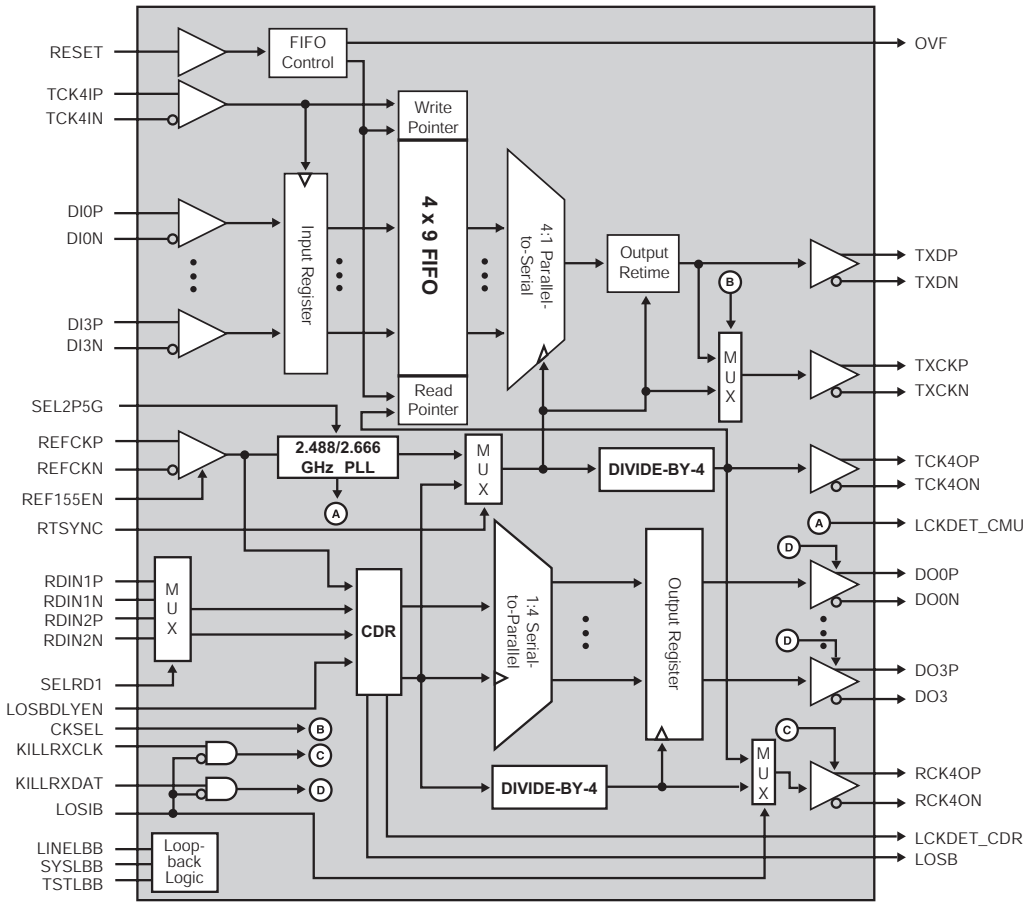
OVERVIEW



The BCM8220 FEC-capable (Forward Error Correction), SONET/SDH transceiver is a fully integrated, SONET OC-48 (2.488/2.667 Gbps) interface serialization/deserialization device with an integrated clock multiplication unit (CMU) and integrated clock and data recovery (CDR) circuit. Output frequency is selectable at 2.488 Gbps or 2.667 Gbps, allowing use of the FEC capability.

On-chip clock synthesis is performed by the high-frequency, low-jitter, phase-locked loop on the BCM8220 transceiver chip, allowing the use of slower 77.76/155.52-MHz (83.35/166.71-MHz) external transmit clock references.

Clock recovery is performed by synchronizing the on-chip VCO directly to the incoming data stream. The low-jitter, LVDS interface guarantees bit error compliance with the Telcordia GR-253-CORE, ANSI, and ITU-T standards. The BCM8220 is packaged in a 14 x 14 mm, 100-pin LQFP package or an 11 x 11 mm, 100-pin BGA package.

Transmitter functions include:

- 4-bit parallel input
- Elastic buffering
- 2.488/2.666 GHz clock generation
- Parallel-to-serial conversion
- Serial differential data output

Receiver functions include:

- 2.488/2.666 Gbps differential data input
- Clock and data recovery
- Serial-to-parallel conversion
- 4-bit parallel output

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BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

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Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com