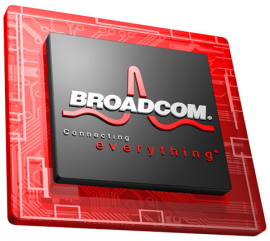
BROADCOM®
Connecting everything®

BCM8211
PRODUCT Brief



2.488 GBPS SONET/SDH TRANSCEIVER WITH INTERNAL LOOP TIMING

FEATURES

- 2.488-Gbps SONET/SDH transceiver with dual differential serial I/O
- Fully integrated CDR, MUX, DEMUX, and CMU
- Selectable LVPECL/CMOS 16-bit, 155.52-Mbps interface to framer or network processor
- On-chip PLL-based clock generator
- Line and system loopback modes
- Loss-of-signal output (LOSB) and input (LOSIB)
- TX and RX lock detect
- Elastic buffering with FIFO overflow alarm
- Selectable 77.76/155.52-MHz reference clock
- Selectable RX clock and RX data squelch on LOS
- Selectable loop timing mode
- Single 2.5V or dual 2.5V/3.3V supplies
- Power dissipation: 1.2W typical
- 14 ∞ 20 mm, 128-pin PQFP package
- Standard CMOS fabrication process

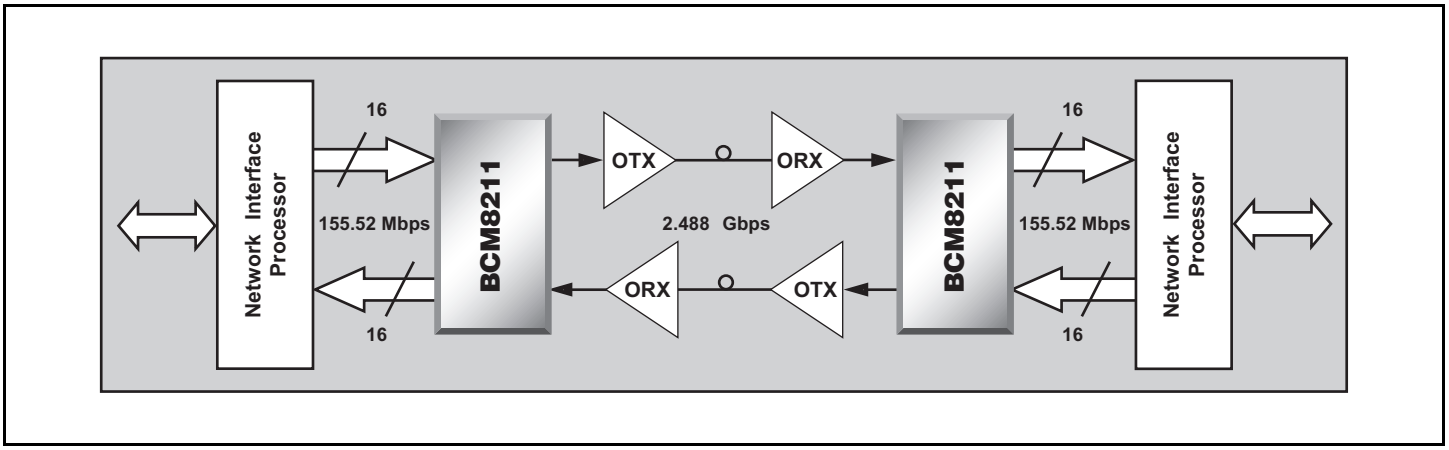
SUMMARY OF BENEFITS

- Low power consumption eliminates external heat sinks, fans for system airflow, and expensive high current power supplies.
- Supports SONET dual-fiber ring architecture.
- High integration reduces design cycle and time to market.
- Provides increased port density per board and system.
- CMOS-based device uses the most effective silicon economy of scale.
- Meets SONET jitter requirements.
- Features low jitter: 3 mUI_{rms} typical.

APPLICATIONS

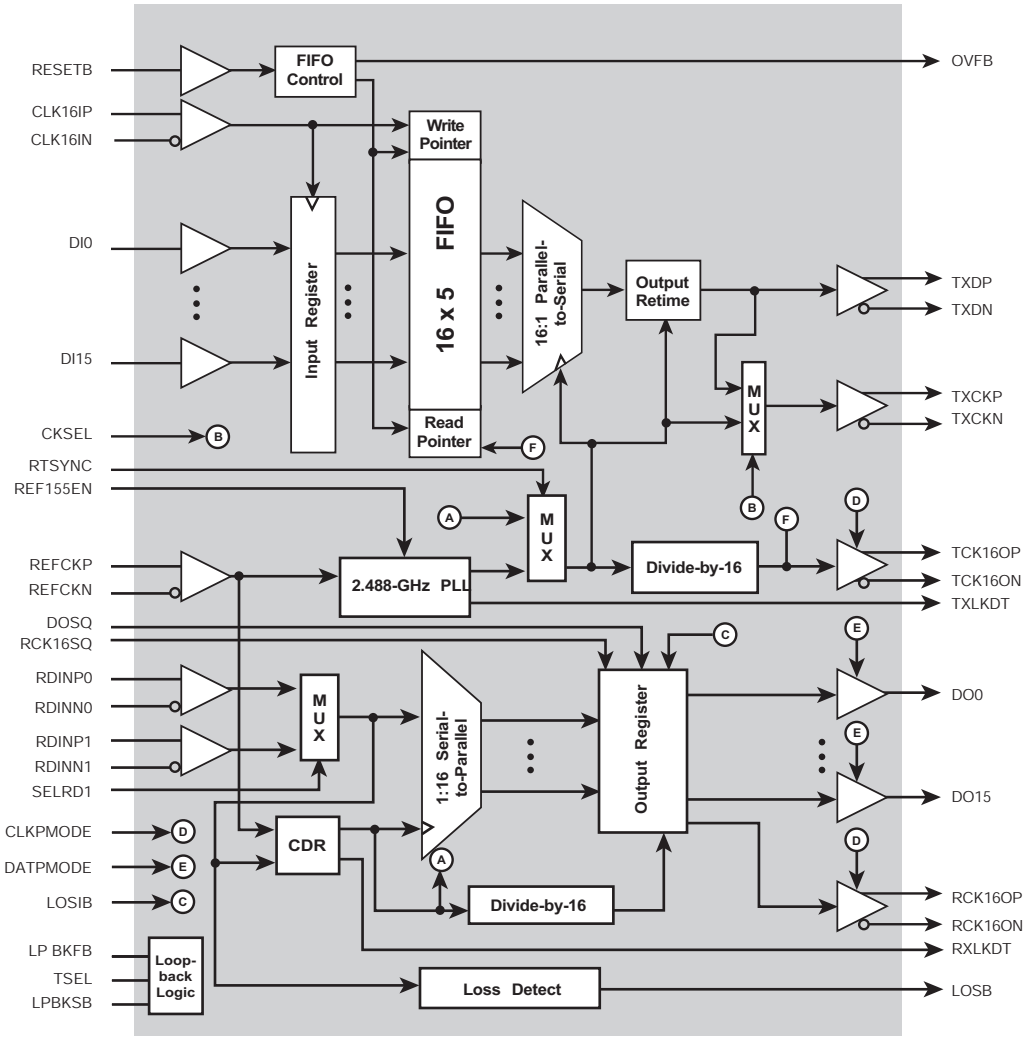
- OC-48/STM-16 transmission equipment
- SONET/SDH optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbone
- SONET/SDH test equipment
- Terabit and edge routers

BCM8211 Application Block Diagram



BROADCOM®

OVERVIEW



The BCM8211 SONET/SDH transceiver is a fully integrated serialization/deserialization SONET OC-48 and SDH STM-16 (2.488 Gbps) interface device with an integrated Clock Multiplication Unit (CMU) and an integrated Clock and Data Recovery (CDR) circuit. On-chip clock synthesis is performed by the high-frequency, low-jitter, phase-locked loop on the BCM8211 transceiver, allowing the use of a slower 77.76/155.52 MHz external transmit clock reference.

Dual RX and TX 2.488-Gbps interfaces support dual-fiber ring architectures. Clock recovery is performed on the device by synchronizing its on-chip VCO directly to the incoming data stream.

The low-jitter LVPECL/CMOS interface guarantees compliance with the bit error rate requirements of the Telcordia GR-253-CORE, ANSI, and ITU-T standards. The BCM8211 is packaged in a 14 x 20 mm, 128-pin PQFP.

The BCM8211 operates in either single 2.5V or dual 2.5/3.3V configuration. The core and CML I/O operate at 2.5V and the LVPECL I/O can operate at either 2.5V or 3.3V.

Connecting everything®

BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

8211-PB06-R 07/02/04

Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com