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BCM8152 PRODUCT Brief

10-GBPS TRANSCEIVER WITH 10G CLOCK, BUS SKEW, AND LIMITING AMPLIFIER

FEATURES

- 10-gigabit Multisource Agreement (MSA)/XFP-compatible
- Fully integrated multirate CDR, DEMUX, CMU, and MUX
- 1SFI-4 parallel interface (16-bit LVDS)
- 10-gigabit serial transmitter clock output
- Limiting amplifier
- On-chip PLL-based clock generator
- Line and system loopback modes
- Receiver and transmitter serial data polarity invert
- Bit order reversal
- Analog loss-of-signal output (ALOSB)
- Transmit and receive lock detect
- 10-word FIFO with overflow alarm absorbs system clock jitter
- Reference clock: 1/16 or 1/64 of the selectable data rate
- Selectable receive clock and receive data squelch
- Selectable loop timing mode
- Internal phase detector and charge pump for cleanup PLL; external VCXO required
- Input threshold offset adjustment and phase adjustment to optimize bit error rate and jitter tolerance margin
- Power supplies: core, LVPECL, LVDS output, CML at 1.8V, LVDS input, and CMOS I/O at 1.8 or 3.3V
- Power dissipation: 1.2W typical

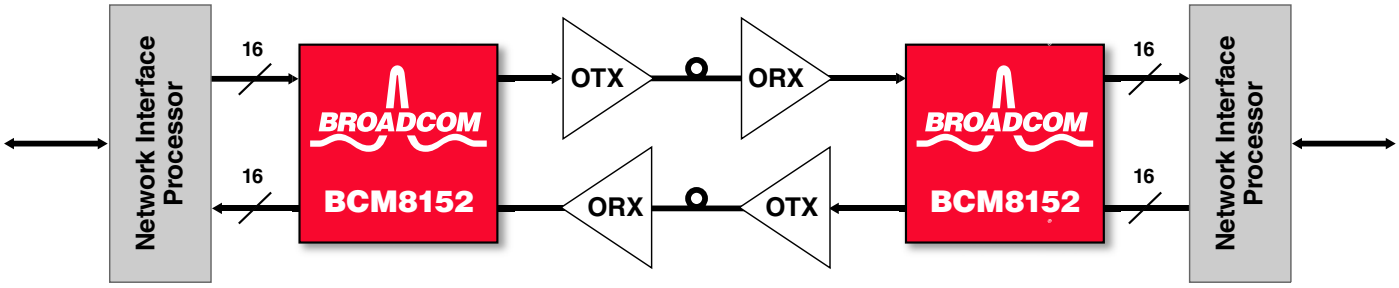
SUMMARY OF BENEFITS

- Provides compliance Optical Internetworking Forum (OIF), Telcordia®, ITU-T, and IEEE 802.3™ ae standards
- Reduces design cycle and time-to-market
- High level of integration allows for higher port density solutions
- Uses the most effective silicon economy of scale for CMOS-based devices
- Standard CMOS fabrication process

APPLICATIONS

- OC-192/STM-64/10-GbE/FEC transmission equipment
- SONET/SDH/10-GbE/10FC/FEC optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbone
- SONET/SDH/10-GbE/10FC/FEC test equipment
- Terabit and edge routers

Functional Block Diagram



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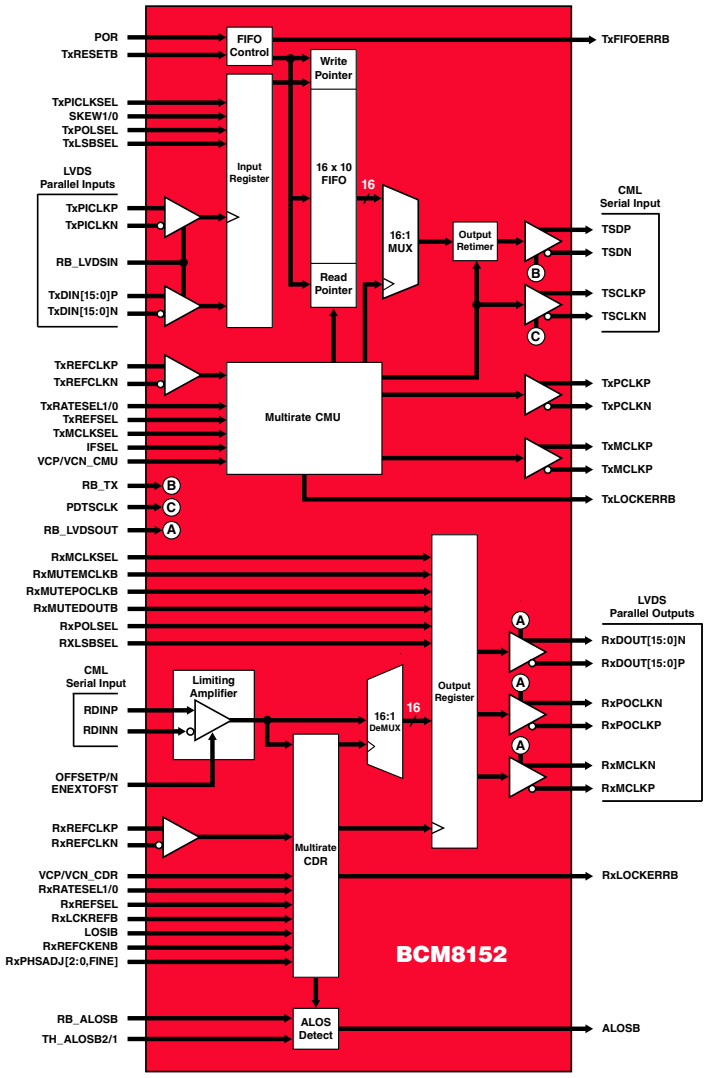

BCM8152 Block Diagram

On-chip clock synthesis is performed by the high-frequency, low-jitter phase locked loop (PLL) on the BCM8152 transceiver chip, allowing the use of a low-frequency reference clock selectable to the line rate divided by either 16 or 64.

Clock recovery is performed on the device by synchronizing its on-chip voltage-controlled oscillator (VCO) directly to the incoming data stream. An on-chip phase detector and charge pump plus external VCXO implements a cleanup PLL. The cleanup PLL can be used to clean up the CDR-recovered clock for loop timing applications or to clean up a noisy system clock.

The low-jitter LVDS interface guarantees compliance with the bit error rate requirements of the Telcordia, ANSI, ITU-T, and IEEE 802.3ae standards.

The BCM8152 is packaged in a 15 x 15-mm, 301-pin BGA, in either standard or Pb-free version.

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