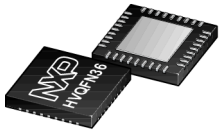


ASL5xxxyHz

Matrix LED Controller (MLC)

Rev. 2.1 — 5 February 2019 Product data sheet

1 General description

The ASL5xxxyHz family is a fully featured and flexible Matrix LED Controller (MLC). It provides a cost effective design solution, specifically targeting advanced automotive exterior lighting applications. The family consists of part numbers with different maximum currents and different driving modes, Smart and direct PWM.

Smart PWM part numbers determine PWM dimming duty cycle from information stored inside the MLC in the form of dimming polynomial curve coefficients. These coefficients are programmable by the customer according to the dimming profile they would like to see. The MLC uses these polynomial coefficients to calculate the PWM duty cycle to 12-bit resolution. The MLC also provides the capability to increase the speed of the PWM dimming curve dynamically or sequence several PWM dimming curves together.

It is possible to store polynomials for up to eight PWM dimming curves. By storing these polynomial coefficients internally, it is not necessary for the microcontroller to send updated PWM dimming information to each LED switch continuously. Instead, the microcontroller selects the PWM curve and LED to which it must be applied. Therefore, the PWM dimming information from the microcontroller is reduced, which reduces the volume of data transfer from the microcontroller to the MLC.

The MLC also provides the functionality to correct for LED brightness variations. This feature is especially useful to ensure a homogenous light output from LEDs that have luminance variations with the same LED current.

The MLC has many diagnostic features, including:

- Direct NTC feedback for monitoring the LED temperature
- Direct identification resistor input for PCB characterization
- Single LED open/short detection and protection
- Internal IC junction temperature monitoring
- Power-on-Reset (POR) monitoring; mandatory for off-board configuration and following safety requirements
- Power OK bit (POK) to ensure that the complete MLC is working as expected
- External components (NTC, ID resistor, charge pump capacitor) monitoring and fail detection
- Full communication diagnosis, including flagging illegal actions
- Possibility to clear Open Circuit (OC) and Short Circuit (SC) flags and reset the internal mosfets dynamically and without a need of a power-on-reset

All this diagnostic information is available to the microcontroller via the MLC interface. A microcontroller controls the MLC through a high-speed serial CAN interface. Through this interface, the microcontroller can control up to 32 MLCs, enabling control of up to 384 LEDs or segments.

The MLC has an internal 200 MHz oscillator that avoids the need of an external quartz (reducing system cost and providing better EMC behavior) for synchronization and clock

generation. All the internal clocks are synchronized with the internal oscillator and the trimming is done via the CAN message (CAN-ID). This process allows for a very accurate clock (accuracy < 0.25 %).

The MLC can be mounted close to the LEDs on an IMS PCB. Because the pinning has been optimized to avoid any crossing tracks, a single-layer PCB can be used. The ASL5xxxyHz family is available in automotive-qualified, thermally enhanced, 36-pin HVQFN and 48-pin HLQFP packages.

The device is designed to meet the stringent requirements of automotive applications, being fully AEC Q100 grade 1 and AEC Q006 qualified. It operates over the –40 °C to +125 °C ambient temperature range.

The Matrix LED Controller (MLC) also offers the possibility to be driven in direct PWM mode. In this mode, the microcontroller needs to update the PWM value in every channel with a certain cycle, determined by the system specifications. These part numbers, ASL5115yHz and ASL5108yHz, also offer 12-bit resolution to ensure a smooth dimming performance to avoid glitches in the output light.

The MLC family also offers two different maximum currents per switch. Part numbers ASL5008yHz and ASL5108yHz offer a maximum current per switch of 0.8 A. Part numbers ASL5015yHz and ASL5115yHz offer a maximum current per switch of 1.5 A.

All part numbers are pin-to-pin compatible, which offers a completely scalable and flexible system solution that can be adapted to any system requirements.

2 Features

- Automotive grade product that is AEC-Q100 grade 1 and AEC-Q006 qualified
- Operating ambient temperature range of –40 °C to +125 °C
- Maximum junction temperature of 175 °C
- Operating input voltage 5 V ± 0.5 V. Vcc pin.
- Able to drive up to 12 LEDs / segments, with a string voltage range up to 57 V
- Able to drive multiple LEDs per switch (MTP configurable)
- 12 channels, arranged in 4 configurable blocks of 3 switches per block
- Each block of three can fully float up to 60 V with respect to ground and can be paralleled with any other block
- Each switch can control up to 1.5 A LED current in the ASL5x15yHz family and up to 0.8 A in the ASL5x08yHz family
- 100 mΩ (Rdson) switches for 1.5 A part numbers and 200 mΩ for 0.8 A part numbers
- PWM dimming with 12-bit resolution and built-in phase shifting for minimum losses
- Internal PWM duty cycle generator with incremental calculation for glitch-free operation in the ASL50xxyHz family—Smart
- On-chip storage of preprogrammed PWM curves to reduce data traffic in ASL50xxyHz family—Smart
- LED brightness variation correction functionality
- On-chip 200 MHz oscillator, avoiding need for external quartz
- CAN-based serial interface with optional external CAN physical layer
- Broadcast messages to reduce system latency and bus load
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Individual LED open and LED short-fault monitoring, with bypass feature on open condition
- NTC input with 6-bit resolution for LED temperature monitoring; directly connected to MLC
- Identification resistor input
- MLC can be used in a configuration of up to 32 ICs in a single CAN network
- Small package outline, leadless HVQFN package with improved Automated Optical Inspection (AOI) capability and leaded HLQFP package
- Low operational current consumption
- Sleep and wake-up modes available
- Standby current consumption < 1.35 mA
- Input under voltage protection
- 9-bit resolution IC junction temperature feedback via CAN interface
- Internally programmed Limp Home Mode (LHM) in case of communication failure
- Built-in charge pump failure operation mode (CPFSO)

3 Applications

- Automotive lighting
  - Matrix/pixel high beam (ADB / Glare-Free High Beam - GFHB)
  - Matrix/pixel low beam (ADB)
  - Dynamic turning indicator
  - Welcoming scenarios
  - Dynamic rear lights

– Dynamic cornering lights

4 Orderable parts

Table 1. Orderable part variations

Type number	Package		
	Name	Description	Version
ASL5015SHN	HVQFN36	Smart internal PWM generator with prestored curves (Smart – 1.5 A) – CAN	SOT1092-4
ASL5115SHN	HVQFN36	Direct PWM data for every channel (Direct – 1.5 A) – CAN	SOT1092-4
ASL5008SHN	HVQFN36	Smart internal PWM generator with prestored curves (Smart – 0.8 A) – CAN	SOT1092-4
ASL5108SHN	HVQFN36	Direct PWM data for every channel (Direct – 0.8 A) – CAN	SOT1092-4
ASL5015FHN	HVQFN36	Smart internal PWM generator with prestored curves (Smart – 1.5 A) – CAN-FD	SOT1092-4
ASL5115FHN	HVQFN36	Direct PWM data for every channel (Direct – 1.5 A) – CAN-FD	SOT1092-4
ASL5008FHN	HVQFN36	Smart internal PWM generator with prestored curves (Smart – 0.8 A) – CAN-FD	SOT1092-4
ASL5108FHN	HVQFN36	Direct PWM data for every channel (Direct – 0.8 A) – CAN-FD	SOT1092-4
ASL5015SHV	HLQFP48	Smart internal PWM generator with prestored curves (Smart – 1.5 A) – CAN	SOT1571-1
ASL5115SHV	HLQFP48	Direct PWM data for every channel (Direct – 1.5 A) – CAN	SOT1571-1
ASL5008SHV	HLQFP48	Smart internal PWM generator with prestored curves (Smart – 0.8 A) – CAN	SOT1571-1
ASL5108SHV	HLQFP48	Direct PWM data for every channel (Direct – 0.8 A) – CAN	SOT1571-1
ASL5015FHV	HLQFP48	Smart internal PWM generator with prestored curves (Smart – 1.5 A) – CAN-FD	SOT1571-1
ASL5115FHV	HLQFP48	Direct PWM data for every channel (Direct – 1.5 A) – CAN-FD	SOT1571-1
ASL5008FHV	HLQFP48	Smart internal PWM generator with prestored curves (Smart – 0.8 A) – CAN-FD	SOT1571-1
ASL5108FHV	HLQFP48	Direct PWM data for every channel (Direct – 0.8 A) – CAN-FD	SOT1571-1

5 Application diagram

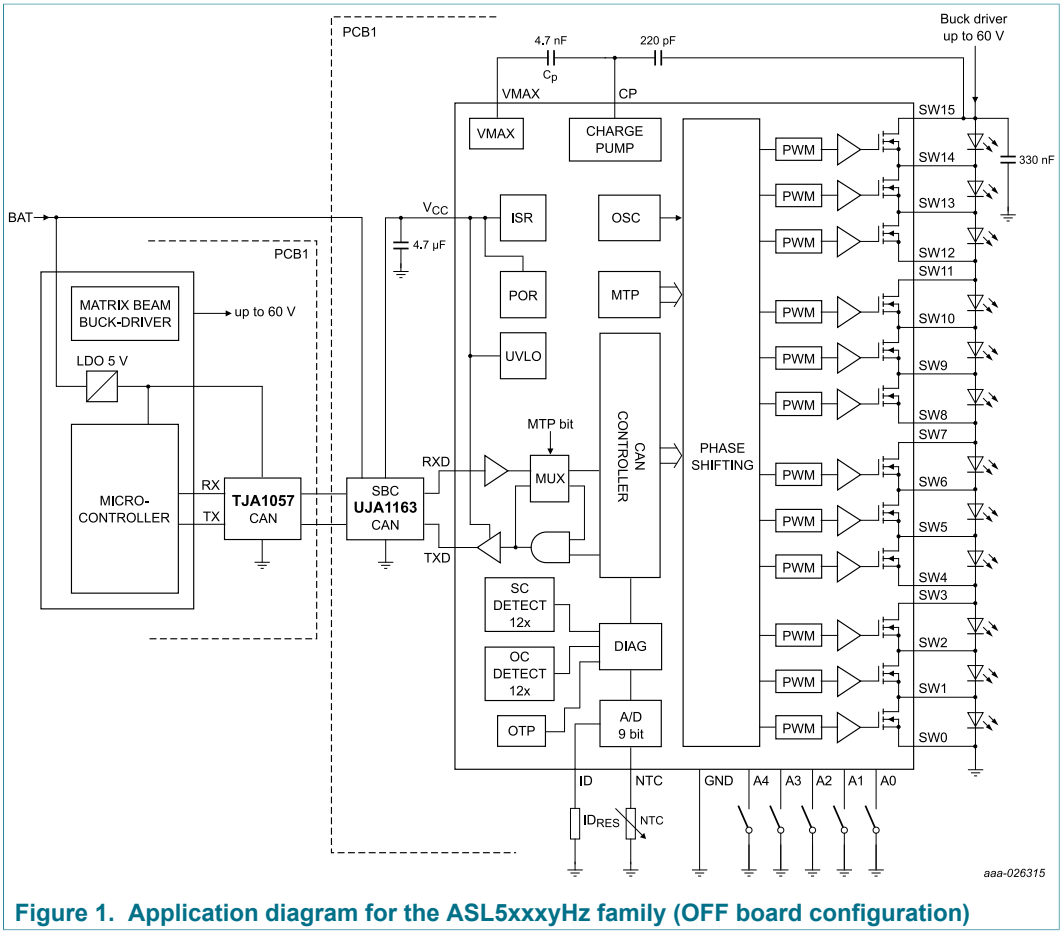


Figure 1. Application diagram for the ASL5xxxyHz family (OFF board configuration)

6 Block diagram

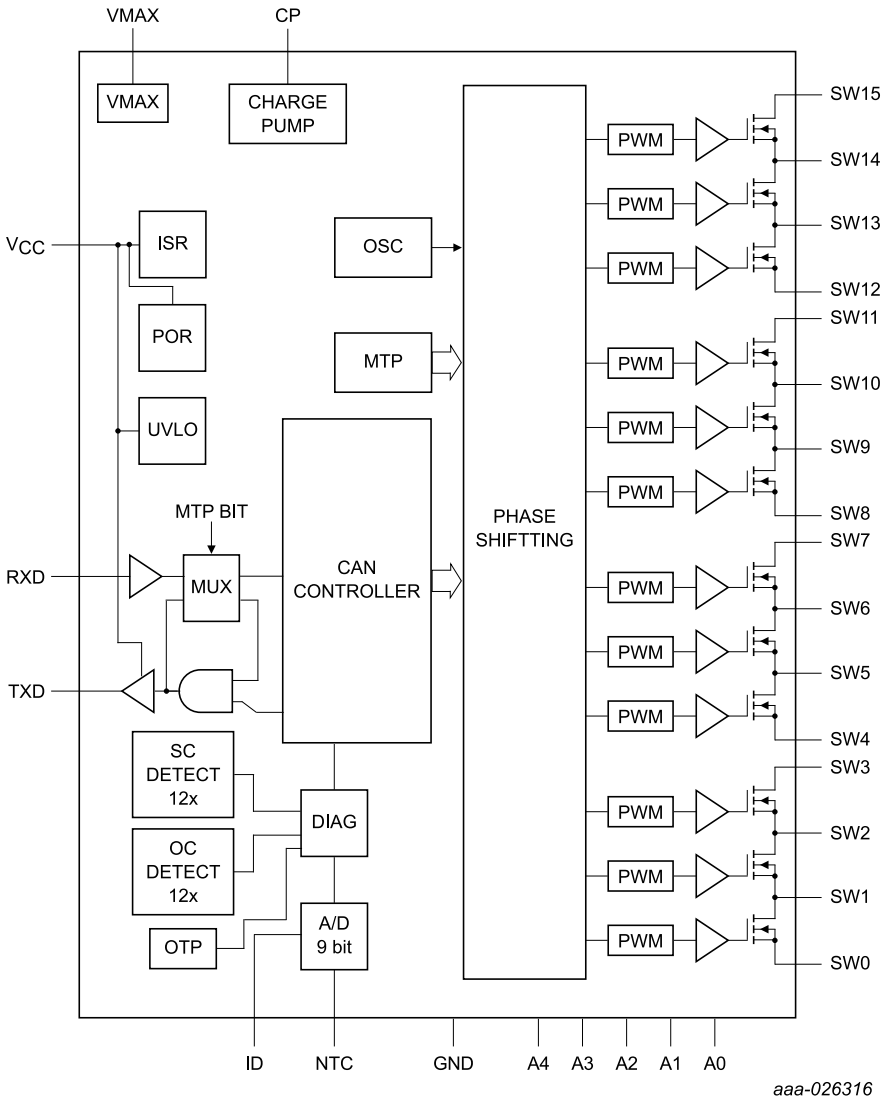


Figure 2. Block diagram

7 Pinning information

7.1 Pinning – HVQFN36 package

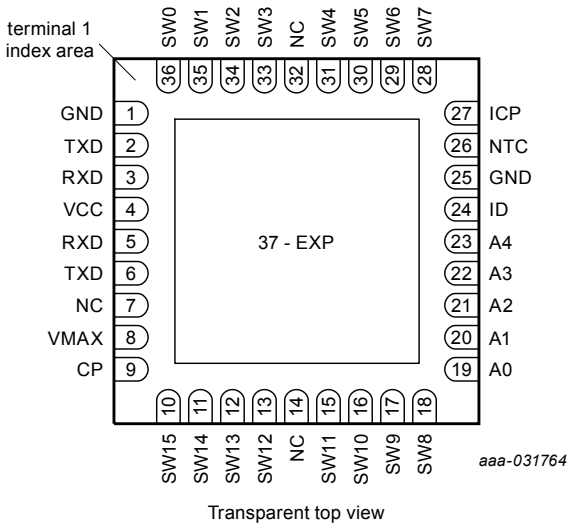


Figure 3. Pin configuration for HVQFN36

7.2 Pin description – HVQFN36 package

Table 2. Pin description

Symbol	Pin	Description
GND	1	Ground
TXD	2	Bus data OUT
RXD	3	Bus data IN
V_{CC}	4	External supply (5 V)
RXD	5	Bus data IN (Internally connected with pin 3)
TXD	6	Bus data OUT (Internally connected with pin 2)
NC	7	Not connected
VMAX	8	Voltage reference for the charge pump
CP	9	External charge pump input
SW15	10	Drain of switch 12
SW14	11	Source of switch 12 and drain of switch 11
SW13	12	Source of switch 11 and drain of switch 10
SW12	13	Source of switch 10
NC	14	Not Connected
SW11	15	Drain of switch 9
SW10	16	Source of switch 9 and drain of switch 8
SW9	17	Source of switch 8 and drain of switch 7
SW8	18	Source of switch 7

Symbol	Pin	Description
A0	19	Address bit 0
A1	20	Address bit 1
A2	21	Address bit 2
A3	22	Address bit 3
A4	23	Address bit 4
ID	24	Connection for the identification resistor
GND	25	Ground
NTC	26	Connection to the NTC
Internally connected	27	ICP (Internally Connected Pin) – Connect to ground
SW7	28	Drain of switch 6
SW6	29	Source of switch 6 and drain of switch 5
SW5	30	Source of switch 5 and drain of switch 4
SW4	31	Source of switch 4
NC	32	Not Connected
SW3	33	Drain of switch 3
SW2	34	Source of switch 3 and drain of switch 2
SW1	35	Source of switch 2 and drain of switch 1
SW0	36	Source of switch 1
EXP	37	Exposed pad – Connect it to ground

NC pins are inserted between two blocks of switches to prevent high voltages between two adjacent pins. An NC pin is also inserted between VMAX and TXD pins. NC pins must float.

The exposed center pad of the package is internally connected to ground. For enhanced thermal and electrical performance, it is highly recommended to connect the exposed center pad the the board's ground.

Both RXD pins and both TXD pins are internally connected to facilitate single-layer PCB layout without jumpers.

7.3 Pinning – HLQFP48 package

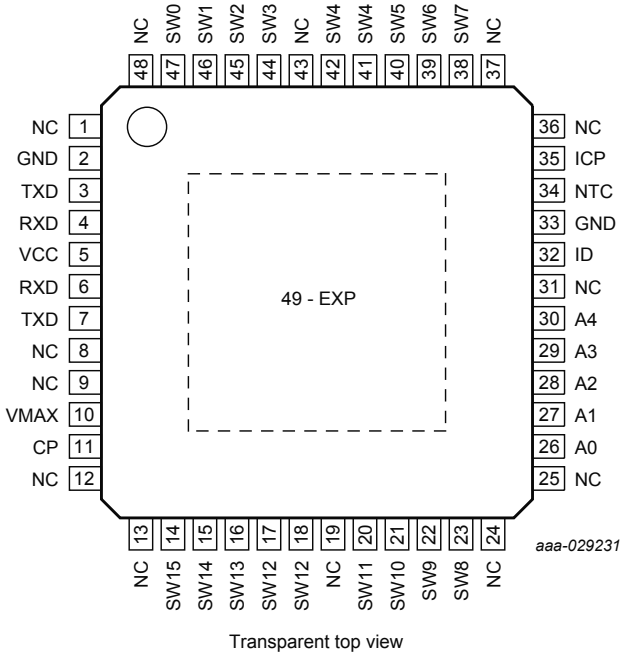


Figure 4. Pin configuration for LQFP48

7.4 Pin description – HLQFP48 package

Table 3. Pin description

Symbol	Pin	Description
NC	1	Not connected
GND	2	Ground
TXD	3	Bus data OUT
RXD	4	Bus data IN
VCC	5	External supply ±10 % (5 V)
RXD	6	Bus data IN
TXD	7	Bus data OUT
NC	8	Not connected (can be used for ground routing)
NC	9	Not connected
VMAX	10	Max. voltage reference for the charge pump
CP	11	External charge pump input
NC	12	Not connected
NC	13	Not connected
SW15	14	Drain of switch 12
SW14	15	Source of switch 12 and drain of switch 11
SW13	16	Source of switch 11 and drain of switch 10
SW12	17	Source of switch 10

Symbol	Pin	Description
SW12	18	Source of switch 10
NC	19	Not connected
SW11	20	Drain of switch 9
SW10	21	Source of switch 9 and drain of switch 8
SW9	22	Source of switch 8 and drain of switch 7
SW8	23	Source of switch 7
NC	24	Not connected
NC	25	Not connected
A0	26	Address bit 0
A1	27	Address bit 1
A2	28	Address bit 2
A3	29	Address bit 3
A4	30	Address bit 4
NC	31	Not connected
BIN	32	Connection for the identification resistor
GND	33	Ground
NTC	34	Connection to the NTC
ICP	35	ICP (Internally Connected Pin) – Connect it to ground
NC	36	Not connected
NC	37	Not connected
SW7	38	Drain of switch 6
SW6	39	Source of switch 6 and Drain of switch 5
SW5	40	Source of switch 5 and Drain of switch 4
SW4	41	Source of switch 4
SW4	42	Source of switch 4
NC	43	Not connected
SW3	44	Drain of switch 3
SW2	45	Source of switch 3 and Drain of switch 2
SW1	46	Source of switch 2 and Drain of switch 1
SW0	47	Source of switch 1
NC	48	Not connected
EXP	49	Exposed pad - Connect it to ground

NC pins are inserted between two blocks of switches to prevent high voltages between two adjacent pins. Two NC pins are also inserted between VMAX and TXD pins. The NC pins must float, only pin 8 can be used for ground routing, since pin 9 (NC) still keep the isolation between ground and high voltage.

The exposed center pad must be connected to ground during layout routing.

Both RXD pins and both TXD pins are internally connected to facilitate single-layer PCB layout without jumpers.

8 Functional description

8.1 Integrated switches for single or multiple LEDs dimming

The floating blocks make it possible for the ASL5xxxyHz family (Matrix LED Controller, MLC) to drive 12 single LEDs or multiple LEDs per switch and multiple strings with different currents and string voltages. The 12 independent switches are separated in 4 floating blocks of 3 switches each. Every block can float at 60 V with respect to ground and can be driven separately or as a unique system.

Figure 5 and Figure 6 show possible configurations.

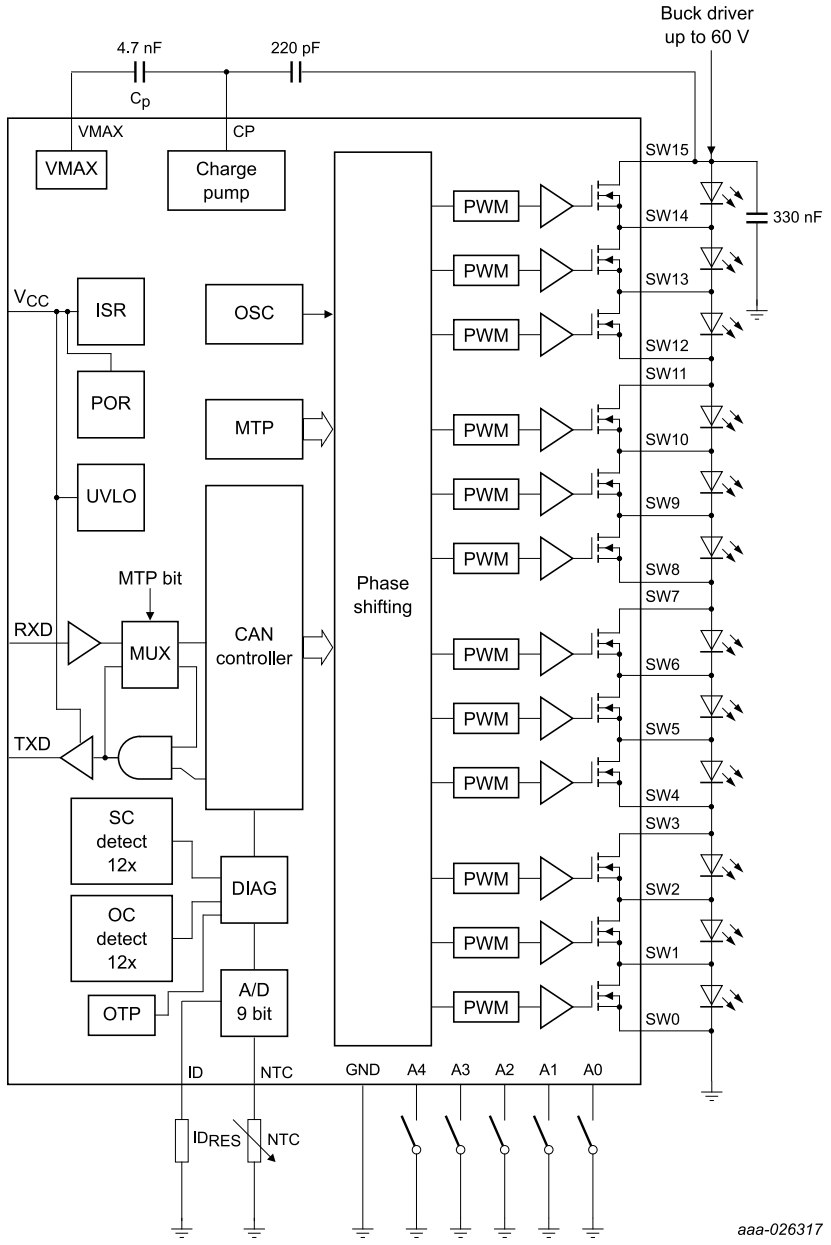


Figure 5. Single LED driving configuration application diagram

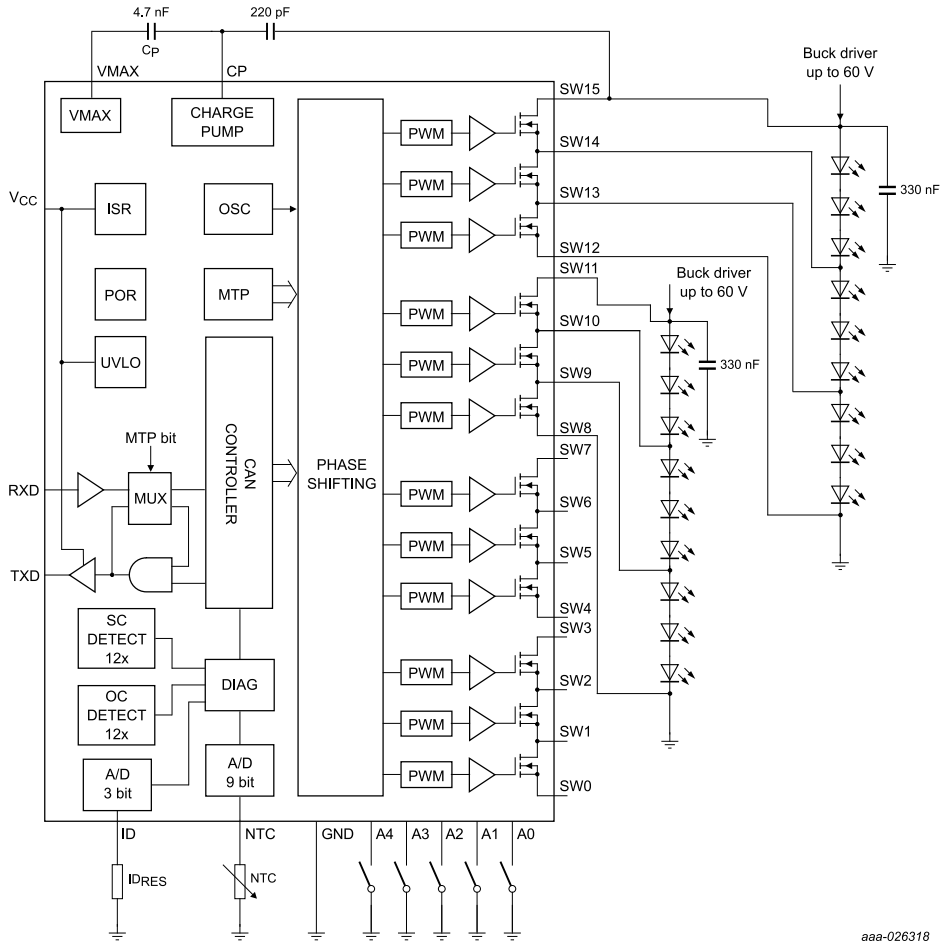


Figure 6. Multiple strings with segment driving configuration application diagram

Polarity must be respected in the internal MOSFET.

8.2 LED current capability and power dissipation

The LED string current is provided by a separate buck or boost converter. The specifications of the matrix controller are matched to the multichannel buck converter ASLx41xSHN. The MLC can also be driven by other buck driver or constant current suppliers. One buck converter output supplies the current for one LED string. For the MLC, the maximum LED string voltage is 57 V, maximum LED string current is 1.5 A in serial configuration, and up to 6 A in parallel configuration for ASL5x15yHzpart numbers. For part numbers ASL5x08yHz, the maximum LED string current is 0.8 A, in serial configuration, and up to 3.2 A when paralleling all switches' blocks.

The internal power dissipation depends on the number of LEDs that are bypassed. The maximum dissipation in the Matrix LED Controller occurs when all switches are closed with 1.5 A LED current through them, the dissipation is estimated to be 5 W at 120 °C junction temperature.

8.3 Internal PWM dimming generator and phase shifting

The ASL5015yHz and ASL5008yHz part numbers have an internal PWM generator module for each channel. The PWM has 12-bit resolution, which means a time accuracy

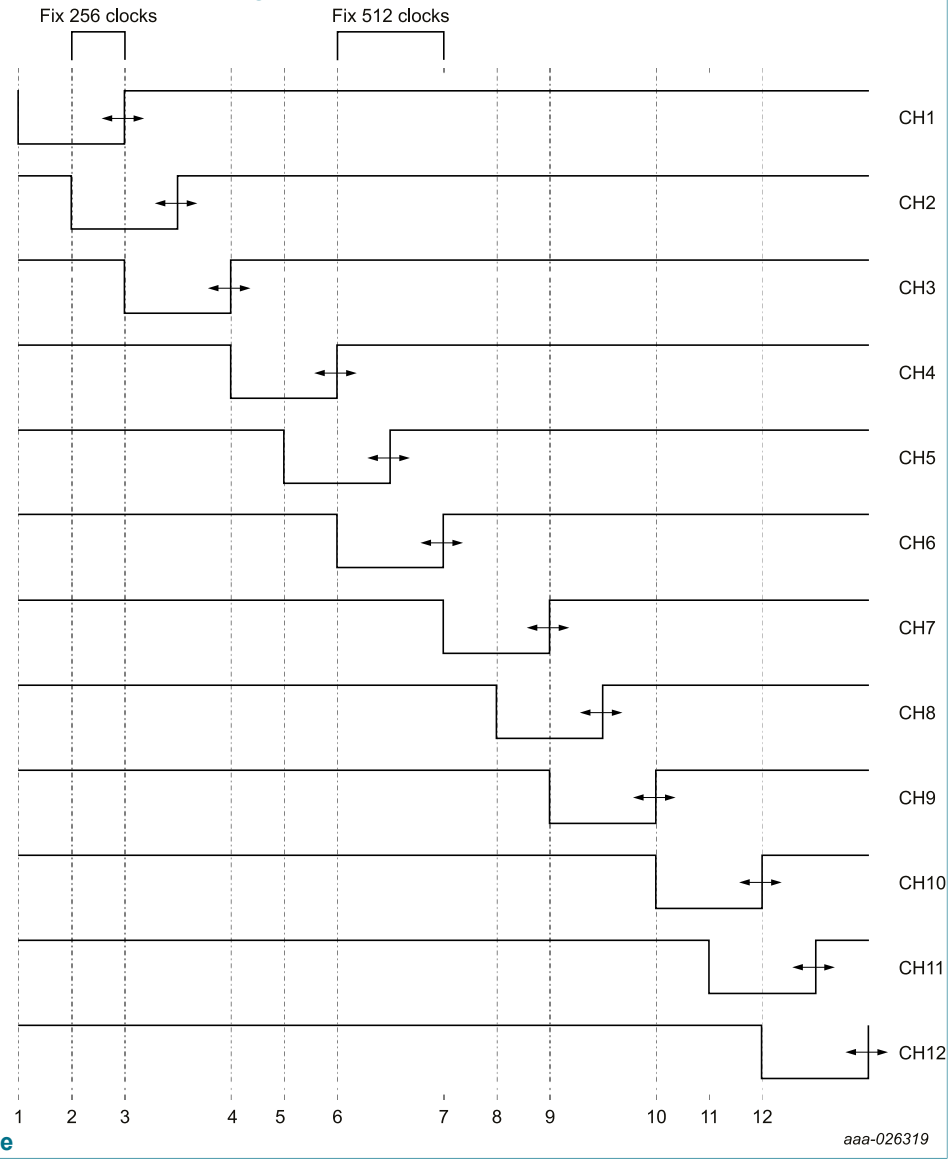
of 4.1 ms/4096 = 1 µs , at 244 Hz or 0.5 µs, at 488 Hz. The resolution in terms of PWM percentage is 0.024 %. This resolution ensures very smooth LED dimming to very low light levels.

When a PWM switch turns on, the forward voltage of the whole string decreases with the V_f of one LED. During the negative slope, there could be a high discharge current from the string capacitor that also flows through the entire LED string. If more than one LED is bypassed at the same time, then this injected current is higher when additional LEDs are bypassed. Therefore, it is desired to close only one switch at a time. For that reason, the MLC incorporates an internal phase-shifting module that ensures closing switches one at a time.

Note: Automated phase shifting feature is applicable to all Matrix LED controllers part numbers.

Figure 7 shows a phase-shifting example in an MLC IC, during just one PWM cycle.

Figure 7. Built in phase shifting sequence



Each block of switches can be assigned to a block of channels and phases; each block can be paralleled with any other block. For paralleling switches, it is necessary that they turn on at the same instant and use the same PWM information.

The shiting between two consecutuve switches of the same block is 256 clocks. The shifting between two consecutive switches of different blocks is 512 clocks.

Two bits per block are required in the MTP to define which group of channels are assigned to a phase sequence. In Figure 8, there is an example of all blocks assigned to different phase shifting sequences.

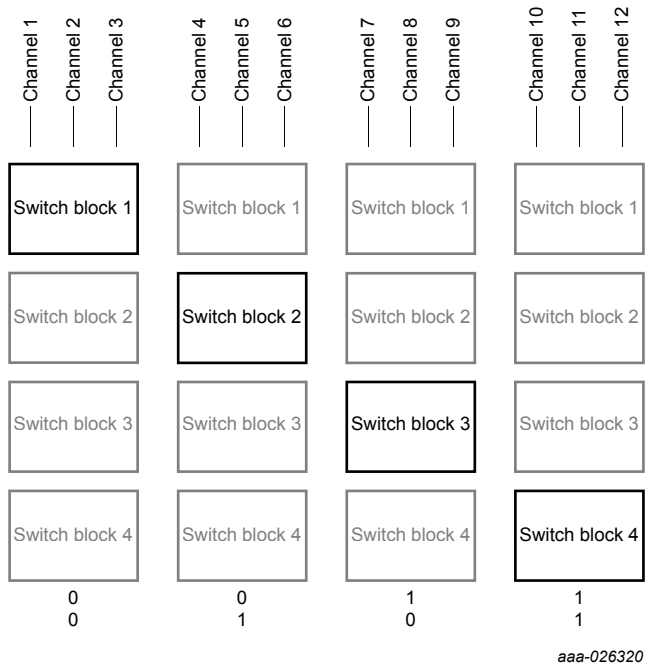


Figure 8. Blocks of switches can be assigned to phase shifting sequences

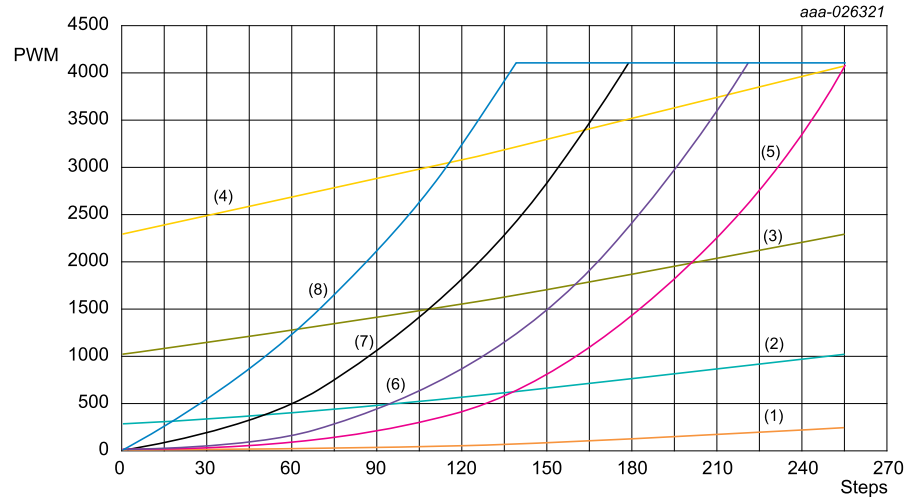
The MTP configuration bits (2 bits) are showed in the bottom side of the blocks. Depending on the selected configuration, a different block may be highlighted in the graph. These two bits are used to select the phase shifting sequence of the associated channels/switches. When blocks are in series, the two bits should be different in each block. For parallel configuration, the blocks that work together should have the same phase shifting sequence (same 2 bits value).

This way of defining the PWM periods guarantees that two or more switches are never closed at the same moment, unless they are in parallel. It makes programming easier and reduces the voltage ripple on the LED string.

The sequence for each individual block can be programmed in the MTP. See Section 14 "Nonvolatile Multitime Programmable Memory (MTP)".

8.4 Programming and execution of PWM dimming – ASL50xxyHz

In order to reduce data traffic over the serial interface, a polynomial curve defines the PWM dimming profile. Coefficients for the PWM dimming polynomial curves can be stored in an internal nonvolatile MTP (Multiple Time Programmable) memory. This programming is done once at the end of the customer production line.



(1) Curve_1_Fade_in/out
(2) Curve_2_Fade_in/out
(3) Curve_3_Fade_in/out
(4) Curve_4_Fade_in/out
(5) Curve_5_Fade_in/out
(6) Curve_6_Fade_in/out
(7) Curve_7_Fade_in/out
(8) Curve_8_Fade_in/out

Figure 9. Example PWM Polynomial curves (Default curves in MTP)

The equation to determine the curve is up to a third-grade polynomial:

$Ax^3 + Bx^2 + Cx + D$

The system makes an absolute calculation with the first x (step) value and then uses an incremental calculation to ensure no glitch between consecutive PWM Duty Cycle values, even when the shift value is changed to modify the curve speed. Absolute calculation is applied only when START command is used, for NOW or AUTO bits, the incremental calculation is used.

Note: *A system emulation tool is available and can reproduce any possible scenario.*

The implementation of a differential calculation ensures a glitch-free system. This method allows a very smooth LED dimming without any undesirable light glitch.

The information to be stored in the MTP are only the polynomial coefficient values A, B, C and D. Then, the system calculates the resulting PWM duty cycle on the fly with an internal PWM generator (in the Smart version, ASL50xxyHz).

Several curves can be sequenced in case of long fade-in or fade-out scenarios. This feature is only available in the Smart versions, ASL50xxyHz.

The ASL5015yHz and ASL5008yHz allow the storage of eight-polynomial curves. The curves can be followed in both directions, depending on whether the stop position is greater or lower than the start position; and the number of fade-in scenarios do not have to be the same as the fade-out ones.

It may be necessary to speed up or slow down a curve or interrupt a fade-in curve to set the PWM duty cycle to 100 % immediately, such as in the case of high-beam flashing. This adjustment is possible by changing the shift value.

The programmed coefficients in the internal MTP can also be negative, for that reason there are 13 bits reserved per coefficient. That gives the possibility to make smoother curves and shapes that are not possible with just positive coefficients. The available

simulation tool supports both signed coefficients and shows the system behavior in any possible condition.

8.4.1 Channel programming registers map

Table 4. Curve selection, auto-bit, shift value, start/stop positions and delay factor (Read/Write)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	CURVID1	SHIFT1[2:0]			AUTO1	NOW1	CURVEID1[2:0]			00000000
01h	STARTPOS1	STARTPOS1[7:0]								00000000
02h	STOPPOS1	STOPPOS1[7:0]								11111111
03h	DELAY1	DELAY1[7:0]								00000000
04h	CURVID2	SHIFT2[2:0]			AUTO2	NOW2	CURVEID2[2:0]			00000000
05h	STARTPOS2	STARTPOS2[7:0]								00000000
06h	STOPPOS2	STOPPOS2[7:0]								11111111
07h	DELAY2	DELAY2[7:0]								00000000
08h	CURVID3	SHIFT3[2:0]			AUTO3	NOW3	CURVEID3[2:0]			00000000
09h	STARTPOS3	STARTPOS3[7:0]								00000000
0Ah	STOPPOS3	STOPPOS3[7:0]								11111111
0Bh	DELAY3	DELAY3[7:0]								00000000
0Ch	CURVID4	SHIFT4[2:0]			AUTO4	NOW4	CURVEID4[2:0]			00000000
0Dh	STARTPOS4	STARTPOS4[7:0]								00000000
0Eh	STOPPOS4	STOPPOS4[7:0]								11111111
0Fh	DELAY4	DELAY4[7:0]								00000000
10h	CURVID5	SHIFT5[2:0]			AUTO5	NOW5	CURVEID5[2:0]			00000000
11h	STARTPOS5	STARTPOS5[7:0]								00000000
12h	STOPPOS5	STOPPOS5[7:0]								11111111
13h	DELAY5	DELAY5[7:0]								00000000
14h	CURVID6	SHIFT6[2:0]			AUTO6	NOW6	CURVEID6[2:0]			00000000
15h	STARTPOS6	STARTPOS6[7:0]								00000000
16h	STOPPOS6	STOPPOS6[7:0]								11111111
17h	DELAY6	DELAY6[7:0]								00000000
18h	CURVID7	SHIFT7[2:0]			AUTO7	NOW7	CURVEID7[2:0]			00000000
19h	STARTPOS7	STARTPOS7[7:0]								00000000
1Ah	STOPPOS7	STOPPOS7[7:0]								11111111
1Bh	DELAY7	DELAY7[7:0]								00000000
1Ch	CURVID8	SHIFT8[2:0]			AUTO8	NOW8	CURVEID8[2:0]			00000000
1Dh	STARTPOS8	STARTPOS8[7:0]								00000000
1Eh	STOPPOS8	STOPPOS8[7:0]								11111111
1Fh	DELAY8	DELAY8[7:0]								00000000
20h	CURVID9	SHIFT9[2:0]			AUTO9	NOW9	CURVEID9[2:0]			00000000

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0	Default
21h	STARTPOS9	STARTPOS9[7:0]								00000000
22h	STOPPOS9	STOPPOS9[7:0]								11111111
23h	DELAY9	DELAY9[7:0]								00000000
24h	CURVID10	SHIFT10[2:0]			AUTO10	NOW10	CURVEID10[2:0]			00000000
25h	STARTPOS10	STARTPOS10[7:0]								00000000
26h	STOPPOS10	STOPPOS10[7:0]								11111111
27h	DELAY10	DELAY10[7:0]								00000000
28h	CURVID11	SHIFT11[2:0]			AUTO11	NOW11	CURVEID11[2:0]			00000000
29h	STARTPOS11	STARTPOS11[7:0]								00000000
2Ah	STOPPOS11	STOPPOS11[7:0]								11111111
2Bh	DELAY11	DELAY11[7:0]								00000000
2Ch	CURVID12	SHIFT12[2:0]			AUTO12	NOW12	CURVEID12[2:0]			00000000
2Dh	STARTPOS12	STARTPOS12[7:0]								00000000
2Eh	STOPPOS12	STOPPOS12[7:0]								11111111
2Fh	DELAY12	DELAY12[7:0]								00000000

SHIFTx: These three bits determine the shift value used in the internal PWM generator. The speed of the curve depends on the shift value. When the lowest shift value is selected (2), the fastest curve is performed. Table 5 shows the different possible values.

Table 5. SHIFT values

SHIFT[2:0]	111	110	101	100	011	010	001	000
Value	2	4	8	16	32	64	128	256

AUTOx: Set this bit to 1 when the channel is already following another curve, so that this new configuration can be followed at the end of the current sequence.

NOWx: To implement changes immediately, set this bit to 1. The system will implement the new SHIFT, AUTO and CURVEID to the specific channel/switch immediately and automatically proceed with the PWM calculation. If this bit is set to 0, then all the other values (SHIFT, AUTO and CURVEID) are stored in the shadow register until the current sequence is done and another trigger is set (START command or AUTO bit).

CURVEIDx: These three bits are used to identify the curve the channel follows during the fade sequence. With three bits, eight curves can be selected.

STARTPOSx: In this register, the start position must be set. The value is referred to as a step from 0 to 255 (8 bits resolution).

STOPPOSx: In this register, the stop position must be set. The value is referred to as a step from 0 to 255 (8 bits resolution).

Note: *Because any curve can be followed in both directions, a fade-in sequence occurs when the start value is smaller than the stop value. As soon as the start value is greater than the stop value, then the sequence is a fade-out one. When using negative coefficients, the curve behavior could change depending on the coefficient values.*

DELAYx: This 8-bit register is used to add a delay to the sequence start. Because it is an 8-bit register and this delay is related to steps, the delay value is from 0 to 255. The delay

time depends on the PWM frequency. For example, if the PWM frequency is 244 Hz, then the delay value has a resolution of 4 ms. If the PWM frequency is 488 Hz, then the delay time resolution is 2 ms. This factor is a great help in simplifying dynamic turning-indicator sequences.

The microcontroller has the possibility of reading back the current PWM values in every cycle. These values are accessible from the register 42h to 59h, as shown in Table 6. This accessibility ensures maximum control of the system and LED board feedback.

Table 6. PWM-Feedback registers (only Read registers)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
42h	ReadCH1-LB	PWM [7:0]							
43h	ReadCH1-MB	unused				PWM [11:8]			
44h	ReadCH2-LB	PWM [7:0]							
45h	ReadCH2-MB	unused				PWM [11:8]			
46h	ReadCH3-LB	PWM [7:0]							
47h	ReadCH3-MB	unused				PWM [11:8]			
48h	ReadCH4-LB	PWM [7:0]							
49h	ReadCH4-MB	unused				PWM [11:8]			
4Ah	ReadCH5-LB	PWM [7:0]							
4Bh	ReadCH5-MB	unused				PWM [11:8]			
4Ch	ReadCH6-LB	PWM [7:0]							
4Dh	ReadCH6-MB	unused				PWM [11:8]			
4Eh	ReadCH7-LB	PWM [7:0]							
4Fh	ReadCH7-MB	unused				PWM [11:8]			
50h	ReadCH8-LB	PWM [7:0]							
51h	ReadCH8-MB	unused				PWM [11:8]			
52h	ReadCH9-LB	PWM [7:0]							
53h	ReadCH9-MB	unused				PWM [11:8]			
54h	ReadCH10-LB	PWM [7:0]							
55h	ReadCH10-MB	unused				PWM [11:8]			
56h	ReadCH11-LB	PWM [7:0]							
57h	ReadCH11-MB	unused				PWM [11:8]			
58h	ReadCH12-LB	PWM [7:0]							
59h	ReadCH12-MB	unused				PWM [11:8]			

Table 7. Immediate OFF commands. Set duty cycle to zero (Read/Write)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
30h	IMMOFFREG1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
31h	IMMOFFREG2	unused				CH12	CH11	CH10	CH9

Registers IMMOFFREG1 and IMMOFFREG2 are used to turn all the channels OFF immediately. That means 100 % duty cycle in the internal FET gate (switch in low ohmic state and bypassing the LEDs) and 0 % PWM duty cycle in the LED or LEDs associated to this channel. These registers can be sent to a selected IC or as a broadcast message, depending on the frame ID only (command bits). The microcontroller can control every channel individually.

Table 8. Start commands for each channel (Read/Write)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
32h	START1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
33h	START2	unused				CH12	CH11	CH10	CH9

Registers START1 and START2, are used to start the sequences. These commands should be sent after all the channels have been programmed with the desired values. The microcontroller can control every channel individually. Other way of starting a channel is programing the CURVEIDx resgister with NOW bit =1, but at least one previous START command must be performed from the moment the MLC startup.

8.5 Delay coefficient – ASL50xxyHz

The delay coefficient can be set in the DELAYx register. See Section 8.4.1 "Channel programming registers map". This setting is individual for each channel and has a resolution of 8 bits. After the delay coefficient is set, a delay for a PWM curve can be programmed and the channel starts following the PWM dimming curve after the programmed step delay.

This feature on the ASL50xxyHz saves many software lines in the MCU and reduces the load on the communication bus. The combination of the delay and the fade-in/fade-out curves can be used in applications such as dynamic turn indicator or welcome scenarios.

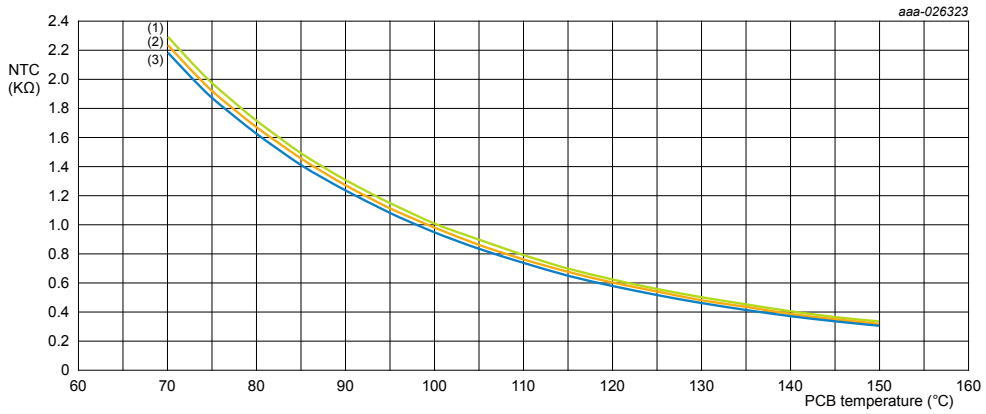
The delay resolution is 4.09 ms in case the PWM frequency is set to 244 Hz or 2 ms if it is set to 488 Hz.

8.6 Diagnostics

8.6.1 Direct NTC input

The MLC is able to read the voltage drop in an attached NTC from 0 V to 1.1 V. This analog voltage drop is converted to a digital value with an internal ADC. The customer can read the 6-bit digital value of this voltage drop in register 39h.

The MLC uses a continuos current of 25 µA to check the NTC status. This check is to determine if an open or short condition is present. The MLC uses a current of 440 µA to measure the voltage drop in the NTC and provide the digital value (only when CAN command 13 or 46 are sent). Figure 10 shows the measurement process. The microcontroller triggers the NTC read with command 13 for selective MLC or command 46 for broadcast trigger.



(1) NTC resistance High
(2) NTC resistance Typical
(3) NTC resistance Low

Figure 10. Typical NTC resistance vs. temperature in the range 70 °C to 130 °C

8.6.2 Direct Identification resistor input

Eight resistors with 1 % precision can be connected to the ID pin to read the identification / characterization information. The current on the ID pin is fixed to 25 µA ±10 %. The value of the resistor is determined at the MLC start-up and is available to the microcontroller in register 3Ah. The ID value is only read during device startup. To get the identification value, the microcontroller can read this register directly or ask for the IC diagnosis, the register 3Ah is included in the 8 bytes of diagnosis answer.

The voltage drop in the ID pin is read and converted to a digital value via an internal ADC. The ID resistors' values are not overlapping in ranges in Table 9.

Table 9. Possible identification resistors for nonoverlapping

Resistor	4.75	8.06	11.3	14.3	17.4	21.5	26.7	32.4	[kΩ]
Value	000	001	010	011	100	101	110	111	binary

8.6.3 LED fault detection

Each PWM switch has an Open Circuit and a Short Circuit comparator, even when the system is in Limp Home mode.

Open Circuit detection (OC): The OC detection threshold can be set to 6 V ±1 V (default value) or 17 V ±1.5 V, see Section 10 "ASL50xxyHz Register map". In case of an OC detection event, the PWM switch is closed and an error bit set. This process allows the IC to bypass this LED and the other LEDs to continue to operate. The bit flag can be reset by removing the supply voltage (V_{CC}) or by a bus command writing a 1 in the register 34h, bit 1. In case of clearing the flags (writing in register 34h), the action is done dynamically and a power-on-reset is not necessary. If the open circuit was just a lapse, then the system recovers automatically when clearing the flags. The open circuit is immediately detected when the switch passes from low ohmic to high ohmic state.

Short Circuit detection (SC): The SC detection limit is set to 1 V ± 0.5 V. The system can use a blanking time of 16 µs (default) or 32 µs, depending on the driving current and the string capacitor. The blanking time can be selected in the internal MTP bit 4, register

60h. The blancking time is applicable from the moment the internal switch passes from a low ohmic to a high ohmic state.

When there is a detection of an SC, the error bit is set and the microcontroller is aware of the fail. The microcontroller can then decide whether to close the switch associated to the shorted LED or not. If the microcontroller decides to close the switch, the rest of the LED string can continue working and just the affected LED is bypassed.

Restore the fail bit flag by a bus command writing a 1 in the register 34h, bit 0 or removing the supply voltage. If the flag is restored with a CAN message (write a 1 in the CLEAR_SC bit of register 34h), then the MLC does not need a power-on-reset. In addition, an automatic recheck action is executed by the IC to confirm whether the fail is still present or not. If the fail is still present, then the MLC will flag it again.

8.6.4 Internal junction temperature warnings

The maximum allowed junction temperature on the ASL5xxxyHz family is 175 °C. The user can program two warning thresholds to be activated. The default values are 140 °C for OTW_1 and 160 °C for OTW_2. As soon as the microcontroller receives these temperature warnings, it decides what action to take. For example, the microcontroller might reduce the LED string current to reduce the junction temperature and the whole system temperature. If the MLC reaches its maximum allowable internal temperature, 175 °C, it will not take any action. The microcontroller must correct any overtemperature situations to prevent a safety violation. OTW_1 and OTW_2 can be programmed in the MTP.

The microcontroller triggers the junction temperature read and consequent flagging with command 13 for selective MLC or command 46 for broadcast trigger.

Table 10. Junction temperature warning bits (Read)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
3Ah	ID	OTW_1	OTW_2	POK	LHM_STATUS	ID[3:1]			ID-FAIL

Note: *If the MLC junction temperature reaches the OTW_2, reduce the LED string current. The OTW measurement has a ±10 % accuracy.*

8.6.5 Undervoltage detection and protection

The MLC incorporates an undervoltage protection on the V_{CC}. The device switches off below 4.3 V.

When an undervoltage condition is detected, all the switches get open (high ohmic state) and the communication with the device is not possible. If Vcc gets recovered, then the IC allows the communication again and a power on reset is not required.

A full system diagnosis should be run after an undervoltage condition.

8.6.6 Diagnosis registers map

8.6.6.1 Register 34h - Status register

Register 34h has read and write rights.

This register can be sent/received to any MLC IC individually or can be a broadcast message. It depends on the CAN frame Extended-ID command.

Table 11. CLEAR - CLEAR control register (address 34h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	POR	ILLEGAL _ COMMAND	MTP_LOCK	REG_ILLE GAL_ACCESS	MTP_ILLE GAL_ACCESS	MTP_ACC ESS_STATUS	CLR_ OC	CLR_ SC
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 12. CLEAR - CLEAR control register (address 34h) bit description

Bit	Symbol	Description
7	POR	Power-on-reset (POR) **0 —** A power-on-reset has happened due to any external interference or power supply fail **1 —** Set by the microcontroller during the MLC startup The microcontroller can check this bit status to know if a POR has happened. If so, the MLC must be programmed with the values of the desired registers again, because after a POR, the MLC returns to the default values.
6	ILLEGAL _COMMAND	Illegal command **0 —** The MLC received a valid command. **1 —** The microcontroller sent a nonexisting command, a wrong message configuration or a command that is restricted to a different part number. The microcontroller writes a 1 in this location to clear the flag.
5	MTP_LOCK	MTP lock **0 —** The MTP is available to be read/write. **1 —** The user attempt to read / write in the MTP with a wrong key for 3 consecutive times. The MTP is not accessible by the micro.
4	REG_ILLEGAL_ACCESS	Register illegal access **0 —** The selected register is accessible by the microcontroller. **1 —** The microcontroller tries to write/read in an invalid register. If the value of this bit is 0 after writing or reading a register, then the action was performed in a valid register. The microcontroller writes a 1 in this location to clear the flag. The flag is not stopping the communication.
3	MTP_ILLEGAL_ACCESS	MTP illegal access **0 —** The register the microcontroller is trying to access is not restricted **1 —** The microcontroller is trying to read/write in a restricted register. The microcontroller should write a 1 in this location to clear the flag.
2	MTP_ACCESS_STATUS	MTP access status **0 —** The MLC was not able to access the required MTP register **1 —** The MLC succeeded accessing the required MTP register. The microcontroller should write a 1 in this location to clear the flag ***Note:*** *If neither MTP_ACCESS_STATUS, MTP_ILLEGAL_STATUS or ILLEGAL_COMMAND is set after MTP read/write request, the request is ignored due to an internal MTP function. The microcontroller must repeat the action.*
1	CLR_OC	Clear open-circuit detection **0 —** Always 0 when the microcontroller reads it. **1 —** Write a 1 in this location to clear all the OC flags and restart the channels.

Bit	Symbol	Description
0	CLR_SC	Clear short-circuit detection **0 —** Always 0 when the microcontroller reads it. **1 —** A 1 in this location to clear all the SC flags and restart the channels.

8.6.6.2 Read diagnostic bits, from MLC to microcontroller

Table 13. Open Circuit and Short Circuit registers (Read only)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
35h	READ_OC1	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1
36h	READ_OC2	unused				OC12	OC11	OC10	OC9
37h	READ_SC1	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1
38h	READ_SC2	unused				SC12	SC11	SC10	SC9

Registers READ_OC1, READ_OC2, READ_SC1, and READ_SC2 are used to read the fail flags. The microcontroller can read these registers to know if any fail occurs during the system operation. These registers can be cleared with the CLEAR register (34h), bits 0 and 1. Or, the microcontroller can clear all the OC and SC flags sending the command 39.

OC stands for "Open Circuit" and the number next to it represents the channel linked to the flag.

SC satnds for "Short Circuit" and the number next to it represents the channel linked to the flag.

Note: *The MLC IC must be turned ON before the Buck converter provides current to the LED string, see start-up sequence in the application notes. When the MLC is ON, it is able to detect the open circuit condition and close the switch associated with the open LED, automatically. If the MLC is not running before the Buck converter and there is an open circuit condition, the MLC is not able to close the switch associated to the failure LED automatically, causing the voltage in the associated switch to be higher than the allowable maximum. This condition may damages the MLC IC. The system startup sequence is to turn ON the MLC IC first and wait until the POK bit is set to 1.*

Table 14. NTC - NTC control register (address 39h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CPFAIL	NTC						NTCFAIL
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 15. NTC - NTC control register (address 39h) bit description

Bit	Symbol	Description
7	CPFAIL	Used for the internal charge pump circuit. **0 —** No open or short condition is detected in the charge pump **1 —** An open or short condition has happened in the external capacitor, the MLC cannot drive the gates of the switches, and the dimming function is not available.

Bit	Symbol	Description
6 to 1	NTC	NTC (voltage drop in the NTC resistance). **111001 —** 0,980 (70 °C) **110111 —** 0,951 (71 °C) **110101 —** 0,924 (72 °C) **110100 —** 0,897 (73 °C) **110010 —** 0,871 (74 °C) **...** **000111 —** 0.136 (150 °C)
0	NTCFAIL	NTC fail **0 —** No Open or Short condition is detected in the NTC pin **1 —** An Open or Short condition is detected in the NTC pin

Table 16. ID - ID control register (address 3Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTW_1	OTW_2	POK	LHM_STATUS	IDENTIFICATION			ID-FAIL
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 17. ID - ID control register (address 3Ah) bit description

Bit	Symbol	Description
7	OTW_1	Overtemperature Warning 1 **0 —** The junction temperature does not reach the programmed threshold **1 —** The junction temperature reaches the programmed threshold
6	OTW_2	Overtemperature Warning 2 **0 —** The junction temperature does not reach the programmed threshold **1 —** The junction temperature reaches the programmed threshold
5	POK	MLC IC check **0 —** MLC IC is not working properly or not fully operational **1 —** MLC IC is working properly and fully operational
4	LHM_STATUS	Limp Home mode status **0 —** MLC is not in LHM state **1 —** The device is in Limp Home mode.

Bit	Symbol	Description
3 to 1	IDENTIFICATION	Resistor value **000 —** Resistor value 1 **001 —** Resistor value 2 **010 —** Resistor value 3 **100 —** Resistor value 4 **011 —** Resistor value 5 **101 —** Resistor value 6 **110 —** Resistor value 7 **111 —** Resistor value 8 In this register, the microcontroller can read the identification resistor value with a 3-bit resolution, from bit 1 to 3. Those three bits give the possibility of using eight different resistors to characterize the board or LEDs used with the MLC IC.
0	ID-FAIL	Identification resistor fail **0 —** No open or short condition is detected in the ID pin. **1 —** An open or short condition is detected in the ID pin.

Table 18. Internal Status - Internal status control register (address 3Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TXD_BUFFER_OVERFLOW	unused						
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 19. Internal Status - Internal status control register (address 3Bh) bit description

Bit	Symbol	Description
7	TXD_BUFFER_ OVERFLOW	Used to flag a message buffer overflow **0 —** The communication buffer has less than three messages in the queue **1 —** The communication buffer has three or more messages in the queue ***Note:*** *The MLC communication buffer has four free spaces. If the microcontroller continues requesting information and does not give time for the MLC to answer, then when the buffer is overflowed, the MLC will start overwriting the content of the last position.*
6 to 0		unused

8.7 Internal oscillator 200 MHz for digital blocks

The internal oscillator provides the clock signal for the internal digital blocks. This block is automatically trimmed to generate a 200 MHz clock signal with 10 % accuracy. The 200 MHz oscillator and an adaptive prescaler gives the 10 MHz needed for the serial CAN communication. The preamble of the CAN message (standard-ID) is used to calibrate the prescaler. Therefore, the CAN clock has an accuracy of less than 0.25 %.

The internal oscillator helps to reduce the system cost and improves the system behavior when synchronizing the internal modules and different MLCs. This feature also helps the MLC system to have a superior EMC behavior.

8.8 Charge Pump

The charge pump mechanism integrated in the ASL5xxxyHz family is able to detect the maximum LED string voltage to have a voltage always at least 5 V higher than the maximum detected LED string voltage. This action allows the internal charge pump circuit to drive all the switches of the MLC without any problem and in a safe way. This intelligent charge pump controls all the blocks, even when they are driving different LED strings with different configurations. The charge pump only requires one external small capacitor.

The multiplexer that is connected to the highest switches in every floating block is responsible for detecting the maximum voltage of the LED string. With this mechanism, the Matrix LED Controller (MLC), is able to detect the maximum voltage in the blocks even when they are controlling different LED strings.

The charge pump mechanism needs an external capacitor. The external capacitor value selections are described in Table 20.

Table 20. External charge pump capacitor selection

N° of switches in parallel	Minimum capacitor	Comments
—	4.7 nF / 16 V / X7R	No blocks in parallel
2	10 nF / 16 V / X7R	2 blocks in parallel
3	15 nF / 16 V / X7R	3 blocks in parallel
4	22 nF / 16 V / X7R	4 blocks in parallel

The selection criteria are based on the current and gate charge required to close the switches safely. When blocks are parallel, more current is required to act in more switches at the same time, for that reason the charge pump capacitor has a greater value.

The maximum allowed capacitor value in the CP pin is 68 nF, because a higher value can affect the IC startup time and may produce a CPFAIL status.

A 220 pF capacitor should be connected between the VMAX pin and ground (100 V capacitor) to reduce the charge pump ripple and the electromagnetic emissions. The capacitor con also be connected between VMAX pin and SW15 pin (16 V capacitor) See Figure 6.

8.9 Charge pump fail-safe operation mode (CPFSO)

In case of failure in the internal charge pump circuit or external charge pump capacitor, the Matrix LED Controller (MLC) enters in a fail-safe operation mode (CPFSO) to provide the maximum operability as possible.

If the charge pump fails, the MLC is not able to drive the following:

- Top switch of the top block, in case of driving LED segment.
- First two switches of the top block, in case of driving single LED per switch.

The charge pump fail-safe operation mode starts when the MLC detects a problem in the charge pump. Depending on the open circuit threshold programmed in the MTP, it opens (high ohmic state) the first switch of the top block (OC = 1) or the first two switches of the top block (OC = 0).

Table 21. OC threshold selection and CPFSx selection in MTP

Register	Bit	Symbol	Description
58h	4	OC1	OC threshold selection for Block 1
59h	4	OC2	OC threshold selection for Block 2
5Ah	4	OC3	OC threshold selection for Block 3
5Bh	4	OC4	OC threshold selection for Block 4
5Ch	15	CPFS0	Select Block 1 as top block
5Dh	15	CPFS1	Select Block 2 as top block
5Eh	15	CPFS2	Select Block 3 as top block
5Fh	15	CPFS3	Select Block 4 as top block

If the OC bit is set to 0, the open circuit threshold is 6 V ±1 V, if it is 1, then the threshold is 17 V ±1.5 V.

In case of OC = 0 and a failure in the charge pump, the MLC opens the first two switches of the Blocks with a 1 in the linked CPFSx bit. When OC = 1, the MLC opens only the top switch of the selected blocks.

With this practice, if the MLC is in normal operation mode, it is able to continue driving the rest of switches with the programmed PWM.

In case the MLC is in LHM, the fail-safe operation reaction is the same and it continues respecting the LHM configuration programmed in the MTP for the rest of the switches.

Note: *CPFS3 is linked to Block 4 of switches; these are the top switches if all blocks are in series. This bit should be the only one set to 1, of CPFSx bits, when all blocks are in serial configuration.*

8.10 Matrix LED controller interface and configuration

The ASL5xxxyHz family incorporates a CAN controller for communication with the microcontroller. CAN-FD versions (ASL5xxxFHz) are also available in the ASL5xxxyHz family. If these versions are required, please contact NXP Semiconductors.

This serial interface is used to write into internal registers and read the data from the diagnostics register. The interface is also used to monitor any fault flags. The microcontroller has full control via the bus interface.

No external clock is required for the oversampling, due to the on-chip 200 MHz oscillator.

More information regarding On-Board and Off-Board configuration can be found in the application notes.

There are two physical options:

- When the microcontroller is located close to the MLC and on the same PCB, there can be a direct connection using the TX and RX lines. No physical layer is needed.
- When the microcontroller is on a separate board or otherwise far away (> 10 cm) from the MLC, two CAN physical layer transceivers are needed. The physical layer will guarantee a robust and reliable communication over a long distance.

In both configurations, the clock signal, generated by the internal oscillator, is divided by an adaptive prescaler to calibrate the clock to the incoming data. This process is to ensure a common communication speed.

Synchronization between MLCs is therefore done through CAN communication. There is no need for a separate sync signal, which can compromise EMI performance and board layout.

The communications protocol is byte-oriented. Because up to 32 devices can be connected together, five bits are sufficient to address the MLC device. Extended ID is used for addressing the device and differentiate between oriented or broadcast message. The Standard ID includes the preamble to synchronize all devices in the bus and ensure a CAN clock accuracy of less than 0.25 %.

8.11 External IC addressing

To make logistics easier, the MLC can be addressed externally with specific hardware configuration of pins from A0 to A4.

Five pins are available to address the MLC externally. Therefore, the system can connect up to 32 MLCs. The same physical layer, in case of an off-board configuration, can control all of these MLCs.

All these pins have an internal pull-up resistor of 60 kΩ. Thus, if a logic 1 is needed, the pin should remain floating. If a logic 0 is needed, the pin should be connected to ground.

8.12 Protection against missing V_{CC}

When V_{CC} is missing, the MLC is off and all switches remain open. But when V_{CC} is present and the device is working properly, it sets a bit in the diagnostics register that the microcontroller can read (POK). The microcontroller should only enable the LED driver when it is able to read this bit.

8.13 LED brightness calibration factor

The LED brightness calibration factor can be programmed and read out from the MTP of the MLC by the microcontroller. This capability allows the customer to correct for any differences in the luminance of LEDs, as a result of LED production spread, automatically inside the MLC.

The LED brightness calibration factor has a 5-bit resolution (from 0 to 31); and for that reason, the brightness reduction can be from 0 % to 24.22 %[1]. With this factor, the microcontroller does not need to adapt the PWM duty cycle for the brightness variation, because it is calculated inside the MLC. Therefore, when the microcontroller associates a prestored dimming curve that delivers 100 % duty cycle to a channel, and this channel has a brightness reduction associated to it, then the LED brightness cannot be 100 %, but reduced by the brightness calibration factor.

The brightness reduction factor is applicable to any PWM duty cycle value and is not a fixed value but a percentage. Two examples are shown below:

LED brightness calibration factor for both examples = 20 (10100 in the MTP)

- Example 1
  - The PWM duty cycle value in the curve is 100 %
  - *Output brightness = 1 * (1 – (20/128)) = 0.84 = 84 %*
- Example 2
  - The PWM duty cycle value in the curve is 50 %

1 The factor division inside of the MLC is by 128.

– *Output brightness = 0.5 * (1 – (20/128) = 0.42 = 42 %*

The examples above demonstrate that the reduced brightness value is not always the same for the different PWM duty cycle values. The default value for all the channels is 0 % reduction.

See Section 14 "Nonvolatile Multitime Programmable Memory (MTP)" for detailed information about the MTP selectable values.

8.14 Limp Home mode operation

When there is no communication with the microcontroller, but V_{CC} is present, the MLC automatically enters Limp Home mode state (LHM). Each channel is either fully ON or fully OFF, as defined by a bit in the MTP. This bit is programmable by the user at the end of the production line. Default state of the switches is all OFF, which means all LEDs are ON.

Table 22. LHM - Limp Home mode control register (address 3Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BYPASS_BINNING	LHM_EXIT			LHM_TIMEOUT			MTP_CFG
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 23. LHM - Limp Home mode control register (address 3Ch) bit description

Bit	Symbol	Description
7	BYPASS_BINNING	Bypass binning. **0 —** Scaling/calibration factor is applied to the final PWM DC calculation **1 —** Scaling/calibration factor is not applied to the final PWM DC calculation This bit can be used to: • Bypass the calibration factor during Camera calibration • Measure single LED brightness during manufacturing process Note: This bit is not related to the Limp Home Mode configuration of triggering.
6 to 4	LHM_EXIT	Limp Home mode deactivation sequence and LHM timeout refresh.[1] **001 —** Deactivation sequence, step 1 **010 —** Deactivation sequence, step 2 **100 —** Deactivation sequence, step 3 **111 —** LHM timeout refresh
3 to 1	LHM_TIMEOUT	Timeout setting for activation of Limp Home mode.[2] **000 —** 4.5 ms, setting 1 **001 —** 9 ms, setting 2 **010 —** 18 ms, setting 3 **011 —** 36 ms, setting 4 **100 —** 72.1 ms, setting 5 **101 —** 144.2 ms, setting 6 **110 —** 288.4 ms, setting 7 **111 —** 576.7 ms, setting 8

Bit	Symbol	Description
0	MTP_CFG	MTP configuration. **0 —** MLC normal operation **1 —** MLC in MTP configuration mode ***Note:*** *To read or write the MTP, the microcontroller must enter MTP configuration mode.*

[1] When refreshing the timeout timer with 111 in bits [6:4], the Limp Home mode timeout setting is written as well in bits [3:1]
[2] When changing the Limp Home mode timeout setting, the LHM_EXIT bits should be set to “111” to refresh the timeout timer

After MTP configuration, the limp home settings are permanently stored. Once the MLC detects a communication failure event (Limp Home mode watch dog timer runs out), the device turns the switches ON or OFF, depending on the Limp Home mode configuration stored in the MTP.

In case the system recovers from the error, Limp Home mode can be left via the exit Limp Home mode sequence. With the completion of the exit sequence, the device operates in normal conditions and the configuration registers are open for write access again. The MLC keeps the LHM configuration in the output until the microcontroller starts another sequence.

Limp Home and normal operation modes offer the same diagnosis behavior. This behavior includes the undervoltage protection as well as the failure behavior (open and short-circuit detection).

8.14.1 Limp Home mode activation

If no write to the Limp Home mode exit bits (register 3Ch, bits 6:4) with data 111 is executed for the timeout time as defined in the Limp Home mode control register, a Limp Home mode is automatically activated. During start-up, the MLC is preconfigured to the maximum allowed watchdog timeout possible (576.7 ms). If this value wants to be changed, the user must set a new watchdog timeout during the configuration of the register. If the microcontroller does not send an LHM_Refresh command before 576.7 ms after the startup, then the MLC automatically enters in Limp Home mode.

Before entering MTP configuration mode, refresh the watchdog timeout. During the MTP configuration, the watchdog is stopped and the refreshing action is not necessary during this time.

8.14.2 Limp Home mode operation

Once the system has entered Limp Home mode, the MLC switches to the configuration as defined in the MTP memory. See Section 14 "Nonvolatile Multitime Programmable Memory (MTP)" for more information about the Limp Home mode configuration.

During Limp Home mode, operation of the CAN interface remains functional, but only the Limp Home mode control register can be written. The other registers offer only read access.

8.14.3 Limp Home mode deactivation

To deactivate Limp Home mode, a dedicated Limp Home mode deactivation sequence is written to the Limp Home mode control register.

Table 24. Limp Home mode deactivation sequence

Deactivation step	Data to LHM_EXIT[6:4]
Step 1	001
Step 2	010
Step 3	100

This sequence could be applied to any single IC or as a broadcast message.

Sequence to exit LHM in a single IC:

CMD 3 = 000011, target MLC's LHM_Exit [6:4] bits with 3 bytes of data in the data field. Only one CAN message is needed to exit the LHM status.

The order in Table 25 shows from byte 0 to byte 2 in the CAN message data field.

Table 25. Limp Home mode exit sequence messages

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
3Ch	LHM	0	0	0	1		111		0

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
3Ch	LHM	0	0	1	0		111		0

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
3Ch	LHM	0	1	0	0		111		0

Message:

Command = 3
Data_0 = 1E
Data_1 = 2E
Data_2 = 4E

Sequence to exit LHM with a broadcast or selective message:

Command 3 is used for selective LHM exit and command 38 for broadcast LHM exit.

Once the deactivation sequence is completed, the MLC is immediately fully operational. LEDs will follow LHM configuration until the microcontroller starts a new sequence.

8.15 Communication interface

The ASL5xxxyHz family uses a CAN interface to communicate with an external microcontroller. The CAN interface can be used for setting all the registers related to the 12 available channels and other configuration registers. See Section 10 "ASL50xxyHz Register map" and Section 11.1 "ASL51xxSHy Register MAP".

If the MLC system is on a board other than the board that has the microcontroller, a CAN physical layer should be used (CAN transceiver) and TXD and RXD should be connected between the transceiver and the different MLC ICs.

If the MLC system is on the same board of the microcontroller, a physical layer is not needed and just the TXD and RXD pins of the different ICs should be connected, as well as a pull-up resistor and a bridge between TXD and RXD line. The pull-up resistor should not allow current higher than 4 mA in the TXD and RXD pins.

The first byte to be read by the MLC is the Most Significant Byte (MSB). Data byte 1 (DB1) in Figure 11.

To ensure a robust communication and an accuracy in the CAN clock of less than 0.25 %, the microcontroller sends a dummy clock trimming every 9 ms. The message uses the CAN command 34 and it has no data in the data field. If another message has a cycle of less than 9 ms, then the clock trimming is done with this message and the dummy clock trimming message is not needed any more.

The MLC can be controlled by several ECUs thanks to the reserved bits in the extended ID. These bits help to identify the different masters controlling the same MLC or controllers and also gives the possibility of setting a priority due to the known arbitration of the CAN protocol.

The master microcontroller can use the same CAN controller to communicate with the rest of the vehicle and with the MLC. The designer just needs to ensure there are no message collisions, which respects ISO CAN rules.

8.16 Application protocol

Master to Slave command is always with Extended ID and fixed value in the Standard ID field for synchronization as shown in Figure 11.

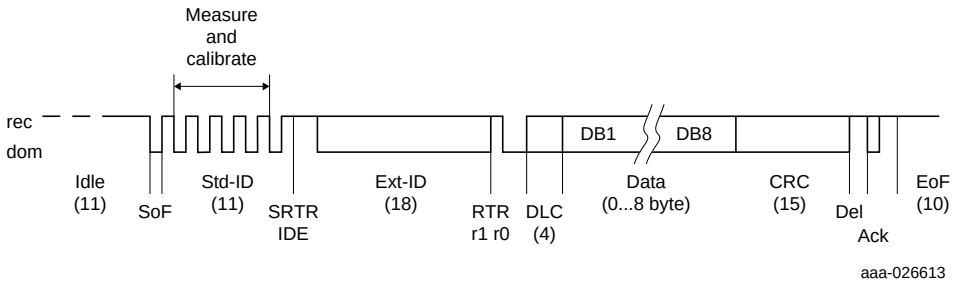


Figure 11. CAN Ext-ID frame

All the MLC ICs are synchronized in every CAN frame they receive, ensuring good synchronization between ICs and a very accurate sampling clock, with an accuracy of less than 0.25 %.

Table 26. Standard-ID and the synchronization sequence

Standard-ID										
1	0	1	0	1	0	1	0	1	0	1

Table 27. Extended-ID format

Extended-ID																	
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved							CMD[10:5]						Address[4:0]				

Reserved = should be 0 to fit with the ID of the supplied DBC file. These bits can also be used to drive the MLC or group of MLCs with multiple masters or to avoid message collision when using the same CAN controller in the main microcontroller to communicate with the rest of the vehicle.

Address [4:0]: MLC device address (up to 32 ICs in the same CAN network)

9 CAN commands

Table 28. CAN and CAN-FD commands

Command CMD[10:5]	Type	Description	PWM Mode (Smart / Direct)	CAN/CAN -FD	CAN Valid DLC	CAN-FD Valid DLC	Other Invalid conditions
0	Selective	Consecutive register write	All	All	2 to 8	3 to 15	LHM Mode || Number of Reg. fitting DLC(CAN-FD)* || No.of Registers = 0
1	Selective	Selective register write	All	All	2, 4, 6, 8	3, 5, 7, 9 to 15	LHM Mode || Number of Reg. fitting DLC(CAN-FD)* || No.of Registers = 0
2	Invalid command						
3	Selective	LHM exit	All	All	3	3	NA
4	Selective	MLC channel start	All	All	2	2	LHM mode
5	Selective	MLC channel immediate OFF	All	All	2	2	LHM mode
6	Selective	LHM refresh	All	All	1	1	NA
7	Selective	Dummy trimming	All	All	0	0	NA
8	Selective	Write direct PWM CH 1,2,3,4	Direct	All	8	NA	LHM mode
9	Selective	Write direct PWM CH 5,6,7,8	Direct	All	8	NA	LHM mode
10	Selective	Write direct PWM CH 9,10,11,12	Direct	All	8	NA	LHM mode
11	Invalid command						
12	Broadcast - 2 MLCs only	Write all PWM registers	Direct	CAN-FD	NA	14	LHM mode
13	Selective	Diagnosis ADC trigger	All	All	0	0	NA
14	Selective	MTP write	All	All	4	4	LHM mode || MTP_Locked || Invalid Key || mtp_cfg = 0
15	Invalid command						
16	Selective	Consecutive register read	All	CAN	1	NA	NA
17	Selective	Selective register read	All	CAN	1 to 8	NA	NA
18	Selective	Diagnosis read	All	All	0	0	NA
19	Selective	Consecutive register read	All	CAN-FD	NA	2	Number of Reg. fitting DLC(CAN-FD)* || No.of Registers = 0
20	Selective	Selective register read	All	CAN-FD	NA	2 to 15	Number of Reg. fitting DLC(CAN-FD)* || No.of Registers = 0
21	Selective	Read smart PWM feedback	Smart	All	0	0	NA

Command CMD[10:5]	Type	Description	PWM Mode (Smart / Direct)	CAN/CAN -FD	CAN Valid DLC	CAN-FD Valid DLC	Other Invalid conditions
22	Invalid command						
23	Invalid command						
24	Invalid command						
25	Invalid command						
26	Invalid command						
27	Invalid command						
28	Invalid command						
29	Invalid command						
30	Selective	MTP read	All	All	2	2	LHM mode || MTP_Locked || Invalid Key
31	Invalid command						
32	Broadcast	MLC channel start	All	All	2	2	LHM mode
33	Broadcast	MLC channel immediate OFF	All	All	2	2	LHM mode
34	Broadcast	Dummy trimming	All	All	0	0	NA
35	Broadcast	POK register read	All	All	0	0	NA
36	Broadcast	POR register read	All	All	0	0	NA
37	Broadcast	LHM refresh	All	All	1	1	NA
38	Broadcast	LHM exit	All	All	3	3	NA
39	Broadcast	Clear all OC/ SC flags	All	All	0	0	NA
40	Broadcast	Diagnosis read	All	All	0	0	NA
41	Broadcast	Go to sleep	All	All	0	0	LHM mode || Partial networking enabled
42	Broadcast	Partial sleep	All	All	4	4	LHM mode || partial networking disabled
43	Broadcast	Partial wake	All	All	4	4	LHM mode || partial networking disabled || Not in Sleep mode
44	Broadcast	Write all PWM registers of all MLCs	Direct	CAN-FD	NA	12	LHM mode
45	Broadcast	Read smart PWM feedback	Smart	All	0	0	NA
46	Broadcast	Diagnosis ADC trigger	All	All	0	0	NA
47	Invalid command						
48	Invalid command						
49	Invalid command						
50	Invalid command						

Command CMD[10:5]	Type	Description	PWM Mode (Smart / Direct)	CAN/CAN -FD	CAN Valid DLC	CAN-FD Valid DLC	Other Invalid conditions
51	Invalid command						
52	Invalid command						
53	Invalid command						
54	Invalid command						
55	Invalid command						
56	Invalid command						
57	Invalid command						
58	Invalid command						
59	Invalid command						
60	Invalid command						
61	Invalid command						
62	Invalid command						
63	Broadcast	Junction temperature read	All	All	0	0	LHM mode

Note: *Invalid Flag is not set when device is in SLEEP mode. Read or write MTP during LHM state is also not a valid scenario.*

Table 29. Number of Register fitting DLC (CAN - FD)

DLC	CMD - 0	CMD - 1	CMD - 19	CMD - 20
0	Invalid	Invalid	Invalid	Invalid
1	Invalid	Invalid	Invalid	Invalid
2	Invalid	Invalid	≤ 64	1
3	1	1	Invalid	≤ 2
4	≤ 2	Invalid	Invalid	≤ 3
5	≤ 3	≤ 2	Invalid	≤ 4
6	≤ 4	Invalid	Invalid	≤ 5
7	≤ 5	≤ 3	Invalid	≤ 6
8	≤ 6	Invalid	Invalid	≤ 7
9	≤ 10	≤ 5	Invalid	≤ 11
10	≤ 14	≤ 7	Invalid	≤ 15
11	≤ 18	≤ 9	Invalid	≤ 19
12	≤ 22	≤ 11	Invalid	≤ 23
13	≤ 30	≤ 15	Invalid	≤ 31
14	≤ 46	≤ 23	Invalid	≤ 47
15	≤ 62	≤ 31	Invalid	≤ 63

For more information regarding CAN commands, refer to the application notes.

Table 30 represents the Standard-ID format when the MLC answers the microcontroller petition.

Table 30. Standard–ID format in a response frame

1	1	1	1	1	1	A4	A3	A2	A1	A0

A4 to A0: MLC IC address

When the microcontroller configures the MLC registers, Standard-ID = 555h is used for baud rate calculations and synchronization. Because the Standard-ID is fixed in the message from the microcontroller to the Matrix controllers, and arbitration is done during this time, the microcontroller always wins the arbitration phase in the second bit.

10 ASL50xxyHz Register map

Table 31. ASL50xxyHz Register map

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0	Reset
0	CURVID1	SH1[7:5]			AUTO1	NOW1	CURVEID1[2:0]			00000000
1	STARTPOS1	STARTPOS1[7:0]								00000000
2	STOPPOS1	STOPPOS1[7:0]								11111111
3	DELAY1	DELAY1[7:0]								00000000
4	CURVID2	SH2[7:5]			AUTO2	NOW2	CURVEID2[2:0]			00000000
5	STARTPOS2	STARTPOS2[7:0]								00000000
6	STOPPOS2	STOPPOS2[7:0]								11111111
7	DELAY2	DELAY2[7:0]								00000000
8	CURVID3	SH3[7:5]			AUTO3	NOW3	CURVEID3[2:0]			00000000
9	STARTPOS3	STARTPOS3[7:0]								00000000
A	STOPPOS3	STOPPOS3[7:0]								11111111
B	DELAY3	DELAY3[7:0]								00000000
C	CURVID4	SH4[7:5]			AUTO4	NOW4	CURVEID4[2:0]			00000000
D	STARTPOS4	STARTPOS4[7:0]								00000000
E	STOPPOS4	STOPPOS4[7:0]								11111111
F	DELAY4	DELAY4[7:0]								00000000
10	CURVID5	SH5[7:5]			AUTO5	NOW5	CURVEID5[2:0]			00000000
11	STARTPOS5	STARTPOS5[7:0]								00000000
12	STOPPOS5	STOPPOS5[7:0]								11111111
13	DELAY5	DELAY5[7:0]								00000000
14	CURVID6	SH6[7:5]			AUTO6	NOW6	CURVEID6[2:0]			00000000
15	STARTPOS6	STARTPOS6[7:0]								00000000
16	STOPPOS6	STOPPOS6[7:0]								11111111
17	DELAY6	DELAY6[7:0]								00000000
18	CURVID7	SH7[7:5]			AUTO7	NOW7	CURVEID7[2:0]			00000000
19	STARTPOS7	STARTPOS7[7:0]								00000000
1A	STOPPOS7	STOPPOS7[7:0]								11111111
1B	DELAY7	DELAY7[7:0]								00000000
1C	CURVID8	SH8[7:5]			AUTO8	NOW8	CURVEID8[2:0]			00000000
1D	STARTPOS	STARTPOS8[7:0]								00000000
1E	STOPPOS	STOPPOS8[7:0]								11111111
1F	DELAY8	DELAY8[7:0]								00000000
20	CURVID9	SH9[7:5]			AUTO9	NOW9	CURVEID9[2:0]			00000000
21	STARTPOS9	STARTPOS9[7:0]								00000000
22	STOPPOS9	STOPPOS9[7:0]								11111111
23	DELAY9	DELAY9[7:0]								00000000
24	CURVID10	SH10[7:5]			AUTO10	NOW10	CURVEID10[2:0]			00000000
25	STARTPOS10	STARTPOS10[7:0]								00000000
26	STOPPOS10	STOPPOS10[7:0]								11111111
27	DELAY10	DELAY10[7:0]								00000000
28	CURVID1	SH11[7:5]			AUTO11	NOW11	CURVEID11[2:0]			00000000
29	STARTPOS11	STARTPOS11[7:0]								00000000
2A	STOPPOS11	STOPPOS11[7:0]								11111111

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0	Reset
2B	DELAY11	DELAY11[7:0]								00000000
2C	CURVID12	SH12[7:5]			AUTO12	NOW12	CURVEID12[2:0]			00000000
2D	STARTPOS12	STARTPOS12[7:0]								00000000
2E	STOPPOS12	STOPPOS12[7:0]								11111111
2F	DELAY12	DELAY12[7:0]								00000000
30	IMMOFF 1	IMMOFF8	IMMOFF7	IMMOFF6	IMMOFF5	IMMOFF4	IMMOFF3	IMMOFF2	IMMOFF1	00000000
31	IMMOFF 2	unused				IMMOFF12	IMMOFF11	IMMOFF10	IMMOFF9	00000000
32	START 1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	00000000
33	START 2	unused				CH12	CH11	CH10	CH9	00000000
34	CLEAR	POR	Illegal_ command	MTP_ Locked	REG_ ILLEGAL_ ACCESS	MTP_ ILLEGAL_ ACCESS	MTP_ ACCESS_ STATUS	CLR_OC	CLR_SC	00000000
35	READ_OC1	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1	00000000
36	READ_OC2	unused				OC12	OC11	OC10	OC9	00000000
37	READ_SC1	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	00000000
38	READ_SC2	unused				SC12	SC11	SC10	SC9	00000000
39	NTC	CPFAIL	NTC[6:1]						NTCFAIL	00000000
3A	ID	OTW_1	OTW_2	POK	LHM_ STATUS	ID[3:1]			ID-FAIL	00000000
3B	Internal_Status	TXD_ Buffer_Full	unused							00000000
3C	LHM	Bypass_ binning	LHM_EXIT[6:4]			LHM_TIMEOUT[3:1]			MTP_CFG	00000000
3D	MTP Write Control1	unused	MTP Register Adress [6:0]							00000000
3E	MTP Write D1	MTP Write Data D1 [7:0]								00000000
3F	MTP Write D2	MTP Write Data D2 [7:0]								00000000
40	MTP Read D1	MTP Read Data D1 [7:0]								00000000
41	MTP Read D2	MTP Read Data D2 [7:0]								00000000
42	ReadCH1-LB	PWM[7:0]								00000000
43	ReadCH1-MB	unused				PWM[11:8]				00000000
44	ReadCH2-LB	PWM[7:0]								00000000
45	ReadCH2-MB	unused				PWM[11:8]				00000000
46	ReadCH3-LB	PWM[7:0]								00000000
47	ReadCH3-MB	unused				PWM[11:8]				00000000
48	ReadCH4-LB	PWM[7:0]								00000000
49	ReadCH4-MB	unused				PWM[11:8]				00000000
4A	ReadCH5-LB	PWM[7:0]								00000000
4B	ReadCH5-MB	unused				PWM[11:8]				00000000
4C	ReadCH6-LB	PWM[7:0]								00000000
4D	ReadCH6-MB	unused				PWM[11:8]				00000000
4E	ReadCH7-LB	PWM[7:0]								00000000
4F	ReadCH7-MB	unused				PWM[11:8]				00000000
50	ReadCH8-LB	PWM[7:0]								00000000
51	ReadCH8-MB	unused				PWM[11:8]				00000000
52	ReadCH9-LB	PWM[7:0]								00000000
53	ReadCH9-MB	unused				PWM[11:8]				00000000
54	ReadCH10-LB	PWM[7:0]								00000000
55	ReadCH10-MB	unused				PWM[11:8]				00000000

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0	Reset
56	ReadCH11-LB	PWM[7:0]								00000000
57	ReadCH11-MB	unused				PWM[11:8]				00000000
58	ReadCH12-LB	PWM[7:0]								00000000
59	ReadCH12-MB	unused				PWM[11:8]				00000000

11 Direct PWM mode – ASL51xxyHz.

The MLC ASL51xxyHz provides the possibility of sending direct PWM data to every channel. The microcontroller provides all the dimming curves; and the PWM duty cycle value must be updated in every PWM period, if the duty cycle has to be changed.

Each channel needs 12 bits for the PWM duty cycle that can be updated every PWM cycle

Full diagnosis is available in these part numbers.

Because the amount of data in the bus is greater than in the smart mode (ASL50xxyHz), a higher baud rate may be needed. The available baud rates in the MLC are 125 Kbps, 250 Kbps, 500 Kbps and 1 Mbps. The communication interface data rate should be selected to fulfill the system latency requirement. This latency is the time from when the microcontroller sends the new PWM duty cycle value to the moment the MLC executes it.

The addressing of the MLC is done using the Extended-ID. The Standard-ID is used for clock synchronization purpose with the fixed sequence/preamble equal to 555h. All the MLCs are synchronized in every CAN massage, ensuring a good synchronization between the different MLC ICs and a very accurate sampling clock, with an accuracy of less than 0.25 %.

11.1 ASL51xxSHy Register MAP

Table 32. ASL51xxSHy register map

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0	Reset Values
0	DIRECT_CH1_LB	PWM[7:0]								00000000
1	DIRECT_CH1_UB	unused				PWM[11:8]				00000000
2	DIRECT_CH2_LB	PWM[7:0]								00000000
3	DIRECT_CH2_UB	unused				PWM[11:8]				00000000
4	DIRECT_CH3_LB	PWM[7:0]								00000000
5	DIRECT_CH3_UB	unused				PWM[11:8]				00000000
6	DIRECT_CH4_LB	PWM[7:0]								00000000
7	DIRECT_CH4_UB	unused				PWM[11:8]				00000000
8	DIRECT_CH5_LB	PWM[7:0]								00000000
9	DIRECT_CH5_UB	unused				PWM[11:8]				00000000
A	DIRECT_CH6_LB	PWM[7:0]								00000000
B	DIRECT_CH6_UB	unused				PWM[11:8]				00000000
C	DIRECT_CH7_LB	PWM[7:0]								00000000
D	DIRECT_CH7_UB	unused				PWM[11:8]				00000000
E	DIRECT_CH8_LB	PWM[7:0]								00000000

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0	Reset Values
F	DIRECT_CH8_UB	unused				PWM[11:8]				00000000
10	DIRECT_CH9_LB	PWM[7:0]								00000000
11	DIRECT_CH9_UB	unused				PWM[11:8]				00000000
12	DIRECT_CH10_LB	PWM[7:0]								00000000
13	DIRECT_CH10_UB	unused				PWM[11:8]				00000000
14	DIRECT_CH11_LB	PWM[7:0]								00000000
15	DIRECT_CH11_UB	unused				PWM[11:8]				00000000
16	DIRECT_CH12_LB	PWM[7:0]								00000000
17	DIRECT_CH12_UB	unused				PWM[11:8]				00000000
18 to 2F	reserved	unused								00000000
30	IMMOFF 1	IMMOFF8	IMMOFF7	IMMOFF6	IMMOFF5	IMMOFF4	IMMOFF3	IMMOFF2	IMMOFF1	00000000
31	IMMOFF 2	unused				IMMO FF12	IMMO FF11	IMMO FF10	IMMOFF9	00000000
32	START 1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	00000000
33	START 2	unused				CH12	CH11	CH10	CH9	00000000
34	CLEAR	POR	Illegal_ command	MTP_ Locked	REG_ ILLEGAL_ ACCESS	MTP_ ILLEGAL_ ACCESS	MTP_ ACCESS_ STATUS	CLR_OC	CLR_SC	00000000
35	READ_OC1	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1	00000000
36	READ_OC2	unused				OC12	OC11	OC10	OC9	00000000
37	READ_SC1	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	00000000
38	READ_SC2	unused				SC12	SC11	SC10	SC9	00000000
39	NTC	CPFAIL	NTC[6:1]						NTCFAIL	00000000
3A	ID	OTW_1	OTW_2	POK	LHM_ STATUS	ID[3:1]			ID-FAIL	00000000
3B	Internal_Status	TXD_ Buffer_ Full	unused							00000000
3C	LHM	BYPASS_ BINNING	LHM_EXIT[6:4]			LHM_TIMEOUT[3:1]			MTP_ CFG	00000000
3D	MTP Write Control1	unused	MTP Register Adress [6:0]							00000000
3E	MTP Write D1	MTP Write Data D1 [7:0]								00000000
3F	MTP Write D2	MTP Write Data D2 [7:0]								00000000
40	MTP Read D1	MTP Read Data D1 [7:0]								00000000
41	MTP Read D2	MTP Read Data D2 [7:0]								00000000

All cells presented in the register map are configurable by the customer. If the microcontroller tries to write in the reserved registers, from 18h to 2Fh, the Matrix LED controller (MLC) will raises an error flag. This means that bit 4 of register 34h, REG_ILLEGAL_ACCESS, is set to 1. This bit can be cleared by writing a 1 on it.

12 Sleep and Wake Up

The MLC can enter in Sleep mode and drastically reduce the current consumption, giving the possibility to make an energy efficient system.

The microcontroller can put the entire Matrix LED Controller to sleep with a single broadcast message:

- **CAN message for Sleep mode (Broadcast):** (Partial Networking must be deactivated)
- Command = 41
- DLC = 000 (no data in the CAN message)

This command is ignored only if the MLC is in Limp Home mode state.

All the MLCs go to sleep when they receive this broadcast message, but the CAN controller continues watching the bus and in case any change occurs in the CAN bus, the CAN controller wakes up the MLC immediately.

In Sleep mode, the MLC consumes less than 1.35 mA. In case the system has MLCs in sleep and others in the same bus in wake (Partial Networking), refer to Section 13 "Partial networking for Sleep and Wake Up (message based)".

Send a message to refresh the Limp Home mode watchdog timer (register 3Ch) right before sending the MLCs to sleep. Refreshing the timer this way avoids reaching the timeout setting during the send-to-sleep process. During sleep mode, the watchdog timer to enter in Limp Home mode in case of communication failure is stopped and refresh action is not required during this mode. Any watchdog refresh action from the microcontroller during Sleep mode wakes up the MLCs.

If the MLC wakes up due to a noise in the CAN bus, the MLC returns to sleep, in case it does not receive any message in the period of the maximum value of the watchdog timer (576.7 ms). In this case, the MLC does not enter the Limp Home mode state, but returns to sleep mode. The MLC wakes up only if the microcontroller orders it to do so.

A synchronization action must be performed in the bus after waking them up. The synchronization is done by sending three consecutive messages from the microcontroller with no data on them (dummy-trimming message). The preamble of these messages is used to trim the CAN clock and synchronize all the MLCs in the bus. A broadcast trimming action is done to be sure that all the MLCs are synchronized and able to send information to the microcontroller.

13 Partial networking for Sleep and Wake Up (message based)

In both messages, Sleep and Wake Up in partial networking, each bit of the bytes of the data field of the CAN message is linked to an MLC. See Table 33. The partial networking control messages, for Sleep or Wake Up, always has 4 bytes of data, the same 32 bits. Due to the address pins (5, from A0 to A4) of the MLC, up to 32 MLCs in the same CAN bus can connect. For that reason, the number of bits in the message fits with the maximum number of MLCs that can be in the same Bus.

These two messages are always broadcast and the MLCs receive the messages whether the MLCs are in normal operation or in sleep mode. These messages are ignored only if the MLC is in Limp Home mode.

In both cases, the MLC reacts only to the bit that is linked with its address. For example, the MLC with address 0 reacts to the first bit of the first byte of the message, or what is the same, it reacts to the value of the MS bit of the first byte. See Table 33.

If the bit is 1, the MLC goes to sleep, in case the message is intended to send the MLC to sleep, or wakes up the IC, in case the message is intended for this action.

Table 33 describes the distribution of the MLCs in the different bytes of the massages.

Table 33. MLCs linked to the bits

Byte_0 (MSB in the CAN message)							
MLC_0	MLC_1	MLC_2	MLC_3	MLC_4	MLC_5	MLC_6	MLC_7
Byte_1							
MLC_8	MLC_9	MLC_10	MLC_11	MLC_12	MLC_13	MLC_14	MLC_15
Byte_2							
MLC_16	MLC_17	MLC_18	MLC_19	MLC_20	MLC_21	MLC_22	MLC_23
Byte_3							
MLC_24	MLC_25	MLC_26	MLC_27	MLC_28	MLC_29	MLC_30	MLC_31

Refresh the Limp Home mode watchdog timer (register 3Ch) right before sending any MLC to sleep, to avoid reaching the timeout setting during the send-to-sleep process. During sleep mode, the watchdog timer is stopped; a refresh action is not required during this mode. If any refresh action is intended during sleep mode, the MLC does not take care of it, because it waits only for a wake-up message.

13.1 CAN message configuration for Partial_Sleep and Partial_Wake

Both messages are broadcast and received by all the MLCs connected to the CAN bus.

CAN message for Partial-Sleep:

Command –> 42
DLC –> 4
Data byte_0 (MSB) –> Byte0
Data byte_1 –> Byte1
Data byte_2 –> Byte2
Data byte_3 –> Byte3

CAN message for Partial-Wake:

Command –> 43
DLC –> 4
Data byte_0 (MSB) –> Byte0
Data byte_1 –> Byte1
Data byte_2 –> Byte2
Data byte_3 –> Byte3

In case of waking any of the MLCs up, a broadcast clock trimming action must be performed. The clock trimming is done by three consecutive messages from the microcontroller with no data on them (dummy trimming message). The preamble of these messages is used to trim the CAN clock and synchronize all the MLCs in the bus.

Note: *When partial networking is based on message recognition, the MLC continues to have part of the analog and CAN controller activated during sleep mode.*

14 Nonvolatile Multitime Programmable Memory (MTP)

The nonvolatile Multitime Programmable Memory (MTP) is used to store:

- Predefined coefficients for the PWM dimming curves (only in ASL50xxyHz — Smart mode)

- PWM frequency selection (244 Hz or 488 Hz)
- Slew rate control per block (individual)
- Switching phase shifting sequences for the different floating blocks
- Limp Home mode sequence
- Communication baud rate
- Open-circuit detection threshold
- Single / Multiple MLCs (internal push/pull configuration)
- LED calibration / scaling factor (5-bits per channel)
- Overtemperature warning (OTW1 and OTW2) thresholds
- Standby mode (full / partial networking)
- MTP Lock Key and counter
- Short-circuit blanking time selection
- Charge pump fail-safe operation mode (CPFSO)
- Free customer data (~ 480-bit)
- Internal configuration (not accessible by user)

The MTP can be programmed at the end of the production line (once the MLC is populated on the PCB). The CAN interface can be used to program all the values in the registers. Table 34 shows the registers to write and read from the MTP, together with a detailed write and read sequence.

Table 34. MTP Read/Write

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
3Dh (R/W)	MTP control	unused	MTP Register Address						
3Eh (R/W)	MTP Write D1	MTP Write Data D1 [7:0]							
3Fh (R/W)	MTP Write D2	MTP Write Data D2 [7:0]							
40h (R)	MTP Read D1	MTP Read Data D1 [7:0]							
41h (R)	MTP Read D2	MTP Read Data D2 [7:0]							

Write and read process flow charts are available in the application notes.

14.1 MTP memory map

Table 35. MTP memory map

No. Bits	Block	MTP Registers (16 bits registers)[1][2]																Address
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	reserved[3]																00h
16	1																	01h
~																		~
112	7	MTP Write Counter0[4]								IC Version[4]								07h
~		reserved																~
880	55																	37h
896	56	Value has no impact[5]								Curve 0 coefficients							A	38h
912	57																B	39h
928	58																C	3Ah
944	59																D	3Bh

No. Bits	Block	MTP Registers (16 bits registers)[1][2]																Address
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
960	60				Curve 1 coefficients												A	3Ch
976	61																B	3Dh
992	62																C	3Eh
1008	63																D	3Fh
1024	64				Curve 2 coefficients												A	40h
1040	65																B	41h
1056	66																C	42h
1072	67																D	43h
1088	68				Curve 3 coefficients												A	44h
1104	69																B	45h
1120	70																C	46h
1136	71																D	47h
1152	72				Curve 4 coefficients												A	48h
1168	73																B	49h
1184	74																C	4Ah
1200	75																D	4Bh
1216	76				Curve 5 coefficients												A	4Ch
1232	77																B	4Dh
1248	78																C	4Eh
1264	79																D	4Fh
1280	80				Curve 6 coefficients												A	50h
1296	81																B	51h
1312	82																C	52h
1328	83																D	53h
1344	84				Curve 7 coefficients												A	54h
1360	85																B	55h
1376	86																C	56h
1392	87																D	57h
1408	88	Overtemperature Warning 1			Overtemperature Warning 0			Phase1		LHM defs1–3			OC1	Slew1[3:0]				58h
1424	89	Value has no impact[5]						Phase2		LHM defs4–6			OC2	Slew2[3:0]				59h
1440	90							Phase3		LHM defs7–9			OC3	Slew3[3:0]				5Ah
1456	91							Phase4		LHM defs10–12			OC4	Slew4[3:0]				5Bh
1472	92	*CPFS0*	LED binning3					LED binning2						LED binning1				5Ch
1488	93	*CPFS1*	LED binning6					LED binning5						LED binning4				5Dh
1504	94	*CPFS2*	LED binning9					LED binning8						LED binning7				5Eh
1520	95	*CPFS3*	LED binning12					LED binning11						LED binning10				5Fh
1536	96	MTP lock key								MTP fail counter		Part netw.	SC timer	CAN speed		Multi-MLC	PWM freq	60h
1552	97	MTP Write Counter1[4]								Diode_Trim_Value[4]								61h

No. Bits	Block	MTP Registers (16 bits registers)[1][2]																Address
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1568	98	Free space (480-bits). User definable. User can write any information in this space.																62h
1584	99																	63h
1600	100																	64h
1616	101																	65h
1632	102																	66h
~																		~
2016	126																	7Eh
2032	127																	7Fh

[1] All cells are read/write unless specified otherwise
[2] All the values stored in the MTP start from the Most Significant bit (MSb) to the Less Significant Bit (LSb).
[3] These cells are used for internal MLC configuration. If the microcontroller tries to read or write in these cells, an error flag is raised (bits 2 and 3 of register 34h).
[4] Read only. If the microcontroller writes a value in this cell, the system does not raise an error flag, but also does not write any value in the cell.
[5] Any value has no impact in the MLC configuration. Write a 0 when a write message is sent.

The internal curves' coefficients have 13 bits each, because they are signed coefficients. If the user wants to program a negative coefficient, the first bit must be a logical 1. Negative coefficients are fully allowed and help to have all possible curves' shapes with a 3rd grade polynomial equation.

Note: Registers from 0x38h to 0x57h (curves coefficients) will not have any effect in the Direct PWM

14.1.1 Registers value selection criteria

Table 36. PWM frequency selection

Register	Bit D0	Frequency
60h	0	244 Hz (default)
	1	488 Hz

Table 37. Slew rate selection

Register	Bit D3	Bit D2	Bit D1	Bit D0	[V/µs]
58h (SR1) 59h (SR2) 5Ah (SR3) 5Bh (SR4)	0	0	0	0	0,2
	0	0	0	1	0,4
	0	0	1	0	0,6
	0	0	1	1	0,9
	0	1	0	0	1,1
	0	1	0	1	1,3
	0	1	1	0	1,5
	0	1	1	1	1,7 (default)
	1	0	0	0	1,9
	1	0	0	1	2,3
	1	0	1	0	2,8

Register	Bit D3	Bit D2	Bit D1	Bit D0	[V/µs]
	1	0	1	1	3,2
	1	1	0	0	3,8
	1	1	0	1	4,5
	1	1	1	0	5,5
	1	1	1	1	6,8

Table 38. Phase shifting sequence in the different floating blocks

Register	Block [bits] (switches)[1]	Conf_1	Conf_2	Default
58h (PS1) 59h (PS2) 5Ah (PS3) 5Bh (PS4)	Block 1 [8:9] (SW0 – SW3)	X	X	00
	Block 2 [8:9] (SW4 – SW7)	X	X	01
	Block 3 [8:9] (SW8 – SW11)	X	X	10
	Block 4 [8:9] (SW12 – SW15)	X	X	11

Conf_1	Conf_2	Channel / Phases
0	0	1, 2 and 3
0	1	4, 5 and 6
1	0	7, 8 and 9
1	1	10, 11 and 12

[1] When blocks are in parallel configuration, the phase shifting sequence must be the same, since both switches associated to the same light source must switch at the same time.

Table 39. Limp Home mode selection (58h, 59h, 5Ah and 5Bh)

Bits	LHx	Selection
7 to 5	0	LED OFF
	1	LED ON

Table 40. Short circuit timer (blanking time after duty cycle rising edge)

Register	Bit D4	Protocol
60h	0	16 µs (default)
	1	32 µs

Table 41. Data rate selection

Register	Bit D3	Bit D2	Data rate
60h	0	0	125 Kb/sec
	0	1	250 Kb/sec
	1	0	500 Kb/sec (default)

Register	Bit D3	Bit D2	Data rate
	1	1	1 Mb/sec

Table 42. Open circuit (OC) threshold selection (58h, 59h, 5Ah and 5Bh)

Bit	Bit D4	OC Threshold[1]
4	0	6 V ±1 V
	1	17 V ±1.5 V (default)

[1] When driving one LED, the default configuration should be used (6 V ±1 V), but if the switch is associated with a segment (more than one LED), the nondefault threshold should be selected (17 V ±1.5 V)

Table 43. System configuration. Single / Multiple MLC

Register	Bit D1	System configuration
60h	0	Single
	1	Multiple (default)

Table 44. Scaling factor selection (5Ch, 5Dh, 5Eh and 5Fh)

Bit D4	Bit D3	Bit D2	Bit D1	Bit D0	Value	Reduction Percentage (%)
0	0	0	0	0	0	0 (Default)
0	0	0	0	1	1	0.78
0	0	0	1	0	2	1.56
0	0	0	1	1	3	2.34
0	0	1	0	0	4	3.13
0	0	1	0	1	5	3.91
0	0	1	1	0	6	4.69
0	0	1	1	1	7	5.47
0	1	0	0	0	8	6.25
0	1	0	0	1	9	7.03
0	1	0	1	0	10	7.81
0	1	0	1	1	11	8.59
0	1	1	0	0	12	9.38
0	1	1	0	1	13	10.16
0	1	1	1	0	14	10.94
0	1	1	1	1	15	11.72
1	0	0	0	0	16	12.5
1	0	0	0	1	17	13.28
1	0	0	1	0	18	14.06

Bit D4	Bit D3	Bit D2	Bit D1	Bit D0	Value	Reduction Percentage (%)
1	0	0	1	1	19	14.84
1	0	1	0	0	20	15.63
1	0	1	0	1	21	16.41
1	0	1	1	0	22	17.19
1	0	1	1	1	23	17.97
1	1	0	0	0	24	18.75
1	1	0	0	1	25	19.53
1	1	0	1	0	26	20.31
1	1	0	1	1	27	21.09
1	1	1	0	0	28	21.88
1	1	1	0	1	29	22.66
1	1	1	1	0	30	23.44
1	1	1	1	1	31	24.22

Table 45. Overtemperature warning (OTW_x) threshold selection

Register	Bits	Temperature Threshold (Defaults)
58h	10 to 12	[100] - 140°C (OTW_0)
	13 to 15	[110] - 160°C (OTW_1)

Overtemperature Warning threshold selection (OTW_0 and OTW_1)									
3 bit register	000	001	010	011	100	101	110	111	Unit
Tj	100	110	120	130	140	150	160	170	[°C]

Note: *The overtemperature warning (OTW) measurement has an accuracy of ±10 °C.*

Table 46. Partial networking selection

Register	Bit D5	ON / OFF
60h	0	OFF (default)
	1	ON

15 Limiting values

Table 47. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter/Pin	Conditions	Min	Max	Unit
V_{max}	Maximum LED string voltage	With respect to ground – All blocks in series	–0.2	60	V
V_{block}	Maximum block voltage	Block of 3 switches	–0.2	57	V
V_{D-S}	Maximum Switch drain-source voltage	At zero current and normal operation	–0.2	19	V

Symbol	Parameter/Pin	Conditions	Min	Max	Unit
$I_{T(RMS)}$	Maximum RMS current per switch	ASL5x15yHz	–0.3	1.5	A
		ASL5x08yHz	–0.15	0.8	A
V_{CP}	CP pin	With respect to Ground	–0.2	72	V
V_{VMAX}	VMAX pin	With respect to ground	–0.2	60	V
V_{TXD}	Pin TXD	With respect to ground	–0.2	6	V
V_{RXD}	Pin RXD	With respect to ground	–0.2	6	V
V_{NTC}	Pin NTC	With respect to ground	–0.2	1.95	V
V_{ID}	Pin ID	With respect to ground	–0.2	1.95	V
V_{Ax}	Pins A0 to A4	With respect to ground	–0.2	6	V
V_{Vcc}	Pin VCC	With respect to ground	–0.2	6	V
V_{ICP}	Pin ICP	Not ground but must be connected to ground	–0.2	1.95	V
T_j	Junction temperature	—	–40	175	°C
T_{stg}	Storage temperature	—	–55	175	°C
T_{MTP}	MTP programming ambient temperature	MLC in MTP programming mode	0	40	°C
$N_{cy(W)MTP}$	Maximum MTP programming times	— Programming temperature between 0 and 40 °C	—	200	cycles
$V_{act(ov)ESD}$	Electrostatic discharge voltage (Component level)	HBM (at any pins)[1]	–2	2	KV
		CDM[2]	–500	500	V
		CDM Corner pins[3]	–750	750	V
	System Level[4][5]	ISO10605 SWx, and VCC pins with respect to GND and 270nF/50V capacitor attached to the pin. ID and NTC pins with respect to GND and 10nF capacitor + 3.3 V diode attached to the pin	–8	8	KV
		IEC61000-4-2 SWx, and VCC pins with respect to GND and 270nF/50V capacitor attached to the pin. ID and NTC pins with respect to GND and 10nF capacitor + 3.3 V diode attached to the pin	-6	6	KV

[1] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 KΩ).
[2] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).
[3] Only applicable for part numbers with HLQFP package.
[4] System level test at any pin that can be connected directly to ECU connector (IEC61000-4-2 & ISO10605). Switches pins and Vcc pin. Model for IEC61000-4-2: 330 Ω / 150 pF. Model for ISO10605: 2 kΩ / 150 pF (unpowered)
[5] System level test board reference schematic can be found in the application notes

16 Thermal characteristics

Table 48. Thermal characteristics

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-mb)}$	Thermal impedance junction to mounting base	HVQFN36	2.1	K/W
		HLQFP48	3.1	K/W

17 Static characteristics

Table 49. Static characteristics

In accordance with the Absolute Maximum Rating System (IEC 60134)

V_{CC} = 4.5 V to 5.5 V; T_j = −40 °C to +175 °C; all voltages are defined with respect to ground; positive currents flow into the IC.

Typical values are given at V_{CC} = 5 V; T_j = 25 °C unless otherwise specified

Symbol	Parameter/Pin	Conditions	Min	Typ	Max	Unit
R_{DSon}	Rdson per switch	ASL5x15yHz	—	100	200	mΩ
R_{DSon}	Rdson per switch	ASL5x08yHz	—	200	400	mΩ
R_{Bond}	Total bond wire resistance per individual block	ASL5x15yHz	—	—	100	mΩ
R_{Bond}	Total bond wire resistance per individual block	ASL5x08yHz	—	—	180	mΩ
$V_{th(det)load(oc)}$	LED Open Circuit detection level	MTP OC Bit = 0	5	6	7	V
		MTP OC Bit = 1	15.25	17	18.5	V
$V_{th(det)load(sc)}$	LED Short Circuit detection level	—	0.5	1	1.5	V
R_{PU}	Address pin (A0 to A4) pull up resistor (weak pull up resistor)	IO = 0	46	62	79	KΩ
$f_{osc(cp)}$	Charge pump frequency	—	4.5	5	5.5	MHz
$f_{osc(CAN)}$	CAN clock frequency	—	—	10	—	MHz
$t_{clk(CAN)}$	CAN clock time accuracy	Message cycle < 10 ms	—	0.25	—	%
$I_{en(NTC)}$	NTC enable current	—	412	440	468	µA
$I_{NTC(oc)}$	NTC open detection current	—	22.5	25	27.5	µA
$N_{res(ADC)}$	ADC resolution	—	—	—	9	bit
$N_{res(ADC-LSB)}$	ADC LSB resolution	—	—	1.1 / 511	—	V
$V_{th(det)load(oc)(NTC)}$	NTC open detection	25 µA	1.1	—	—	V
$I_{en(ID)}$	ID resistor current	—	22.5	25	27.5	µA
ΔV_{ID}	ID resistor ranges	ID = 000	79	—	160	mV
		ID = 001	160	—	242	mV
		ID = 010	242	—	320	mV
		ID = 011	320	—	396	mV

Symbol	Parameter/Pin	Conditions	Min	Typ	Max	Unit
		ID = 100	396	—	486	mV
		ID = 101	486	—	603	mV
		ID = 110	603	—	739	mV
		ID = 111	739	—	905	mV
$V_{th(det)load(sc)(ID)}$	ID resistor short state	—	0	—	80	mV
$V_{th(det)load(oc)(ID)}$	ID resistor open state	—	905	—	1100	mV
$N_{res(PWM)}$	PWM Resolution	Output	—	12	—	bits
		Internal	—	20	—	bits
$f_{data(CAN)}$	CAN data rate	MTP reg. 0x60h, bits 2-3 = 00	—	125	—	Kbps
$f_{data(CAN)}$	CAN data rate	MTP reg. 0x60h, bits 2-3 = 01	—	250	—	Kbps
$f_{data(CAN)}$	CAN data rate	MTP reg. 0x60h, bits 2-3 = 10	—	500	—	Kbps
$f_{data(CAN)}$	CAN data rate	MTP reg. 0x60h, bits 2-3 = 11	—	1000	—	Kbps
V_{VCC}	V_{CC} operational range	—	4.5	5	5.5	V
$V_{VCC(latch)reset}$	V_{CC} under voltage threshold	Threshold only used during Vcc ramp up	4	—	4.5	V
V_{IH}	I/O High level input voltage (TxD, Rxd, A0 – A4)	—	0.7 x V_{CC}	—	V_{CC} + 0.5	V
V_{IL}	I/O Low level input voltage (TxD, Rxd, A0 – A4)	—	–0.2	—	0.3 x V_{CC}	V
$I_{P(sleep)}$	Sleep mode supply current	V_{CC} = 5 V, MLC address = 11111 (31), Tj<125 °C	0.7	0.9	1.35	mA
C_{TXD}	TXD pin capacitance	— TXD1 and TXD2[1]	—	1.5	2	pF
C_{RXD}	RXD pin capacitance	RXD1 and RXD2[1]	—	1.5	2	pF
I_{CC}	MLC supply current	Vcc = 5 V, MLC address = 11111 (31), Charge pump idle. Tj = 150 °C	—	7.8	10	mA
I_{Cp}	Current consumption of the charge pump	Charge pump toggling with no switching. Tj = 150 °C. VCC = 5 V		0.3	0.36	mA
I_{CAN}	Current consumption due to full CAN communication			1		mA
IAx	Pins A0 to A4 current consumption	Pin grounded. Vcc = 5 V[2]	63	80	109	µA
VUVLO	Under voltage Lockout level	Threshold only used during Vcc ramp down	3.9	4.3	4.5	V
$V_{hys(det)uv}$	V_{CC} under voltage hysteresis	—	30	100	120	mV

Symbol	Parameter/Pin	Conditions	Min	Typ	Max	Unit
VVcc(start)	Vcc start up voltage (internal IPs enable threshold)[3]	—	3.3	3.7	4.1	V
$T_{JT(acc)}$	Junction temperature read accuracy	Measurement triggered by CAN command 63. MLC returns the internal diode voltage drop. The junction temperature must be calculated with the formula. See application notes.	-10		10	°C
$T_{OTW(acc)}$	Over Temperature Warning (OTW) accuracy	Flags in register 0x3Ah (bit 6 and 7)	-10		10	°C

[1] Guaranteed by design
[2] When the address pins (A0 to A4) are grounded to get the lowest MLC addresses, each pin current consumption must be added to the normal operation and sleep mode current.
[3] For detailed IC startup timing, check application notes "MLC Timing" section

18 Dynamic characteristics

Table 50. Dynamic characteristics

In accordance with the Absolute Maximum Rating System (IEC 60134)

V_{CC} = 4.5 V to 5.5 V; T_j = –40 °C to +175 °C; all voltages are defined with respect to ground; positive currents flow into the IC.

Typical values are given at V_{CC} = 5 V; T_j = 25 °C unless otherwise specified

Optional (must be used together with Static characteristics)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SR	Slew rate (programmable per block)	V_{CC} = 5 V	0.2	—	6.8	V/µs
f_{PWM}	Switch PWM frequency	MTP reg. 60h, bit 0 = 0	243.39	244	244.61	Hz
f_{PWM}	Switch PWM frequency	MTP reg. 60h, bit 0 = 1	486.78	488	489.22	Hz
tstartup	Start-Up time	Cap. between CP and VMAX = 22 nF	—	1.8	2	ms
Tphase	Phase shifting time	f_{PWM} = 244 Hz	—	256	—	µs
tdet(fail)	fail detection time	SC and OC	—	100	400	ns
tprog(MTP)	MTP Erase-Program process	Per line	5	—	10	ms
tread(MTP)	MTP Read time	Per line	—	1	—	µs
dPWM	PWM Duty Cycle	With 12-bit resolution	0	—	100	%
tdet(NTC)	NTC detection time	—	90	100	110	µs
tdet(NTC)(oc)	NTC open detection time	—	90	100	110	µs
tto(wd)	LHM watchdog time-out time	Setting 1	4.05	4.5	4.95	ms
		Setting 2	8.1	9	9.9	ms
		Setting 3	16.2	18	19.8	ms
		Setting 4	32.4	36	39.6	ms
		Setting 5	64.9	72.1	79.3	ms
		Setting 6	129.8	144.2	158.6	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Setting 7	259.5	288.4	317.3	ms
		Setting 8	519	576.7	634.4	ms

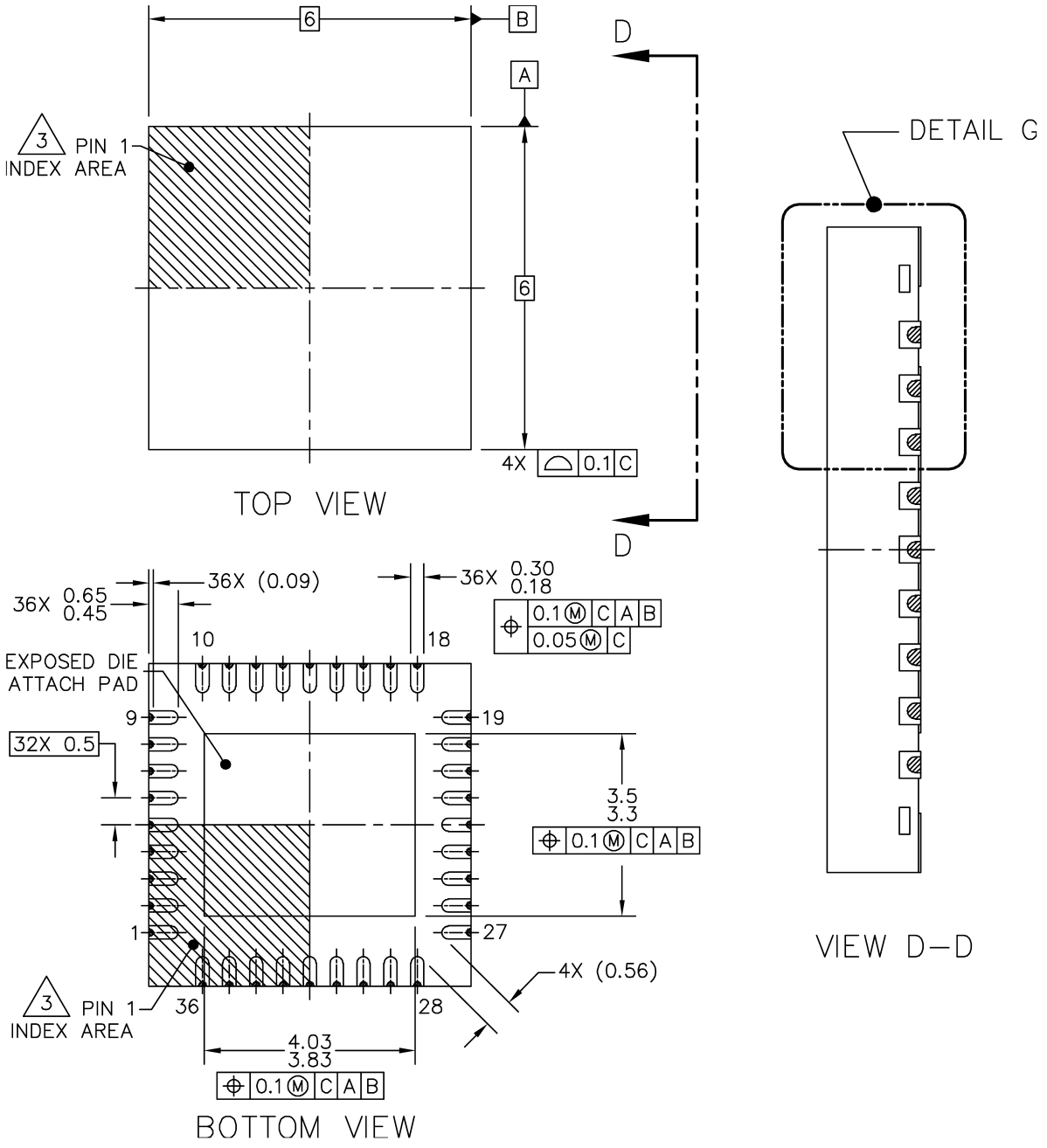
19 Packaging

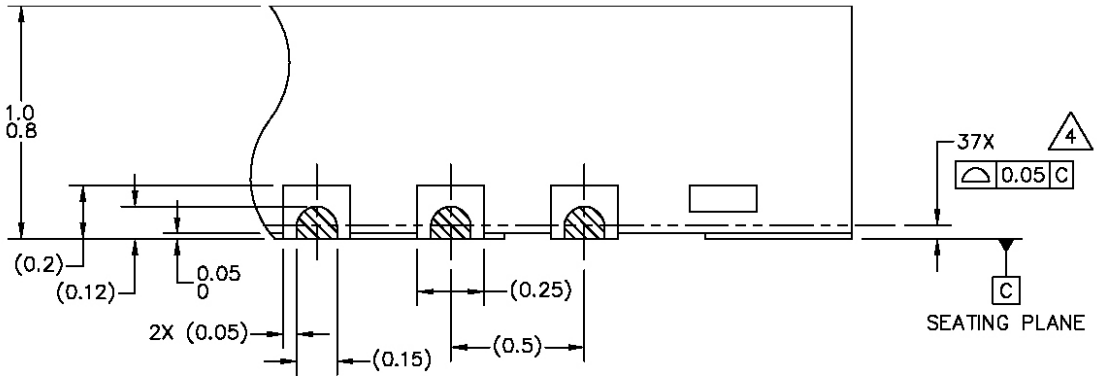
19.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

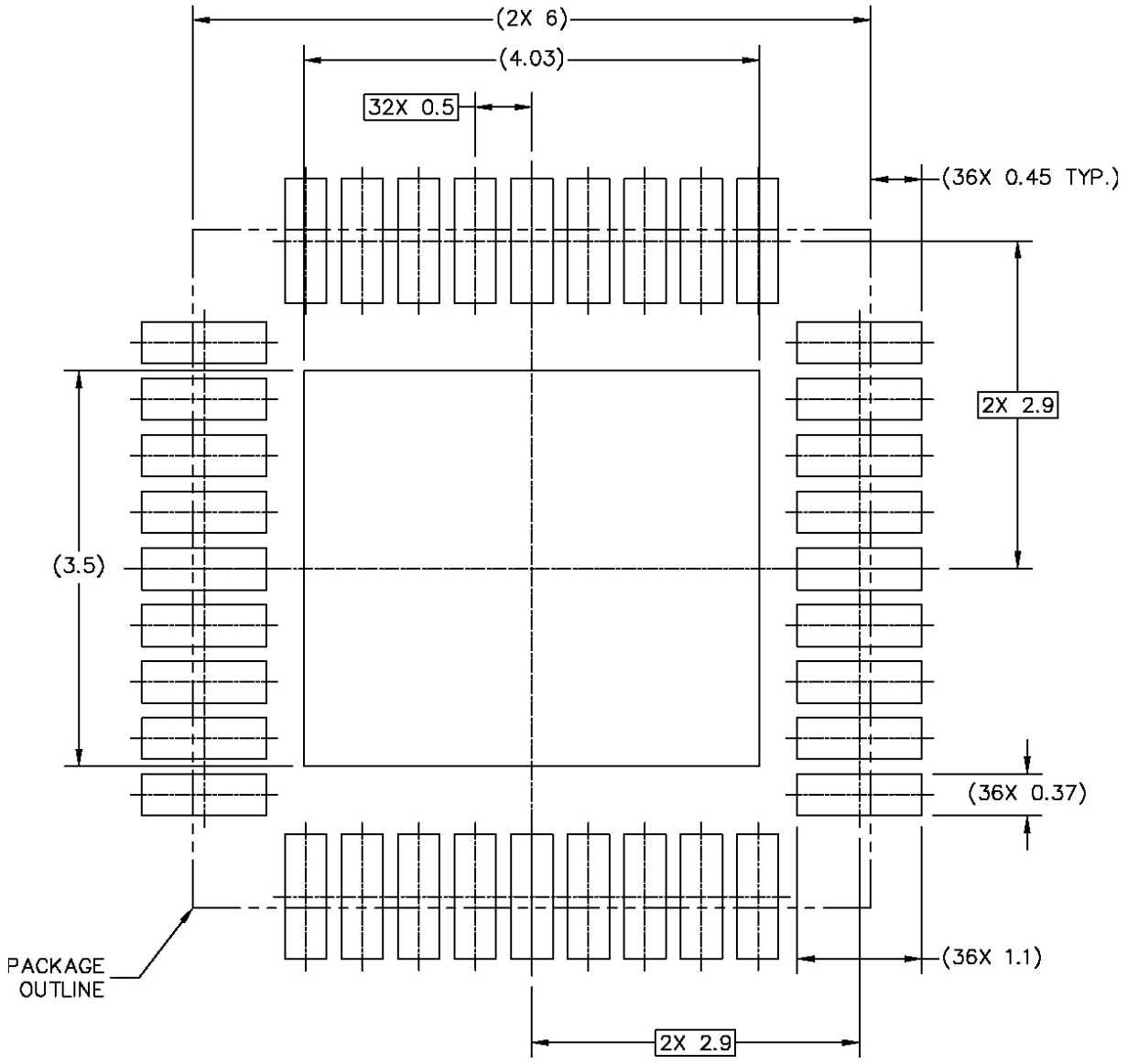
Table 51. Package Outline

Package	Package outline drawing number
36-pin HVQFN	SOT1092-4
48-pin HLQFP	SOT1571-1





DETAIL G
VIEW ROTATED 90° CW



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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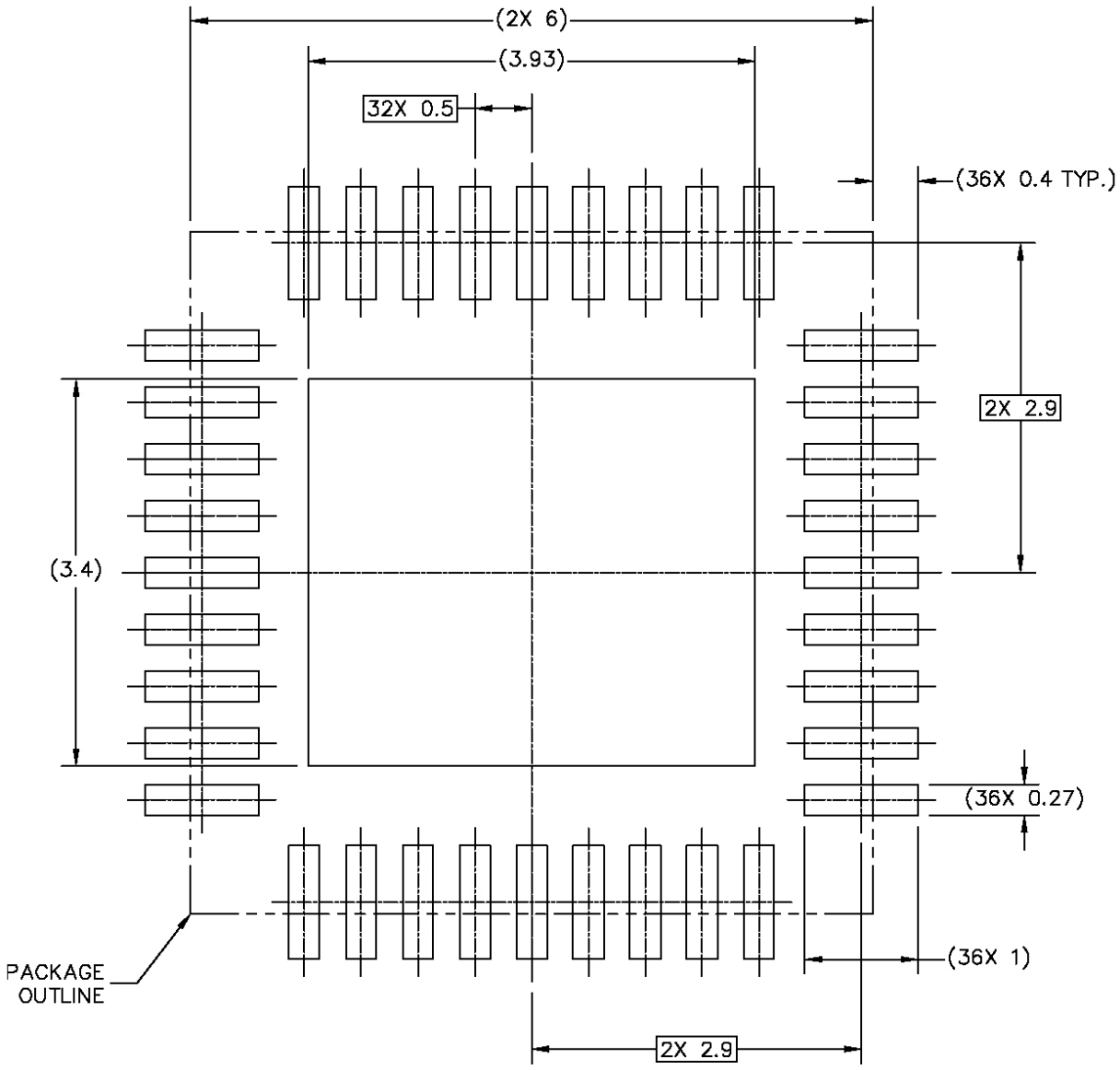

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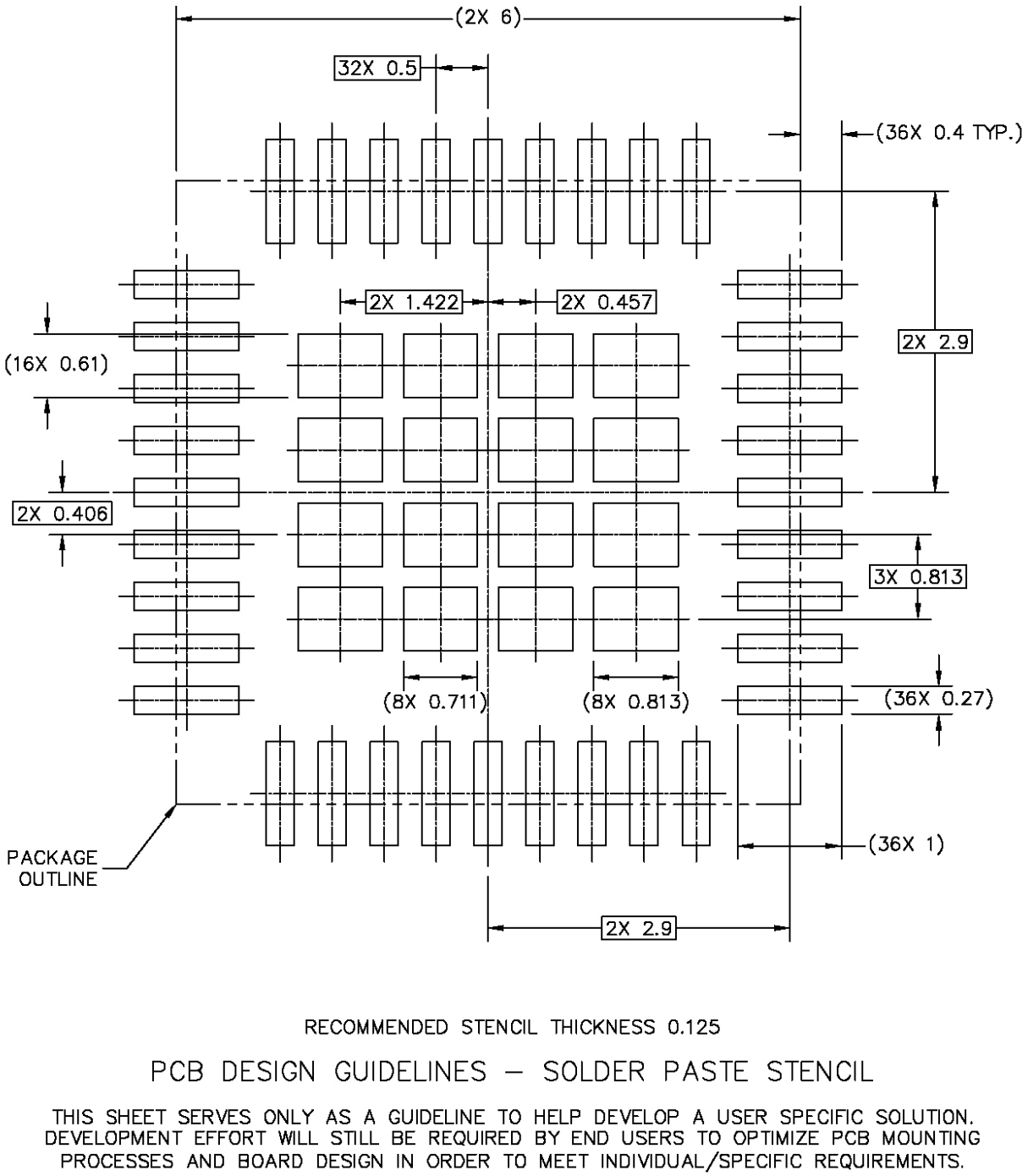
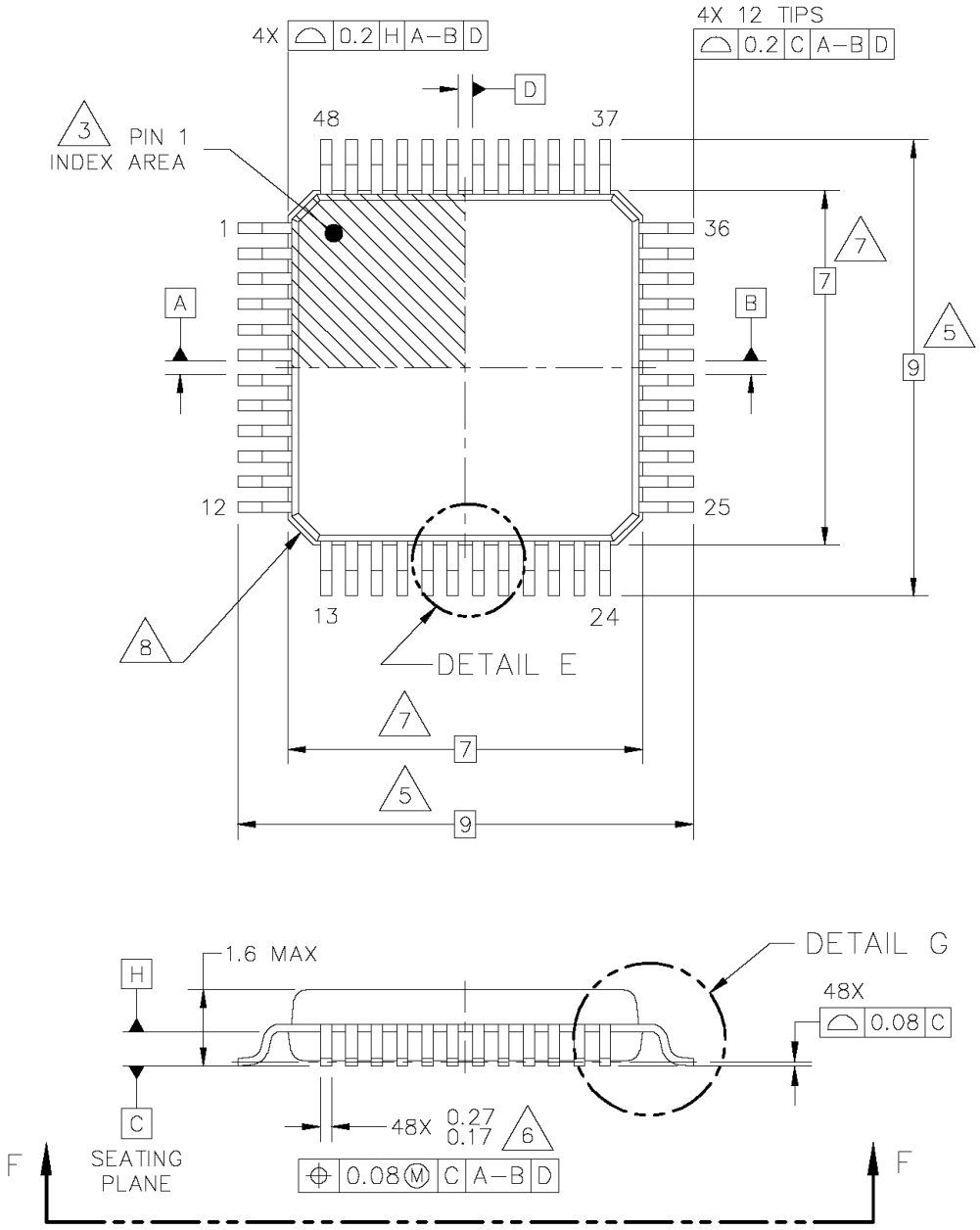
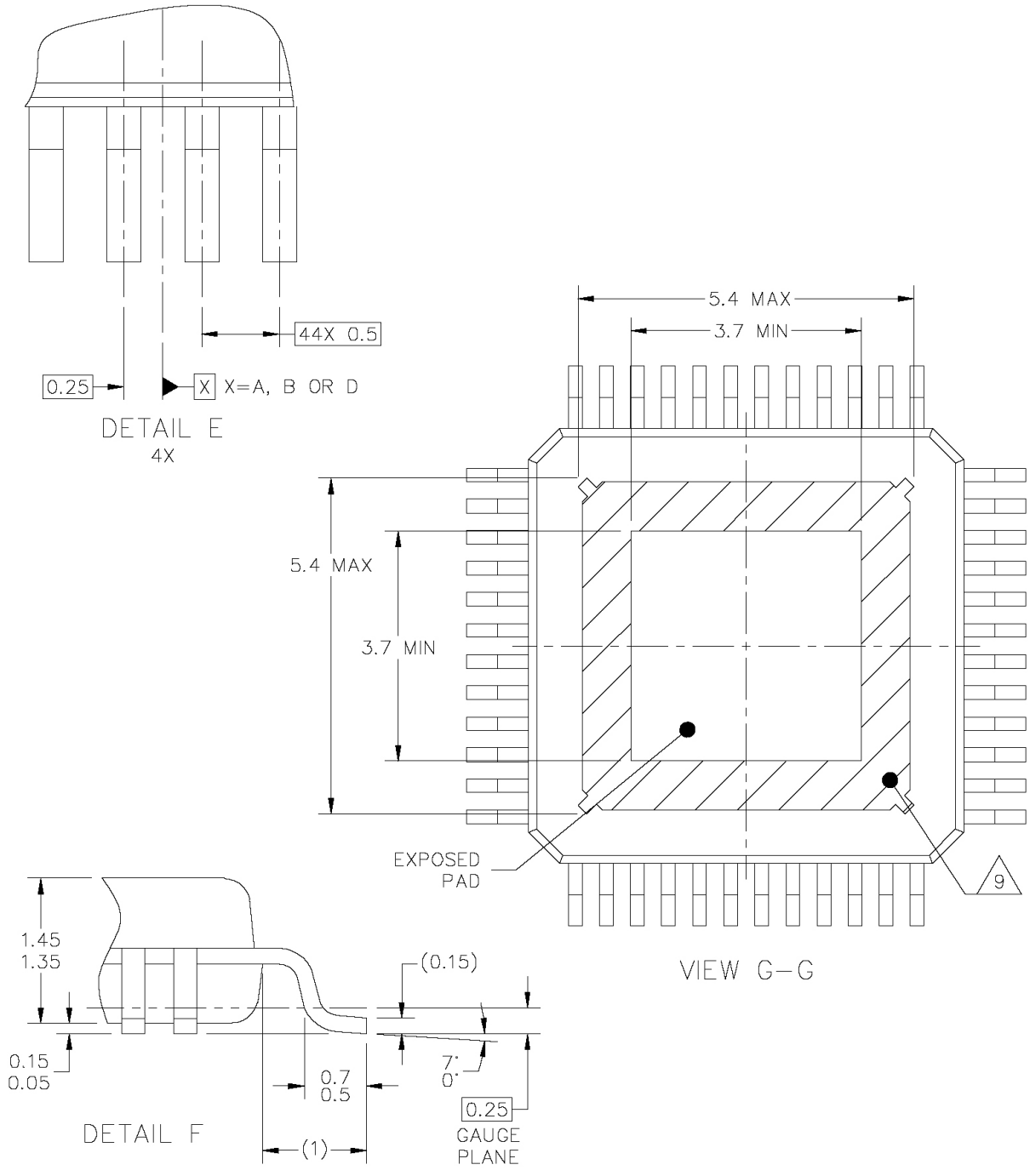
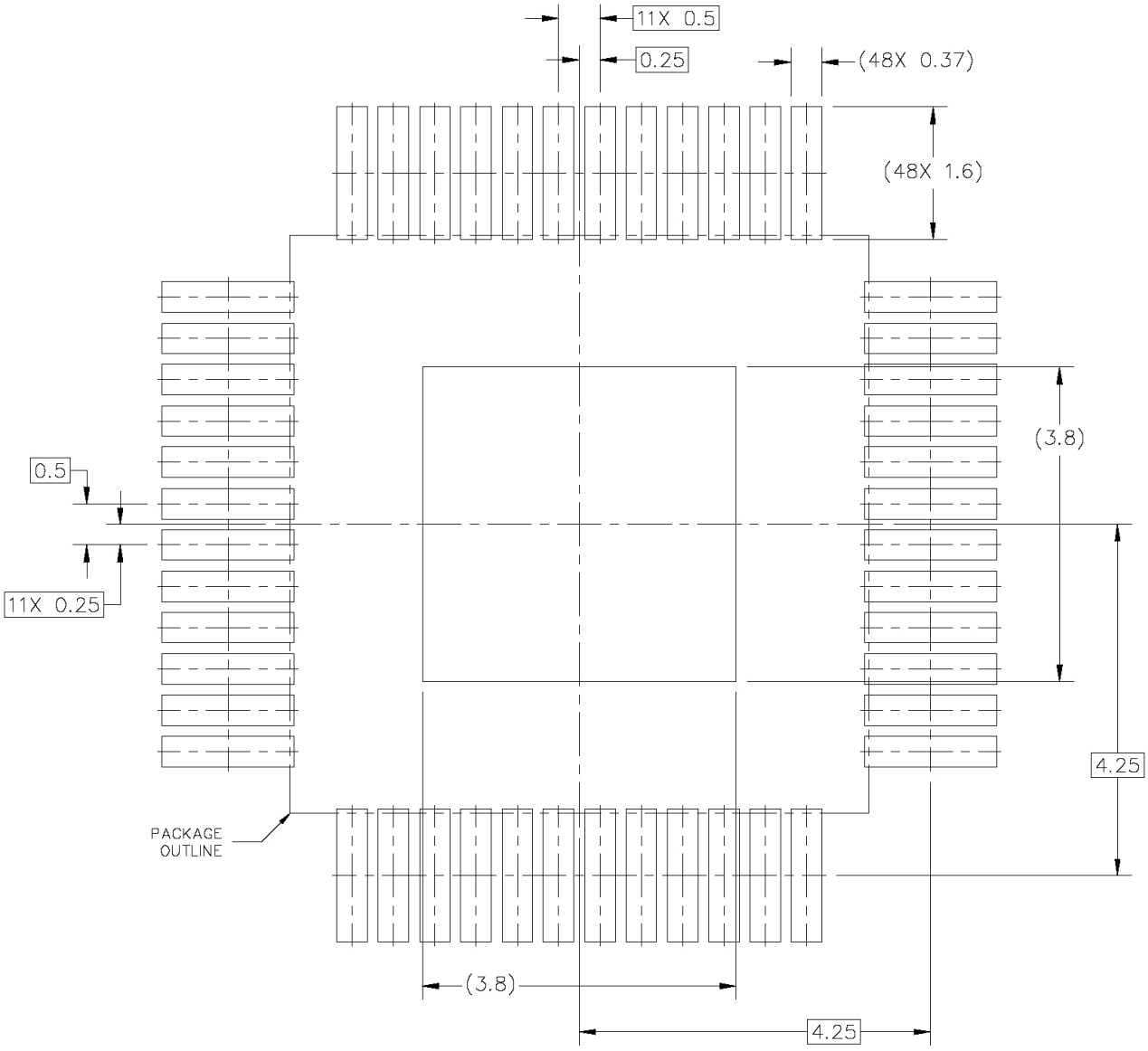


Figure 12. Package outline – HVQFN package







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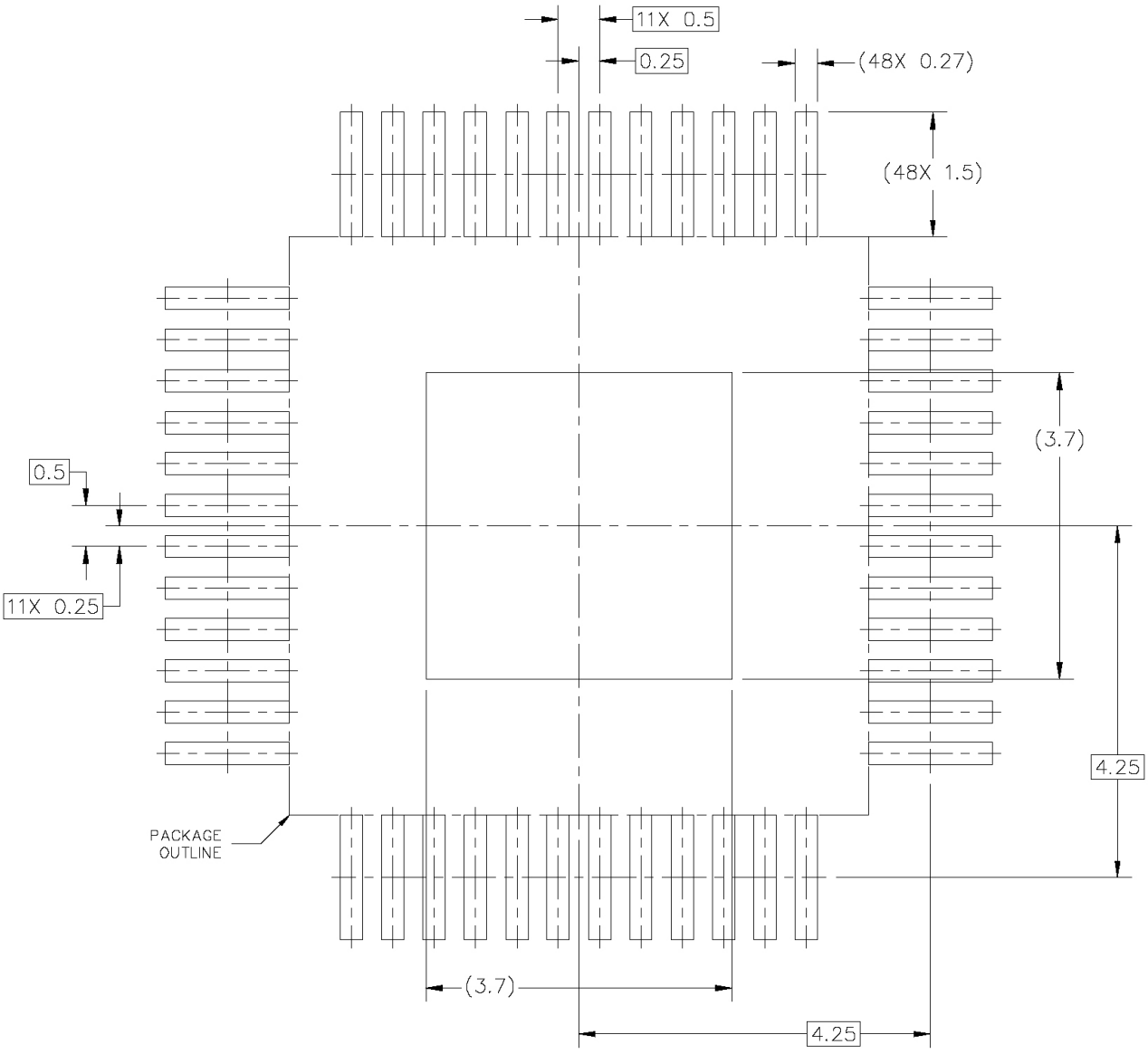

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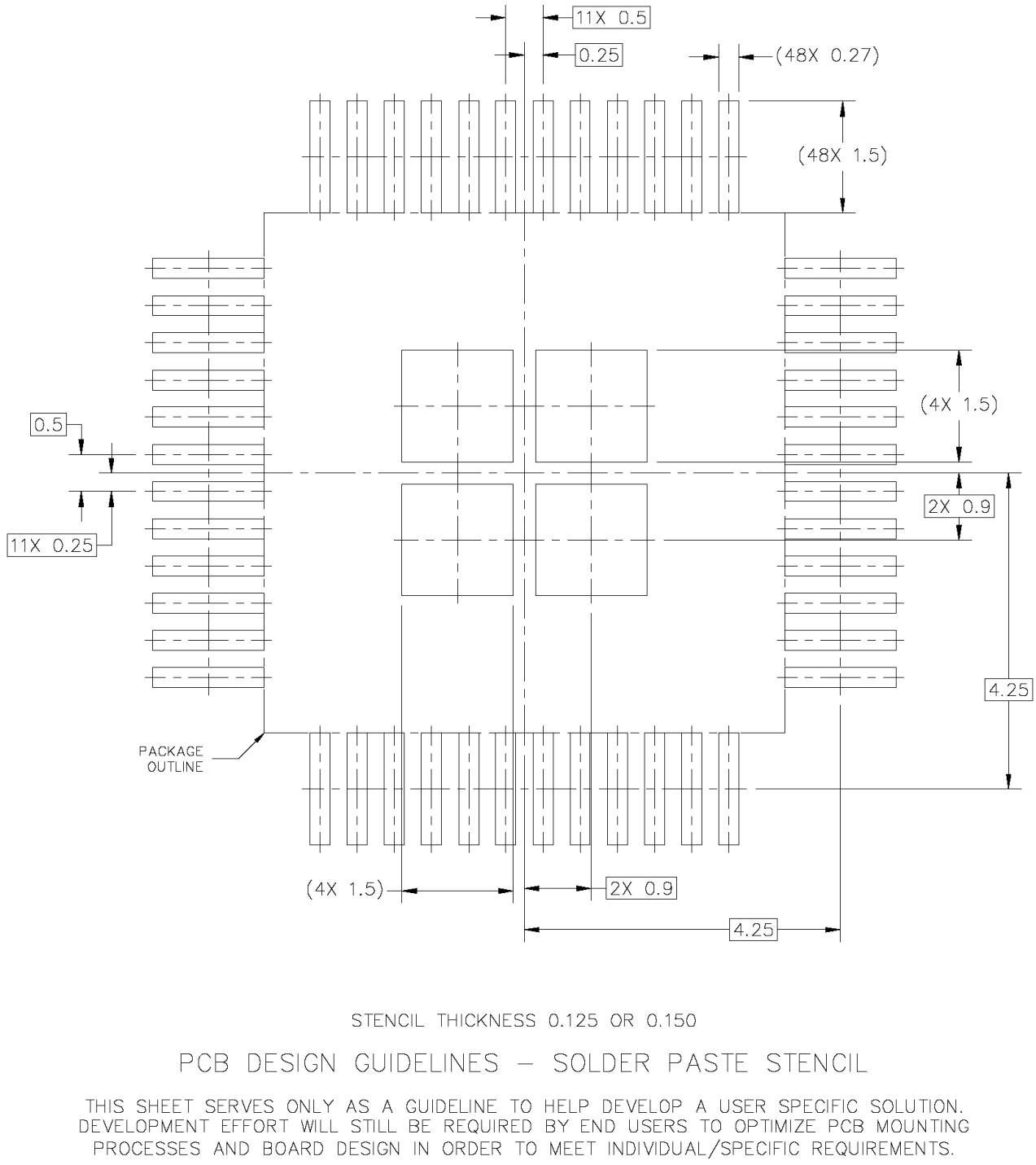

Figure 13. Package outline – HLQFP package

20 Revision history

Table 52. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ASL5xxxyHN v.1.1	20180829	Product	VUVLO change from 4.1 to 3.9 V $V_{VCC(latch)reset}$ change from 4.05 to 4 V AEC Q006 notation was added in general description section	—
ASL5xxxyHz v.2	20180907	Product	Integrates HLQFP48 part numbers Includes HLQFP48 package description, package thermal resistance, CDM corner pins (limiting values) and pinning information	ASL5xxxyHN v. 1.1
ASL5xxxyHz V.2.1	20190205	Product	VMAX was updated from 57 V to 60 V; Vvmax pin max rating value was updated from 57 V to 60 V; Vcp pin max rating value was updated from 69 V to 72 V	

21 Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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