

AM335x Sitara™ Processors

1 Device Overview

1.1 Features

- Up to 1-GHz Sitara™ ARM® Cortex®-A8 32-Bit RISC Processor
 - NEON™ SIMD Coprocessor
 - 32KB of L1 Instruction and 32KB of Data Cache With Single-Error Detection (Parity)
 - 256KB of L2 Cache With Error Correcting Code (ECC)
 - 176KB of On-Chip Boot ROM
 - 64KB of Dedicated RAM
 - Emulation and Debug - JTAG
 - Interrupt Controller (up to 128 Interrupt Requests)
- On-Chip Memory (Shared L3 RAM)
 - 64KB of General-Purpose On-Chip Memory Controller (OCMC) RAM
 - Accessible to All Masters
 - Supports Retention for Fast Wakeup
- External Memory Interfaces (EMIF)
 - mDDR(LPDDR), DDR2, DDR3, DDR3L Controller:
 - mDDR: 200-MHz Clock (400-MHz Data Rate)
 - DDR2: 266-MHz Clock (532-MHz Data Rate)
 - DDR3: 400-MHz Clock (800-MHz Data Rate)
 - DDR3L: 400-MHz Clock (800-MHz Data Rate)
 - 16-Bit Data Bus
 - 1GB of Total Addressable Space
 - Supports One x16 or Two x8 Memory Device Configurations
 - General-Purpose Memory Controller (GPMC)
 - Flexible 8-Bit and 16-Bit Asynchronous Memory Interface With up to Seven Chip Selects (NAND, NOR, Muxed-NOR, SRAM)
 - Uses BCH Code to Support 4-, 8-, or 16-Bit ECC
 - Uses Hamming Code to Support 1-Bit ECC
 - Error Locator Module (ELM)
 - Used in Conjunction With the GPMC to Locate Addresses of Data Errors from Syndrome Polynomials Generated Using a BCH Algorithm
 - Supports 4-, 8-, and 16-Bit per 512-Byte Block Error Location Based on BCH Algorithms
- Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)
 - Supports Protocols such as EtherCAT®, PROFIBUS, PROFINET, EtherNet/IP™, and More
- Two Programmable Real-Time Units (PRUs)
 - 32-Bit Load/Store RISC Processor Capable of Running at 200 MHz
 - 8KB of Instruction RAM With Single-Error Detection (Parity)
 - 8KB of Data RAM With Single-Error Detection (Parity)
 - Single-Cycle 32-Bit Multiplier With 64-Bit Accumulator
 - Enhanced GPIO Module Provides Shift-In/Out Support and Parallel Latch on External Signal
- 12KB of Shared RAM With Single-Error Detection (Parity)
- Three 120-Byte Register Banks Accessible by Each PRU
- Interrupt Controller (INTC) for Handling System Input Events
- Local Interconnect Bus for Connecting Internal and External Masters to the Resources Inside the PRU-ICSS
- Peripherals Inside the PRU-ICSS:
 - One UART Port With Flow Control Pins, Supports up to 12 Mbps
 - One Enhanced Capture (eCAP) Module
 - Two MII Ethernet Ports that Support Industrial Ethernet, such as EtherCAT
 - One MDIO Port
- Power, Reset, and Clock Management (PRCM) Module
 - Controls the Entry and Exit of Stand-By and Deep-Sleep Modes
 - Responsible for Sleep Sequencing, Power Domain Switch-Off Sequencing, Wake-Up Sequencing, and Power Domain Switch-On Sequencing
- Clocks
 - Integrated 15- to 35-MHz High-Frequency Oscillator Used to Generate a Reference Clock for Various System and Peripheral Clocks
 - Supports Individual Clock Enable and Disable Control for Subsystems and Peripherals to Facilitate Reduced Power Consumption
 - Five ADPLLs to Generate System Clocks (MPU Subsystem, DDR Interface, USB and



- Peripherals [MMC and SD, UART, SPI, I²C], L3, L4, Ethernet, GFX [SGX530], LCD Pixel Clock)
 - Power
 - Two Nonswitchable Power Domains (Real-Time Clock [RTC], Wake-Up Logic [WAKEUP])
 - Three Switchable Power Domains (MPU Subsystem [MPU], SGX530 [GFX], Peripherals and Infrastructure [PER])
 - Implements SmartReflex™ Class 2B for Core Voltage Scaling Based On Die Temperature, Process Variation, and Performance (Adaptive Voltage Scaling [AVS])
 - Dynamic Voltage Frequency Scaling (DVFS)
- Real-Time Clock (RTC)
 - Real-Time Date (Day-Month-Year-Day of Week) and Time (Hours-Minutes-Seconds) Information
 - Internal 32.768-kHz Oscillator, RTC Logic and 1.1-V Internal LDO
 - Independent Power-on-Reset (RTC_PWRONRSTn) Input
 - Dedicated Input Pin (EXT_WAKEUP) for External Wake Events
 - Programmable Alarm Can be Used to Generate Internal Interrupts to the PRCM (for Wakeup) or Cortex-A8 (for Event Notification)
 - Programmable Alarm Can be Used With External Output (PMIC_POWER_EN) to Enable the Power Management IC to Restore Non-RTC Power Domains
- Peripherals
 - Up to Two USB 2.0 High-Speed OTG Ports With Integrated PHY
 - Up to Two Industrial Gigabit Ethernet MACs (10, 100, 1000 Mbps)
 - Integrated Switch
 - Each MAC Supports MII, RMII, RGMII, and MDIO Interfaces
 - Ethernet MACs and Switch Can Operate Independent of Other Functions
 - IEEE 1588v2 Precision Time Protocol (PTP)
 - Up to Two Controller-Area Network (CAN) Ports
 - Supports CAN Version 2 Parts A and B
 - Up to Two Multichannel Audio Serial Ports (McASPs)
 - Transmit and Receive Clocks up to 50 MHz
 - Up to Four Serial Data Pins per McASP Port With Independent TX and RX Clocks
 - Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and Similar Formats
 - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
 - FIFO Buffers for Transmit and Receive (256 Bytes)
 - Up to Six UARTs
 - All UARTs Support IrDA and CIR Modes
 - All UARTs Support RTS and CTS Flow Control
 - UART1 Supports Full Modem Control
 - Up to Two Master and Slave McSPI Serial Interfaces
 - Up to Two Chip Selects
 - Up to 48 MHz
 - Up to Three MMC, SD, SDIO Ports
 - 1-, 4- and 8-Bit MMC, SD, SDIO Modes
 - MMCSD0 has Dedicated Power Rail for 1.8-V or 3.3-V Operation
 - Up to 48-MHz Data Transfer Rate
 - Supports Card Detect and Write Protect
 - Complies With MMC4.3, SD, SDIO 2.0 Specifications
 - Up to Three I²C Master and Slave Interfaces
 - Standard Mode (up to 100 kHz)
 - Fast Mode (up to 400 kHz)
 - Up to Four Banks of General-Purpose I/O (GPIO) Pins
 - 32 GPIO Pins per Bank (Multiplexed With Other Functional Pins)
 - GPIO Pins Can be Used as Interrupt Inputs (up to Two Interrupt Inputs per Bank)
 - Up to Three External DMA Event Inputs that can Also be Used as Interrupt Inputs
 - Eight 32-Bit General-Purpose Timers
 - DMTIMER1 is a 1-ms Timer Used for Operating System (OS) Ticks
 - DMTIMER4–DMTIMER7 are Pinned Out
 - One Watchdog Timer
 - SGX530 3D Graphics Engine
 - Tile-Based Architecture Delivering up to 20 Million Polygons per Second
 - Universal Scalable Shader Engine (USSE) is a Multithreaded Engine Incorporating Pixel and Vertex Shader Functionality
 - Advanced Shader Feature Set in Excess of Microsoft VS3.0, PS3.0, and OGL2.0
 - Industry Standard API Support of Direct3D Mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0, and OpenMax
 - Fine-Grained Task Switching, Load Balancing, and Power Management
 - Advanced Geometry DMA-Driven Operation for Minimum CPU Interaction

- Programmable High-Quality Image Anti-Aliasing
- Fully Virtualized Memory Addressing for OS Operation in a Unified Memory Architecture
- LCD Controller
 - Up to 24-Bit Data Output; 8 Bits per Pixel (RGB)
 - Resolution up to 2048 x 2048 (With Maximum 126-MHz Pixel Clock)
 - Integrated LCD Interface Display Driver (LIDD) Controller
 - Integrated Raster Controller
 - Integrated DMA Engine to Pull Data from the External Frame Buffer Without Burdening the Processor via Interrupts or a Firmware Timer
 - 512-Word Deep Internal FIFO
 - Supported Display Types:
 - Character Displays - Uses LIDD Controller to Program these Displays
 - Passive Matrix LCD Displays - Uses LCD Raster Display Controller to Provide Timing and Data for Constant Graphics Refresh to a Passive Display
 - Active Matrix LCD Displays - Uses External Frame Buffer Space and the Internal DMA Engine to Drive Streaming Data to the Panel
- 12-Bit Successive Approximation Register (SAR) ADC
 - 200K Samples per Second
 - Input can be Selected from any of the Eight Analog Inputs Multiplexed Through an 8:1 Analog Switch
 - Can be Configured to Operate as a 4-Wire, 5-Wire, or 8-Wire Resistive Touch Screen Controller (TSC) Interface
- Up to Three 32-Bit eCAP Modules
 - Configurable as Three Capture Inputs or Three Auxiliary PWM Outputs
- Up to Three Enhanced High-Resolution PWM Modules (eHRPWMs)
 - Dedicated 16-Bit Time-Base Counter With Time and Frequency Controls
 - Configurable as Six Single-Ended, Six Dual-Edge Symmetric, or Three Dual-Edge Asymmetric Outputs
- Up to Three 32-Bit Enhanced Quadrature Encoder Pulse (eQEP) Modules
- Device Identification
 - Contains Electrical Fuse Farm (FuseFarm) of Which Some Bits are Factory Programmable
 - Production ID
 - Device Part Number (Unique JTAG ID)
 - Device Revision (Readable by Host ARM)
- Debug Interface Support
 - JTAG and cJTAG for ARM (Cortex-A8 and PRCM), PRU-ICSS Debug
 - Supports Device Boundary Scan
 - Supports IEEE 1500
- DMA
 - On-Chip Enhanced DMA Controller (EDMA) has Three Third-Party Transfer Controllers (TPTCs) and One Third-Party Channel Controller (TPCC), Which Supports up to 64 Programmable Logical Channels and Eight QDMA Channels. EDMA is Used for:
 - Transfers to and from On-Chip Memories
 - Transfers to and from External Storage (EMIF, GPMC, Slave Peripherals)
- Inter-Processor Communication (IPC)
 - Integrates Hardware-Based Mailbox for IPC and Spinlock for Process Synchronization Between Cortex-A8, PRCM, and PRU-ICSS
 - Mailbox Registers that Generate Interrupts
 - Four Initiators (Cortex-A8, PRCM, PRU0, PRU1)
 - Spinlock has 128 Software-Assigned Lock Registers
- Security
 - Crypto Hardware Accelerators (AES, SHA, RNG)
 - Secure Boot
- Boot Modes
 - Boot Mode is Selected Through Boot Configuration Pins Latched on the Rising Edge of the PWRONRSTn Reset Input Pin
- Packages:
 - 298-Pin S-PBGA-N298 Via Channel Package (ZCE Suffix), 0.65-mm Ball Pitch
 - 324-Pin S-PBGA-N324 Package (ZCZ Suffix), 0.80-mm Ball Pitch

1.2 Applications

- Gaming Peripherals
- Home and Industrial Automation
- Consumer Medical Appliances
- Printers
- Smart Toll Systems
- Connected Vending Machines
- Weighing Scales
- Educational Consoles
- Advanced Toys

1.3 Description

The AM335x microprocessors, based on the ARM Cortex-A8 processor, are enhanced with image, graphics processing, peripherals and industrial interface options such as EtherCAT and PROFIBUS. The devices support high-level operating systems (HLOS). Linux[®] and Android[™] are available free of charge from TI.

The AM335x microprocessor contains the subsystems shown in the [Functional Block Diagram](#) and a brief description of each follows:

The contains the subsystems shown in the [Functional Block Diagram](#) and a brief description of each follows:

The microprocessor unit (MPU) subsystem is based on the ARM Cortex-A8 processor and the PowerVR SGX[™] Graphics Accelerator subsystem provides 3D graphics acceleration to support display and gaming effects.

The PRU-ICSS is separate from the ARM core, allowing independent operation and clocking for greater efficiency and flexibility. The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos, and others. Additionally, the programmable nature of the PRU-ICSS, along with its access to pins, events and all system-on-chip (SoC) resources, provides flexibility in implementing fast, real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of SoC.

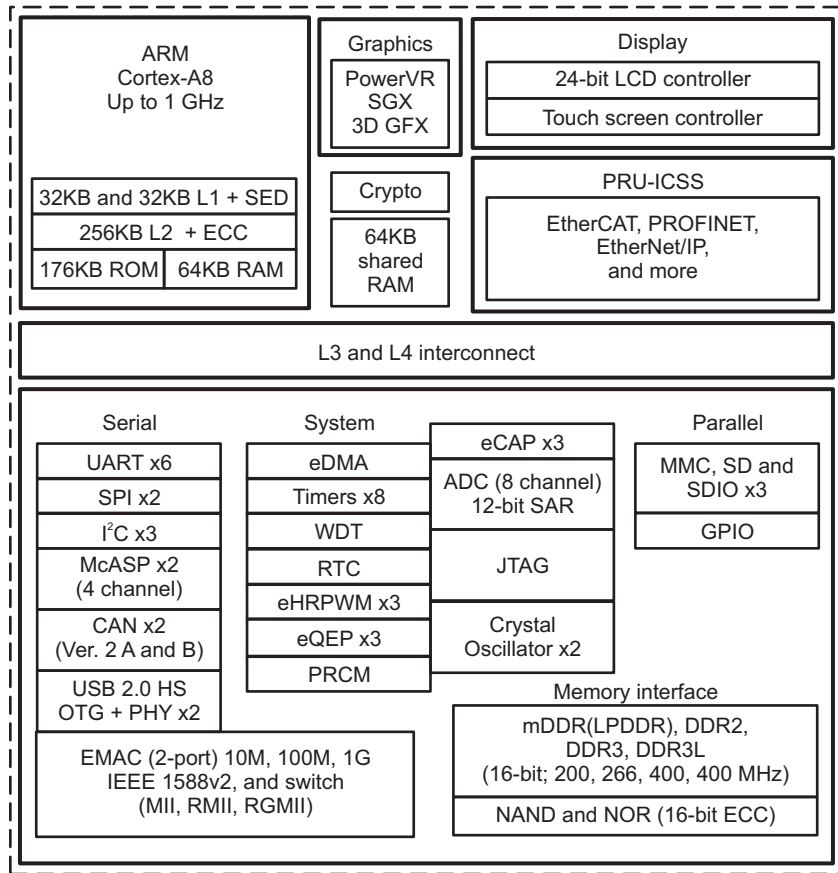
Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE |
|----------------------|--------------------------|--------------------------------------|
| AM3359ZCZ | NFBGA (324) | 15.0 mm × 15.0 mm |
| AM3358ZCZ | NFBGA (324) | 15.0 mm × 15.0 mm |
| AM3357ZCZ | NFBGA (324) | 15.0 mm × 15.0 mm |
| AM3356ZCZ, AM3356ZCE | NFBGA (324), NFBGA (298) | 15.0 mm × 15.0 mm, 13.0 mm × 13.0 mm |
| AM3354ZCZ, AM3354ZCE | NFBGA (324), NFBGA (298) | 15.0 mm × 15.0 mm, 13.0 mm × 13.0 mm |
| AM3352ZCZ, AM3352ZCE | NFBGA (324), NFBGA (298) | 15.0 mm × 15.0 mm, 13.0 mm × 13.0 mm |
| AM3351ZCE | NFBGA (298) | 13.0 mm × 13.0 mm |

(1) For more information, see [Section 9, Mechanical, Packaging, and Orderable Information](#).

1.4 Functional Block Diagram

Figure 1-1 shows the AM335x microprocessor functional block diagram.



Copyright © 2016, Texas Instruments Incorporated

Figure 1-1. AM335x Functional Block Diagram

Table of Contents

| | | | | | |
|----------|---|----------------------------|----------|---|----------------------------|
| 1 | Device Overview | 1 | 7.2 | Recommended Clock and Control Signal Transition Behavior | 115 |
| 1.1 | Features | 1 | 7.3 | OPP50 Support | 115 |
| 1.2 | Applications | 4 | 7.4 | Controller Area Network (CAN) | 116 |
| 1.3 | Description | 4 | 7.5 | DMTimer | 117 |
| 1.4 | Functional Block Diagram | 5 | 7.6 | Ethernet Media Access Controller (EMAC) and Switch | 118 |
| 2 | Revision History | 7 | 7.7 | External Memory Interfaces | 126 |
| 3 | Device Comparison | 8 | 7.8 | I ² C | 189 |
| 3.1 | Related Products | 9 | 7.9 | JTAG Electrical Data and Timing | 191 |
| 4 | Terminal Configuration and Functions | 10 | 7.10 | LCD Controller (LCDC) | 192 |
| 4.1 | Pin Diagram | 10 | 7.11 | Multichannel Audio Serial Port (McASP) | 208 |
| 4.2 | Pin Attributes | 18 | 7.12 | Multichannel Serial Port Interface (McSPI) | 213 |
| 4.3 | Signal Descriptions | 50 | 7.13 | Multimedia Card (MMC) Interface | 219 |
| 5 | Specifications | 79 | 7.14 | Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) | 222 |
| 5.1 | Absolute Maximum Ratings | 79 | 7.15 | Universal Asynchronous Receiver Transmitter (UART) | 231 |
| 5.2 | ESD Ratings | 80 | 8 | Device and Documentation Support | 234 |
| 5.3 | Power-On Hours (POH) | 81 | 8.1 | Device Nomenclature | 234 |
| 5.4 | Operating Performance Points (OPPs) | 81 | 8.2 | Tools and Software | 235 |
| 5.5 | Recommended Operating Conditions | 84 | 8.3 | Documentation Support | 239 |
| 5.6 | Power Consumption Summary | 86 | 8.4 | Related Links | 242 |
| 5.7 | DC Electrical Characteristics | 88 | 8.5 | Community Resources | 242 |
| 5.8 | Thermal Resistance Characteristics for ZCE and ZCZ Packages | 92 | 8.6 | Trademarks | 243 |
| 5.9 | External Capacitors | 93 | 8.7 | Electrostatic Discharge Caution | 243 |
| 5.10 | Touch Screen Controller and Analog-to-Digital Subsystem Electrical Parameters | 96 | 8.8 | Glossary | 243 |
| 6 | Power and Clocking | 98 | 9 | Mechanical, Packaging, and Orderable Information | 244 |
| 6.1 | Power Supplies | 98 | 9.1 | Via Channel | 244 |
| 6.2 | Clock Specifications | 106 | 9.2 | Packaging Information | 244 |
| 7 | Peripheral Information and Timings | 115 | | | |
| 7.1 | Parameter Information | 115 | | | |

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision I (December 2015) to Revision J | Page |
|--|---------------------|
| • Added Secure boot to Security feature list | 3 |
| • Added extended temperature range for the AM3351 device in Table 3-1 | 8 |
| • Added Section 3.1 , Related Products | 9 |
| • Reformatted and added content to Section 8 , Device and Documentation Support..... | 234 |

3 Device Comparison

Table 3-1 lists the features supported across different AM335x devices.

Table 3-1. Device Features Comparison

| FUNCTION | AM3351 | AM3352 | AM3354 | AM3356 | AM3357 | AM3358 | AM3359 |
|---|--|--|--|---|---|---|---|
| ARM Cortex-A8 | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Frequency ⁽¹⁾ | 300 MHz 600 MHz | 300 MHz 600 MHz 800 MHz 1000 MHz | 600 MHz 800 MHz 1000 MHz | 300 MHz 600 MHz 800 MHz | 300 MHz 600 MHz 800 MHz | 600 MHz 800 MHz 1000 MHz | 600 MHz 800 MHz |
| MIPS ⁽²⁾ | 600 1200 | 600 1200 1600 2000 | 1200 1600 2000 | 600 1200 1600 | 600 1200 1600 | 1200 1600 2000 | 1200 1600 |
| On-chip L1 cache | 64KB | 64KB | 64KB | 64KB | 64KB | 64KB | 64KB |
| On-chip L2 cache | 256KB | 256KB | 256KB | 256KB | 256KB | 256KB | 256KB |
| Graphics accelerator (SGX530) | — | — | 3D | — | — | 3D | 3D |
| Hardware acceleration | Crypto accelerator | Crypto accelerator | Crypto accelerator | Crypto accelerator | Crypto accelerator | Crypto accelerator | Crypto accelerator |
| Programmable real-time unit subsystem and industrial communication subsystem (PRU-ICSS) | — | — | — | Features including basic Industrial protocols; ZCE: Limited PRU I/Os pinned out | Features including all Industrial protocols | Features including basic Industrial protocols | Features including all Industrial protocols |
| On-chip memory | 128KB | 128KB | 128KB | 128KB | 128KB | 128KB | 128KB |
| Display options | LCD | LCD | LCD | LCD | LCD | LCD | LCD |
| General-purpose memory | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) |
| DRAM ⁽³⁾ | 1 16-bit (LPDDR-400, DDR2-532, DDR3-800) | 1 16-bit (LPDDR-400, DDR2-532, DDR3-800) | 1 16-bit (LPDDR-400, DDR2-532, DDR3-800) | 1 16-bit (LPDDR-400, DDR2-532, DDR3-800) | 1 16-bit (LPDDR-400, DDR2-532, DDR3-800) | 1 16-bit (LPDDR-400, DDR2-532, DDR3-800) | 1 16-bit (LPDDR-400, DDR2-532, DDR3-800) |
| Universal serial bus (USB) | ZCE: 1 port | ZCE: 1 port ZCZ: 2 ports | ZCE: 1 port ZCZ: 2 ports | ZCE: 1 port ZCZ: 2 ports | No ZCE Available ZCZ: 2 ports | No ZCE Available ZCZ: 2 ports | No ZCE Available ZCZ: 2 ports |
| Ethernet media access controller (EMAC) with 2-port switch | 10/100/1000 ZCE: 1 port | 10/100/1000 ZCE: 1 port ZCZ: 2 ports | 10/100/1000 ZCE: 1 port ZCZ: 2 ports | 10/100/1000 ZCE: 1 port ZCZ: 2 ports | 10/100/1000 No ZCE Available ZCZ: 2 ports | 10/100/1000 No ZCE Available ZCZ: 2 ports | 10/100/1000 No ZCE Available ZCZ: 2 ports |
| Multimedia card (MMC) | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Controller-area network (CAN) | — | 2 | 2 | 2 | 2 | 2 | 2 |
| Universal asynchronous receiver and transmitter (UART) | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| Analog-to-digital converter (ADC) | 8-ch 12-bit | 8-ch 12-bit | 8-ch 12-bit | 8-ch 12-bit | 8-ch 12-bit | 8-ch 12-bit | 8-ch 12-bit |
| Enhanced high-resolution PWM modules (eHRPWM) | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Enhanced capture modules (eCAP) | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Enhanced quadrature encoder pulse (eQEP) | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Real-time clock (RTC) | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Inter-integrated circuit (I ² C) | 3 | 3 | 3 | 3 | 3 | 3 | 3 |

Table 3-1. Device Features Comparison (continued)

| FUNCTION | AM3351 | AM3352 | AM3354 | AM3356 | AM3357 | AM3358 | AM3359 |
|--|---------------------------|---|--|--|-----------------------------|--|-----------------------------|
| Multichannel audio serial port (McASP) | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Multichannel serial port interface (McSPI) | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Enhanced direct memory access (EDMA) | 64-Ch | 64-Ch | 64-Ch | 64-Ch | 64-Ch | 64-Ch | 64-Ch |
| Input/output (I/O) supply | 1.8 V, 3.3 V | 1.8 V, 3.3 V | 1.8 V, 3.3 V | 1.8 V, 3.3 V | 1.8 V, 3.3 V | 1.8 V, 3.3 V | 1.8 V, 3.3 V |
| Operating temperature range | 0 to 90°C –40 to 105°C | –40 to 125°C ⁽⁴⁾ –40 to 105°C –40 to 90°C 0 to 90°C | –40 to 105°C –40 to 90°C 0 to 90°C | –40 to 105°C –40 to 90°C 0 to 90°C | –40 to 105°C –40 to 90°C | –40 to 105°C –40 to 90°C 0 to 90°C | –40 to 105°C –40 to 90°C |

(1) Frequencies listed correspond to silicon revision 2.x. Earlier silicon revisions support 275 MHz, 500 MHz, 600 MHz, and 720 MHz.

(2) MIPS listed correspond to silicon revision 2.x. Earlier silicon revisions support 560, 1000, 1200, and 1440.

(3) DRAM speeds listed are data rates.

(4) Industrial extended temperature only supported for 300-MHz and 600-MHz frequencies.

3.1 Related Products

For information about other devices in this family of products, see the following links:

Sitara Processors Scalable processors based on ARM Cortex-A cores with flexible peripherals, connectivity and unified software support – perfect for sensors to servers.

TI's ARM Cortex-A8 Advantage The ARM Cortex-A8 core is highly-optimized by ARM for performance and power efficiency. With the ability to scale in speed from 300 MHz to 1.35 GHz, the ARM Cortex-A8-based processor can meet the requirements for power optimized devices with a power budget of less than the Cortex-A8 core a dual-issue superscalar, achieving twice the instructions executed per clock cycle at 2 DMIPS/MHz.

AM335x Sitara Processors Scalable ARM Cortex-A8-based core from 300 MHz up to 1 GHz, 3D graphics option for enhanced user interface, dual-core PRU-ICSS for industrial Ethernet protocols and position feedback control, and premium secure boot option.

Companion Products for AM335x Sitara Processors Review products that are frequently purchased or used with this product.

TI Designs for AM335x Sitara Processors The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagram

NOTE

The terms 'ball', 'pin', and 'terminal' are used interchangeably throughout the document. An attempt is made to use 'ball' only when referring to the physical package.

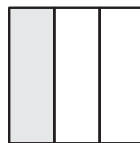
4.1.1 ZCE Package Pin Maps (Top View)

The pin maps that follow show the pin assignments on the ZCE package in three sections (left, middle, and right).

Table 4-1. ZCE Pin Map [Section Left - Top View]

| | A | B | C | D | E | F |
|----|---------------|-------------------|-------------------|------------------|-------------------|------------|
| 19 | VSS | I2C0_SCL | UART1_TXD | UART1_RTSn | UART0_RXD | UART0_CTSn |
| 18 | SPI0_SCLK | SPI0_D0 | I2C0_SDA | UART1_RXD | ECAP0_IN_PWM0_OUT | UART0_RTSn |
| 17 | SPI0_CS0 | SPI0_D1 | EXTINTn | XXXX | UART1_CTSn | UART0_TXD |
| 16 | WARMRSTn | SPI0_CS1 | XXXX | XXXX | XXXX | VDDS |
| 15 | EMU0 | XDMA_EVENT_INTR1 | XDMA_EVENT_INTR0 | XXXX | PWRONRSTn | XXXX |
| 14 | TDO | TCK | TMS | EMU1 | XXXX | VDDSHV6 |
| 13 | TRSTn | TDI | CAP_VBB_MPU | CAP_VDD_SRAM_MPU | VDDSHV6 | VSS |
| 12 | AIN7 | AIN5 | VDDS_SRAM_MPU_BB | VDDS | VDDSHV6 | VSS |
| 11 | AIN1 | AIN3 | XXXX | XXXX | VDDSHV6 | VDD_CORE |
| 10 | AIN6 | CAP_VDD_SRAM_CORE | VDDS_SRAM_CORE_BG | VSS | VSS | XXXX |
| 9 | VREFP | VREFN | XXXX | XXXX | VSS | VDD_CORE |
| 8 | AIN2 | AIN0 | AIN4 | VSSA_ADC | VSS | VSS |
| 7 | RTC_KALDO_ENn | RTC_PWRONRSTn | PMIC_POWER_EN | VDDA_ADC | VSS | VSS |
| 6 | RTC_XTALIN | RESERVED | VDDS_RTC | CAP_VDD_RTC | XXXX | VSS |
| 5 | RTC_XTALOUT | EXT_WAKEUP | VDDS_PLL_DDR | XXXX | DDR_A4 | XXXX |
| 4 | DDR_WEn | DDR_BA2 | XXXX | XXXX | XXXX | DDR_A12 |
| 3 | DDR_BA0 | DDR_A3 | DDR_A8 | XXXX | DDR_A15 | DDR_A0 |
| 2 | DDR_A5 | DDR_A9 | DDR_CK | DDR_A7 | DDR_A10 | DDR_RASn |
| 1 | VSS | DDR_A6 | DDR_CKn | DDR_A2 | DDR_BA1 | DDR_CASn |

Pin map section location

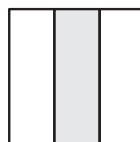


Left

ZCE Pin Map [Section Middle - Top View]

| | G | H | J | K | L | M |
|----|-------------|--------------|----------|---------------|------------|-------------|
| 19 | MMC0_CLK | MMC0_DAT3 | MI11_COL | MI11_RX_ER | MI11_RX_DV | MI11_RX_CLK |
| 18 | MMC0_DAT0 | MMC0_DAT2 | MI11_CRS | RMII1_REF_CLK | MI11_TXD0 | MI11_TXD1 |
| 17 | MMC0_CMD | MMC0_DAT1 | XXXX | MI11_TX_EN | XXXX | MI11_TXD3 |
| 16 | USB0_DRVBUS | VDDS_PLL_MPU | XXXX | VDD_CORE | XXXX | VDDS |
| 15 | VDDSHV4 | VDDSHV4 | VSS | VDD_CORE | VSS | VDDSHV5 |
| 14 | XXXX | VDDSHV4 | VSS | XXXX | VSS | VDDSHV5 |
| 13 | XXXX | VDD_CORE | VDD_CORE | XXXX | VDD_CORE | VDD_CORE |
| 12 | VSS | VDD_CORE | VDD_CORE | VSS | VDD_CORE | VDD_CORE |
| 11 | VDD_CORE | VSS | VSS | VSS | VSS | VSS |
| 10 | XXXX | VSS | XXXX | XXXX | XXXX | VSS |
| 9 | VDD_CORE | VSS | VSS | VSS | VSS | VSS |
| 8 | VSS | VDD_CORE | VDD_CORE | VSS | VDD_CORE | VDD_CORE |
| 7 | XXXX | VDD_CORE | VDD_CORE | XXXX | VDD_CORE | VDD_CORE |
| 6 | XXXX | VDDS_DDR | VSS | XXXX | VSS | VDDS_DDR |
| 5 | VDDS_DDR | VDDS_DDR | VSS | VDDS_DDR | VSS | VDDS_DDR |
| 4 | DDR_A11 | DDR_VREF | XXXX | VDDS_DDR | XXXX | DDR_D11 |
| 3 | DDR_CKE | DDR_A14 | XXXX | DDR_DQM1 | XXXX | DDR_D10 |
| 2 | DDR_RESETh | DDR_CSn0 | DDR_A1 | DDR_D8 | DDR_DQSn1 | DDR_D12 |
| 1 | DDR_ODT | DDR_A13 | DDR_VTP | DDR_D9 | DDR_DQS1 | DDR_D13 |

Pin map section location

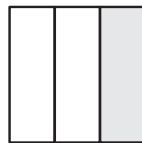


Middle

ZCE Pin Map [Section Right - Top View]

| | N | P | R | T | U | V | W |
|----|------------|----------|---------------|-------------------|------------|---------------|----------------|
| 19 | MI1_TX_CLK | MI1_RXD1 | MDC | USB0_VBUS | USB0_DP | USB0_ID | VSS |
| 18 | MI1_TXD2 | MI1_RXD0 | VDDA3P3V_USB0 | USB0_CE | USB0_DM | GPMC_BEn1 | GPMC_WPn |
| 17 | MI1_RXD3 | MDIO | VDDA1P8V_USB0 | XXXX | GPMC_CSn3 | GPMC_AD15 | GPMC_AD14 |
| 16 | MI1_RXD2 | VSSA_USB | XXXX | XXXX | XXXX | GPMC_CLK | GPMC_AD9 |
| 15 | VDDSHV5 | XXXX | GPMC_WAIT0 | XXXX | GPMC_CSn2 | GPMC_AD8 | GPMC_AD7 |
| 14 | XXXX | VSS | XXXX | VDDS | GPMC_AD6 | GPMC_CSn1 | GPMC_AD5 |
| 13 | XXXX | VSS | VDDSHV1 | GPMC_AD13 | GPMC_AD12 | GPMC_AD4 | GPMC_AD3 |
| 12 | VSS | VSS | VDDSHV1 | GPMC_AD10 | GPMC_AD11 | GPMC_AD2 | XTALOUT |
| 11 | VDD_CORE | VDD_CORE | VDDSHV1 | XXXX | XXXX | VSS_OSC | XTALIN |
| 10 | XXXX | XXXX | VSS | VSS | VDDS_OSC | GPMC_ADVn_ALE | GPMC_AD0 |
| 9 | VDD_CORE | VDD_CORE | VDDSHV1 | XXXX | XXXX | GPMC_AD1 | GPMC_OEn_REn |
| 8 | VSS | VSS | VDDSHV1 | VDDS_PLL_CORE_LCD | GPMC_WEn | GPMC_BEn0_CLE | GPMC_CSn0 |
| 7 | XXXX | VSS | VDDSHV6 | LCD_HSYNC | LCD_VSYNC | LCD_DATA15 | LCD_AC_BIAS_EN |
| 6 | XXXX | VDDSHV6 | XXXX | VDDS | LCD_DATA13 | LCD_DATA12 | LCD_DATA14 |
| 5 | VDDS_DDR | XXXX | VPP | XXXX | LCD_DATA10 | LCD_DATA11 | LCD_PCLK |
| 4 | DDR_D0 | DDR_D1 | XXXX | XXXX | XXXX | LCD_DATA8 | LCD_DATA9 |
| 3 | DDR_DQM0 | DDR_D4 | DDR_D7 | XXXX | LCD_DATA7 | LCD_DATA6 | LCD_DATA5 |
| 2 | DDR_D14 | DDR_D2 | DDR_DQSn0 | DDR_D6 | LCD_DATA1 | LCD_DATA3 | LCD_DATA4 |
| 1 | DDR_D15 | DDR_D3 | DDR_DQS0 | DDR_D5 | LCD_DATA0 | LCD_DATA2 | VSS |

Pin map section location



Right

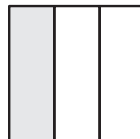
4.1.2 ZCZ Package Pin Maps (Top View)

The pin maps that follow show the pin assignments on the ZCZ package in three sections (left, middle, and right).

ZCZ Pin Map [Section Left - Top View]

| | A | B | C | D | E | F |
|----|------------------|---------------|-------------------|-------------------|-------------------|--------------|
| 18 | VSS | EXTINTn | ECAP0_IN_PWM0_OUT | UART1_CTSn | UART0_CTSn | MMC0_DAT2 |
| 17 | SPI0_SCLK | SPI0_D0 | I2C0_SDA | UART1_RTSn | UART0_RTSn | MMC0_DAT3 |
| 16 | SPI0_CS0 | SPI0_D1 | I2C0_SCL | UART1_RXD | UART0_TXD | USB0_DRVVBUS |
| 15 | XDMA_EVENT_INTR0 | PWRONRSTn | SPI0_CS1 | UART1_TXD | UART0_RXD | USB1_DRVVBUS |
| 14 | MCASP0_AHCLKX | EMU1 | EMU0 | XDMA_EVENT_INTR1 | VDDS | VDDSHV6 |
| 13 | MCASP0_ACLKX | MCASP0_FSX | MCASP0_FSR | MCASP0_AXR1 | VDDSHV6 | VDD_MPU |
| 12 | TCK | MCASP0_ACLKR | MCASP0_AHCLKR | MCASP0_AXR0 | VDDSHV6 | VDD_MPU |
| 11 | TDO | TDI | TMS | CAP_VDD_SRAM_MPU | VDDSHV6 | VDD_MPU |
| 10 | WARMRSTn | TRSTn | CAP_VBB_MPU | VDDS_SRAM_MPU_BB | VDDSHV6 | VDD_MPU |
| 9 | VREFN | VREFP | AIN7 | CAP_VDD_SRAM_CORE | VDDS_SRAM_CORE_BG | VDDS |
| 8 | AIN6 | AIN5 | AIN4 | VDDA_ADC | VSSA_ADC | VSS |
| 7 | AIN3 | AIN2 | AIN1 | VDDS_RTC | VDDS_PLL_DDR | VDD_CORE |
| 6 | RTC_XTALIN | AIN0 | PMIC_POWER_EN | CAP_VDD_RTC | VDDS | VDD_CORE |
| 5 | VSS_RTC | RTC_PWRONRSTn | EXT_WAKEUP | DDR_A6 | VDDS_DDR | VDDS_DDR |
| 4 | RTC_XTALOUT | RTC_KALDO_ENn | DDR_BA0 | DDR_A8 | DDR_A2 | DDR_A10 |
| 3 | RESERVED | DDR_BA2 | DDR_A3 | DDR_A15 | DDR_A12 | DDR_A0 |
| 2 | VDD_MPU_MON | DDR_WEn | DDR_A4 | DDR_CK | DDR_A7 | DDR_A11 |
| 1 | VSS | DDR_A5 | DDR_A9 | DDR_CKn | DDR_BA1 | DDR_CASn |

Pin map section location

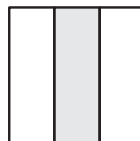


Left

ZCZ Pin Map [Section Middle - Top View]

| | G | H | J | K | L | M |
|----|------------|--------------|------------|-------------|-------------|-----------|
| 18 | MMC0_CMD | RMI1_REF_CLK | MII1_TXD3 | MII1_TX_CLK | MII1_RX_CLK | MDC |
| 17 | MMC0_CLK | MII1_CRS | MII1_RX_DV | MII1_TXD0 | MII1_RXD3 | MDIO |
| 16 | MMC0_DAT0 | MII1_COL | MII1_TX_EN | MII1_TXD1 | MII1_RXD2 | MII1_RXD0 |
| 15 | MMC0_DAT1 | VDDS_PLL_MPU | MII1_RX_ER | MII1_TXD2 | MII1_RXD1 | USB0_CE |
| 14 | VDDSHV6 | VDDSHV4 | VDDSHV4 | VDDSHV5 | VDDSHV5 | VSSA_USB |
| 13 | VDD_MPU | VDD_MPU | VDD_MPU | VDDS | VSS | VDD_CORE |
| 12 | VSS | VSS | VDD_CORE | VDD_CORE | VSS | VSS |
| 11 | VSS | VDD_CORE | VSS | VSS | VSS | VDD_CORE |
| 10 | VDD_CORE | VSS | VSS | VSS | VSS | VSS |
| 9 | VSS | VSS | VSS | VSS | VDD_CORE | VSS |
| 8 | VSS | VSS | VSS | VDD_CORE | VDD_CORE | VSS |
| 7 | VDD_CORE | VSS | VSS | VSS | VDD_CORE | VSS |
| 6 | VDD_CORE | VSS | VSS | VDD_CORE | VDD_CORE | VSS |
| 5 | VDDS_DDR | VDDS_DDR | VDDS_DDR | VDDS_DDR | VDDS_DDR | VPP |
| 4 | DDR_RASn | DDR_A14 | DDR_VREF | DDR_D12 | DDR_D14 | DDR_D1 |
| 3 | DDR_CKE | DDR_A13 | DDR_VTP | DDR_D11 | DDR_D13 | DDR_D0 |
| 2 | DDR_RESETh | DDR_CSn0 | DDR_DQM1 | DDR_D10 | DDR_DQSn1 | DDR_DQM0 |
| 1 | DDR_ODT | DDR_A1 | DDR_D8 | DDR_D9 | DDR_DQS1 | DDR_D15 |

Pin map section location

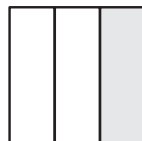


Middle

ZCZ Pin Map [Section Right - Top View]

| | N | P | R | T | U | V |
|----|---------------|-----------------------------------|----------------------------|---------------------------------------|-----------------------|-----------------------|
| 18 | USB0_DM | USB1_CE | USB1_DM | USB1_VBUS | GPMC_BE _{n1} | VSS |
| 17 | USB0_DP | USB1_ID | USB1_DP | GPMC_WAIT0 | GPMC_WP _n | GPMC_A11 |
| 16 | VDDA1P8V_USB0 | USB0_ID | VDDA1P8V_USB1 | GPMC_A10 | GPMC_A9 | GPMC_A8 |
| 15 | VDDA3P3V_USB0 | USB0_VBUS | VDDA3P3V_USB1 | GPMC_A7 | GPMC_A6 | GPMC_A5 |
| 14 | VSSA_USB | VDDS | GPMC_A4 | GPMC_A3 | GPMC_A2 | GPMC_A1 |
| 13 | VDD_CORE | VDDSHV3 | GPMC_A0 | GPMC_CS _{n3} | GPMC_AD15 | GPMC_AD14 |
| 12 | VDD_CORE | VDDSHV3 | GPMC_AD13 | GPMC_AD12 | GPMC_AD11 | GPMC_CLK |
| 11 | VSS | VDDSHV2 | VDDS_OSC | GPMC_AD10 | XTALOUT | VSS_OSC |
| 10 | VSS | VDDSHV2 | VDDS_PLL_CORE_LCD | GPMC_AD9 | GPMC_AD8 | XTALIN |
| 9 | VDD_CORE | VDDS | GPMC_AD6 | GPMC_AD7 | GPMC_CS _{n1} | GPMC_CS _{n2} |
| 8 | VDD_CORE | VDDSHV1 | GPMC_AD2 | GPMC_AD3 | GPMC_AD4 | GPMC_AD5 |
| 7 | VSS | VDDSHV1 | GPMC_ADV _n _ALE | GPMC_OE _n _RE _n | GPMC_AD0 | GPMC_AD1 |
| 6 | VDDS | VDDSHV6 | LCD_AC_BIAS_EN | GPMC_BE _{n0} _CLE | GPMC_WE _n | GPMC_CS _{n0} |
| 5 | VDDSHV6 | VDDSHV6 | LCD_HSYNC | LCD_DATA15 | LCD_VSYNC | LCD_PCLK |
| 4 | DDR_D5 | DDR_D7 | LCD_DATA3 | LCD_DATA7 | LCD_DATA11 | LCD_DATA14 |
| 3 | DDR_D4 | DDR_D6 | LCD_DATA2 | LCD_DATA6 | LCD_DATA10 | LCD_DATA13 |
| 2 | DDR_D3 | DDR_DQ _S _{n0} | LCD_DATA1 | LCD_DATA5 | LCD_DATA9 | LCD_DATA12 |
| 1 | DDR_D2 | DDR_DQ _S ₀ | LCD_DATA0 | LCD_DATA4 | LCD_DATA8 | VSS |

Pin map section location



Right

4.2 Pin Attributes

The *AM335x and AMIC110 Sitara Processors Technical Reference Manual* and this document may reference internal signal names when discussing peripheral input and output signals because many of the AM335x package terminals can be multiplexed to one of several peripheral signals. The following table has a Pin Name column that lists all device terminal names and a Signal Name column that lists all internal signal names multiplexed to each terminal which provides a cross reference of internal signal names to terminal names. This table also identifies other important terminal characteristics.

- (1) **BALL NUMBER:** Package ball numbers associated with each signals.
- (2) **PIN NAME:** The name of the package pin or terminal.
Note: The table does not take into account subsystem terminal multiplexing options.
- (3) **SIGNAL NAME:** The signal name for that pin in the mode being used.
- (4) **MODE:** Multiplexing mode number.
 - a. Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the terminal corresponds to the name of the terminal. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.
Note: The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.
 - b. Modes 1 to 7 are possible modes for alternate functions. On each terminal, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
- (5) **TYPE:** Signal direction
 - I = Input
 - O = Output
 - I/O = Input and Output
 - D = Open drain
 - DS = Differential
 - A = Analog
 - PWR = Power
 - GND = Ground**Note:** In the safe_mode, the buffer is configured in high-impedance.
- (6) **BALL RESET STATE:** State of the terminal while the active low PWRONRSTn terminal is low.
 - 0: The buffer drives V_{OL} (pulldown or pullup resistor not activated)
 - 0(PD): The buffer drives V_{OL} with an active pulldown resistor
 - 1: The buffer drives V_{OH} (pulldown or pullup resistor not activated)
 - 1(PU): The buffer drives V_{OH} with an active pullup resistor
 - Z: High-impedance
 - L: High-impedance with an active pulldown resistor
 - H: High-impedance with an active pullup resistor
- (7) **BALL RESET REL. STATE:** State of the terminal after the active low PWRONRSTn terminal transitions from low to high.
 - 0: The buffer drives V_{OL} (pulldown or pullup resistor not activated)
 - 0(PD): The buffer drives V_{OL} with an active pulldown resistor
 - 1: The buffer drives V_{OH} (pulldown or pullup resistor not activated)
 - 1(PU): The buffer drives V_{OH} with an active pullup resistor
 - Z: High-impedance.
 - L: High-impedance with an active pulldown resistor
 - H: High-impedance with an active pullup resistor
- (8) **RESET REL. MODE:** The mode is automatically configured after the active low PWRONRSTn terminal transitions from low to high.
- (9) **POWER:** The voltage supply that powers the I/O buffers of the terminal.
- (10) **HYS:** Indicates if the input buffer is with hysteresis.
- (11) **BUFFER STRENGTH:** Drive strength of the associated output buffer.
- (12) **PULLUP OR PULLDOWN TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
- (13) **I/O CELL:** I/O cell information.
Note: Configuring two terminals to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

Table 4-2. Pin Attributes (ZCE and ZCZ Packages)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|-------------------|-------------------|----------|-------------------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|-------------------|
| B8 | B6 | AIN0 | AIN0 | 0 | A ⁽²²⁾ | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | 25 | NA | Analog |
| A11 | C7 | AIN1 | AIN1 | 0 | A ⁽²¹⁾ | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | 25 | NA | Analog |
| A8 | B7 | AIN2 | AIN2 | 0 | A ⁽²¹⁾ | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | 25 | NA | Analog |
| B11 | A7 | AIN3 | AIN3 | 0 | A ⁽²⁰⁾ | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | 25 | NA | Analog |
| C8 | C8 | AIN4 | AIN4 | 0 | A ⁽²⁰⁾ | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | 25 | NA | Analog |
| B12 | B8 | AIN5 | AIN5 | 0 | A | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | NA | NA | Analog |
| A10 | A8 | AIN6 | AIN6 | 0 | A | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | NA | NA | Analog |
| A12 | C9 | AIN7 | AIN7 | 0 | A | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | NA | NA | Analog |
| C13 | C10 | CAP_VBB_MPU | CAP_VBB_MPU | NA | A | | | | | | | | |
| D6 | D6 | CAP_VDD_RTC | CAP_VDD_RTC | NA | A | | | | | | | | |
| B10 | D9 | CAP_VDD_SRAM_CORE | CAP_VDD_SRAM_CORE | NA | A | | | | | | | | |
| D13 | D11 | CAP_VDD_SRAM_MPU | CAP_VDD_SRAM_MPU | NA | A | | | | | | | | |
| F3 | F3 | DDR_A0 | ddr_a0 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| J2 | H1 | DDR_A1 | ddr_a1 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| D1 | E4 | DDR_A2 | ddr_a2 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| B3 | C3 | DDR_A3 | ddr_a3 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| E5 | C2 | DDR_A4 | ddr_a4 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| A2 | B1 | DDR_A5 | ddr_a5 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| B1 | D5 | DDR_A6 | ddr_a6 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| D2 | E2 | DDR_A7 | ddr_a7 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| C3 | D4 | DDR_A8 | ddr_a8 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| B2 | C1 | DDR_A9 | ddr_a9 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| E2 | F4 | DDR_A10 | ddr_a10 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |
| G4 | F2 | DDR_A11 | ddr_a11 | 0 | O | H | 1 | 0 | VDDSD_DDR / VDDSD_DDR | NA | 8 | PU/PD | LVC MOS/SSTL/HSTL |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------|-----------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|------------------|
| F4 | E3 | DDR_A12 | ddr_a12 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| H1 | H3 | DDR_A13 | ddr_a13 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| H3 | H4 | DDR_A14 | ddr_a14 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| E3 | D3 | DDR_A15 | ddr_a15 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| A3 | C4 | DDR_BA0 | ddr_ba0 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| E1 | E1 | DDR_BA1 | ddr_ba1 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| B4 | B3 | DDR_BA2 | ddr_ba2 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| F1 | F1 | DDR_CASn | ddr_casn | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| C2 | D2 | DDR_CK | ddr_ck | 0 | O | L | 0 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| G3 | G3 | DDR_CKE | ddr_cke | 0 | O | L | 0 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| C1 | D1 | DDR_CKn | ddr_nck | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| H2 | H2 | DDR_CSn0 | ddr_csn0 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| N4 | M3 | DDR_D0 | ddr_d0 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| P4 | M4 | DDR_D1 | ddr_d1 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| P2 | N1 | DDR_D2 | ddr_d2 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| P1 | N2 | DDR_D3 | ddr_d3 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| P3 | N3 | DDR_D4 | ddr_d4 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| T1 | N4 | DDR_D5 | ddr_d5 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| T2 | P3 | DDR_D6 | ddr_d6 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| R3 | P4 | DDR_D7 | ddr_d7 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| K2 | J1 | DDR_D8 | ddr_d8 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| K1 | K1 | DDR_D9 | ddr_d9 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| M3 | K2 | DDR_D10 | ddr_d10 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|-------------------|-----------------------------|----------|-------------------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|------------------|
| M4 | K3 | DDR_D11 | ddr_d11 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| M2 | K4 | DDR_D12 | ddr_d12 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| M1 | L3 | DDR_D13 | ddr_d13 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| N2 | L4 | DDR_D14 | ddr_d14 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| N1 | M1 | DDR_D15 | ddr_d15 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| N3 | M2 | DDR_DQM0 | ddr_dqm0 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| K3 | J2 | DDR_DQM1 | ddr_dqm1 | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| R1 | P1 | DDR_DQS0 | ddr_dqs0 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| L1 | L1 | DDR_DQS1 | ddr_dqs1 | 0 | I/O | L | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| R2 | P2 | DDR_DQSn0 | ddr_dqsn0 | 0 | I/O | H | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| L2 | L2 | DDR_DQSn1 | ddr_dqsn1 | 0 | I/O | H | Z | 0 | VDDSDDR / VDDSDDR | Yes | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| G1 | G1 | DDR_ODT | ddr_odt | 0 | O | L | 0 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| F2 | G4 | DDR_RASn | ddr_rasn | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| G2 | G2 | DDR_RESEtn | ddr_resetn | 0 | O | L | 0 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| H4 | J4 | DDR_VREF | ddr_vref | 0 | A ⁽¹⁸⁾ | NA | NA | NA | VDDSDDR / VDDSDDR | NA | NA | NA | Analog |
| J1 | J3 | DDR_VTP | ddr_vtp | 0 | I ⁽¹⁹⁾ | NA | NA | NA | VDDSDDR / VDDSDDR | NA | NA | NA | Analog |
| A4 | B2 | DDR_WEn | ddr_wen | 0 | O | H | 1 | 0 | VDDSDDR / VDDSDDR | NA | 8 | PU/PD | LVCNOS/SSTL/HSTL |
| E18 | C18 | ECAP0_IN_PWM0_OUT | eCAP0_in_PWM0_out | 0 | I/O | Z | L | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVCNOS |
| | | | uart3_txd | 1 | O | | | | | | | | |
| | | | spi1_cs1 | 2 | I/O | | | | | | | | |
| | | | pr1_ecap0_ecap_capin_apwm_o | 3 | I/O | | | | | | | | |
| | | | spi1_sclk | 4 | I/O | | | | | | | | |
| | | | mmc0_sdwp | 5 | I | | | | | | | | |
| | | | xdma_event_intr2 | 6 | I | | | | | | | | |
| | | | gpio0_7 | 7 | I/O | | | | | | | | |
| A15 | C14 | EMU0 | EMU0 | 0 | I/O | H | H | 0 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVCNOS |
| | | | gpio3_7 | 7 | I/O | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|--------------|------------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| D14 | B14 | EMU1 | EMU1 | 0 | I/O | H | H | 0 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpio3_8 | 7 | I/O | | | | | | | | | |
| C17 | B18 | EXTINTn | nNMI | 0 | I | Z | H | 0 | VDDSHV6 / VDDSHV6 | Yes | NA | PU/PD | LVC MOS | |
| B5 | C5 | EXT_WAKEUP | EXT_WAKEUP | 0 | I | L | Z | 0 | VDDS_RTC / VDDS_RTC | Yes | NA | NA | LVC MOS | |
| NA | R13 | GPMC_A0 | gpmc_a0 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gmii2_txen | 1 | O | | | | | | | | | |
| | | | rgmii2_tctl | 2 | O | | | | | | | | | |
| | | | rmii2_txen | 3 | O | | | | | | | | | |
| | | | gpmc_a16 | 4 | O | | | | | | | | | |
| | | | pr1_mii_mt1_clk | 5 | I | | | | | | | | | |
| | | | ehrpwm1_tripzone_input | 6 | I | | | | | | | | | |
| | | | gpio1_16 | 7 | I/O | | | | | | | | | |
| NA | V14 | GPMC_A1 | gpmc_a1 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gmii2_rxdv | 1 | I | | | | | | | | | |
| | | | rgmii2_rctl | 2 | I | | | | | | | | | |
| | | | mmc2_dat0 | 3 | I/O | | | | | | | | | |
| | | | gpmc_a17 | 4 | O | | | | | | | | | |
| | | | pr1_mii1_txd3 | 5 | O | | | | | | | | | |
| | | | ehrpwm0_synco | 6 | O | | | | | | | | | |
| | | | gpio1_17 | 7 | I/O | | | | | | | | | |
| NA | U14 | GPMC_A2 | gpmc_a2 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gmii2_txd3 | 1 | O | | | | | | | | | |
| | | | rgmii2_td3 | 2 | O | | | | | | | | | |
| | | | mmc2_dat1 | 3 | I/O | | | | | | | | | |
| | | | gpmc_a18 | 4 | O | | | | | | | | | |
| | | | pr1_mii1_txd2 | 5 | O | | | | | | | | | |
| | | | ehrpwm1A | 6 | O | | | | | | | | | |
| | | | gpio1_18 | 7 | I/O | | | | | | | | | |
| NA | T14 | GPMC_A3 | gpmc_a3 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gmii2_txd2 | 1 | O | | | | | | | | | |
| | | | rgmii2_td2 | 2 | O | | | | | | | | | |
| | | | mmc2_dat2 | 3 | I/O | | | | | | | | | |
| | | | gpmc_a19 | 4 | O | | | | | | | | | |
| | | | pr1_mii1_txd1 | 5 | O | | | | | | | | | |
| | | | ehrpwm1B | 6 | O | | | | | | | | | |
| | | | gpio1_19 | 7 | I/O | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------|-----------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| NA | R14 | GPMC_A4 | gpmc_a4 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | | gmii2_txd1 | 1 | O | | | | | | | | |
| | | | rgmii2_td1 | 2 | O | | | | | | | | |
| | | | rmii2_txd1 | 3 | O | | | | | | | | |
| | | | gpmc_a20 | 4 | O | | | | | | | | |
| | | | pr1_mii1_txd0 | 5 | O | | | | | | | | |
| | | | eQEP1A_in | 6 | I | | | | | | | | |
| gpio1_20 | 7 | I/O | | | | | | | | | | | |
| NA | V15 | GPMC_A5 | gpmc_a5 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | | gmii2_txd0 | 1 | O | | | | | | | | |
| | | | rgmii2_td0 | 2 | O | | | | | | | | |
| | | | rmii2_txd0 | 3 | O | | | | | | | | |
| | | | gpmc_a21 | 4 | O | | | | | | | | |
| | | | pr1_mii1_rxd3 | 5 | I | | | | | | | | |
| | | | eQEP1B_in | 6 | I | | | | | | | | |
| gpio1_21 | 7 | I/O | | | | | | | | | | | |
| NA | U15 | GPMC_A6 | gpmc_a6 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | | gmii2_txclk | 1 | I | | | | | | | | |
| | | | rgmii2_tclk | 2 | O | | | | | | | | |
| | | | mmc2_dat4 | 3 | I/O | | | | | | | | |
| | | | gpmc_a22 | 4 | O | | | | | | | | |
| | | | pr1_mii1_rxd2 | 5 | I | | | | | | | | |
| | | | eQEP1_index | 6 | I/O | | | | | | | | |
| gpio1_22 | 7 | I/O | | | | | | | | | | | |
| NA | T15 | GPMC_A7 | gpmc_a7 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | | gmii2_rxclk | 1 | I | | | | | | | | |
| | | | rgmii2_rclk | 2 | I | | | | | | | | |
| | | | mmc2_dat5 | 3 | I/O | | | | | | | | |
| | | | gpmc_a23 | 4 | O | | | | | | | | |
| | | | pr1_mii1_rxd1 | 5 | I | | | | | | | | |
| | | | eQEP1_strobe | 6 | I/O | | | | | | | | |
| gpio1_23 | 7 | I/O | | | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|-------------------------|--------------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| NA | V16 | GPMC_A8 | gpmc_a8 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS |
| | | | gmii2_rxd3 | 1 | I | | | | | | | | |
| | | | rgmii2_rd3 | 2 | I | | | | | | | | |
| | | | mmc2_dat6 | 3 | I/O | | | | | | | | |
| | | | gpmc_a24 | 4 | O | | | | | | | | |
| | | | pr1_mii1_rxd0 | 5 | I | | | | | | | | |
| | | | mcasp0_aclkx | 6 | I/O | | | | | | | | |
| | | | gpio1_24 | 7 | I/O | | | | | | | | |
| NA | U16 | GPMC_A9 ⁽¹⁰⁾ | gpmc_a9 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS |
| | | | gmii2_rxd2 | 1 | I | | | | | | | | |
| | | | rgmii2_rd2 | 2 | I | | | | | | | | |
| | | | mmc2_dat7 / rmii2_crs_dv | 3 | I/O | | | | | | | | |
| | | | gpmc_a25 | 4 | O | | | | | | | | |
| | | | pr1_mii_mr1_clk | 5 | I | | | | | | | | |
| | | | mcasp0_fsx | 6 | I/O | | | | | | | | |
| | | | gpio1_25 | 7 | I/O | | | | | | | | |
| NA | T16 | GPMC_A10 | gpmc_a10 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS |
| | | | gmii2_rxd1 | 1 | I | | | | | | | | |
| | | | rgmii2_rd1 | 2 | I | | | | | | | | |
| | | | rmii2_rxd1 | 3 | I | | | | | | | | |
| | | | gpmc_a26 | 4 | O | | | | | | | | |
| | | | pr1_mii1_rxdv | 5 | I | | | | | | | | |
| | | | mcasp0_axr0 | 6 | I/O | | | | | | | | |
| | | | gpio1_26 | 7 | I/O | | | | | | | | |
| NA | V17 | GPMC_A11 | gpmc_a11 | 0 | O | L | L | 7 | NA / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS |
| | | | gmii2_rxd0 | 1 | I | | | | | | | | |
| | | | rgmii2_rd0 | 2 | I | | | | | | | | |
| | | | rmii2_rxd0 | 3 | I | | | | | | | | |
| | | | gpmc_a27 | 4 | O | | | | | | | | |
| | | | pr1_mii1_rxer | 5 | I | | | | | | | | |
| | | | mcasp0_axr1 | 6 | I/O | | | | | | | | |
| | | | gpio1_27 | 7 | I/O | | | | | | | | |
| W10 | U7 | GPMC_AD0 | gpmc_ad0 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS |
| | | | mmc1_dat0 | 1 | I/O | | | | | | | | |
| | | | gpio1_0 | 7 | I/O | | | | | | | | |
| V9 | V7 | GPMC_AD1 | gpmc_ad1 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS |
| | | | mmc1_dat1 | 1 | I/O | | | | | | | | |
| | | | gpio1_1 | 7 | I/O | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------|-----------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| V12 | R8 | GPMC_AD2 | gpmc_ad2 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS |
| | | | mmc1_dat2 | 1 | I/O | | | | | | | | |
| | | | gpio1_2 | 7 | I/O | | | | | | | | |
| W13 | T8 | GPMC_AD3 | gpmc_ad3 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS |
| | | | mmc1_dat3 | 1 | I/O | | | | | | | | |
| | | | gpio1_3 | 7 | I/O | | | | | | | | |
| V13 | U8 | GPMC_AD4 | gpmc_ad4 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS |
| | | | mmc1_dat4 | 1 | I/O | | | | | | | | |
| | | | gpio1_4 | 7 | I/O | | | | | | | | |
| W14 | V8 | GPMC_AD5 | gpmc_ad5 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS |
| | | | mmc1_dat5 | 1 | I/O | | | | | | | | |
| | | | gpio1_5 | 7 | I/O | | | | | | | | |
| U14 | R9 | GPMC_AD6 | gpmc_ad6 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS |
| | | | mmc1_dat6 | 1 | I/O | | | | | | | | |
| | | | gpio1_6 | 7 | I/O | | | | | | | | |
| W15 | T9 | GPMC_AD7 | gpmc_ad7 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS |
| | | | mmc1_dat7 | 1 | I/O | | | | | | | | |
| | | | gpio1_7 | 7 | I/O | | | | | | | | |
| V15 | U10 | GPMC_AD8 | gpmc_ad8 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVC MOS |
| | | | lcd_data23 | 1 | O | | | | | | | | |
| | | | mmc1_dat0 | 2 | I/O | | | | | | | | |
| | | | mmc2_dat4 | 3 | I/O | | | | | | | | |
| | | | ehrpwm2A | 4 | O | | | | | | | | |
| | | | pr1_mii_mt0_clk | 5 | I | | | | | | | | |
| | | | gpio0_22 | 7 | I/O | | | | | | | | |
| W16 | T10 | GPMC_AD9 | gpmc_ad9 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVC MOS |
| | | | lcd_data22 | 1 | O | | | | | | | | |
| | | | mmc1_dat1 | 2 | I/O | | | | | | | | |
| | | | mmc2_dat5 | 3 | I/O | | | | | | | | |
| | | | ehrpwm2B | 4 | O | | | | | | | | |
| | | | pr1_mii0_col | 5 | I | | | | | | | | |
| | | | gpio0_23 | 7 | I/O | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------|------------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| T12 | T11 | GPMC_AD10 | gpmc_ad10 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | | lcd_data21 | 1 | O | | | | | | | | |
| | | | mmc1_dat2 | 2 | I/O | | | | | | | | |
| | | | mmc2_dat6 | 3 | I/O | | | | | | | | |
| | | | ehrpwm2_tripzone_input | 4 | I | | | | | | | | |
| | | | pr1_mii0_txen | 5 | O | | | | | | | | |
| gpio0_26 | 7 | I/O | | | | | | | | | | | |
| U12 | U12 | GPMC_AD11 | gpmc_ad11 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | | lcd_data20 | 1 | O | | | | | | | | |
| | | | mmc1_dat3 | 2 | I/O | | | | | | | | |
| | | | mmc2_dat7 | 3 | I/O | | | | | | | | |
| | | | ehrpwm0_synco | 4 | O | | | | | | | | |
| | | | pr1_mii0_txd3 | 5 | O | | | | | | | | |
| gpio0_27 | 7 | I/O | | | | | | | | | | | |
| U13 | T12 | GPMC_AD12 | gpmc_ad12 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | | lcd_data19 | 1 | O | | | | | | | | |
| | | | mmc1_dat4 | 2 | I/O | | | | | | | | |
| | | | mmc2_dat0 | 3 | I/O | | | | | | | | |
| | | | eQEP2A_in | 4 | I | | | | | | | | |
| | | | pr1_mii0_txd2 | 5 | O | | | | | | | | |
| pr1_pru0_pru_r30_14 | 6 | O | | | | | | | | | | | |
| gpio1_12 | 7 | I/O | | | | | | | | | | | |
| T13 | R12 | GPMC_AD13 | gpmc_ad13 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | | lcd_data18 | 1 | O | | | | | | | | |
| | | | mmc1_dat5 | 2 | I/O | | | | | | | | |
| | | | mmc2_dat1 | 3 | I/O | | | | | | | | |
| | | | eQEP2B_in | 4 | I | | | | | | | | |
| | | | pr1_mii0_txd1 | 5 | O | | | | | | | | |
| pr1_pru0_pru_r30_15 | 6 | O | | | | | | | | | | | |
| gpio1_13 | 7 | I/O | | | | | | | | | | | |
| W17 | V13 | GPMC_AD14 | gpmc_ad14 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | | lcd_data17 | 1 | O | | | | | | | | |
| | | | mmc1_dat6 | 2 | I/O | | | | | | | | |
| | | | mmc2_dat2 | 3 | I/O | | | | | | | | |
| | | | eQEP2_index | 4 | I/O | | | | | | | | |
| | | | pr1_mii0_txd0 | 5 | O | | | | | | | | |
| pr1_pru0_pru_r31_14 | 6 | I | | | | | | | | | | | |
| gpio1_14 | 7 | I/O | | | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|---------------|-----------------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| V17 | U13 | GPMC_AD15 | gpmc_ad15 | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVC MOS | |
| | | | lcd_data16 | 1 | O | | | | | | | | | |
| | | | mmc1_dat7 | 2 | I/O | | | | | | | | | |
| | | | mmc2_dat3 | 3 | I/O | | | | | | | | | |
| | | | eQEP2_strobe | 4 | I/O | | | | | | | | | |
| | | | pr1_ecap0_ecap_capin_apwm_o | 5 | I/O | | | | | | | | | |
| | | | pr1_pru0_pru_r31_15 | 6 | I | | | | | | | | | |
| gpio1_15 | 7 | I/O | | | | | | | | | | | | |
| V10 | R7 | GPMC_ADVn_ALE | gpmc_advn_ale | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS | |
| | | | timer4 | 2 | I/O | | | | | | | | | |
| | | | gpio2_2 | 7 | I/O | | | | | | | | | |
| V8 | T6 | GPMC_BEn0_CLE | gpmc_be0n_cle | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS | |
| | | | timer5 | 2 | I/O | | | | | | | | | |
| | | | gpio2_5 | 7 | I/O | | | | | | | | | |
| V18 | U18 | GPMC_BEn1 | gpmc_be1n | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gmii2_col | 1 | I | | | | | | | | | |
| | | | gpmc_csn6 | 2 | O | | | | | | | | | |
| | | | mmc2_dat3 | 3 | I/O | | | | | | | | | |
| | | | gpmc_dir | 4 | O | | | | | | | | | |
| | | | pr1_mii1_rxlink | 5 | I | | | | | | | | | |
| | | | mcasp0_aclkr | 6 | I/O | | | | | | | | | |
| gpio1_28 | 7 | I/O | | | | | | | | | | | | |
| V16 | V12 | GPMC_CLK | gpmc_clk | 0 | I/O | L | L | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVC MOS | |
| | | | lcd_memory_clk | 1 | O | | | | | | | | | |
| | | | gpmc_wait1 | 2 | I | | | | | | | | | |
| | | | mmc2_clk | 3 | I/O | | | | | | | | | |
| | | | pr1_mii1_crs | 4 | I | | | | | | | | | |
| | | | pr1_mdio_mdclk | 5 | O | | | | | | | | | |
| | | | mcasp0_fsr | 6 | I/O | | | | | | | | | |
| gpio2_1 | 7 | I/O | | | | | | | | | | | | |
| W8 | V6 | GPMC_CSn0 | gpmc_csn0 | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpio1_29 | 7 | I/O | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------------------|---------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| V14 | U9 | GPMC_CSn1 | gpmc_csn1 | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | | gpmc_clk | 1 | I/O | | | | | | | | |
| | | | mmc1_clk | 2 | I/O | | | | | | | | |
| | | | pr1_edio_data_in6 | 3 | I | | | | | | | | |
| | | | pr1_edio_data_out6 | 4 | O | | | | | | | | |
| | | | pr1_pru1_pru_r30_12 | 5 | O | | | | | | | | |
| | | | pr1_pru1_pru_r31_12 | 6 | I | | | | | | | | |
| gpio1_30 | 7 | I/O | | | | | | | | | | | |
| U15 | V9 | GPMC_CSn2 | gpmc_csn2 | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | | gpmc_be1n | 1 | O | | | | | | | | |
| | | | mmc1_cmd | 2 | I/O | | | | | | | | |
| | | | pr1_edio_data_in7 | 3 | I | | | | | | | | |
| | | | pr1_edio_data_out7 | 4 | O | | | | | | | | |
| | | | pr1_pru1_pru_r30_13 | 5 | O | | | | | | | | |
| | | | pr1_pru1_pru_r31_13 | 6 | I | | | | | | | | |
| gpio1_31 | 7 | I/O | | | | | | | | | | | |
| U17 | T13 | GPMC_CSn3 ⁽⁶⁾ | gpmc_csn3 | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | | gpmc_a3 | 1 | O | | | | | | | | |
| | | | rmii2_crs_dv | 2 | I | | | | | | | | |
| | | | mmc2_cmd | 3 | I/O | | | | | | | | |
| | | | pr1_mii0_crs | 4 | I | | | | | | | | |
| | | | pr1_mdio_data | 5 | I/O | | | | | | | | |
| | | | EMU4 | 6 | I/O | | | | | | | | |
| gpio2_0 | 7 | I/O | | | | | | | | | | | |
| W9 | T7 | GPMC_OEn_REn | gpmc_oen_ren | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | | timer7 | 2 | I/O | | | | | | | | |
| | | | gpio2_3 | 7 | I/O | | | | | | | | |
| R15 | T17 | GPMC_WAIT0 | gpmc_wait0 | 0 | I | H | H | 7 | VDDSHV1 / VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | | gmii2_crs | 1 | I | | | | | | | | |
| | | | gpmc_csn4 | 2 | O | | | | | | | | |
| | | | rmii2_crs_dv | 3 | I | | | | | | | | |
| | | | mmc1_sdcd | 4 | I | | | | | | | | |
| | | | pr1_mii1_col | 5 | I | | | | | | | | |
| | | | uart4_rxd | 6 | I | | | | | | | | |
| gpio0_30 | 7 | I/O | | | | | | | | | | | |
| U8 | U6 | GPMC_WEn | gpmc_wen | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | | timer6 | 2 | I/O | | | | | | | | |
| | | | gpio2_4 | 7 | I/O | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|--------------------------|---------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| W18 | U17 | GPMC_WPn | gpmc_wpn | 0 | O | H | H | 7 | VDDSHV1 / VDDSHV3 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gmii2_rxerr | 1 | I | | | | | | | | | |
| | | | gpmc_csn5 | 2 | O | | | | | | | | | |
| | | | rmii2_rxerr | 3 | I | | | | | | | | | |
| | | | mmc2_sdcd | 4 | I | | | | | | | | | |
| | | | pr1_mii1_txen | 5 | O | | | | | | | | | |
| | | | uart4_txd | 6 | O | | | | | | | | | |
| | | | gpio0_31 | 7 | I/O | | | | | | | | | |
| C18 | C17 | I2C0_SDA | I2C0_SDA | 0 | I/OD | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | timer4 | 1 | I/O | | | | | | | | | |
| | | | uart2_ctsn | 2 | I | | | | | | | | | |
| | | | eCAP2_in_PWM2_out | 3 | I/O | | | | | | | | | |
| | | | gpio3_5 | 7 | I/O | | | | | | | | | |
| B19 | C16 | I2C0_SCL | I2C0_SCL | 0 | I/OD | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | timer7 | 1 | I/O | | | | | | | | | |
| | | | uart2_rtsn | 2 | O | | | | | | | | | |
| | | | eCAP1_in_PWM1_out | 3 | I/O | | | | | | | | | |
| | | | gpio3_6 | 7 | I/O | | | | | | | | | |
| W7 | R6 | LCD_AC_BIAS_EN | lcd_ac_bias_en | 0 | O | Z | L | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a11 | 1 | O | | | | | | | | | |
| | | | pr1_mii1_crs | 2 | I | | | | | | | | | |
| | | | pr1_edio_data_in5 | 3 | I | | | | | | | | | |
| | | | pr1_edio_data_out5 | 4 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r30_11 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_11 | 6 | I | | | | | | | | | |
| | | | gpio2_25 | 7 | I/O | | | | | | | | | |
| U1 | R1 | LCD_DATA0 ⁽⁵⁾ | lcd_data0 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a0 | 1 | O | | | | | | | | | |
| | | | pr1_mii_mt0_clk | 2 | I | | | | | | | | | |
| | | | ehrpwm2A | 3 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r30_0 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_0 | 6 | I | | | | | | | | | |
| | | | | | | gpio2_6 | 7 | I/O | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] (25) | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|---------------|------------------------|----------|----------|---------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| U2 | R2 | LCD_DATA1 (5) | lcd_data1 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a1 | 1 | O | | | | | | | | | |
| | | | pr1_mii0_txen | 2 | O | | | | | | | | | |
| | | | ehrpwm2B | 3 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r30_1 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_1 | 6 | I | | | | | | | | | |
| | | | gpio2_7 | 7 | I/O | | | | | | | | | |
| V1 | R3 | LCD_DATA2 (5) | lcd_data2 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a2 | 1 | O | | | | | | | | | |
| | | | pr1_mii0_txd3 | 2 | O | | | | | | | | | |
| | | | ehrpwm2_tripzone_input | 3 | I | | | | | | | | | |
| | | | pr1_pru1_pru_r30_2 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_2 | 6 | I | | | | | | | | | |
| | | | gpio2_8 | 7 | I/O | | | | | | | | | |
| V2 | R4 | LCD_DATA3 (5) | lcd_data3 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a3 | 1 | O | | | | | | | | | |
| | | | pr1_mii0_txd2 | 2 | O | | | | | | | | | |
| | | | ehrpwm0_synco | 3 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r30_3 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_3 | 6 | I | | | | | | | | | |
| | | | gpio2_9 | 7 | I/O | | | | | | | | | |
| W2 | T1 | LCD_DATA4 (5) | lcd_data4 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a4 | 1 | O | | | | | | | | | |
| | | | pr1_mii0_txd1 | 2 | O | | | | | | | | | |
| | | | eQEP2A_in | 3 | I | | | | | | | | | |
| | | | pr1_pru1_pru_r30_4 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_4 | 6 | I | | | | | | | | | |
| | | | gpio2_10 | 7 | I/O | | | | | | | | | |
| W3 | T2 | LCD_DATA5 (5) | lcd_data5 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a5 | 1 | O | | | | | | | | | |
| | | | pr1_mii0_txd0 | 2 | O | | | | | | | | | |
| | | | eQEP2B_in | 3 | I | | | | | | | | | |
| | | | pr1_pru1_pru_r30_5 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_5 | 6 | I | | | | | | | | | |
| | | | gpio2_11 | 7 | I/O | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------------------|------------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| V3 | T3 | LCD_DATA6 ⁽⁵⁾ | lcd_data6 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | gpmc_a6 | 1 | O | | | | | | | | |
| | | | pr1_edio_data_in6 | 2 | I | | | | | | | | |
| | | | eQEP2_index | 3 | I/O | | | | | | | | |
| | | | pr1_edio_data_out6 | 4 | O | | | | | | | | |
| | | | pr1_pru1_pru_r30_6 | 5 | O | | | | | | | | |
| | | | pr1_pru1_pru_r31_6 | 6 | I | | | | | | | | |
| | | | gpio2_12 | 7 | I/O | | | | | | | | |
| U3 | T4 | LCD_DATA7 ⁽⁵⁾ | lcd_data7 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | gpmc_a7 | 1 | O | | | | | | | | |
| | | | pr1_edio_data_in7 | 2 | I | | | | | | | | |
| | | | eQEP2_strobe | 3 | I/O | | | | | | | | |
| | | | pr1_edio_data_out7 | 4 | O | | | | | | | | |
| | | | pr1_pru1_pru_r30_7 | 5 | O | | | | | | | | |
| | | | pr1_pru1_pru_r31_7 | 6 | I | | | | | | | | |
| | | | gpio2_13 | 7 | I/O | | | | | | | | |
| V4 | U1 | LCD_DATA8 ⁽⁵⁾ | lcd_data8 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | gpmc_a12 | 1 | O | | | | | | | | |
| | | | ehrpwm1_tripzone_input | 2 | I | | | | | | | | |
| | | | mcasp0_aclcx | 3 | I/O | | | | | | | | |
| | | | uart5_txd | 4 | O | | | | | | | | |
| | | | pr1_mii0_rxd3 | 5 | I | | | | | | | | |
| | | | uart2_ctsn | 6 | I | | | | | | | | |
| | | | gpio2_14 | 7 | I/O | | | | | | | | |
| W4 | U2 | LCD_DATA9 ⁽⁵⁾ | lcd_data9 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | gpmc_a13 | 1 | O | | | | | | | | |
| | | | ehrpwm0_synco | 2 | O | | | | | | | | |
| | | | mcasp0_fsx | 3 | I/O | | | | | | | | |
| | | | uart5_rxd | 4 | I | | | | | | | | |
| | | | pr1_mii0_rxd2 | 5 | I | | | | | | | | |
| | | | uart2_rtsn | 6 | O | | | | | | | | |
| | | | gpio2_15 | 7 | I/O | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | | |
|---------------------|---------------------|---------------------------|-----------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|--|
| U5 | U3 | LCD_DATA10 ⁽⁵⁾ | lcd_data10 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | | |
| | | | gpmc_a14 | 1 | O | | | | | | | | | | |
| | | | ehrpwm1A | 2 | O | | | | | | | | | | |
| | | | mcasp0_axr0 | 3 | I/O | | | | | | | | | | |
| | | | pr1_mii0_rxd1 | 5 | I | | | | | | | | | | |
| | | | uart3_ctsn | 6 | I | | | | | | | | | | |
| | | | gpio2_16 | 7 | I/O | | | | | | | | | | |
| V5 | U4 | LCD_DATA11 ⁽⁵⁾ | lcd_data11 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | | |
| | | | gpmc_a15 | 1 | O | | | | | | | | | | |
| | | | ehrpwm1B | 2 | O | | | | | | | | | | |
| | | | mcasp0_ahclr | 3 | I/O | | | | | | | | | | |
| | | | mcasp0_axr2 | 4 | I/O | | | | | | | | | | |
| | | | pr1_mii0_rxd0 | 5 | I | | | | | | | | | | |
| | | | uart3_rtsn | 6 | O | | | | | | | | | | |
| gpio2_17 | 7 | I/O | | | | | | | | | | | | | |
| V6 | V2 | LCD_DATA12 ⁽⁵⁾ | lcd_data12 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | | |
| | | | gpmc_a16 | 1 | O | | | | | | | | | | |
| | | | eQEP1A_in | 2 | I | | | | | | | | | | |
| | | | mcasp0_aclkr | 3 | I/O | | | | | | | | | | |
| | | | mcasp0_axr2 | 4 | I/O | | | | | | | | | | |
| | | | pr1_mii0_rxlink | 5 | I | | | | | | | | | | |
| | | | uart4_ctsn | 6 | I | | | | | | | | | | |
| gpio0_8 | 7 | I/O | | | | | | | | | | | | | |
| U6 | V3 | LCD_DATA13 ⁽⁵⁾ | lcd_data13 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | | |
| | | | gpmc_a17 | 1 | O | | | | | | | | | | |
| | | | eQEP1B_in | 2 | I | | | | | | | | | | |
| | | | mcasp0_fsr | 3 | I/O | | | | | | | | | | |
| | | | mcasp0_axr3 | 4 | I/O | | | | | | | | | | |
| | | | pr1_mii0_rxer | 5 | I | | | | | | | | | | |
| | | | uart4_rtsn | 6 | O | | | | | | | | | | |
| gpio0_9 | 7 | I/O | | | | | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|---------------------------|---------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| W6 | V4 | LCD_DATA14 ⁽⁵⁾ | lcd_data14 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a18 | 1 | O | | | | | | | | | |
| | | | eQEP1_index | 2 | I/O | | | | | | | | | |
| | | | mcasp0_axr1 | 3 | I/O | | | | | | | | | |
| | | | uart5_rxd | 4 | I | | | | | | | | | |
| | | | pr1_mii_mr0_clk | 5 | I | | | | | | | | | |
| | | | uart5_ctsn | 6 | I | | | | | | | | | |
| gpio0_10 | 7 | I/O | | | | | | | | | | | | |
| V7 | T5 | LCD_DATA15 ⁽⁵⁾ | lcd_data15 | 0 | I/O | Z | Z | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a19 | 1 | O | | | | | | | | | |
| | | | eQEP1_strobe | 2 | I/O | | | | | | | | | |
| | | | mcasp0_ahclkx | 3 | I/O | | | | | | | | | |
| | | | mcasp0_axr3 | 4 | I/O | | | | | | | | | |
| | | | pr1_mii0_rxdv | 5 | I | | | | | | | | | |
| | | | uart5_rtsn | 6 | O | | | | | | | | | |
| gpio0_11 | 7 | I/O | | | | | | | | | | | | |
| T7 | R5 | LCD_HSYNC ⁽⁷⁾ | lcd_hsync | 0 | O | Z | L | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a9 | 1 | O | | | | | | | | | |
| | | | gpmc_a2 | 2 | O | | | | | | | | | |
| | | | pr1_edio_data_in3 | 3 | I | | | | | | | | | |
| | | | pr1_edio_data_out3 | 4 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r30_9 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_9 | 6 | I | | | | | | | | | |
| gpio2_23 | 7 | I/O | | | | | | | | | | | | |
| W5 | V5 | LCD_PCLK | lcd_pclk | 0 | O | Z | L | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a10 | 1 | O | | | | | | | | | |
| | | | pr1_mii0_crs | 2 | I | | | | | | | | | |
| | | | pr1_edio_data_in4 | 3 | I | | | | | | | | | |
| | | | pr1_edio_data_out4 | 4 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r30_10 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_10 | 6 | I | | | | | | | | | |
| gpio2_24 | 7 | I/O | | | | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|--------------------------|--------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| U7 | U5 | LCD_VSYNC ⁽⁷⁾ | lcd_vsync | 0 | O | Z | L | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a8 | 1 | O | | | | | | | | | |
| | | | gpmc_a1 | 2 | O | | | | | | | | | |
| | | | pr1_edio_data_in2 | 3 | I | | | | | | | | | |
| | | | pr1_edio_data_out2 | 4 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r30_8 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_8 | 6 | I | | | | | | | | | |
| | | | gpio2_22 | 7 | I/O | | | | | | | | | |
| NA | B13 | MCASP0_FSX | mcasp0_fsx | 0 | I/O | L | L | 7 | NA / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | ehrpwm0B | 1 | O | | | | | | | | | |
| | | | spi1_d0 | 3 | I/O | | | | | | | | | |
| | | | mmc1_sdcd | 4 | I | | | | | | | | | |
| | | | pr1_pru0_pru_r30_1 | 5 | O | | | | | | | | | |
| | | | pr1_pru0_pru_r31_1 | 6 | I | | | | | | | | | |
| | | | | | | gpio3_15 | 7 | I/O | | | | | | |
| NA | B12 | MCASP0_ACLKR | mcasp0_aclkr | 0 | I/O | L | L | 7 | NA / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | eQEP0A_in | 1 | I | | | | | | | | | |
| | | | mcasp0_axr2 | 2 | I/O | | | | | | | | | |
| | | | mcasp1_aclkx | 3 | I/O | | | | | | | | | |
| | | | mmc0_sdwp | 4 | I | | | | | | | | | |
| | | | pr1_pru0_pru_r30_4 | 5 | O | | | | | | | | | |
| | | | pr1_pru0_pru_r31_4 | 6 | I | | | | | | | | | |
| | | | gpio3_18 | 7 | I/O | | | | | | | | | |
| NA | C12 | MCASP0_AHCLKR | mcasp0_ahclkr | 0 | I/O | L | L | 7 | NA / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS | |
| | | | ehrpwm0_synci | 1 | I | | | | | | | | | |
| | | | mcasp0_axr2 | 2 | I/O | | | | | | | | | |
| | | | spi1_cs0 | 3 | I/O | | | | | | | | | |
| | | | eCAP2_in_PWM2_out | 4 | I/O | | | | | | | | | |
| | | | pr1_pru0_pru_r30_3 | 5 | O | | | | | | | | | |
| | | | pr1_pru0_pru_r31_3 | 6 | I | | | | | | | | | |
| | | | gpio3_17 | 7 | I/O | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|---------------|------------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| NA | A14 | MCASP0_AHCLKX | mcasp0_ahclkx | 0 | I/O | L | L | 7 | NA / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | eQEP0_strobe | 1 | I/O | | | | | | | | |
| | | | mcasp0_axr3 | 2 | I/O | | | | | | | | |
| | | | mcasp1_axr1 | 3 | I/O | | | | | | | | |
| | | | EMU4 | 4 | I/O | | | | | | | | |
| | | | pr1_pru0_pru_r30_7 | 5 | O | | | | | | | | |
| | | | pr1_pru0_pru_r31_7 | 6 | I | | | | | | | | |
| | | | gpio3_21 | 7 | I/O | | | | | | | | |
| NA | A13 | MCASP0_ACLKX | mcasp0_aclkx | 0 | I/O | L | L | 7 | NA / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | ehrpwm0A | 1 | O | | | | | | | | |
| | | | spi1_sclk | 3 | I/O | | | | | | | | |
| | | | mmc0_sdcd | 4 | I | | | | | | | | |
| | | | pr1_pru0_pru_r30_0 | 5 | O | | | | | | | | |
| | | | pr1_pru0_pru_r31_0 | 6 | I | | | | | | | | |
| | | | | | | gpio3_14 | 7 | I/O | | | | | |
| NA | C13 | MCASP0_FSR | mcasp0_fsr | 0 | I/O | L | L | 7 | NA / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | eQEP0B_in | 1 | I | | | | | | | | |
| | | | mcasp0_axr3 | 2 | I/O | | | | | | | | |
| | | | mcasp1_fsx | 3 | I/O | | | | | | | | |
| | | | EMU2 | 4 | I/O | | | | | | | | |
| | | | pr1_pru0_pru_r30_5 | 5 | O | | | | | | | | |
| | | | pr1_pru0_pru_r31_5 | 6 | I | | | | | | | | |
| | | | gpio3_19 | 7 | I/O | | | | | | | | |
| NA | D12 | MCASP0_AXR0 | mcasp0_axr0 | 0 | I/O | L | L | 7 | NA / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | ehrpwm0_tripzone_input | 1 | I | | | | | | | | |
| | | | spi1_d1 | 3 | I/O | | | | | | | | |
| | | | mmc2_sdcd | 4 | I | | | | | | | | |
| | | | pr1_pru0_pru_r30_2 | 5 | O | | | | | | | | |
| | | | pr1_pru0_pru_r31_2 | 6 | I | | | | | | | | |
| | | | | | | gpio3_16 | 7 | I/O | | | | | |
| NA | D13 | MCASP0_AXR1 | mcasp0_axr1 | 0 | I/O | L | L | 7 | NA / VDDSHV6 | Yes | 6 | PU/PD | LVC MOS |
| | | | eQEP0_index | 1 | I/O | | | | | | | | |
| | | | mcasp1_axr0 | 3 | I/O | | | | | | | | |
| | | | EMU3 | 4 | I/O | | | | | | | | |
| | | | pr1_pru0_pru_r30_6 | 5 | O | | | | | | | | |
| | | | pr1_pru0_pru_r31_6 | 6 | I | | | | | | | | |
| | | | | | | gpio3_20 | 7 | I/O | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|--------------|-----------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| R19 | M18 | MDC | mdio_clk | 0 | O | H | H | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCNOS | |
| | | | timer5 | 1 | I/O | | | | | | | | | |
| | | | uart5_txd | 2 | O | | | | | | | | | |
| | | | uart3_rtsn | 3 | O | | | | | | | | | |
| | | | mmc0_sdwp | 4 | I | | | | | | | | | |
| | | | mmc1_clk | 5 | I/O | | | | | | | | | |
| | | | mmc2_clk | 6 | I/O | | | | | | | | | |
| | | | gpio0_1 | 7 | I/O | | | | | | | | | |
| P17 | M17 | MDIO | mdio_data | 0 | I/O | H | H | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCNOS | |
| | | | timer6 | 1 | I/O | | | | | | | | | |
| | | | uart5_rxd | 2 | I | | | | | | | | | |
| | | | uart3_ctsn | 3 | I | | | | | | | | | |
| | | | mmc0_sdccl | 4 | I | | | | | | | | | |
| | | | mmc1_cmd | 5 | I/O | | | | | | | | | |
| | | | mmc2_cmd | 6 | I/O | | | | | | | | | |
| | | | gpio0_0 | 7 | I/O | | | | | | | | | |
| L19 | J17 | MII1_RX_DV | gmii1_rxdv | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCNOS | |
| | | | lcd_memory_clk | 1 | O | | | | | | | | | |
| | | | rgmii1_rctl | 2 | I | | | | | | | | | |
| | | | uart5_txd | 3 | O | | | | | | | | | |
| | | | mcasp1_acllx | 4 | I/O | | | | | | | | | |
| | | | mmc2_dat0 | 5 | I/O | | | | | | | | | |
| | | | mcasp0_aclkr | 6 | I/O | | | | | | | | | |
| | | | gpio3_4 | 7 | I/O | | | | | | | | | |
| K17 | J16 | MII1_TX_EN | gmii1_txen | 0 | O | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCNOS | |
| | | | rmii1_txen | 1 | O | | | | | | | | | |
| | | | rgmii1_tctl | 2 | O | | | | | | | | | |
| | | | timer4 | 3 | I/O | | | | | | | | | |
| | | | mcasp1_axr0 | 4 | I/O | | | | | | | | | |
| | | | eQEP0_index | 5 | I/O | | | | | | | | | |
| | | | mmc2_cmd | 6 | I/O | | | | | | | | | |
| | | | gpio3_3 | 7 | I/O | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|--------------|-----------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| K19 | J15 | MII1_RX_ER | gmii1_rxerr | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | rmii1_rxerr | 1 | I | | | | | | | | | |
| | | | spi1_d1 | 2 | I/O | | | | | | | | | |
| | | | l2C1_SCL | 3 | I/OD | | | | | | | | | |
| | | | mcasp1_fsx | 4 | I/O | | | | | | | | | |
| | | | uart5_rtsn | 5 | O | | | | | | | | | |
| | | | uart2_txd | 6 | O | | | | | | | | | |
| | | | gpio3_2 | 7 | I/O | | | | | | | | | |
| M19 | L18 | MII1_RX_CLK | gmii1_rxclk | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | uart2_txd | 1 | O | | | | | | | | | |
| | | | rgmii1_rclk | 2 | I | | | | | | | | | |
| | | | mmc0_dat6 | 3 | I/O | | | | | | | | | |
| | | | mmc1_dat1 | 4 | I/O | | | | | | | | | |
| | | | uart1_dsrn | 5 | I | | | | | | | | | |
| | | | mcasp0_fsx | 6 | I/O | | | | | | | | | |
| | | | gpio3_10 | 7 | I/O | | | | | | | | | |
| N19 | K18 | MII1_TX_CLK | gmii1_txclk | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | uart2_rxd | 1 | I | | | | | | | | | |
| | | | rgmii1_tclk | 2 | O | | | | | | | | | |
| | | | mmc0_dat7 | 3 | I/O | | | | | | | | | |
| | | | mmc1_dat0 | 4 | I/O | | | | | | | | | |
| | | | uart1_dcdn | 5 | I | | | | | | | | | |
| | | | mcasp0_aclck | 6 | I/O | | | | | | | | | |
| | | | gpio3_9 | 7 | I/O | | | | | | | | | |
| J19 | H16 | MII1_COL | gmii1_col | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | rmii2_refclk | 1 | I/O | | | | | | | | | |
| | | | spi1_sclk | 2 | I/O | | | | | | | | | |
| | | | uart5_rxd | 3 | I | | | | | | | | | |
| | | | mcasp1_axr2 | 4 | I/O | | | | | | | | | |
| | | | mmc2_dat3 | 5 | I/O | | | | | | | | | |
| | | | mcasp0_axr2 | 6 | I/O | | | | | | | | | |
| | | | gpio3_0 | 7 | I/O | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|--------------|-----------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| J18 | H17 | MII1_CRS | gmii1_crs | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | rmii1_crs_dv | 1 | I | | | | | | | | | |
| | | | spi1_d0 | 2 | I/O | | | | | | | | | |
| | | | l2C1_SDA | 3 | I/OD | | | | | | | | | |
| | | | mcasp1_aclkx | 4 | I/O | | | | | | | | | |
| | | | uart5_ctsn | 5 | I | | | | | | | | | |
| | | | uart2_rxd | 6 | I | | | | | | | | | |
| | | | gpio3_1 | 7 | I/O | | | | | | | | | |
| P18 | M16 | MII1_RXD0 | gmii1_rxd0 | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | rmii1_rxd0 | 1 | I | | | | | | | | | |
| | | | rgmii1_rd0 | 2 | I | | | | | | | | | |
| | | | mcasp1_ahclkx | 3 | I/O | | | | | | | | | |
| | | | mcasp1_ahclkr | 4 | I/O | | | | | | | | | |
| | | | mcasp1_aclkr | 5 | I/O | | | | | | | | | |
| | | | mcasp0_axr3 | 6 | I/O | | | | | | | | | |
| | | | gpio2_21 | 7 | I/O | | | | | | | | | |
| P19 | L15 | MII1_RXD1 | gmii1_rxd1 | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | rmii1_rxd1 | 1 | I | | | | | | | | | |
| | | | rgmii1_rd1 | 2 | I | | | | | | | | | |
| | | | mcasp1_axr3 | 3 | I/O | | | | | | | | | |
| | | | mcasp1_fsr | 4 | I/O | | | | | | | | | |
| | | | eQEP0_strobe | 5 | I/O | | | | | | | | | |
| | | | mmc2_clk | 6 | I/O | | | | | | | | | |
| | | | gpio2_20 | 7 | I/O | | | | | | | | | |
| N16 | L16 | MII1_RXD2 | gmii1_rxd2 | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | uart3_txd | 1 | O | | | | | | | | | |
| | | | rgmii1_rd2 | 2 | I | | | | | | | | | |
| | | | mmc0_dat4 | 3 | I/O | | | | | | | | | |
| | | | mmc1_dat3 | 4 | I/O | | | | | | | | | |
| | | | uart1_rin | 5 | I | | | | | | | | | |
| | | | mcasp0_axr1 | 6 | I/O | | | | | | | | | |
| | | | gpio2_19 | 7 | I/O | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------|-----------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| N17 | L17 | MII1_RXD3 | gmii1_rxd3 | 0 | I | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCMOS |
| | | | uart3_rxd | 1 | I | | | | | | | | |
| | | | rgmii1_rd3 | 2 | I | | | | | | | | |
| | | | mmc0_dat5 | 3 | I/O | | | | | | | | |
| | | | mmc1_dat2 | 4 | I/O | | | | | | | | |
| | | | uart1_dtrn | 5 | O | | | | | | | | |
| | | | mcasp0_axr0 | 6 | I/O | | | | | | | | |
| gpio2_18 | 7 | I/O | | | | | | | | | | | |
| L18 | K17 | MII1_TXD0 | gmii1_txd0 | 0 | O | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCMOS |
| | | | rmii1_txd0 | 1 | O | | | | | | | | |
| | | | rgmii1_td0 | 2 | O | | | | | | | | |
| | | | mcasp1_axr2 | 3 | I/O | | | | | | | | |
| | | | mcasp1_aclkr | 4 | I/O | | | | | | | | |
| | | | eQEP0B_in | 5 | I | | | | | | | | |
| | | | mmc1_clk | 6 | I/O | | | | | | | | |
| gpio0_28 | 7 | I/O | | | | | | | | | | | |
| M18 | K16 | MII1_TXD1 | gmii1_txd1 | 0 | O | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCMOS |
| | | | rmii1_txd1 | 1 | O | | | | | | | | |
| | | | rgmii1_td1 | 2 | O | | | | | | | | |
| | | | mcasp1_fsr | 3 | I/O | | | | | | | | |
| | | | mcasp1_axr1 | 4 | I/O | | | | | | | | |
| | | | eQEP0A_in | 5 | I | | | | | | | | |
| | | | mmc1_cmd | 6 | I/O | | | | | | | | |
| gpio0_21 | 7 | I/O | | | | | | | | | | | |
| N18 | K15 | MII1_TXD2 | gmii1_txd2 | 0 | O | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCMOS |
| | | | dcan0_rx | 1 | I | | | | | | | | |
| | | | rgmii1_td2 | 2 | O | | | | | | | | |
| | | | uart4_txd | 3 | O | | | | | | | | |
| | | | mcasp1_axr0 | 4 | I/O | | | | | | | | |
| | | | mmc2_dat2 | 5 | I/O | | | | | | | | |
| | | | mcasp0_ahclkx | 6 | I/O | | | | | | | | |
| gpio0_17 | 7 | I/O | | | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------|---------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| M17 | J18 | MII1_TXD3 | gmii1_txd3 | 0 | O | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVCMOS |
| | | | dcan0_tx | 1 | O | | | | | | | | |
| | | | rgmii1_td3 | 2 | O | | | | | | | | |
| | | | uart4_rxd | 3 | I | | | | | | | | |
| | | | mcasp1_fsx | 4 | I/O | | | | | | | | |
| | | | mmc2_dat1 | 5 | I/O | | | | | | | | |
| | | | mcasp0_fsr | 6 | I/O | | | | | | | | |
| gpio0_16 | 7 | I/O | | | | | | | | | | | |
| G17 | G18 | MMC0_CMD | mmc0_cmd | 0 | I/O | H | H | 7 | VDDSHV4 / VDDSHV4 | Yes | 6 | PU/PD | LVCMOS |
| | | | gpmc_a25 | 1 | O | | | | | | | | |
| | | | uart3_rtsn | 2 | O | | | | | | | | |
| | | | uart2_txd | 3 | O | | | | | | | | |
| | | | dcan1_rx | 4 | I | | | | | | | | |
| | | | pr1_pru0_pru_r30_13 | 5 | O | | | | | | | | |
| | | | pr1_pru0_pru_r31_13 | 6 | I | | | | | | | | |
| gpio2_31 | 7 | I/O | | | | | | | | | | | |
| G19 | G17 | MMC0_CLK | mmc0_clk | 0 | I/O | H | H | 7 | VDDSHV4 / VDDSHV4 | Yes | 6 | PU/PD | LVCMOS |
| | | | gpmc_a24 | 1 | O | | | | | | | | |
| | | | uart3_ctsn | 2 | I | | | | | | | | |
| | | | uart2_rxd | 3 | I | | | | | | | | |
| | | | dcan1_tx | 4 | O | | | | | | | | |
| | | | pr1_pru0_pru_r30_12 | 5 | O | | | | | | | | |
| | | | pr1_pru0_pru_r31_12 | 6 | I | | | | | | | | |
| gpio2_30 | 7 | I/O | | | | | | | | | | | |
| G18 | G16 | MMC0_DAT0 | mmc0_dat0 | 0 | I/O | H | H | 7 | VDDSHV4 / VDDSHV4 | Yes | 6 | PU/PD | LVCMOS |
| | | | gpmc_a23 | 1 | O | | | | | | | | |
| | | | uart5_rtsn | 2 | O | | | | | | | | |
| | | | uart3_txd | 3 | O | | | | | | | | |
| | | | uart1_rin | 4 | I | | | | | | | | |
| | | | pr1_pru0_pru_r30_11 | 5 | O | | | | | | | | |
| | | | pr1_pru0_pru_r31_11 | 6 | I | | | | | | | | |
| gpio2_29 | 7 | I/O | | | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|-------------------------|---------------------|----------|----------|--------------------------------------|---------------------------|---------------------|-----------------------------------|----------|---------------------------|------------------------|---------------|--|
| H17 | G15 | MMC0_DAT1 | mmc0_dat1 | 0 | I/O | H | H | 7 | VDDSHV4 / VDDSHV4 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a22 | 1 | O | | | | | | | | | |
| | | | uart5_ctsn | 2 | I | | | | | | | | | |
| | | | uart3_rxd | 3 | I | | | | | | | | | |
| | | | uart1_dtrn | 4 | O | | | | | | | | | |
| | | | pr1_pru0_pru_r30_10 | 5 | O | | | | | | | | | |
| | | | pr1_pru0_pru_r31_10 | 6 | I | | | | | | | | | |
| gpio2_28 | 7 | I/O | | | | | | | | | | | | |
| H18 | F18 | MMC0_DAT2 | mmc0_dat2 | 0 | I/O | H | H | 7 | VDDSHV4 / VDDSHV4 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a21 | 1 | O | | | | | | | | | |
| | | | uart4_rtsn | 2 | O | | | | | | | | | |
| | | | timer6 | 3 | I/O | | | | | | | | | |
| | | | uart1_dsrn | 4 | I | | | | | | | | | |
| | | | pr1_pru0_pru_r30_9 | 5 | O | | | | | | | | | |
| | | | pr1_pru0_pru_r31_9 | 6 | I | | | | | | | | | |
| gpio2_27 | 7 | I/O | | | | | | | | | | | | |
| H19 | F17 | MMC0_DAT3 | mmc0_dat3 | 0 | I/O | H | H | 7 | VDDSHV4 / VDDSHV4 | Yes | 6 | PU/PD | LVC MOS | |
| | | | gpmc_a20 | 1 | O | | | | | | | | | |
| | | | uart4_ctsn | 2 | I | | | | | | | | | |
| | | | timer5 | 3 | I/O | | | | | | | | | |
| | | | uart1_dcdn | 4 | I | | | | | | | | | |
| | | | pr1_pru0_pru_r30_8 | 5 | O | | | | | | | | | |
| | | | pr1_pru0_pru_r31_8 | 6 | I | | | | | | | | | |
| gpio2_26 | 7 | I/O | | | | | | | | | | | | |
| C7 | C6 | PMIC_POWER_EN | PMIC_POWER_EN | 0 | O | H | 1 | 0 | VDDS_RTC / VDDS_RTC | NA | 6 | NA | LVC MOS | |
| E15 | B15 | PWRONRSTn | porz | 0 | I | Z | Z | 0 | VDDSHV6 / VDDSHV6 ⁽¹²⁾ | Yes | NA | NA | LVC MOS | |
| B6 | A3 | RESERVED ⁽³⁾ | testout | 0 | O | NA | NA | NA | VDDSHV6 / VDDSHV6 | NA | NA | NA | Analog | |
| K18 | H18 | RMII1_REF_CLK | rmii1_refclk | 0 | I/O | L | L | 7 | VDDSHV5 / VDDSHV5 | Yes | 6 | PU/PD | LVC MOS | |
| | | | xdma_event_intr2 | 1 | I | | | | | | | | | |
| | | | spi1_cs0 | 2 | I/O | | | | | | | | | |
| | | | uart5_txd | 3 | O | | | | | | | | | |
| | | | mcasp1_axr3 | 4 | I/O | | | | | | | | | |
| | | | mmc0_pow | 5 | O | | | | | | | | | |
| | | | mcasp1_ahclkx | 6 | I/O | | | | | | | | | |
| gpio0_29 | 7 | I/O | | | | | | | | | | | | |
| A7 | B4 | RTC_KALDO_ENn | ENZ_KALDO_1P8V | 0 | I | Z | Z | 0 | VDDS_RTC / VDDS_RTC | NA | NA | NA | Analog | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|---------------|--------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| B7 | B5 | RTC_PWRONRSTn | RTC_PORz | 0 | I | Z | Z | 0 | VDDS_RTC / VDDS_RTC | Yes | NA | NA | LVCMOS |
| A6 | A6 | RTC_XTALIN | OSC1_IN | 0 | I | H | H | 0 | VDDS_RTC / VDDS_RTC | Yes | NA | PU ⁽¹⁾ | LVCMOS |
| A5 | A4 | RTC_XTALOUT | OSC1_OUT | 0 | O | Z ⁽²³⁾ | Z ⁽²³⁾ | 0 | VDDS_RTC / VDDS_RTC | NA | NA ⁽¹⁵⁾ | NA | LVCMOS |
| A18 | A17 | SPI0_SCLK | spi0_sclk | 0 | I/O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | | uart2_rxd | 1 | I | | | | | | | | |
| | | | I2C2_SDA | 2 | I/OD | | | | | | | | |
| | | | ehrpwm0A | 3 | O | | | | | | | | |
| | | | pr1_uart0_cts_n | 4 | I | | | | | | | | |
| | | | pr1_edio_sof | 5 | O | | | | | | | | |
| | | | EMU2 | 6 | I/O | | | | | | | | |
| | | | gpio0_2 | 7 | I/O | | | | | | | | |
| A17 | A16 | SPI0_CS0 | spi0_cs0 | 0 | I/O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | | mmc2_sdwp | 1 | I | | | | | | | | |
| | | | I2C1_SCL | 2 | I/OD | | | | | | | | |
| | | | ehrpwm0_syncl | 3 | I | | | | | | | | |
| | | | pr1_uart0_txd | 4 | O | | | | | | | | |
| | | | pr1_edio_data_in1 | 5 | I | | | | | | | | |
| | | | pr1_edio_data_out1 | 6 | O | | | | | | | | |
| | | | gpio0_5 | 7 | I/O | | | | | | | | |
| B16 | C15 | SPI0_CS1 | spi0_cs1 | 0 | I/O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | | uart3_rxd | 1 | I | | | | | | | | |
| | | | eCAP1_in_PWM1_out | 2 | I/O | | | | | | | | |
| | | | mmc0_pow | 3 | O | | | | | | | | |
| | | | xdma_event_intr2 | 4 | I | | | | | | | | |
| | | | mmc0_sdcld | 5 | I | | | | | | | | |
| | | | EMU4 | 6 | I/O | | | | | | | | |
| | | | gpio0_6 | 7 | I/O | | | | | | | | |
| B18 | B17 | SPI0_D0 | spi0_d0 | 0 | I/O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | | uart2_txd | 1 | O | | | | | | | | |
| | | | I2C2_SCL | 2 | I/OD | | | | | | | | |
| | | | ehrpwm0B | 3 | O | | | | | | | | |
| | | | pr1_uart0_rts_n | 4 | O | | | | | | | | |
| | | | pr1_edio_latch_in | 5 | I | | | | | | | | |
| | | | EMU3 | 6 | I/O | | | | | | | | |
| | | | gpio0_3 | 7 | I/O | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---------------------|---------------------|--------------|------------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| B17 | B16 | SPI0_D1 | spi0_d1 | 0 | I/O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | | mmc1_sdwp | 1 | I | | | | | | | | |
| | | | I2C1_SDA | 2 | I/OD | | | | | | | | |
| | | | ehrpwm0_tripzone_input | 3 | I | | | | | | | | |
| | | | pr1_uart0_rxd | 4 | I | | | | | | | | |
| | | | pr1_edio_data_in0 | 5 | I | | | | | | | | |
| | | | pr1_edio_data_out0 | 6 | O | | | | | | | | |
| | | | gpio0_4 | 7 | I/O | | | | | | | | |
| B14 | A12 | TCK | TCK | 0 | I | H | H | 0 | VDDSHV6 / VDDSHV6 | Yes | NA | PU/PD | LVCMOS |
| B13 | B11 | TDI | TDI | 0 | I | H | H | 0 | VDDSHV6 / VDDSHV6 | Yes | NA | PU/PD | LVCMOS |
| A14 | A11 | TDO | TDO | 0 | O | H | H | 0 | VDDSHV6 / VDDSHV6 | NA | 4 | PU/PD | LVCMOS |
| C14 | C11 | TMS | TMS | 0 | I | H | H | 0 | VDDSHV6 / VDDSHV6 | Yes | NA | PU/PD | LVCMOS |
| A13 | B10 | TRSTn | nTRST | 0 | I | L | L | 0 | VDDSHV6 / VDDSHV6 | Yes | NA | PU/PD | LVCMOS |
| F17 | E16 | UART0_TXD | uart0_txd | 0 | O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVCMOS |
| | | | spi1_cs1 | 1 | I/O | | | | | | | | |
| | | | dcan0_rx | 2 | I | | | | | | | | |
| | | | I2C2_SCL | 3 | I/OD | | | | | | | | |
| | | | eCAP1_in_PWM1_out | 4 | I/O | | | | | | | | |
| | | | pr1_pru1_pru_r30_15 | 5 | O | | | | | | | | |
| | | | pr1_pru1_pru_r31_15 | 6 | I | | | | | | | | |
| | | | gpio1_11 | 7 | I/O | | | | | | | | |
| F19 | E18 | UART0_CTSn | uart0_ctsn | 0 | I | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVCMOS |
| | | | uart4_rxd | 1 | I | | | | | | | | |
| | | | dcan1_tx | 2 | O | | | | | | | | |
| | | | I2C1_SDA | 3 | I/OD | | | | | | | | |
| | | | spi1_d0 | 4 | I/O | | | | | | | | |
| | | | timer7 | 5 | I/O | | | | | | | | |
| | | | pr1_edc_sync0_out | 6 | O | | | | | | | | |
| | | | gpio1_8 | 7 | I/O | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|--------------|---------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|--|
| E19 | E15 | UART0_RXD | uart0_rxd | 0 | I | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | spi1_cs0 | 1 | I/O | | | | | | | | | |
| | | | dcan0_tx | 2 | O | | | | | | | | | |
| | | | l2C2_SDA | 3 | I/OD | | | | | | | | | |
| | | | eCAP2_in_PWM2_out | 4 | I/O | | | | | | | | | |
| | | | pr1_pru1_pru_r30_14 | 5 | O | | | | | | | | | |
| | | | pr1_pru1_pru_r31_14 | 6 | I | | | | | | | | | |
| gpio1_10 | 7 | I/O | | | | | | | | | | | | |
| F18 | E17 | UART0_RTSn | uart0_rtsn | 0 | O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | uart4_txd | 1 | O | | | | | | | | | |
| | | | dcan1_rx | 2 | I | | | | | | | | | |
| | | | l2C1_SCL | 3 | I/OD | | | | | | | | | |
| | | | spi1_d1 | 4 | I/O | | | | | | | | | |
| | | | spi1_cs0 | 5 | I/O | | | | | | | | | |
| | | | pr1_edc_sync1_out | 6 | O | | | | | | | | | |
| gpio1_9 | 7 | I/O | | | | | | | | | | | | |
| C19 | D15 | UART1_TXD | uart1_txd | 0 | O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | mmc2_sdwp | 1 | I | | | | | | | | | |
| | | | dcan1_rx | 2 | I | | | | | | | | | |
| | | | l2C1_SCL | 3 | I/OD | | | | | | | | | |
| | | | pr1_uart0_txd | 5 | O | | | | | | | | | |
| | | | pr1_pru0_pru_r31_16 | 6 | I | | | | | | | | | |
| | | | gpio0_15 | 7 | I/O | | | | | | | | | |
| D18 | D16 | UART1_RXD | uart1_rxd | 0 | I | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | mmc1_sdwp | 1 | I | | | | | | | | | |
| | | | dcan1_tx | 2 | O | | | | | | | | | |
| | | | l2C1_SDA | 3 | I/OD | | | | | | | | | |
| | | | pr1_uart0_rxd | 5 | I | | | | | | | | | |
| | | | pr1_pru1_pru_r31_16 | 6 | I | | | | | | | | | |
| | | | gpio0_14 | 7 | I/O | | | | | | | | | |
| D19 | D17 | UART1_RTSn | uart1_rtsn | 0 | O | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | timer5 | 1 | I/O | | | | | | | | | |
| | | | dcan0_rx | 2 | I | | | | | | | | | |
| | | | l2C2_SCL | 3 | I/OD | | | | | | | | | |
| | | | spi1_cs1 | 4 | I/O | | | | | | | | | |
| | | | pr1_uart0_rts_n | 5 | O | | | | | | | | | |
| | | | pr1_edc_latch1_in | 6 | I | | | | | | | | | |
| gpio0_13 | 7 | I/O | | | | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] | |
|---------------------|---------------------|---------------|-------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---|---------------------|---------------------------|------------------------|---------------|--|
| E17 | D18 | UART1_CTSn | uart1_ctsn | 0 | I | Z | H | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | timer6 | 1 | I/O | | | | | | | | | |
| | | | dcan0_tx | 2 | O | | | | | | | | | |
| | | | l2c2_sda | 3 | I/OD | | | | | | | | | |
| | | | spi1_cs0 | 4 | I/O | | | | | | | | | |
| | | | pr1_uart0_cts_n | 5 | I | | | | | | | | | |
| | | | pr1_edc_latch0_in | 6 | I | | | | | | | | | |
| | | | gpio0_12 | 7 | I/O | | | | | | | | | |
| T18 | M15 | USB0_CE | USB0_CE | 0 | A | Z | Z | 0 | VDDA*_USB0 / VDDA*_USB0 ⁽²⁶⁾ | NA | NA | NA | Analog | |
| T19 | P15 | USB0_VBUS | USB0_VBUS | 0 | A | Z | Z | 0 | VDDA*_USB0 / VDDA*_USB0 ⁽²⁶⁾ | NA | NA | NA | Analog | |
| U18 | N18 | USB0_DM | USB0_DM | 0 | A | Z | Z | 0 ⁽¹³⁾ | VDDA*_USB0 / VDDA*_USB0 ⁽²⁶⁾ | Yes ⁽¹⁶⁾ | 8 ⁽¹⁶⁾ | NA | Analog | |
| G16 | F16 | USB0_DRVVBUS | USB0_DRVVBUS | 0 | O | L | 0(PD) | 0 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | gpio0_18 | 7 | I/O | | | | | | | | | |
| V19 | P16 | USB0_ID | USB0_ID | 0 | A | Z | Z | 0 | VDDA*_USB0 / VDDA*_USB0 ⁽²⁶⁾ | NA | NA | NA | Analog | |
| U19 | N17 | USB0_DP | USB0_DP | 0 | A | Z | Z | 0 ⁽¹³⁾ | VDDA*_USB0 / VDDA*_USB0 ⁽²⁶⁾ | Yes ⁽¹⁶⁾ | 8 ⁽¹⁶⁾ | NA | Analog | |
| NA | P18 | USB1_CE | USB1_CE | 0 | A | Z | Z | 0 | NA / VDDA*_USB1 ⁽²⁷⁾ | NA | NA | NA | Analog | |
| NA | P17 | USB1_ID | USB1_ID | 0 | A | Z | Z | 0 | NA / VDDA*_USB1 ⁽²⁷⁾ | NA | NA | NA | Analog | |
| NA | T18 | USB1_VBUS | USB1_VBUS | 0 | A | Z | Z | 0 | NA / VDDA*_USB1 ⁽²⁷⁾ | NA | NA | NA | Analog | |
| NA | R17 | USB1_DP | USB1_DP | 0 | A | Z | Z | 0 ⁽¹⁴⁾ | NA / VDDA*_USB1 ⁽²⁷⁾ | Yes ⁽¹⁷⁾ | 8 ⁽¹⁷⁾ | NA | Analog | |
| NA | F15 | USB1_DRVVBUS | USB1_DRVVBUS | 0 | O | L | 0(PD) | 0 | NA / VDDSHV6 | Yes | 4 | PU/PD | LVC MOS | |
| | | | gpio3_13 | 7 | I/O | | | | | | | | | |
| NA | R18 | USB1_DM | USB1_DM | 0 | A | Z | Z | 0 ⁽¹⁴⁾ | NA / VDDA*_USB1 ⁽²⁷⁾ | Yes ⁽¹⁷⁾ | 8 ⁽¹⁷⁾ | NA | Analog | |
| R17 | N16 | VDDA1P8V_USB0 | VDDA1P8V_USB0 | NA | PWR | | | | | | | | | |
| NA | R16 | VDDA1P8V_USB1 | VDDA1P8V_USB1 | NA | PWR | | | | | | | | | |
| R18 | N15 | VDDA3P3V_USB0 | VDDA3P3V_USB0 | NA | PWR | | | | | | | | | |
| NA | R15 | VDDA3P3V_USB1 | VDDA3P3V_USB1 | NA | PWR | | | | | | | | | |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|--|--|-------------------|-----------------------------|----------|----------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| D7 | D8 | VDDA_ADC | VDDA_ADC | NA | PWR | | | | | | | | |
| D12, F16, M16, T6, T14 | E6, E14, F9, K13, N6, P9, P14 | VDDS | VDDS | NA | PWR | | | | | | | | |
| R8, R9, R11, R12, R13 | P7, P8 | VDDSHV1 | VDDSHV1 | NA | PWR | | | | | | | | |
| NA | P10, P11 | VDDSHV2 | VDDSHV2 | NA | PWR | | | | | | | | |
| NA | P12, P13 | VDDSHV3 | VDDSHV3 | NA | PWR | | | | | | | | |
| G15, H14, H15 | H14, J14 | VDDSHV4 | VDDSHV4 | NA | PWR | | | | | | | | |
| M14, M15, N15 | K14, L14 | VDDSHV5 | VDDSHV5 | NA | PWR | | | | | | | | |
| E11, E12, E13, F14, P6, R7 | E10, E11, E12, E13, F14, G14, N5, P5, P6 | VDDSHV6 | VDDSHV6 | NA | PWR | | | | | | | | |
| G5, H5, H6, K4, K5, M5, M6, N5 | E5, F5, G5, H5, J5, K5, L5 | VDDS_DDR | VDDS_DDR | NA | PWR | | | | | | | | |
| U10 | R11 | VDDS_OSC | VDDS_OSC | NA | PWR | | | | | | | | |
| T8 | R10 | VDDS_PLL_CORE_LCD | VDDS_PLL_CORE_LCD | NA | PWR | | | | | | | | |
| C5 | E7 | VDDS_PLL_DDR | VDDS_PLL_DDR | NA | PWR | | | | | | | | |
| H16 | H15 | VDDS_PLL_MPU | VDDS_PLL_MPU | NA | PWR | | | | | | | | |
| C6 | D7 | VDDS_RTC | VDDS_RTC | NA | PWR | | | | | | | | |
| C10 | E9 | VDDS_SRAM_CORE_BG | VDDS_SRAM_CORE_BG | NA | PWR | | | | | | | | |
| C12 | D10 | VDDS_SRAM_MPU_BB | VDDS_SRAM_MPU_BB | NA | PWR | | | | | | | | |
| F9, F11, G9, G11, H7, H8, H12, H13, J7, J8, J12, J13, K15, K16, L7, L8, L12, L13, M7, M8, M12, M13, N9, N11, P9, P11 | F6, F7, G6, G7, G10, H11, J12, K6, K8, K12, L6, L7, L8, L9, M11, M13, N8, N9, N12, N13 | VDD_CORE | VDD_CORE | NA | PWR | | | | | | | | |
| NA | F10, F11, F12, F13, G13, H13, J13 | VDD_MPU | VDD_MPU ⁽³⁰⁾ | NA | PWR | | | | | | | | |
| NA | A2 | VDD_MPU_MON | VDD_MPU_MON ⁽³¹⁾ | NA | A | | | | | | | | |
| R5 | M5 | VPP | VPP | NA | PWR | | | | | | | | |
| B9 | A9 | VREFN | VREFN | 0 | AP | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | NA | NA | Analog |
| A9 | B9 | VREFFP | VREFFP | 0 | AP | Z | Z | 0 | VDDA_ADC / VDDA_ADC | NA | NA | NA | Analog |

Table 4-2. Pin Attributes (ZCE and ZCZ Packages) (continued)

| ZCE BALL NUMBER [1] | ZCZ BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] ⁽²⁵⁾ | BALL RESET REL. STATE [7] | RESET REL. MODE [8] | ZCE POWER / ZCZ POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULLUP /DOWN TYPE [12] | I/O CELL [13] |
|---|--|------------------|-------------------------|----------|---------------------|--------------------------------------|---------------------------|---------------------|---------------------------|----------|---------------------------|------------------------|---------------|
| A1, A19, D10, E7, E8, E9, E10, F6, F7, F8, F12, F13, G8, G12, H9, H10, H11, J5, J6, J9, J11, J14, J15, K8, K9, K11, K12, L5, L6, L9, L11, L14, L15, M9, M10, M11, N8, N12, P7, P8, P12, P13, P14, R10, T10, W1, W19 | A1, A18, F8, G8, G9, G11, G12, H6, H7, H8, H9, H10, H12, J6, J7, J8, J9, J10, J11, K7, K9, K10, K11, L10, L11, L12, L13, M6, M7, M8, M9, M10, M12, N7, N10, N11, V1, V18 | VSS | VSS | NA | GND | | | | | | | | |
| D8 | E8 | VSSA_ADC | VSSA_ADC | NA | GND | | | | | | | | |
| P16 | M14, N14 | VSSA_USB | VSSA_USB | NA | GND | | | | | | | | |
| V11 | V11 | VSS_OSC | VSS_OSC ⁽²⁸⁾ | NA | A | | | | | | | | |
| NA | A5 | VSS_RTC | VSS_RTC ⁽²⁹⁾ | NA | A | | | | | | | | |
| A16 | A10 | WARMRSTn | nRESETIN_OUT | 0 | I/OD ⁽⁸⁾ | 0 | 0(PU) ⁽¹¹⁾ | 0 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVCMOS |
| C15 | A15 | XDMA_EVENT_INTR0 | xdma_event_intr0 | 0 | I | Z | (4) | (9) | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVCMOS |
| | | | timer4 | 2 | I/O | | | | | | | | |
| | | | clkout1 | 3 | O | | | | | | | | |
| | | | spi1_cs1 | 4 | I/O | | | | | | | | |
| | | | pr1_pru1_pru_r31_16 | 5 | I | | | | | | | | |
| | | | EMU2 | 6 | I/O | | | | | | | | |
| | | | gpio0_19 | 7 | I/O | | | | | | | | |
| B15 | D14 | XDMA_EVENT_INTR1 | xdma_event_intr1 | 0 | I | Z | L | 7 | VDDSHV6 / VDDSHV6 | Yes | 4 | PU/PD | LVCMOS |
| | | | tlckin | 2 | I | | | | | | | | |
| | | | clkout2 | 3 | O | | | | | | | | |
| | | | timer7 | 4 | I/O | | | | | | | | |
| | | | pr1_pru0_pru_r31_16 | 5 | I | | | | | | | | |
| | | | EMU3 | 6 | I/O | | | | | | | | |
| | | | gpio0_20 | 7 | I/O | | | | | | | | |
| W11 | V10 | XTALIN | OSC0_IN | 0 | I | Z | Z | 0 | VDDS_OSC / VDDS_OSC | Yes | NA | PD ⁽²⁾ | LVCMOS |
| W12 | U11 | XTALOUT | OSC0_OUT | 0 | O | (24) | (24) | 0 | VDDS_OSC / VDDS_OSC | NA | NA ⁽¹⁵⁾ | NA | LVCMOS |

- (1) An internal 10 kohm pullup is turned on when the oscillator is disabled. The oscillator is disabled by default after power is applied.
- (2) An internal 15 kohm pulldown is turned on when the oscillator is disabled. The oscillator is enabled by default after power is applied.
- (3) Do not connect anything to this terminal.
- (4) If sysboot[5] is low on the rising edge of PWRONRSTn, this terminal has an internal pulldown turned on after reset is released. If sysboot[5] is high on the rising edge or PWRONRSTn, this terminal will initially be driven low after reset is released then it begins to toggle at the same frequency of the XTALIN terminal.
- (5) LCD_DATA[15:0] terminals are respectively SYSBOOT[15:0] inputs, latched on the rising edge of PWRONRSTn.
- (6) Mode1 and Mode2 signal assignments for this terminal are only available with silicon revision 2.0 or newer devices.
- (7) Mode2 signal assignment for this terminal is only available with silicon revision 2.0 or newer devices.
- (8) Refer to the External Warm Reset section of the AM335x Technical Reference Manual for more information related to the operation of this terminal.
- (9) Reset Release Mode = 7 if sysboot[5] is low. Mode = 3 if sysboot[5] is high.
- (10) Silicon revision 1.0 devices only provide the MMC2_DAT7 signal when Mode3 is selected. Silicon revision 2.0 and newer devices implement another level of pin multiplexing which provides the original MMC2_DAT7 signal or RMII2_CRSDV signal when Mode3 is selected. This new level of pin multiplexing is selected with bit zero of the SMA2 register. For more details refer to Section 1.2 of the AM335x Technical Reference Manual.
- (11) The 0(PU) indicates that this terminal is initially low based on the description in the AM335x Technical Reference Manual. However, it is also has a weak internal pullup applied.
- (12) The input voltage thresholds for this input are not a function of VDDSHV6. Please refer to the DC Electrical Characteristics section for details related to electrical parameters associated with this input terminal.
- (13) The internal USB PHY can be configured to multiplex the UART2_TX or UART2_RX signals to this terminal. For more details refer to USB GPIO Details section of the AM335x Technical Reference Manual.
- (14) The internal USB PHY can be configured to multiplex the UART3_TX or UART3_RX signals to this terminal. For more details refer to USB GPIO Details section of the AM335x Technical Reference Manual.
- (15) This output should only be used to source the recommended crystal circuit.
- (16) This parameter only applies when this USB PHY terminal is operating in UART2 mode.
- (17) This parameter only applies when this USB PHY terminal is operating in UART3 mode.
- (18) This terminal is a analog input used to set the switching threshold of the DDR input buffers to $(VDDSDDR / 2)$.
- (19) This terminal is a analog passive signal that connects to an external 49.9 ohm 1%, 20mW reference resistor which is used to calibrate the DDR input/output buffers.
- (20) This terminal is analog input that may also be configured as an open-drain output.
- (21) This terminal is analog input that may also be configured as an open-source or open-drain output.
- (22) This terminal is analog input that may also be configured as an open-source output.
- (23) This terminal is high-Z when the oscillator is disabled. This terminal is driven high if RTC_XTALIN is less than VIL, driven low if RTC_XTALIN is greater than VIH, and driven to a unknown value if RTC_XTALIN is between VIL and VIH when the oscillator is enabled. The oscillator is disabled by default after power is applied.
- (24) This terminal is high-Z when the oscillator is disabled. This terminal is driven high if XTALIN is less than VIL, driven low if XTALIN is greater than VIH, and driven to a unknown value if XTALIN is between VIL and VIH when the oscillator is enabled. The oscillator is enabled by default after power is applied.
- (25) For all pins with content in the Ball Reset State column of this table, the terminal is not defined until all the supplies are ramped.
- (26) This terminal requires two power supplies, VDDA3p3v_USB0 and VDDA1p8v_USB0. The "*" character in the power supply name is a wild card that represents "3p3v" and "1p8v".
- (27) This terminal requires two power supplies, VDDA3p3v_USB1 and VDDA1p8v_USB1. The "*" character in the power supply name is a wild card that represents "3p3v" and "1p8v".
- (28) Refer to [Section 6.2.2](#) for additional details about VSS_OSC.
- (29) Refer to [Section 6.2.2](#) for additional details about VSS_RTC.
- (30) This power rail is connected to VDD_CORE in the ZCE package.
- (31) This terminal provides a Kelvin connection to VDD_MPU. It can be connected to the power supply feedback input to provide remote sensing which compensates for voltage drop in the

PCB power distribution network and package. When the Kelvin connection is not used it should be connected to the same power source as VDD_MPU.

4.3 Signal Descriptions

The AM335x device contains many peripheral interfaces. In order to reduce package size and lower overall system cost while maintaining maximum functionality, many of the AM335x terminals can multiplex up to eight signal functions. Although there are many combinations of pin multiplexing that are possible, only a certain number of sets, called I/O Sets, are valid due to timing limitations. These valid I/O Sets were carefully chosen to provide many possible application scenarios for the user.

Texas Instruments has developed a Windows-based application called Pin Mux Utility that helps a system designer select the appropriate pin-multiplexing configuration for their AM335x-based product design. The Pin Mux Utility provides a way to select valid I/O Sets of specific peripheral interfaces to ensure the pin-multiplexing configuration selected for a design only uses valid I/O Sets supported by the AM335x device.

- (1) **SIGNAL NAME:** The signal name
- (2) **DESCRIPTION:** Description of the signal
- (3) **TYPE:** Ball type for this specific function:
 - I = Input
 - O = Output
 - I/O = Input/Output
 - D = Open drain
 - DS = Differential
 - A = Analog
- (4) **BALL:** Package ball location

Table 4-3. ADC Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------------------|----------|--------------|--------------|
| AIN0 | Analog Input/Output | A | B8 | B6 |
| AIN1 | Analog Input/Output | A | A11 | C7 |
| AIN2 | Analog Input/Output | A | A8 | B7 |
| AIN3 | Analog Input/Output | A | B11 | A7 |
| AIN4 | Analog Input/Output | A | C8 | C8 |
| AIN5 | Analog Input | A | B12 | B8 |
| AIN6 | Analog Input | A | A10 | A8 |
| AIN7 | Analog Input | A | A12 | C9 |
| VREFN | Analog Negative Reference Input | AP | B9 | A9 |
| VREFP | Analog Positive Reference Input | AP | A9 | B9 |

Table 4-4. Debug Subsystem Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|------------------------------|----------|--------------|---------------|
| EMU0 | MISC EMULATION PIN | I/O | A15 | C14 |
| EMU1 | MISC EMULATION PIN | I/O | D14 | B14 |
| EMU2 | MISC EMULATION PIN | I/O | A18, C15 | A15, A17, C13 |
| EMU3 | MISC EMULATION PIN | I/O | B15, B18 | B17, D13, D14 |
| EMU4 | MISC EMULATION PIN | I/O | B16, U17 | A14, C15, T13 |
| nTRST | JTAG TEST RESET (ACTIVE LOW) | I | A13 | B10 |
| TCK | JTAG TEST CLOCK | I | B14 | A12 |
| TDI | JTAG TEST DATA INPUT | I | B13 | B11 |
| TDO | JTAG TEST DATA OUTPUT | O | A14 | A11 |
| TMS | JTAG TEST MODE SELECT | I | C14 | C11 |

Table 4-5. LCD Controller Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|--------------------------------|----------|--------------|--------------|
| lcd_ac_bias_en | LCD AC bias enable chip select | O | W7 | R6 |
| lcd_data0 | LCD data bus | I/O | U1 | R1 |
| lcd_data1 | LCD data bus | I/O | U2 | R2 |
| lcd_data10 | LCD data bus | I/O | U5 | U3 |
| lcd_data11 | LCD data bus | I/O | V5 | U4 |
| lcd_data12 | LCD data bus | I/O | V6 | V2 |
| lcd_data13 | LCD data bus | I/O | U6 | V3 |
| lcd_data14 | LCD data bus | I/O | W6 | V4 |
| lcd_data15 | LCD data bus | I/O | V7 | T5 |
| lcd_data16 | LCD data bus | O | V17 | U13 |

Table 4-5. LCD Controller Signals Description (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------|----------|--------------|--------------|
| lcd_data17 | LCD data bus | O | W17 | V13 |
| lcd_data18 | LCD data bus | O | T13 | R12 |
| lcd_data19 | LCD data bus | O | U13 | T12 |
| lcd_data2 | LCD data bus | I/O | V1 | R3 |
| lcd_data20 | LCD data bus | O | U12 | U12 |
| lcd_data21 | LCD data bus | O | T12 | T11 |
| lcd_data22 | LCD data bus | O | W16 | T10 |
| lcd_data23 | LCD data bus | O | V15 | U10 |
| lcd_data3 | LCD data bus | I/O | V2 | R4 |
| lcd_data4 | LCD data bus | I/O | W2 | T1 |
| lcd_data5 | LCD data bus | I/O | W3 | T2 |
| lcd_data6 | LCD data bus | I/O | V3 | T3 |
| lcd_data7 | LCD data bus | I/O | U3 | T4 |
| lcd_data8 | LCD data bus | I/O | V4 | U1 |
| lcd_data9 | LCD data bus | I/O | W4 | U2 |
| lcd_hsync | LCD Horizontal Sync | O | T7 | R5 |
| lcd_memory_clk | LCD MCLK | O | L19, V16 | J17, V12 |
| lcd_pclk | LCD pixel clock | O | W5 | V5 |
| lcd_vsync | LCD Vertical Sync | O | U7 | U5 |

4.3.1 External Memory Interfaces

Table 4-6. External Memory Interfaces/DDR Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---|----------|--------------|--------------|
| ddr_a0 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | F3 | F3 |
| ddr_a1 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | J2 | H1 |
| ddr_a10 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | E2 | F4 |
| ddr_a11 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | G4 | F2 |
| ddr_a12 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | F4 | E3 |
| ddr_a13 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | H1 | H3 |
| ddr_a14 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | H3 | H4 |
| ddr_a15 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | E3 | D3 |
| ddr_a2 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | D1 | E4 |
| ddr_a3 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | B3 | C3 |
| ddr_a4 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | E5 | C2 |
| ddr_a5 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | A2 | B1 |
| ddr_a6 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | B1 | D5 |
| ddr_a7 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | D2 | E2 |
| ddr_a8 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | C3 | D4 |
| ddr_a9 | DDR SDRAM ROW/COLUMN ADDRESS OUTPUT | O | B2 | C1 |
| ddr_ba0 | DDR SDRAM BANK ADDRESS OUTPUT | O | A3 | C4 |
| ddr_ba1 | DDR SDRAM BANK ADDRESS OUTPUT | O | E1 | E1 |
| ddr_ba2 | DDR SDRAM BANK ADDRESS OUTPUT | O | B4 | B3 |
| ddr_casn | DDR SDRAM COLUMN ADDRESS STROBE OUTPUT (ACTIVE LOW) | O | F1 | F1 |
| ddr_ck | DDR SDRAM CLOCK OUTPUT (Differential+) | O | C2 | D2 |
| ddr_cke | DDR SDRAM CLOCK ENABLE OUTPUT | O | G3 | G3 |
| ddr_csn0 | DDR SDRAM CHIP SELECT OUTPUT | O | H2 | H2 |
| ddr_d0 | DDR SDRAM DATA INPUT/OUTPUT | I/O | N4 | M3 |
| ddr_d1 | DDR SDRAM DATA INPUT/OUTPUT | I/O | P4 | M4 |
| ddr_d10 | DDR SDRAM DATA INPUT/OUTPUT | I/O | M3 | K2 |
| ddr_d11 | DDR SDRAM DATA INPUT/OUTPUT | I/O | M4 | K3 |
| ddr_d12 | DDR SDRAM DATA INPUT/OUTPUT | I/O | M2 | K4 |
| ddr_d13 | DDR SDRAM DATA INPUT/OUTPUT | I/O | M1 | L3 |
| ddr_d14 | DDR SDRAM DATA INPUT/OUTPUT | I/O | N2 | L4 |
| ddr_d15 | DDR SDRAM DATA INPUT/OUTPUT | I/O | N1 | M1 |
| ddr_d2 | DDR SDRAM DATA INPUT/OUTPUT | I/O | P2 | N1 |
| ddr_d3 | DDR SDRAM DATA INPUT/OUTPUT | I/O | P1 | N2 |

Table 4-6. External Memory Interfaces/DDR Signals Description (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---|----------|--------------|--------------|
| ddr_d4 | DDR SDRAM DATA INPUT/OUTPUT | I/O | P3 | N3 |
| ddr_d5 | DDR SDRAM DATA INPUT/OUTPUT | I/O | T1 | N4 |
| ddr_d6 | DDR SDRAM DATA INPUT/OUTPUT | I/O | T2 | P3 |
| ddr_d7 | DDR SDRAM DATA INPUT/OUTPUT | I/O | R3 | P4 |
| ddr_d8 | DDR SDRAM DATA INPUT/OUTPUT | I/O | K2 | J1 |
| ddr_d9 | DDR SDRAM DATA INPUT/OUTPUT | I/O | K1 | K1 |
| ddr_dqm0 | DDR WRITE ENABLE / DATA MASK FOR DATA[7:0] | O | N3 | M2 |
| ddr_dqm1 | DDR WRITE ENABLE / DATA MASK FOR DATA[15:8] | O | K3 | J2 |
| ddr_dqs0 | DDR DATA STROBE FOR DATA[7:0] (Differential+) | I/O | R1 | P1 |
| ddr_dqs1 | DDR DATA STROBE FOR DATA[15:8] (Differential+) | I/O | L1 | L1 |
| ddr_dqsn0 | DDR DATA STROBE FOR DATA[7:0] (Differential-) | I/O | R2 | P2 |
| ddr_dqsn1 | DDR DATA STROBE FOR DATA[15:8] (Differential-) | I/O | L2 | L2 |
| ddr_nck | DDR SDRAM CLOCK OUTPUT (Differential-) | O | C1 | D1 |
| ddr_odt | ODT OUTPUT | O | G1 | G1 |
| ddr_rasn | DDR SDRAM ROW ADDRESS STROBE OUTPUT (ACTIVE LOW) | O | F2 | G4 |
| ddr_resen | DDR3/DDR3L RESET OUTPUT (ACTIVE LOW) | O | G2 | G2 |
| ddr_vref | Voltage Reference Input | A | H4 | J4 |
| ddr_vtp | VTP Compensation Resistor | I | J1 | J3 |
| ddr_wen | DDR SDRAM WRITE ENABLE OUTPUT (ACTIVE LOW) | O | A4 | B2 |

Table 4-7. External Memory Interfaces/General-Purpose Memory Controller Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| gpmc_a0 | GPMC Address | O | U1 | R1, R13 |
| gpmc_a1 | GPMC Address | O | U2, U7 | R2, U5, V14 |
| gpmc_a10 | GPMC Address | O | W5 | T16, V5 |
| gpmc_a11 | GPMC Address | O | W7 | R6, V17 |
| gpmc_a12 | GPMC Address | O | V4 | U1 |
| gpmc_a13 | GPMC Address | O | W4 | U2 |
| gpmc_a14 | GPMC Address | O | U5 | U3 |
| gpmc_a15 | GPMC Address | O | V5 | U4 |
| gpmc_a16 | GPMC Address | O | V6 | R13, V2 |
| gpmc_a17 | GPMC Address | O | U6 | V14, V3 |
| gpmc_a18 | GPMC Address | O | W6 | U14, V4 |
| gpmc_a19 | GPMC Address | O | V7 | T14, T5 |
| gpmc_a2 | GPMC Address | O | T7, V1 | R3, R5, U14 |
| gpmc_a20 | GPMC Address | O | H19 | F17, R14 |
| gpmc_a21 | GPMC Address | O | H18 | F18, V15 |
| gpmc_a22 | GPMC Address | O | H17 | G15, U15 |
| gpmc_a23 | GPMC Address | O | G18 | G16, T15 |
| gpmc_a24 | GPMC Address | O | G19 | G17, V16 |

**Table 4-7. External Memory Interfaces/General-Purpose Memory Controller Signals
Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---|----------|--------------|--------------|
| gpmc_a25 | GPMC Address | O | G17 | G18, U16 |
| gpmc_a26 | GPMC Address | O | NA | T16 |
| gpmc_a27 | GPMC Address | O | NA | V17 |
| gpmc_a3 | GPMC Address | O | U17, V2 | R4, T13, T14 |
| gpmc_a4 | GPMC Address | O | W2 | R14, T1 |
| gpmc_a5 | GPMC Address | O | W3 | T2, V15 |
| gpmc_a6 | GPMC Address | O | V3 | T3, U15 |
| gpmc_a7 | GPMC Address | O | U3 | T15, T4 |
| gpmc_a8 | GPMC Address | O | U7 | U5, V16 |
| gpmc_a9 | GPMC Address | O | T7 | R5, U16 |
| gpmc_ad0 | GPMC Address and Data | I/O | W10 | U7 |
| gpmc_ad1 | GPMC Address and Data | I/O | V9 | V7 |
| gpmc_ad10 | GPMC Address and Data | I/O | T12 | T11 |
| gpmc_ad11 | GPMC Address and Data | I/O | U12 | U12 |
| gpmc_ad12 | GPMC Address and Data | I/O | U13 | T12 |
| gpmc_ad13 | GPMC Address and Data | I/O | T13 | R12 |
| gpmc_ad14 | GPMC Address and Data | I/O | W17 | V13 |
| gpmc_ad15 | GPMC Address and Data | I/O | V17 | U13 |
| gpmc_ad2 | GPMC Address and Data | I/O | V12 | R8 |
| gpmc_ad3 | GPMC Address and Data | I/O | W13 | T8 |
| gpmc_ad4 | GPMC Address and Data | I/O | V13 | U8 |
| gpmc_ad5 | GPMC Address and Data | I/O | W14 | V8 |
| gpmc_ad6 | GPMC Address and Data | I/O | U14 | R9 |
| gpmc_ad7 | GPMC Address and Data | I/O | W15 | T9 |
| gpmc_ad8 | GPMC Address and Data | I/O | V15 | U10 |
| gpmc_ad9 | GPMC Address and Data | I/O | W16 | T10 |
| gpmc_advn_ale | GPMC Address Valid / Address Latch Enable | O | V10 | R7 |
| gpmc_be0n_cle | GPMC Byte Enable 0 / Command Latch Enable | O | V8 | T6 |
| gpmc_be1n | GPMC Byte Enable 1 | O | U15, V18 | U18, V9 |
| gpmc_clk | GPMC Clock | I/O | V14, V16 | U9, V12 |
| gpmc_csn0 | GPMC Chip Select | O | W8 | V6 |
| gpmc_csn1 | GPMC Chip Select | O | V14 | U9 |
| gpmc_csn2 | GPMC Chip Select | O | U15 | V9 |
| gpmc_csn3 | GPMC Chip Select | O | U17 | T13 |
| gpmc_csn4 | GPMC Chip Select | O | R15 | T17 |
| gpmc_csn5 | GPMC Chip Select | O | W18 | U17 |
| gpmc_csn6 | GPMC Chip Select | O | V18 | U18 |
| gpmc_dir | GPMC Data Direction | O | V18 | U18 |
| gpmc_oen_ren | GPMC Output / Read Enable | O | W9 | T7 |
| gpmc_wait0 | GPMC Wait 0 | I | R15 | T17 |
| gpmc_wait1 | GPMC Wait 1 | I | V16 | V12 |
| gpmc_wen | GPMC Write Enable | O | U8 | U6 |
| gpmc_wpn | GPMC Write Protect | O | W18 | U17 |

4.3.2 General-Purpose IOs

Table 4-8. General-Purpose IOs/GPIO0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| gpio0_0 | GPIO | I/O | P17 | M17 |
| gpio0_1 | GPIO | I/O | R19 | M18 |
| gpio0_10 | GPIO | I/O | W6 | V4 |
| gpio0_11 | GPIO | I/O | V7 | T5 |
| gpio0_12 | GPIO | I/O | E17 | D18 |
| gpio0_13 | GPIO | I/O | D19 | D17 |
| gpio0_14 | GPIO | I/O | D18 | D16 |
| gpio0_15 | GPIO | I/O | C19 | D15 |
| gpio0_16 | GPIO | I/O | M17 | J18 |
| gpio0_17 | GPIO | I/O | N18 | K15 |
| gpio0_18 | GPIO | I/O | G16 | F16 |
| gpio0_19 | GPIO | I/O | C15 | A15 |
| gpio0_2 | GPIO | I/O | A18 | A17 |
| gpio0_20 | GPIO | I/O | B15 | D14 |
| gpio0_21 | GPIO | I/O | M18 | K16 |
| gpio0_22 | GPIO | I/O | V15 | U10 |
| gpio0_23 | GPIO | I/O | W16 | T10 |
| gpio0_26 | GPIO | I/O | T12 | T11 |
| gpio0_27 | GPIO | I/O | U12 | U12 |
| gpio0_28 | GPIO | I/O | L18 | K17 |
| gpio0_29 | GPIO | I/O | K18 | H18 |
| gpio0_3 | GPIO | I/O | B18 | B17 |
| gpio0_30 | GPIO | I/O | R15 | T17 |
| gpio0_31 | GPIO | I/O | W18 | U17 |
| gpio0_4 | GPIO | I/O | B17 | B16 |
| gpio0_5 | GPIO | I/O | A17 | A16 |
| gpio0_6 | GPIO | I/O | B16 | C15 |
| gpio0_7 | GPIO | I/O | E18 | C18 |
| gpio0_8 | GPIO | I/O | V6 | V2 |
| gpio0_9 | GPIO | I/O | U6 | V3 |

Table 4-9. General-Purpose IOs/GPIO1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| gpio1_0 | GPIO | I/O | W10 | U7 |
| gpio1_1 | GPIO | I/O | V9 | V7 |
| gpio1_10 | GPIO | I/O | E19 | E15 |
| gpio1_11 | GPIO | I/O | F17 | E16 |
| gpio1_12 | GPIO | I/O | U13 | T12 |
| gpio1_13 | GPIO | I/O | T13 | R12 |
| gpio1_14 | GPIO | I/O | W17 | V13 |
| gpio1_15 | GPIO | I/O | V17 | U13 |
| gpio1_16 | GPIO | I/O | NA | R13 |
| gpio1_17 | GPIO | I/O | NA | V14 |
| gpio1_18 | GPIO | I/O | NA | U14 |

Table 4-9. General-Purpose IOs/GPIO1 Signals Description (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| gpio1_19 | GPIO | I/O | NA | T14 |
| gpio1_2 | GPIO | I/O | V12 | R8 |
| gpio1_20 | GPIO | I/O | NA | R14 |
| gpio1_21 | GPIO | I/O | NA | V15 |
| gpio1_22 | GPIO | I/O | NA | U15 |
| gpio1_23 | GPIO | I/O | NA | T15 |
| gpio1_24 | GPIO | I/O | NA | V16 |
| gpio1_25 | GPIO | I/O | NA | U16 |
| gpio1_26 | GPIO | I/O | NA | T16 |
| gpio1_27 | GPIO | I/O | NA | V17 |
| gpio1_28 | GPIO | I/O | V18 | U18 |
| gpio1_29 | GPIO | I/O | W8 | V6 |
| gpio1_3 | GPIO | I/O | W13 | T8 |
| gpio1_30 | GPIO | I/O | V14 | U9 |
| gpio1_31 | GPIO | I/O | U15 | V9 |
| gpio1_4 | GPIO | I/O | V13 | U8 |
| gpio1_5 | GPIO | I/O | W14 | V8 |
| gpio1_6 | GPIO | I/O | U14 | R9 |
| gpio1_7 | GPIO | I/O | W15 | T9 |
| gpio1_8 | GPIO | I/O | F19 | E18 |
| gpio1_9 | GPIO | I/O | F18 | E17 |

Table 4-10. General-Purpose IOs/GPIO2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| gpio2_0 | GPIO | I/O | U17 | T13 |
| gpio2_1 | GPIO | I/O | V16 | V12 |
| gpio2_10 | GPIO | I/O | W2 | T1 |
| gpio2_11 | GPIO | I/O | W3 | T2 |
| gpio2_12 | GPIO | I/O | V3 | T3 |
| gpio2_13 | GPIO | I/O | U3 | T4 |
| gpio2_14 | GPIO | I/O | V4 | U1 |
| gpio2_15 | GPIO | I/O | W4 | U2 |
| gpio2_16 | GPIO | I/O | U5 | U3 |
| gpio2_17 | GPIO | I/O | V5 | U4 |
| gpio2_18 | GPIO | I/O | N17 | L17 |
| gpio2_19 | GPIO | I/O | N16 | L16 |
| gpio2_2 | GPIO | I/O | V10 | R7 |
| gpio2_20 | GPIO | I/O | P19 | L15 |
| gpio2_21 | GPIO | I/O | P18 | M16 |
| gpio2_22 | GPIO | I/O | U7 | U5 |
| gpio2_23 | GPIO | I/O | T7 | R5 |
| gpio2_24 | GPIO | I/O | W5 | V5 |
| gpio2_25 | GPIO | I/O | W7 | R6 |
| gpio2_26 | GPIO | I/O | H19 | F17 |
| gpio2_27 | GPIO | I/O | H18 | F18 |
| gpio2_28 | GPIO | I/O | H17 | G15 |

Table 4-10. General-Purpose IOs/GPIO2 Signals Description (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| gpio2_29 | GPIO | I/O | G18 | G16 |
| gpio2_3 | GPIO | I/O | W9 | T7 |
| gpio2_30 | GPIO | I/O | G19 | G17 |
| gpio2_31 | GPIO | I/O | G17 | G18 |
| gpio2_4 | GPIO | I/O | U8 | U6 |
| gpio2_5 | GPIO | I/O | V8 | T6 |
| gpio2_6 | GPIO | I/O | U1 | R1 |
| gpio2_7 | GPIO | I/O | U2 | R2 |
| gpio2_8 | GPIO | I/O | V1 | R3 |
| gpio2_9 | GPIO | I/O | V2 | R4 |

Table 4-11. General-Purpose IOs/GPIO3 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| gpio3_0 | GPIO | I/O | J19 | H16 |
| gpio3_1 | GPIO | I/O | J18 | H17 |
| gpio3_10 | GPIO | I/O | M19 | L18 |
| gpio3_13 | GPIO | I/O | NA | F15 |
| gpio3_14 | GPIO | I/O | NA | A13 |
| gpio3_15 | GPIO | I/O | NA | B13 |
| gpio3_16 | GPIO | I/O | NA | D12 |
| gpio3_17 | GPIO | I/O | NA | C12 |
| gpio3_18 | GPIO | I/O | NA | B12 |
| gpio3_19 | GPIO | I/O | NA | C13 |
| gpio3_2 | GPIO | I/O | K19 | J15 |
| gpio3_20 | GPIO | I/O | NA | D13 |
| gpio3_21 | GPIO | I/O | NA | A14 |
| gpio3_3 | GPIO | I/O | K17 | J16 |
| gpio3_4 | GPIO | I/O | L19 | J17 |
| gpio3_5 | GPIO | I/O | C18 | C17 |
| gpio3_6 | GPIO | I/O | B19 | C16 |
| gpio3_7 | GPIO | I/O | A15 | C14 |
| gpio3_8 | GPIO | I/O | D14 | B14 |
| gpio3_9 | GPIO | I/O | N19 | K18 |

4.3.3 Miscellaneous

Table 4-12. Miscellaneous/Miscellaneous Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|------------------|--|----------|---------------|---------------|
| clkout1 | Clock out1 | O | C15 | A15 |
| clkout2 | Clock out2 | O | B15 | D14 |
| ENZ_KALDO_1P8V | Active low enable input for internal CAP_VDD_RTC voltage regulator | I | A7 | B4 |
| EXT_WAKEUP | EXT_WAKEUP input | I | B5 | C5 |
| nNMI | External Interrupt to ARM Cortex-A8 core | I | C17 | B18 |
| nRESETIN_OUT | Active low Warm Reset | I/OD | A16 | A10 |
| OSC0_IN | High frequency oscillator input | I | W11 | V10 |
| OSC0_OUT | High frequency oscillator output | O | W12 | U11 |
| OSC1_IN | Low frequency (32.768 kHz) Real Time Clock oscillator input | I | A6 | A6 |
| OSC1_OUT | Low frequency (32.768 kHz) Real Time Clock oscillator output | O | A5 | A4 |
| PMIC_POWER_EN | PMIC_POWER_EN output | O | C7 | C6 |
| porz | Active low Power on Reset | I | E15 | B15 |
| RTC_PORz | Active low RTC reset input | I | B7 | B5 |
| tclkin | Timer Clock In | I | B15 | D14 |
| xdma_event_intr0 | External DMA Event or Interrupt 0 | I | C15 | A15 |
| xdma_event_intr1 | External DMA Event or Interrupt 1 | I | B15 | D14 |
| xdma_event_intr2 | External DMA Event or Interrupt 2 | I | B16, E18, K18 | C15, C18, H18 |

4.3.3.1 eCAP

Table 4-13. eCAP/eCAP0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-------------------|---|----------|--------------|--------------|
| eCAP0_in_PWM0_out | Enhanced Capture 0 input or Auxiliary PWM0 output | I/O | E18 | C18 |

Table 4-14. eCAP/eCAP1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-------------------|---|----------|---------------|---------------|
| eCAP1_in_PWM1_out | Enhanced Capture 1 input or Auxiliary PWM1 output | I/O | B16, B19, F17 | C15, C16, E16 |

Table 4-15. eCAP/eCAP2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-------------------|---|----------|--------------|---------------|
| eCAP2_in_PWM2_out | Enhanced Capture 2 input or Auxiliary PWM2 output | I/O | C18, E19 | C12, C17, E15 |

4.3.3.2 eHRPWM
Table 4-16. eHRPWM/eHRPWM0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|------------------------|--|----------|--------------|------------------|
| ehrpwm0A | eHRPWM0 A output. | O | A18 | A13, A17 |
| ehrpwm0B | eHRPWM0 B output. | O | B18 | B13, B17 |
| ehrpwm0_synci | Sync input to eHRPWM0 module from an external pin | I | A17 | A16, C12 |
| ehrpwm0_synco | Sync Output from eHRPWM0 module to an external pin | O | U12, V2, W4 | R4, U12, U2, V14 |
| ehrpwm0_tripzone_input | eHRPWM0 trip zone input | I | B17 | B16, D12 |

Table 4-17. eHRPWM/eHRPWM1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|------------------------|-------------------------|----------|--------------|--------------|
| ehrpwm1A | eHRPWM1 A output. | O | U5 | U14, U3 |
| ehrpwm1B | eHRPWM1 B output. | O | V5 | T14, U4 |
| ehrpwm1_tripzone_input | eHRPWM1 trip zone input | I | V4 | R13, U1 |

Table 4-18. eHRPWM/eHRPWM2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|------------------------|-------------------------|----------|--------------|--------------|
| ehrpwm2A | eHRPWM2 A output. | O | U1, V15 | R1, U10 |
| ehrpwm2B | eHRPWM2 B output. | O | U2, W16 | R2, T10 |
| ehrpwm2_tripzone_input | eHRPWM2 trip zone input | I | T12, V1 | R3, T11 |

4.3.3.3 eQEP

Table 4-19. eQEP/eQEP0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------|----------|--------------|--------------|
| eQEP0A_in | eQEP0A quadrature input | I | M18 | B12, K16 |
| eQEP0B_in | eQEP0B quadrature input | I | L18 | C13, K17 |
| eQEP0_index | eQEP0 index. | I/O | K17 | D13, J16 |
| eQEP0_strobe | eQEP0 strobe. | I/O | P19 | A14, L15 |

Table 4-20. eQEP/eQEP1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------|----------|--------------|--------------|
| eQEP1A_in | eQEP1A quadrature input | I | V6 | R14, V2 |
| eQEP1B_in | eQEP1B quadrature input | I | U6 | V15, V3 |
| eQEP1_index | eQEP1 index. | I/O | W6 | U15, V4 |
| eQEP1_strobe | eQEP1 strobe. | I/O | V7 | T15, T5 |

Table 4-21. eQEP/eQEP2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------|----------|--------------|--------------|
| eQEP2A_in | eQEP2A quadrature input | I | U13, W2 | T1, T12 |
| eQEP2B_in | eQEP2B quadrature input | I | T13, W3 | R12, T2 |
| eQEP2_index | eQEP2 index. | I/O | V3, W17 | T3, V13 |
| eQEP2_strobe | eQEP2 strobe. | I/O | U3, V17 | T4, U13 |

4.3.3.4 Timer

Table 4-22. Timer/Timer4 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------------|----------|-----------------------|----------------------|
| timer4 | Timer trigger event / PWM out | I/O | C15, C18, K17, V10 | A15, C17, J16, R7 |

Table 4-23. Timer/Timer5 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------------|----------|----------------------|----------------------|
| timer5 | Timer trigger event / PWM out | I/O | D19, H19, R19, V8 | D17, F17, M18, T6 |

Table 4-24. Timer/Timer6 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------------|----------|----------------------|----------------------|
| timer6 | Timer trigger event / PWM out | I/O | E17, H18, P17, U8 | D18, F18, M17, U6 |

Table 4-25. Timer/Timer7 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------------|----------|----------------------|----------------------|
| timer7 | Timer trigger event / PWM out | I/O | B15, B19, F19, W9 | C16, D14, E18, T7 |

4.3.4 PRU-ICSS

Table 4-26. PRU-ICSS/eCAP Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------------------|---|----------|--------------|--------------|
| pr1_ecap0_ecap_capin_apwm_o | Enhanced capture input or Auxiliary PWM out | I/O | E18, V17 | C18, U13 |

Table 4-27. PRU-ICSS/ECAT Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|--------------------|-----------------|----------|--------------|--------------|
| pr1_edc_latch0_in | Data In | I | E17 | D18 |
| pr1_edc_latch1_in | Data In | I | D19 | D17 |
| pr1_edc_sync0_out | Data Out | O | F19 | E18 |
| pr1_edc_sync1_out | Data Out | O | F18 | E17 |
| pr1_edio_data_in0 | Data In | I | B17 | B16 |
| pr1_edio_data_in1 | Data In | I | A17 | A16 |
| pr1_edio_data_in2 | Data In | I | U7 | U5 |
| pr1_edio_data_in3 | Data In | I | T7 | R5 |
| pr1_edio_data_in4 | Data In | I | W5 | V5 |
| pr1_edio_data_in5 | Data In | I | W7 | R6 |
| pr1_edio_data_in6 | Data In | I | V14, V3 | T3, U9 |
| pr1_edio_data_in7 | Data In | I | U15, U3 | T4, V9 |
| pr1_edio_data_out0 | Data Out | O | B17 | B16 |
| pr1_edio_data_out1 | Data Out | O | A17 | A16 |
| pr1_edio_data_out2 | Data Out | O | U7 | U5 |
| pr1_edio_data_out3 | Data Out | O | T7 | R5 |
| pr1_edio_data_out4 | Data Out | O | W5 | V5 |
| pr1_edio_data_out5 | Data Out | O | W7 | R6 |
| pr1_edio_data_out6 | Data Out | O | V14, V3 | T3, U9 |
| pr1_edio_data_out7 | Data Out | O | U15, U3 | T4, V9 |
| pr1_edio_latch_in | Latch In | I | B18 | B17 |
| pr1_edio_sof | Start of Frame | O | A18 | A17 |

Table 4-28. PRU-ICSS/MDIO Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| pr1_mdio_data | MDIO Data | I/O | U17 | T13 |
| pr1_mdio_mdclk | MDIO Clk | O | V16 | V12 |

Table 4-29. PRU-ICSS/MII0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|------------------------|----------|--------------|--------------|
| pr1_mii0_col | MII Collision Detect | I | W16 | T10 |
| pr1_mii0_crs | MII Carrier Sense | I | U17, W5 | T13, V5 |
| pr1_mii0_rxd0 | MII Receive Data bit 0 | I | V5 | U4 |
| pr1_mii0_rxd1 | MII Receive Data bit 1 | I | U5 | U3 |
| pr1_mii0_rxd2 | MII Receive Data bit 2 | I | W4 | U2 |
| pr1_mii0_rxd3 | MII Receive Data bit 3 | I | V4 | U1 |
| pr1_mii0_rxdv | MII Receive Data Valid | I | V7 | T5 |
| pr1_mii0_rxer | MII Receive Data Error | I | U6 | V3 |

Table 4-29. PRU-ICSS/MII0 Signals Description (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------|----------|--------------|--------------|
| pr1_mii0_rxlink | MII Receive Link | I | V6 | V2 |
| pr1_mii0_txd0 | MII Transmit Data bit 0 | O | W17, W3 | T2, V13 |
| pr1_mii0_txd1 | MII Transmit Data bit 1 | O | T13, W2 | R12, T1 |
| pr1_mii0_txd2 | MII Transmit Data bit 2 | O | U13, V2 | R4, T12 |
| pr1_mii0_txd3 | MII Transmit Data bit 3 | O | U12, V1 | R3, U12 |
| pr1_mii0_txen | MII Transmit Enable | O | T12, U2 | R2, T11 |
| pr1_mii_mr0_clk | MII Receive Clock | I | W6 | V4 |
| pr1_mii_mt0_clk | MII Transmit Clock | I | U1, V15 | R1, U10 |

Table 4-30. PRU-ICSS/MII1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------|----------|--------------|--------------|
| pr1_mii1_col | MII Collision Detect | I | R15 | T17 |
| pr1_mii1_crs | MII Carrier Sense | I | V16, W7 | R6, V12 |
| pr1_mii1_rxd0 | MII Receive Data bit 0 | I | NA | V16 |
| pr1_mii1_rxd1 | MII Receive Data bit 1 | I | NA | T15 |
| pr1_mii1_rxd2 | MII Receive Data bit 2 | I | NA | U15 |
| pr1_mii1_rxd3 | MII Receive Data bit 3 | I | NA | V15 |
| pr1_mii1_rxdv | MII Receive Data Valid | I | NA | T16 |
| pr1_mii1_rxer | MII Receive Data Error | I | NA | V17 |
| pr1_mii1_rxlink | MII Receive Link | I | V18 | U18 |
| pr1_mii1_txd0 | MII Transmit Data bit 0 | O | NA | R14 |
| pr1_mii1_txd1 | MII Transmit Data bit 1 | O | NA | T14 |
| pr1_mii1_txd2 | MII Transmit Data bit 2 | O | NA | U14 |
| pr1_mii1_txd3 | MII Transmit Data bit 3 | O | NA | V14 |
| pr1_mii1_txen | MII Transmit Enable | O | W18 | U17 |
| pr1_mii_mr1_clk | MII Receive Clock | I | NA | U16 |
| pr1_mii_mt1_clk | MII Transmit Clock | I | NA | R13 |

Table 4-31. PRU-ICSS/UART0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|----------------------|----------|--------------|--------------|
| pr1_uart0_cts_n | UART Clear to Send | I | A18, E17 | A17, D18 |
| pr1_uart0_rts_n | UART Request to Send | O | B18, D19 | B17, D17 |
| pr1_uart0_rxd | UART Receive Data | I | B17, D18 | B16, D16 |
| pr1_uart0_txd | UART Transmit Data | O | A17, C19 | A16, D15 |

4.3.4.1 PRU0

Table 4-32. PRU0/General-Purpose Inputs Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|---------------------|-----------------------------|----------|--------------|--------------|
| pr1_pru0_pru_r31_0 | PRU0 Data In | I | NA | A13 |
| pr1_pru0_pru_r31_1 | PRU0 Data In | I | NA | B13 |
| pr1_pru0_pru_r31_10 | PRU0 Data In | I | H17 | G15 |
| pr1_pru0_pru_r31_11 | PRU0 Data In | I | G18 | G16 |
| pr1_pru0_pru_r31_12 | PRU0 Data In | I | G19 | G17 |
| pr1_pru0_pru_r31_13 | PRU0 Data In | I | G17 | G18 |
| pr1_pru0_pru_r31_14 | PRU0 Data In | I | W17 | V13 |
| pr1_pru0_pru_r31_15 | PRU0 Data In | I | V17 | U13 |
| pr1_pru0_pru_r31_16 | PRU0 Data In Capture Enable | I | B15, C19 | D14, D15 |
| pr1_pru0_pru_r31_2 | PRU0 Data In | I | NA | D12 |
| pr1_pru0_pru_r31_3 | PRU0 Data In | I | NA | C12 |
| pr1_pru0_pru_r31_4 | PRU0 Data In | I | NA | B12 |
| pr1_pru0_pru_r31_5 | PRU0 Data In | I | NA | C13 |
| pr1_pru0_pru_r31_6 | PRU0 Data In | I | NA | D13 |
| pr1_pru0_pru_r31_7 | PRU0 Data In | I | NA | A14 |
| pr1_pru0_pru_r31_8 | PRU0 Data In | I | H19 | F17 |
| pr1_pru0_pru_r31_9 | PRU0 Data In | I | H18 | F18 |

Table 4-33. PRU0/General-Purpose Outputs Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|---------------------|-----------------|----------|--------------|--------------|
| pr1_pru0_pru_r30_0 | PRU0 Data Out | O | NA | A13 |
| pr1_pru0_pru_r30_1 | PRU0 Data Out | O | NA | B13 |
| pr1_pru0_pru_r30_10 | PRU0 Data Out | O | H17 | G15 |
| pr1_pru0_pru_r30_11 | PRU0 Data Out | O | G18 | G16 |
| pr1_pru0_pru_r30_12 | PRU0 Data Out | O | G19 | G17 |
| pr1_pru0_pru_r30_13 | PRU0 Data Out | O | G17 | G18 |
| pr1_pru0_pru_r30_14 | PRU0 Data Out | O | U13 | T12 |
| pr1_pru0_pru_r30_15 | PRU0 Data Out | O | T13 | R12 |
| pr1_pru0_pru_r30_2 | PRU0 Data Out | O | NA | D12 |
| pr1_pru0_pru_r30_3 | PRU0 Data Out | O | NA | C12 |
| pr1_pru0_pru_r30_4 | PRU0 Data Out | O | NA | B12 |
| pr1_pru0_pru_r30_5 | PRU0 Data Out | O | NA | C13 |
| pr1_pru0_pru_r30_6 | PRU0 Data Out | O | NA | D13 |
| pr1_pru0_pru_r30_7 | PRU0 Data Out | O | NA | A14 |
| pr1_pru0_pru_r30_8 | PRU0 Data Out | O | H19 | F17 |
| pr1_pru0_pru_r30_9 | PRU0 Data Out | O | H18 | F18 |

4.3.4.2 PRU1
Table 4-34. PRU1/General-Purpose Inputs Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|---------------------|-----------------------------|----------|--------------|--------------|
| pr1_pru1_pru_r31_0 | PRU1 Data In | I | U1 | R1 |
| pr1_pru1_pru_r31_1 | PRU1 Data In | I | U2 | R2 |
| pr1_pru1_pru_r31_10 | PRU1 Data In | I | W5 | V5 |
| pr1_pru1_pru_r31_11 | PRU1 Data In | I | W7 | R6 |
| pr1_pru1_pru_r31_12 | PRU1 Data In | I | V14 | U9 |
| pr1_pru1_pru_r31_13 | PRU1 Data In | I | U15 | V9 |
| pr1_pru1_pru_r31_14 | PRU1 Data In | I | E19 | E15 |
| pr1_pru1_pru_r31_15 | PRU1 Data In | I | F17 | E16 |
| pr1_pru1_pru_r31_16 | PRU1 Data In Capture Enable | I | C15, D18 | A15, D16 |
| pr1_pru1_pru_r31_2 | PRU1 Data In | I | V1 | R3 |
| pr1_pru1_pru_r31_3 | PRU1 Data In | I | V2 | R4 |
| pr1_pru1_pru_r31_4 | PRU1 Data In | I | W2 | T1 |
| pr1_pru1_pru_r31_5 | PRU1 Data In | I | W3 | T2 |
| pr1_pru1_pru_r31_6 | PRU1 Data In | I | V3 | T3 |
| pr1_pru1_pru_r31_7 | PRU1 Data In | I | U3 | T4 |
| pr1_pru1_pru_r31_8 | PRU1 Data In | I | U7 | U5 |
| pr1_pru1_pru_r31_9 | PRU1 Data In | I | T7 | R5 |

Table 4-35. PRU1/General-Purpose Outputs Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|---------------------|-----------------|----------|--------------|--------------|
| pr1_pru1_pru_r30_0 | PRU1 Data Out | O | U1 | R1 |
| pr1_pru1_pru_r30_1 | PRU1 Data Out | O | U2 | R2 |
| pr1_pru1_pru_r30_10 | PRU1 Data Out | O | W5 | V5 |
| pr1_pru1_pru_r30_11 | PRU1 Data Out | O | W7 | R6 |
| pr1_pru1_pru_r30_12 | PRU1 Data Out | O | V14 | U9 |
| pr1_pru1_pru_r30_13 | PRU1 Data Out | O | U15 | V9 |
| pr1_pru1_pru_r30_14 | PRU1 Data Out | O | E19 | E15 |
| pr1_pru1_pru_r30_15 | PRU1 Data Out | O | F17 | E16 |
| pr1_pru1_pru_r30_2 | PRU1 Data Out | O | V1 | R3 |
| pr1_pru1_pru_r30_3 | PRU1 Data Out | O | V2 | R4 |
| pr1_pru1_pru_r30_4 | PRU1 Data Out | O | W2 | T1 |
| pr1_pru1_pru_r30_5 | PRU1 Data Out | O | W3 | T2 |
| pr1_pru1_pru_r30_6 | PRU1 Data Out | O | V3 | T3 |
| pr1_pru1_pru_r30_7 | PRU1 Data Out | O | U3 | T4 |
| pr1_pru1_pru_r30_8 | PRU1 Data Out | O | U7 | U5 |
| pr1_pru1_pru_r30_9 | PRU1 Data Out | O | T7 | R5 |

4.3.5 Removable Media Interfaces

Table 4-36. Removable Media Interfaces/MMC0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------------------|----------|--------------|---------------|
| mmc0_clk | MMC/SD/SDIO Clock | I/O | G19 | G17 |
| mmc0_cmd | MMC/SD/SDIO Command | I/O | G17 | G18 |
| mmc0_dat0 | MMC/SD/SDIO Data Bus | I/O | G18 | G16 |
| mmc0_dat1 | MMC/SD/SDIO Data Bus | I/O | H17 | G15 |
| mmc0_dat2 | MMC/SD/SDIO Data Bus | I/O | H18 | F18 |
| mmc0_dat3 | MMC/SD/SDIO Data Bus | I/O | H19 | F17 |
| mmc0_dat4 | MMC/SD/SDIO Data Bus | I/O | N16 | L16 |
| mmc0_dat5 | MMC/SD/SDIO Data Bus | I/O | N17 | L17 |
| mmc0_dat6 | MMC/SD/SDIO Data Bus | I/O | M19 | L18 |
| mmc0_dat7 | MMC/SD/SDIO Data Bus | I/O | N19 | K18 |
| mmc0_pow | MMC/SD Power Switch Control | O | B16, K18 | C15, H18 |
| mmc0_sdcd | SD Card Detect | I | B16, P17 | A13, C15, M17 |
| mmc0_sdwps | SD Write Protect | I | E18, R19 | B12, C18, M18 |

Table 4-37. Removable Media Interfaces/MMC1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|----------------------|----------|---------------|--------------|
| mmc1_clk | MMC/SD/SDIO Clock | I/O | L18, R19, V14 | K17, M18, U9 |
| mmc1_cmd | MMC/SD/SDIO Command | I/O | M18, P17, U15 | K16, M17, V9 |
| mmc1_dat0 | MMC/SD/SDIO Data Bus | I/O | N19, V15, W10 | K18, U10, U7 |
| mmc1_dat1 | MMC/SD/SDIO Data Bus | I/O | M19, V9, W16 | L18, T10, V7 |
| mmc1_dat2 | MMC/SD/SDIO Data Bus | I/O | N17, T12, V12 | L17, R8, T11 |
| mmc1_dat3 | MMC/SD/SDIO Data Bus | I/O | N16, U12, W13 | L16, T8, U12 |
| mmc1_dat4 | MMC/SD/SDIO Data Bus | I/O | U13, V13 | T12, U8 |
| mmc1_dat5 | MMC/SD/SDIO Data Bus | I/O | T13, W14 | R12, V8 |
| mmc1_dat6 | MMC/SD/SDIO Data Bus | I/O | U14, W17 | R9, V13 |
| mmc1_dat7 | MMC/SD/SDIO Data Bus | I/O | V17, W15 | T9, U13 |
| mmc1_sdcd | SD Card Detect | I | R15 | B13, T17 |
| mmc1_sdwps | SD Write Protect | I | B17, D18 | B16, D16 |

Table 4-38. Removable Media Interfaces/MMC2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|----------------------|----------|---------------|---------------|
| mmc2_clk | MMC/SD/SDIO Clock | I/O | P19, R19, V16 | L15, M18, V12 |
| mmc2_cmd | MMC/SD/SDIO Command | I/O | K17, P17, U17 | J16, M17, T13 |
| mmc2_dat0 | MMC/SD/SDIO Data Bus | I/O | L19, U13 | J17, T12, V14 |
| mmc2_dat1 | MMC/SD/SDIO Data Bus | I/O | M17, T13 | J18, R12, U14 |
| mmc2_dat2 | MMC/SD/SDIO Data Bus | I/O | N18, W17 | K15, T14, V13 |
| mmc2_dat3 | MMC/SD/SDIO Data Bus | I/O | J19, V17, V18 | H16, U13, U18 |
| mmc2_dat4 | MMC/SD/SDIO Data Bus | I/O | V15 | U10, U15 |
| mmc2_dat5 | MMC/SD/SDIO Data Bus | I/O | W16 | T10, T15 |
| mmc2_dat6 | MMC/SD/SDIO Data Bus | I/O | T12 | T11, V16 |
| mmc2_dat7 | MMC/SD/SDIO Data Bus | I/O | U12 | U12 |
| mmc2_sdcd | SD Card Detect | I | W18 | D12, U17 |
| mmc2_sdwps | SD Write Protect | I | A17, C19 | A16, D15 |

4.3.6 Serial Communication Interfaces

4.3.6.1 CAN

Table 4-39. CAN/DCAN0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------|----------|---------------|---------------|
| dcan0_rx | DCAN0 Receive Data | I | D19, F17, N18 | D17, E16, K15 |
| dcan0_tx | DCAN0 Transmit Data | O | E17, E19, M17 | D18, E15, J18 |

Table 4-40. CAN/DCAN1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------|----------|---------------|---------------|
| dcan1_rx | DCAN1 Receive Data | I | C19, F18, G17 | D15, E17, G18 |
| dcan1_tx | DCAN1 Transmit Data | O | D18, F19, G19 | D16, E18, G17 |

4.3.6.2 GEMAC_CPSW

Table 4-41. GEMAC_CPSW/MDIO Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| mdio_clk | MDIO Clk | O | R19 | M18 |
| mdio_data | MDIO Data | I/O | P17 | M17 |

Table 4-42. GEMAC_CPSW/MII1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------|----------|--------------|--------------|
| gmii1_col | MII Colision | I | J19 | H16 |
| gmii1_crs | MII Carrier Sense | I | J18 | H17 |
| gmii1_rxclk | MII Receive Clock | I | M19 | L18 |
| gmii1_rxd0 | MII Receive Data bit 0 | I | P18 | M16 |
| gmii1_rxd1 | MII Receive Data bit 1 | I | P19 | L15 |
| gmii1_rxd2 | MII Receive Data bit 2 | I | N16 | L16 |
| gmii1_rxd3 | MII Receive Data bit 3 | I | N17 | L17 |
| gmii1_rxdv | MII Receive Data Valid | I | L19 | J17 |
| gmii1_rxer | MII Receive Data Error | I | K19 | J15 |
| gmii1_txclk | MII Transmit Clock | I | N19 | K18 |
| gmii1_txd0 | MII Transmit Data bit 0 | O | L18 | K17 |
| gmii1_txd1 | MII Transmit Data bit 1 | O | M18 | K16 |
| gmii1_txd2 | MII Transmit Data bit 2 | O | N18 | K15 |
| gmii1_txd3 | MII Transmit Data bit 3 | O | M17 | J18 |
| gmii1_txen | MII Transmit Enable | O | K17 | J16 |

Table 4-43. GEMAC_CPSW/MII2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-------------------------|----------|--------------|--------------|
| gmii2_col | MII Colision | I | V18 | U18 |
| gmii2_crs | MII Carrier Sense | I | R15 | T17 |
| gmii2_rxclk | MII Receive Clock | I | NA | T15 |
| gmii2_rxd0 | MII Receive Data bit 0 | I | NA | V17 |
| gmii2_rxd1 | MII Receive Data bit 1 | I | NA | T16 |
| gmii2_rxd2 | MII Receive Data bit 2 | I | NA | U16 |
| gmii2_rxd3 | MII Receive Data bit 3 | I | NA | V16 |
| gmii2_rxdv | MII Receive Data Valid | I | NA | V14 |
| gmii2_rxer | MII Receive Data Error | I | W18 | U17 |
| gmii2_txclk | MII Transmit Clock | I | NA | U15 |
| gmii2_txd0 | MII Transmit Data bit 0 | O | NA | V15 |
| gmii2_txd1 | MII Transmit Data bit 1 | O | NA | R14 |
| gmii2_txd2 | MII Transmit Data bit 2 | O | NA | T14 |
| gmii2_txd3 | MII Transmit Data bit 3 | O | NA | U14 |
| gmii2_txen | MII Transmit Enable | O | NA | R13 |

Table 4-44. GEMAC_CPSW/RGMII1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------|----------|--------------|--------------|
| rgmii1_rclk | RGMII Receive Clock | I | M19 | L18 |

Table 4-44. GEMAC_CPSW/RGMII1 Signals Description (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------------|----------|--------------|--------------|
| rgmii1_rctl | RGMII Receive Control | I | L19 | J17 |
| rgmii1_rd0 | RGMII Receive Data bit 0 | I | P18 | M16 |
| rgmii1_rd1 | RGMII Receive Data bit 1 | I | P19 | L15 |
| rgmii1_rd2 | RGMII Receive Data bit 2 | I | N16 | L16 |
| rgmii1_rd3 | RGMII Receive Data bit 3 | I | N17 | L17 |
| rgmii1_tclk | RGMII Transmit Clock | O | N19 | K18 |
| rgmii1_tctl | RGMII Transmit Control | O | K17 | J16 |
| rgmii1_td0 | RGMII Transmit Data bit 0 | O | L18 | K17 |
| rgmii1_td1 | RGMII Transmit Data bit 1 | O | M18 | K16 |
| rgmii1_td2 | RGMII Transmit Data bit 2 | O | N18 | K15 |
| rgmii1_td3 | RGMII Transmit Data bit 3 | O | M17 | J18 |

Table 4-45. GEMAC_CPSW/RGMII2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------------|----------|--------------|--------------|
| rgmii2_rclk | RGMII Receive Clock | I | NA | T15 |
| rgmii2_rctl | RGMII Receive Control | I | NA | V14 |
| rgmii2_rd0 | RGMII Receive Data bit 0 | I | NA | V17 |
| rgmii2_rd1 | RGMII Receive Data bit 1 | I | NA | T16 |
| rgmii2_rd2 | RGMII Receive Data bit 2 | I | NA | U16 |
| rgmii2_rd3 | RGMII Receive Data bit 3 | I | NA | V16 |
| rgmii2_tclk | RGMII Transmit Clock | O | NA | U15 |
| rgmii2_tctl | RGMII Transmit Control | O | NA | R13 |
| rgmii2_td0 | RGMII Transmit Data bit 0 | O | NA | V15 |
| rgmii2_td1 | RGMII Transmit Data bit 1 | O | NA | R14 |
| rgmii2_td2 | RGMII Transmit Data bit 2 | O | NA | T14 |
| rgmii2_td3 | RGMII Transmit Data bit 3 | O | NA | U14 |

Table 4-46. GEMAC_CPSW/RMII1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------------------|----------|--------------|--------------|
| rmii1_crs_dv | RMII Carrier Sense / Data Valid | I | J18 | H17 |
| rmii1_refclk | RMII Reference Clock | I/O | K18 | H18 |
| rmii1_rxd0 | RMII Receive Data bit 0 | I | P18 | M16 |
| rmii1_rxd1 | RMII Receive Data bit 1 | I | P19 | L15 |
| rmii1_rxer | RMII Receive Data Error | I | K19 | J15 |
| rmii1_txd0 | RMII Transmit Data bit 0 | O | L18 | K17 |
| rmii1_txd1 | RMII Transmit Data bit 1 | O | M18 | K16 |
| rmii1_txen | RMII Transmit Enable | O | K17 | J16 |

Table 4-47. GEMAC_CPSW/RMII2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|---------------------------------|----------|--------------|--------------|
| rmii2_crs_dv | RMII Carrier Sense / Data Valid | I | R15, U17 | T13, T17 |
| rmii2_refclk | RMII Reference Clock | I/O | J19 | H16 |
| rmii2_rxd0 | RMII Receive Data bit 0 | I | NA | V17 |
| rmii2_rxd1 | RMII Receive Data bit 1 | I | NA | T16 |

Table 4-47. GEMAC_CPSW/RMII2 Signals Description (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|--------------------------|----------|--------------|--------------|
| rmi2_rxer | RMII Receive Data Error | I | W18 | U17 |
| rmi2_txd0 | RMII Transmit Data bit 0 | O | NA | V15 |
| rmi2_txd1 | RMII Transmit Data bit 1 | O | NA | R14 |
| rmi2_txen | RMII Transmit Enable | O | NA | R13 |

4.3.6.3 I2C
Table 4-48. I2C/I2C0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| I2C0_SCL | I2C0 Clock | I/OD | B19 | C16 |
| I2C0_SDA | I2C0 Data | I/OD | C18 | C17 |

Table 4-49. I2C/I2C1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------------|--------------------|
| I2C1_SCL | I2C1 Clock | I/OD | A17, C19, F18, K19 | A16, D15, E17, J15 |
| I2C1_SDA | I2C1 Data | I/OD | B17, D18, F19, J18 | B16, D16, E18, H17 |

Table 4-50. I2C/I2C2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|---------------|---------------|
| I2C2_SCL | I2C2 Clock | I/OD | B18, D19, F17 | B17, D17, E16 |
| I2C2_SDA | I2C2 Data | I/OD | A18, E17, E19 | A17, D18, E15 |

4.3.6.4 McASP

Table 4-51. McASP/MCASP0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|------------------------------|----------|--------------|-----------------------|
| mcasp0_aclkr | McASP0 Receive Bit Clock | I/O | L19, V18, V6 | B12, J17, U18, V2 |
| mcasp0_aclkx | McASP0 Transmit Bit Clock | I/O | N19, V4 | A13, K18, U1, V16 |
| mcasp0_ahclkr | McASP0 Receive Master Clock | I/O | V5 | C12, U4 |
| mcasp0_ahclkx | McASP0 Transmit Master Clock | I/O | N18, V7 | A14, K15, T5 |
| mcasp0_axr0 | McASP0 Serial Data (IN/OUT) | I/O | N17, U5 | D12, L17, T16, U3 |
| mcasp0_axr1 | McASP0 Serial Data (IN/OUT) | I/O | N16, W6 | D13, L16, V17, V4 |
| mcasp0_axr2 | McASP0 Serial Data (IN/OUT) | I/O | J19, V5, V6 | B12, C12, H16, U4, V2 |
| mcasp0_axr3 | McASP0 Serial Data (IN/OUT) | I/O | P18, U6, V7 | A14, C13, M16, T5, V3 |
| mcasp0_fsr | McASP0 Receive Frame Sync | I/O | M17, U6, V16 | C13, J18, V12, V3 |
| mcasp0_fsx | McASP0 Transmit Frame Sync | I/O | M19, W4 | B13, L18, U16, U2 |

Table 4-52. McASP/MCASP1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|------------------------------|----------|--------------|---------------|
| mcasp1_aclkr | McASP1 Receive Bit Clock | I/O | L18, P18 | K17, M16 |
| mcasp1_aclkx | McASP1 Transmit Bit Clock | I/O | J18, L19 | B12, H17, J17 |
| mcasp1_ahclkr | McASP1 Receive Master Clock | I/O | P18 | M16 |
| mcasp1_ahclkx | McASP1 Transmit Master Clock | I/O | K18, P18 | H18, M16 |
| mcasp1_axr0 | McASP1 Serial Data (IN/OUT) | I/O | K17, N18 | D13, J16, K15 |
| mcasp1_axr1 | McASP1 Serial Data (IN/OUT) | I/O | M18 | A14, K16 |
| mcasp1_axr2 | McASP1 Serial Data (IN/OUT) | I/O | J19, L18 | H16, K17 |
| mcasp1_axr3 | McASP1 Serial Data (IN/OUT) | I/O | K18, P19 | H18, L15 |
| mcasp1_fsr | McASP1 Receive Frame Sync | I/O | M18, P19 | K16, L15 |
| mcasp1_fsx | McASP1 Transmit Frame Sync | I/O | K19, M17 | C13, J15, J18 |

4.3.6.5 SPI
Table 4-53. SPI/SPI0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| spi0_cs0 | SPI Chip Select | I/O | A17 | A16 |
| spi0_cs1 | SPI Chip Select | I/O | B16 | C15 |
| spi0_d0 | SPI Data | I/O | B18 | B17 |
| spi0_d1 | SPI Data | I/O | B17 | B16 |
| spi0_sclk | SPI Clock | I/O | A18 | A17 |

Table 4-54. SPI/SPI1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|-----------------|----------|--------------------|-------------------------|
| spi1_cs0 | SPI Chip Select | I/O | E17, E19, F18, K18 | C12, D18, E15, E17, H18 |
| spi1_cs1 | SPI Chip Select | I/O | C15, D19, E18, F17 | A15, C18, D17, E16 |
| spi1_d0 | SPI Data | I/O | F19, J18 | B13, E18, H17 |
| spi1_d1 | SPI Data | I/O | F18, K19 | D12, E17, J15 |
| spi1_sclk | SPI Clock | I/O | E18, J19 | A13, C18, H16 |

4.3.6.6 UART

Table 4-55. UART/UART0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|----------------------|----------|--------------|--------------|
| uart0_ctsn | UART Clear to Send | I | F19 | E18 |
| uart0_rtsn | UART Request to Send | O | F18 | E17 |
| uart0_rxd | UART Receive Data | I | E19 | E15 |
| uart0_txd | UART Transmit Data | O | F17 | E16 |

Table 4-56. UART/UART1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|--------------------------|----------|--------------|--------------|
| uart1_ctsn | UART Clear to Send | I | E17 | D18 |
| uart1_dcdn | UART Data Carrier Detect | I | H19, N19 | F17, K18 |
| uart1_dsrn | UART Data Set Ready | I | H18, M19 | F18, L18 |
| uart1_dtrn | UART Data Terminal Ready | O | H17, N17 | G15, L17 |
| uart1_rin | UART Ring Indicator | I | G18, N16 | G16, L16 |
| uart1_rtsn | UART Request to Send | O | D19 | D17 |
| uart1_rxd | UART Receive Data | I | D18 | D16 |
| uart1_txd | UART Transmit Data | O | C19 | D15 |

Table 4-57. UART/UART2 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|----------------------|----------|-----------------------|-----------------------|
| uart2_ctsn | UART Clear to Send | I | C18, V4 | C17, U1 |
| uart2_rtsn | UART Request to Send | O | B19, W4 | C16, U2 |
| uart2_rxd | UART Receive Data | I | A18, G19, J18, N19 | A17, G17, H17, K18 |
| uart2_txd | UART Transmit Data | O | B18, G17, K19, M19 | B17, G18, J15, L18 |

Table 4-58. UART/UART3 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|----------------------|----------|---------------|---------------|
| uart3_ctsn | UART Clear to Send | I | G19, P17, U5 | G17, M17, U3 |
| uart3_rtsn | UART Request to Send | O | G17, R19, V5 | G18, M18, U4 |
| uart3_rxd | UART Receive Data | I | B16, H17, N17 | C15, G15, L17 |
| uart3_txd | UART Transmit Data | O | E18, G18, N16 | C18, G16, L16 |

Table 4-59. UART/UART4 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|----------------------|----------|---------------|---------------|
| uart4_ctsn | UART Clear to Send | I | H19, V6 | F17, V2 |
| uart4_rtsn | UART Request to Send | O | H18, U6 | F18, V3 |
| uart4_rxd | UART Receive Data | I | F19, M17, R15 | E18, J18, T17 |
| uart4_txd | UART Transmit Data | O | F18, N18, W18 | E17, K15, U17 |

Table 4-60. UART/UART5 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|----------------------|----------|-------------------|-------------------|
| uart5_ctsn | UART Clear to Send | I | H17, J18, W6 | G15, H17, V4 |
| uart5_rtsn | UART Request to Send | O | G18, K19, V7 | G16, J15, T5 |
| uart5_rxd | UART Receive Data | I | J19, P17, W4, W6 | H16, M17, U2, V4 |
| uart5_txd | UART Transmit Data | O | K18, L19, R19, V4 | H18, J17, M18, U1 |

4.3.6.7 USB

Table 4-61. USB/USB0 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|--|----------|--------------|--------------|
| USB0_CE | USB0 Active high Charger Enable output | A | T18 | M15 |
| USB0_DM | USB0 Data minus | A | U18 | N18 |
| USB0_DP | USB0 Data plus | A | U19 | N17 |
| USB0_DRVVBUS | USB0 Active high VBUS control output | O | G16 | F16 |
| USB0_ID | USB0 OTG ID (Micro-A or Micro-B Plug) | A | V19 | P16 |
| USB0_VBUS | USB0 VBUS | A | T19 | P15 |

Table 4-62. USB/USB1 Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCE BALL [4] | ZCZ BALL [4] |
|-----------------|--|----------|--------------|--------------|
| USB1_CE | USB1 Active high Charger Enable output | A | NA | P18 |
| USB1_DM | USB1 Data minus | A | NA | R18 |
| USB1_DP | USB1 Data plus | A | NA | R17 |
| USB1_DRVVBUS | USB1 Active high VBUS control output | O | NA | F15 |
| USB1_ID | USB1 OTG ID (Micro-A or Micro-B Plug) | A | NA | P17 |
| USB1_VBUS | USB1 VBUS | A | NA | T18 |

5 Specifications

5.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

| | | MIN | MAX | UNIT |
|--|--|--|------|------|
| VDD_MPU ⁽³⁾ | Supply voltage for the MPU core domain | -0.5 | 1.5 | V |
| VDD_CORE | Supply voltage for the core domain | -0.5 | 1.5 | V |
| CAP_VDD_RTC ⁽⁴⁾ | Supply voltage for the RTC core domain | -0.5 | 1.5 | V |
| VPP ⁽⁵⁾ | Supply voltage for the FUSE ROM domain | -0.5 | 2.2 | V |
| VDDS_RTC | Supply voltage for the RTC domain | -0.5 | 2.1 | V |
| VDDS_OSC | Supply voltage for the System oscillator | -0.5 | 2.1 | V |
| VDDS_SRAM_CORE_BG | Supply voltage for the Core SRAM LDOs | -0.5 | 2.1 | V |
| VDDS_SRAM_MPU_BB | Supply voltage for the MPU SRAM LDOs | -0.5 | 2.1 | V |
| VDDS_PLL_DDR | Supply voltage for the DPLL DDR | -0.5 | 2.1 | V |
| VDDS_PLL_CORE_LCD | Supply voltage for the DPLL Core and LCD | -0.5 | 2.1 | V |
| VDDS_PLL_MPU | Supply voltage for the DPLL MPU | -0.5 | 2.1 | V |
| VDDS_DDR | Supply voltage for the DDR I/O domain | -0.5 | 2.1 | V |
| VDDS | Supply voltage for all dual-voltage I/O domains | -0.5 | 2.1 | V |
| VDDA1P8V_USB0 | Supply voltage for USBPHY | -0.5 | 2.1 | V |
| VDDA1P8V_USB1 ⁽⁶⁾ | Supply voltage for USBPHY | -0.5 | 2.1 | V |
| VDDA_ADC | Supply voltage for ADC | -0.5 | 2.1 | V |
| VDDSHV1 | Supply voltage for the dual-voltage I/O domain | -0.5 | 3.8 | V |
| VDDSHV2 ⁽⁶⁾ | Supply voltage for the dual-voltage I/O domain | -0.5 | 3.8 | V |
| VDDSHV3 ⁽⁶⁾ | Supply voltage for the dual-voltage I/O domain | -0.5 | 3.8 | V |
| VDDSHV4 | Supply voltage for the dual-voltage I/O domain | -0.5 | 3.8 | V |
| VDDSHV5 | Supply voltage for the dual-voltage I/O domain | -0.5 | 3.8 | V |
| VDDSHV6 | Supply voltage for the dual-voltage I/O domain | -0.5 | 3.8 | V |
| VDDA3P3V_USB0 | Supply voltage for USBPHY | -0.5 | 4 | V |
| VDDA3P3V_USB1 ⁽⁶⁾ | Supply voltage for USBPHY | -0.5 | 4 | V |
| USB0_VBUS ⁽⁷⁾ | Supply voltage for USB VBUS comparator input | -0.5 | 5.25 | V |
| USB1_VBUS ⁽⁶⁾⁽⁷⁾ | Supply voltage for USB VBUS comparator input | -0.5 | 5.25 | V |
| DDR_VREF | Supply voltage for the DDR SSTL and HSTL reference voltage | -0.3 | 1.1 | V |
| Steady state max voltage at all I/O pins ⁽⁸⁾ | | -0.5 V to I/O supply voltage + 0.3 V | | |
| USB0_ID ⁽⁹⁾ | Steady state maximum voltage for the USB ID input | -0.5 | 2.1 | V |
| USB1_ID ⁽⁶⁾⁽⁹⁾ | Steady state maximum voltage for the USB ID input | -0.5 | 2.1 | V |
| Transient overshoot and undershoot specification at I/O terminal | | 25% of corresponding I/O supply voltage for up to 30% of signal period | | |
| Latch-up performance ⁽¹⁰⁾ | Class II (105°C) | 45 | | mA |
| Storage temperature, T _{stg} ⁽¹¹⁾ | | -55 | 155 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to their associated VSS or VSSA_x.
- (3) Not available on the ZCE package. VDD_MPU is merged with VDD_CORE on the ZCE package.
- (4) This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.
- (5) During functional operation, this pin is a no connect.
- (6) Not available on the ZCE package.
- (7) This terminal is connected to a fail-safe I/O and does not have a dependence on any I/O supply voltage.
- (8) This parameter applies to all I/O terminals which are not fail-safe and the requirement applies to all values of I/O supply voltage. For example, if the voltage applied to a specific I/O supply is 0 volts the valid input voltage range for any I/O powered by that supply will be -0.5 to +0.3 V. Apply special attention anytime peripheral devices are not powered from the same power sources used to power the

Absolute Maximum Ratings (continued)

over junction temperature range (unless otherwise noted)(1)(2)

respective I/O supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.

- (9) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSSA_USB with a resistance less than 10 Ω or greater than 100 k Ω . The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
- (10) Based on JEDEC JESD78D [IC Latch-Up Test].
- (11) For tape and reel the storage temperature range is [–10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.

Fail-safe I/O terminals are designed such they do not have dependencies on the respective I/O power supply voltage. This allows external voltage sources to be connected to these I/O terminals when the respective I/O power supplies are turned off. The USB0_VBUS and USB1_VBUS are the only fail-safe I/O terminals. All other I/O terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the **steady state max. Voltage at all I/O pins** parameter in [Section 5.1](#).

5.2 ESD Ratings

| | | | VALUE | UNIT |
|------------------|--|--|-------|------|
| V _{ESD} | Electrostatic discharge (ESD) performance: | Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001 ⁽¹⁾ | ±2000 | V |
| | | Charged Device Model (CDM), per JESD22-C101 ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Power-On Hours (POH)

Table 5-1. Reliability Data⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

| OPERATING CONDITION | COMMERCIAL | | INDUSTRIAL | | EXTENDED | | INDUSTRIAL EXTENDED | |
|---------------------|---------------------------------|-------------------------------|---------------------------------|-------------------------------|---------------------------------|-------------------------------|---------------------------------|-------------------------------|
| | JUNCTION TEMP (T _J) | LIFETIME (POH) ⁽⁵⁾ | JUNCTION TEMP (T _J) | LIFETIME (POH) ⁽⁵⁾ | JUNCTION TEMP (T _J) | LIFETIME (POH) ⁽⁵⁾ | JUNCTION TEMP (T _J) | LIFETIME (POH) ⁽⁵⁾ |
| Nitro | 0°C to 90°C | 100K | -40°C to 90°C | 100K | -40°C to 105°C | 37K | -40°C to 125°C | – |
| Turbo | 0°C to 90°C | 100K | -40°C to 90°C | 100K | -40°C to 105°C | 80K | -40°C to 125°C | – |
| OPP120 | 0°C to 90°C | 100K | -40°C to 90°C | 100K | -40°C to 105°C | 100K | -40°C to 125°C | – |
| OPP100 | 0°C to 90°C | 100K | -40°C to 90°C | 100K | -40°C to 105°C | 100K | -40°C to 125°C | 35K |
| OPP50 | 0°C to 90°C | 100K | -40°C to 90°C | 100K | -40°C to 105°C | 100K | -40°C to 125°C | 95K |

- (1) The power-on hours (POH) information in this table is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
- (2) To avoid significant degradation, the device power-on hours (POH) must be limited as described in this table.
- (3) Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.
- (4) The previous notations cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for TI semiconductor products.
- (5) POH = Power-on hours when the device is fully functional.

5.4 Operating Performance Points (OPPs)

Device OPPs are defined in [Table 5-2](#) through [Table 5-9](#).

Table 5-2. VDD_CORE OPPs for ZCZ Package With Device Revision Code "Blank"⁽¹⁾

| VDD_CORE OPP Device Rev. "Blank" | VDD_CORE | | | DDR3, DDR3L ⁽²⁾ | DDR2 ⁽²⁾ | mDDR ⁽²⁾ | L3 and L4 |
|----------------------------------|----------|---------|---------|----------------------------|---------------------|---------------------|-----------------|
| | MIN | NOM | MAX | | | | |
| OPP100 | 1.056 V | 1.100 V | 1.144 V | 400 MHz | 266 MHz | 200 MHz | 200 and 100 MHz |
| OPP50 | 0.912 V | 0.950 V | 0.988 V | — | 125 MHz | 90 MHz | 100 and 50 MHz |

- (1) Frequencies in this table indicate maximum performance for a given OPP condition.
- (2) This parameter represents the maximum memory clock frequency. Because data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

Table 5-3. VDD_MPU OPPs for ZCZ Package With Device Revision Code "Blank"⁽¹⁾

| VDD_MPU OPP Device Rev. "Blank" | VDD_MPU | | | ARM (A8) |
|---------------------------------|---------|---------|---------|----------|
| | MIN | NOM | MAX | |
| Turbo | 1.210 V | 1.260 V | 1.326 V | 720 MHz |
| OPP120 | 1.152 V | 1.200 V | 1.248 V | 600 MHz |
| OPP100 ⁽²⁾ | 1.056 V | 1.100 V | 1.144 V | 500 MHz |
| OPP100 ⁽³⁾ | 1.056 V | 1.100 V | 1.144 V | 275 MHz |

- (1) Frequencies in this table indicate maximum performance for a given OPP condition.
- (2) Applies to all orderable AM335__ZCZ_50 (500-MHz speed grade) or higher devices.
- (3) Applies to all orderable AM335__ZCZ_27 (275-MHz speed grade) devices.

Table 5-4. Valid Combinations of VDD_CORE and VDD_MPU OPPs for ZCZ Package With Device Revision Code "Blank"

| VDD_CORE | VDD_MPU |
|----------|---------|
| OPP50 | OPP100 |
| OPP100 | OPP100 |
| OPP100 | OPP120 |
| OPP100 | Turbo |

Table 5-5. VDD_CORE OPPs for ZCE Package With Device Revision Code "Blank"⁽¹⁾

| VDD_CORE OPP Device Rev. "Blank" | VDD_MPU ⁽²⁾ | | | ARM (A8) | DDR3, DDR3L ⁽³⁾ | DDR2 ⁽³⁾ | mDDR ⁽³⁾ | L3 and L4 |
|----------------------------------|------------------------|---------|---------|----------|----------------------------|---------------------|---------------------|-----------------|
| | MIN | NOM | MAX | | | | | |
| OPP100 | 1.056 V | 1.100 V | 1.144 V | 500 MHz | 400 MHz | 266 MHz | 200 MHz | 200 and 100 MHz |
| OPP100 | 1.056 V | 1.100 V | 1.144 V | 275 MHz | 400 MHz | 266 MHz | 200 MHz | 200 and 100 MHz |

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) VDD_MPU is merged with VDD_CORE on the ZCE package.

(3) This parameter represents the maximum memory clock frequency. Because data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

Table 5-6. VDD_CORE OPPs for ZCZ Package With Device Revision Code "A" or Newer⁽¹⁾

| VDD_CORE OPP Rev "A" or Newer | VDD_CORE | | | DDR3, DDR3L ⁽²⁾ | DDR2 ⁽²⁾ | mDDR ⁽²⁾ | L3 and L4 |
|-------------------------------|----------|---------|---------|----------------------------|---------------------|---------------------|-----------------|
| | MIN | NOM | MAX | | | | |
| OPP100 | 1.056 V | 1.100 V | 1.144 V | 400 MHz | 266 MHz | 200 MHz | 200 and 100 MHz |
| OPP50 | 0.912 V | 0.950 V | 0.988 V | — | 125 MHz | 90 MHz | 100 and 50 MHz |

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) This parameter represents the maximum memory clock frequency. Because data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

Table 5-7. VDD_MPU OPPs for ZCZ Package With Device Revision Code "A" or Newer⁽¹⁾

| VDD_MPU OPP Rev "A" or Newer | VDD_MPU | | | ARM (A8) |
|------------------------------|---------|---------|---------|----------|
| | MIN | NOM | MAX | |
| Nitro | 1.272 V | 1.325 V | 1.378 V | 1 GHz |
| Turbo | 1.210 V | 1.260 V | 1.326 V | 800 MHz |
| OPP120 | 1.152 V | 1.200 V | 1.248 V | 720 MHz |
| OPP100 ⁽²⁾ | 1.056 V | 1.100 V | 1.144 V | 600 MHz |
| OPP100 ⁽³⁾ | 1.056 V | 1.100 V | 1.144 V | 300 MHz |
| OPP50 | 0.912 V | 0.950 V | 0.988 V | 300 MHz |

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) Applies to all orderable AM3359_ZCZ_60 (600-MHz speed grade) or higher devices.

(3) Applies to all orderable AM3359_ZCZ_30 (300-MHz speed grade) devices.

Table 5-8. Valid Combinations of VDD_CORE and VDD_MPU OPPs for ZCZ Package With Device Revision Code "A" or Newer

| VDD_CORE | VDD_MPU |
|----------|---------|
| OPP50 | OPP50 |
| OPP50 | OPP100 |
| OPP100 | OPP50 |
| OPP100 | OPP100 |
| OPP100 | OPP120 |
| OPP100 | Turbo |
| OPP100 | Nitro |

Table 5-9. VDD_CORE OPPs for ZCE Package With Device Revision Code "A" or Newer⁽¹⁾

| VDD_CORE OPP Rev "A" or newer | VDD_MPU ⁽²⁾ | | | ARM (A8) | DDR3, DDR3L ⁽³⁾ | DDR2 ⁽³⁾ | mDDR ⁽³⁾ | L3 and L4 |
|--|------------------------|---------|---------|----------|-------------------------------|---------------------|---------------------|-----------------|
| | MIN | NOM | MAX | | | | | |
| OPP100 | 1.056 V | 1.100 V | 1.144 V | 600 MHz | 400 MHz | 266 MHz | 200 MHz | 200 and 100 MHz |
| OPP100 | 1.056 V | 1.100 V | 1.144 V | 300 MHz | 400 MHz | 266 MHz | 200 MHz | 200 and 100 MHz |
| OPP50 | 0.912 V | 0.950 V | 0.988 V | 300 MHz | – | 125 MHz | 90 MHz | 100 and 50 MHz |

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) VDD_MPU is merged with VDD_CORE on the ZCE package.

(3) This parameter represents the maximum memory clock frequency. Because data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

5.5 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

| SUPPLY NAME | DESCRIPTION | MIN | NOM | MAX | UNIT |
|----------------------------------|--|-------|-------|-------|------|
| VDD_CORE ⁽¹⁾ | Supply voltage range for core domain; OPP100 | 1.056 | 1.100 | 1.144 | V |
| | Supply voltage range for core domain; OPP50 | 0.912 | 0.950 | 0.988 | |
| VDD_MPU ⁽¹⁾⁽²⁾ | Supply voltage range for MPU domain, Nitro | 1.272 | 1.325 | 1.378 | V |
| | Supply voltage range for MPU domain; Turbo | 1.210 | 1.260 | 1.326 | |
| | Supply voltage range for MPU domain; OPP120 | 1.152 | 1.200 | 1.248 | |
| | Supply voltage range for MPU domain; OPP100 | 1.056 | 1.100 | 1.144 | |
| | Supply voltage range for MPU domain; OPP50 | 0.912 | 0.950 | 0.988 | |
| CAP_VDD_RTC ⁽³⁾ | Supply voltage range for RTC domain input | 0.900 | 1.100 | 1.250 | V |
| VDDS_RTC | Supply voltage range for RTC domain | 1.710 | 1.800 | 1.890 | V |
| VDDS_DDR | Supply voltage range for DDR I/O domain (DDR2) | 1.710 | 1.800 | 1.890 | V |
| | Supply voltage range for DDR I/O domain (DDR3) | 1.425 | 1.500 | 1.575 | |
| | Supply voltage range for DDR I/O domain (DDR3L) | 1.283 | 1.350 | 1.418 | |
| VDDS ⁽⁴⁾ | Supply voltage range for all dual-voltage I/O domains | 1.710 | 1.800 | 1.890 | V |
| VDDS_SRAM_CORE_BG | Supply voltage range for Core SRAM LDOs, analog | 1.710 | 1.800 | 1.890 | V |
| VDDS_SRAM_MPU_BB | Supply voltage range for MPU SRAM LDOs, analog | 1.710 | 1.800 | 1.890 | V |
| VDDS_PLL_DDR ⁽⁵⁾ | Supply voltage range for DPLL DDR, analog | 1.710 | 1.800 | 1.890 | V |
| VDDS_PLL_CORE_LCD ⁽⁵⁾ | Supply voltage range for DPLL CORE and LCD, analog | 1.710 | 1.800 | 1.890 | V |
| VDDS_PLL_MPU ⁽⁵⁾ | Supply voltage range for DPLL MPU, analog | 1.710 | 1.800 | 1.890 | V |
| VDDS_OSC | Supply voltage range for system oscillator I/Os, analog | 1.710 | 1.800 | 1.890 | V |
| VDDA1P8V_USB0 ⁽⁵⁾ | Supply voltage range for USBPHY and PER DPLL, analog, 1.8 V | 1.710 | 1.800 | 1.890 | V |
| VDDA1P8V_USB1 ⁽⁶⁾ | Supply voltage range for USB PHY, analog, 1.8 V | 1.710 | 1.800 | 1.890 | V |
| VDDA3P3V_USB0 | Supply voltage range for USB PHY, analog, 3.3 V | 3.135 | 3.300 | 3.465 | V |
| VDDA3P3V_USB1 ⁽⁶⁾ | Supply voltage range for USB PHY, analog, 3.3 V | 3.135 | 3.300 | 3.465 | V |
| VDDA_ADC | Supply voltage range for ADC, analog | 1.710 | 1.800 | 1.890 | V |
| VDDSHV1 | Supply voltage range for dual-voltage I/O domain (1.8-V operation) | 1.710 | 1.800 | 1.890 | V |
| VDDSHV2 ⁽⁶⁾ | Supply voltage range for dual-voltage I/O domain (1.8-V operation) | 1.710 | 1.800 | 1.890 | V |

Recommended Operating Conditions (continued)

over junction temperature range (unless otherwise noted)

| SUPPLY NAME | DESCRIPTION | MIN | NOM | MAX | UNIT |
|---|---|---------------------------|---------------------------|---------------------------|------|
| VDDSHV3 ⁽⁶⁾ | Supply voltage range for dual-voltage I/O domain (1.8-V operation) | 1.710 | 1.800 | 1.890 | V |
| VDDSHV4 | Supply voltage range for dual-voltage I/O domain (1.8-V operation) | 1.710 | 1.800 | 1.890 | V |
| VDDSHV5 | Supply voltage range for dual-voltage I/O domain (1.8-V operation) | 1.710 | 1.800 | 1.890 | V |
| VDDSHV6 | Supply voltage range for dual-voltage I/O domain (1.8-V operation) | 1.710 | 1.800 | 1.890 | V |
| VDDSHV1 | Supply voltage range for dual-voltage I/O domain (3.3-V operation) | 3.135 | 3.300 | 3.465 | V |
| VDDSHV2 ⁽⁶⁾ | Supply voltage range for dual-voltage I/O domain (3.3-V operation) | 3.135 | 3.300 | 3.465 | V |
| VDDSHV3 ⁽⁶⁾ | Supply voltage range for dual-voltage I/O domain (3.3-V operation) | 3.135 | 3.300 | 3.465 | V |
| VDDSHV4 | Supply voltage range for dual-voltage I/O domain (3.3-V operation) | 3.135 | 3.300 | 3.465 | V |
| VDDSHV5 | Supply voltage range for dual-voltage I/O domain (3.3-V operation) | 3.135 | 3.300 | 3.465 | V |
| VDDSHV6 | Supply voltage range for dual-voltage I/O domain (3.3-V operation) | 3.135 | 3.300 | 3.465 | V |
| DDR_VREF | Voltage range for DDR SSTL and HSTL reference input (DDR2, DDR3, DDR3L) | $0.49 \times VDDSD_{DDR}$ | $0.50 \times VDDSD_{DDR}$ | $0.51 \times VDDSD_{DDR}$ | V |
| USB0_VBUS | Voltage range for USB VBUS comparator input | 0.000 | 5.000 | 5.250 | V |
| USB1_VBUS ⁽⁶⁾ | Voltage range for USB VBUS comparator input | 0.000 | 5.000 | 5.250 | V |
| USB0_ID | Voltage range for the USB ID input | | ⁽⁷⁾ | | V |
| USB1_ID ⁽⁶⁾ | Voltage range for the USB ID input | | ⁽⁷⁾ | | V |
| Operating temperature range, T _J | Commercial temperature | 0 | | 90 | °C |
| | Industrial temperature | –40 | | 90 | |
| | Extended temperature | –40 | | 105 | |

- (1) The supply voltage defined by OPP100 should be applied to this power domain before the device is released from reset.
- (2) Not available on the ZCE package. VDD_MPU is merged with VDD_CORE on the ZCE package.
- (3) This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.
- (4) VDDS should be supplied irrespective of 1.8- or 3.3-V mode of operation of the dual-voltage I/Os.
- (5) For more details on power supply requirements, see [Section 6.1.4](#).
- (6) Not available on the ZCE package.
- (7) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSSA_USB with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.

5.6 Power Consumption Summary

Table 5-10 summarizes the power consumption at the AM335x power terminals.

Table 5-10. Maximum Current Ratings at AM335x Power Terminals⁽¹⁾

| SUPPLY NAME | DESCRIPTION | MAX | UNIT | |
|------------------------------|--|------------------|------|-----|
| VDD_CORE ⁽²⁾ | Maximum current rating for the core domain; OPP100 | 400 | mA | |
| | Maximum current rating for the core domain; OPP50 | 250 | | |
| VDD_MPU ⁽²⁾ | Maximum current rating for the MPU domain; Nitro | at 1 GHz 1000 | mA | |
| | Maximum current rating for the MPU domain; Turbo | at 800 MHz | | 800 |
| | | at 720 MHz | | 720 |
| | Maximum current rating for the MPU domain; OPP120 | at 720 MHz | | 720 |
| | | at 600 MHz | | 600 |
| | Maximum current rating for the MPU domain; OPP100 | at 600 MHz | | 600 |
| | | at 500 MHz | | 500 |
| | | at 300 MHz | | 380 |
| | | at 275 MHz | | 350 |
| | Maximum current rating for the MPU domain; OPP50 | at 300 MHz | | 330 |
| at 275 MHz | | 300 | | |
| CAP_VDD_RTC ⁽³⁾ | Maximum current rating for RTC domain input and LDO output | 2 | mA | |
| VDDS_RTC | Maximum current rating for the RTC domain | 5 | mA | |
| VDDS_DDR | Maximum current rating for DDR I/O domain | 250 | mA | |
| VDDS | Maximum current rating for all dual-voltage I/O domains | 50 | mA | |
| VDDS_SRAM_CORE_BG | Maximum current rating for core SRAM LDOs | 10 | mA | |
| VDDS_SRAM_MPU_BB | Maximum current rating for MPU SRAM LDOs | 10 | mA | |
| VDDS_PLL_DDR | Maximum current rating for the DPLL DDR | 10 | mA | |
| VDDS_PLL_CORE_LCD | Maximum current rating for the DPLL Core and LCD | 20 | mA | |
| VDDS_PLL_MPU | Maximum current rating for the DPLL MPU | 10 | mA | |
| VDDS_OSC | Maximum current rating for the system oscillator I/Os | 5 | mA | |
| VDDA1P8V_USB0 | Maximum current rating for USBPHY 1.8 V | 25 | mA | |
| VDDA1P8V_USB1 ⁽⁴⁾ | Maximum current rating for USBPHY 1.8 V | 25 | mA | |
| VDDA3P3V_USB0 | Maximum current rating for USBPHY 3.3 V | 40 | mA | |
| VDDA3P3V_USB1 ⁽⁴⁾ | Maximum current rating for USBPHY 3.3 V | 40 | mA | |
| VDDA_ADC | Maximum current rating for ADC | 10 | mA | |
| VDDSHV1 ⁽⁵⁾ | Maximum current rating for dual-voltage I/O domain | 50 | mA | |
| VDDSHV2 ⁽⁴⁾ | Maximum current rating for dual-voltage I/O domain | 50 | mA | |
| VDDSHV3 ⁽⁴⁾ | Maximum current rating for dual-voltage I/O domain | 50 | mA | |
| VDDSHV4 | Maximum current rating for dual-voltage I/O domain | 50 | mA | |
| VDDSHV5 | Maximum current rating for dual-voltage I/O domain | 50 | mA | |
| VDDSHV6 | Maximum current rating for dual-voltage I/O domain | 100 | mA | |

(1) Current ratings specified in this table are worst-case estimates. Actual application power supply estimates could be lower. For more information, see [AM335x Power Consumption Summary](#).

(2) VDD_MPU is merged with VDD_CORE and is not available separately on the ZCE package. The maximum current rating for VDD_CORE on the ZCE package is the sum of VDD_CORE and VDD_MPU shown in this table.

(3) This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.

(4) Not available on the ZCE package.

(5) VDDSHV1 and VDDSHV2 are merged in the ZCE package. The maximum current rating for VDDSHV1 on the ZCE package is the sum of VDDSHV1 and VDDSHV2 shown in this table.

Table 5-11 summarizes the power consumption of the AM335x low-power modes.

Table 5-11. AM335x Low-Power Modes Power Consumption Summary

| POWER MODES | APPLICATION STATE | POWER DOMAINS, CLOCKS, AND VOLTAGE SUPPLY STATES | NOM | MAX | UNIT |
|-------------|--|--|------|------|------|
| Standby | DDR memory is in self-refresh and contents are preserved. Wake up from any GPIO. Cortex-A8 context/register contents are lost and must be saved before entering standby. On exit, context must be restored from DDR. For wakeup, boot ROM executes and branches to system resume. | Power supplies: <ul style="list-style-type: none"> All power supplies are ON. VDD_MPU = 0.95 V (nom) VDD_CORE = 0.95 V (nom) Clocks: <ul style="list-style-type: none"> Main Oscillator (OSC0) = ON All DPLLs are in bypass. Power domains: <ul style="list-style-type: none"> PD_PER = ON PD_MPU = OFF PD_GFX = OFF PD_WKUP = ON DDR is in self-refresh. | 16.5 | 22.0 | mW |
| Deepsleep1 | On-chip peripheral registers are preserved. Cortex-A8 context/registers are lost, so the application must save them to the L3 OCMC RAM or DDR before entering DeepSleep. DDR is in self-refresh. For wakeup, boot ROM executes and branches to system resume. | Power supplies: <ul style="list-style-type: none"> All power supplies are ON. VDD_MPU = 0.95 V (nom) VDD_CORE = 0.95 V (nom) Clocks: <ul style="list-style-type: none"> Main Oscillator (OSC0) = OFF All DPLLs are in bypass. Power domains: <ul style="list-style-type: none"> PD_PER = ON PD_MPU = OFF PD_GFX = OFF PD_WKUP = ON DDR is in self-refresh. | 6.0 | 10.0 | mW |
| Deepsleep0 | PD_PER peripheral and Cortex-A8/MPU register information will be lost. On-chip peripheral register (context) information of PD-PER domain must be saved by application to SDRAM before entering this mode. DDR is in self-refresh. For wakeup, boot ROM executes and branches to peripheral context restore followed by system resume. | Power supplies: <ul style="list-style-type: none"> All power supplies are ON. VDD_MPU = 0.95 V (nom) VDD_CORE = 0.95 V (nom) Clocks: <ul style="list-style-type: none"> Main Oscillator (OSC0) = OFF All DPLLs are in bypass. Power domains: <ul style="list-style-type: none"> PD_PER = OFF PD_MPU = OFF PD_GFX = OFF PD_WKUP = ON DDR is in self-refresh. | 3.0 | 4.3 | mW |

5.7 DC Electrical Characteristics

 over recommended ranges of supply voltage and operating temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|--|--------------------------------|-----------------------------|------------------------------|------|
| DDR_RESETn,DDR_CSn0,DDR_CKE,DDR_CK,DDR_CKn,DDR_CASn,DDR_RASn,DDR_WEn,DDR_BA0,DDR_BA1,DDR_BA2,DDR_A0,DDR_A1,DDR_A2,DDR_A3,DDR_A4,DDR_A5,DDR_A6,DDR_A7,DDR_A8,DDR_A9,DDR_A10,DDR_A11,DDR_A12,DDR_A13,DDR_A14,DDR_A15,DDR_ODT,DDR_D0,DDR_D1,DDR_D2,DDR_D3,DDR_D4,DDR_D5,DDR_D6,DDR_D7,DDR_D8,DDR_D9,DDR_D10,DDR_D11,DDR_D12,DDR_D13,DDR_D14,DDR_D15,DDR_DQM0,DDR_DQM1,DDR_DQS0,DDR_DQSn0,DDR_DQS1,DDR_DQSn1 Pins (mDDR - LVCMOS Mode) | | | | | |
| V _{IH} | High-level input voltage | 0.65 × V _{DDSD_DDR} | | | V |
| V _{IL} | Low-level input voltage | | | 0.35 × V _{DDSD_DDR} | V |
| V _{HYS} | Hysteresis voltage at an input | 0.07 | | 0.25 | V |
| V _{OH} | High level output voltage, driver enabled, pullup or pulldown disabled | I _{OH} = 8 mA | V _{DDSD_DDR} – 0.4 | | V |
| V _{OL} | Low level output voltage, driver enabled, pullup or pulldown disabled | I _{OL} = 8 mA | 0.4 | | V |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | 10 | | μA |
| | Input leakage current, Receiver disabled, pullup enabled | | –240 | | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 80 | | |
| I _{OZ} | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | 10 | | μA |
| DDR_RESETn,DDR_CSn0,DDR_CKE,DDR_CK,DDR_CKn,DDR_CASn,DDR_RASn,DDR_WEn,DDR_BA0,DDR_BA1,DDR_BA2,DDR_A0,DDR_A1,DDR_A2,DDR_A3,DDR_A4,DDR_A5,DDR_A6,DDR_A7,DDR_A8,DDR_A9,DDR_A10,DDR_A11,DDR_A12,DDR_A13,DDR_A14,DDR_A15,DDR_ODT,DDR_D0,DDR_D1,DDR_D2,DDR_D3,DDR_D4,DDR_D5,DDR_D6,DDR_D7,DDR_D8,DDR_D9,DDR_D10,DDR_D11,DDR_D12,DDR_D13,DDR_D14,DDR_D15,DDR_DQM0,DDR_DQM1,DDR_DQS0,DDR_DQSn0,DDR_DQS1,DDR_DQSn1 Pins (DDR2 - SSTL Mode) | | | | | |
| V _{IH} | High-level input voltage | DDR_VREF + 0.125 | | | V |
| V _{HYS} | Hysteresis voltage at an input | N/A | | | V |
| V _{OH} | High-level output voltage, driver enabled, pullup or pulldown disabled | I _{OH} = 8 mA | V _{DDSD_DDR} – 0.4 | | V |
| V _{OL} | Low-level output voltage, driver enabled, pullup or pulldown disabled | I _{OL} = 8 mA | 0.4 | | V |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | 10 | | μA |
| | Input leakage current, Receiver disabled, pullup enabled | | –240 | | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 80 | | |
| I _{OZ} | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | 10 | | μA |
| DDR_RESETn,DDR_CSn0,DDR_CKE,DDR_CK,DDR_CKn,DDR_CASn,DDR_RASn,DDR_WEn,DDR_BA0,DDR_BA1,DDR_BA2,DDR_A0,DDR_A1,DDR_A2,DDR_A3,DDR_A4,DDR_A5,DDR_A6,DDR_A7,DDR_A8,DDR_A9,DDR_A10,DDR_A11,DDR_A12,DDR_A13,DDR_A14,DDR_A15,DDR_ODT,DDR_D0,DDR_D1,DDR_D2,DDR_D3,DDR_D4,DDR_D5,DDR_D6,DDR_D7,DDR_D8,DDR_D9,DDR_D10,DDR_D11,DDR_D12,DDR_D13,DDR_D14,DDR_D15,DDR_DQM0,DDR_DQM1,DDR_DQS0,DDR_DQSn0,DDR_DQS1,DDR_DQSn1 Pins (DDR3, DDR3L - HSTL Mode) | | | | | |
| V _{IH} | High-level input voltage | V _{DDSD_DDR} = 1.5 V | DDR_VREF + 0.1 | | V |
| | | V _{DDSD_DDR} = 1.35 V | DDR_VREF + 0.09 | | |
| V _{IL} | Low-level input voltage | V _{DDSD_DDR} = 1.5 V | DDR_VREF – 0.1 | | V |
| | | V _{DDSD_DDR} = 1.35 V | DDR_VREF – 0.09 | | |
| V _{HYS} | Hysteresis voltage at an input | N/A | | | V |
| V _{OH} | High-level output voltage, driver enabled, pullup or pulldown disabled | I _{OH} = 8 mA | V _{DDSD_DDR} – 0.4 | | V |
| V _{OL} | Low-level output voltage, driver enabled, pullup or pulldown disabled | I _{OL} = 8 mA | 0.4 | | V |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | 10 | | μA |
| | Input leakage current, Receiver disabled, pullup enabled | | –240 | | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 80 | | |
| I _{OZ} | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | 10 | | μA |

DC Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | MIN | NOM | MAX | UNIT | |
|---|--|------------------------|----------------|-------|------|-----|
| ECAPO_IN_PWM0_OUT,UART0_CTSn,UART0_RTSn,UART0_RXD,UART0_TXD,UART1_CTSn,UART1_RTSn,UART1_RXD,UART1_TXD,I2C0_SDA,I2C0_SCL,XDMA_EVENT_INTR0,XDMA_EVENT_INTR1,WARMRSTn,EXTINTn,TMS,TDO,USB0_DRVVBUS,USB1_DRVVBUS (VDDSHV6 = 1.8 V) | | | | | | |
| V _{IH} | High-level input voltage | 0.65 × VDDSHV6 | | | V | |
| V _{IL} | Low-level input voltage | | 0.35 × VDDSHV6 | | V | |
| V _{HYS} | Hysteresis voltage at an input | 0.18 | | 0.305 | V | |
| V _{OH} | High-level output voltage, driver enabled, pullup or pulldown disabled | I _{OH} = 4 mA | VDDSHV6 – 0.45 | | V | |
| V _{OL} | Low-level output voltage, driver enabled, pullup or pulldown disabled | I _{OL} = 4 mA | | 0.45 | V | |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | | 8 | μA | |
| | Input leakage current, Receiver disabled, pullup enabled | | –161 | –100 | | –52 |
| | Input leakage current, Receiver disabled, pulldown enabled | | 52 | 100 | | 170 |
| I _{OZ} | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | | 8 | μA | |
| ECAPO_IN_PWM0_OUT,UART0_CTSn,UART0_RTSn,UART0_RXD,UART0_TXD,UART1_CTSn,UART1_RTSn,UART1_RXD,UART1_TXD,I2C0_SDA,I2C0_SCL,XDMA_EVENT_INTR0,XDMA_EVENT_INTR1,WARMRSTn,EXTINTn,TMS,TDO,USB0_DRVVBUS,USB1_DRVVBUS (VDDSHV6 = 3.3 V) | | | | | | |
| V _{IH} | High-level input voltage | 2 | | | V | |
| V _{IL} | Low-level input voltage | | | 0.8 | V | |
| V _{HYS} | Hysteresis voltage at an input | 0.265 | | 0.44 | V | |
| V _{OH} | High-level output voltage, driver enabled, pullup or pulldown disabled | I _{OH} = 4 mA | VDDSHV6 – 0.45 | | V | |
| V _{OL} | Low-level output voltage, driver enabled, pullup or pulldown disabled | I _{OL} = 4 mA | | 0.45 | V | |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | | 18 | μA | |
| | Input leakage current, Receiver disabled, pullup enabled | | –243 | –100 | | –19 |
| | Input leakage current, Receiver disabled, pulldown enabled | | 51 | 110 | | 210 |
| I _{OZ} | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | | 18 | μA | |
| TCK (VDDSHV6 = 1.8 V) | | | | | | |
| V _{IH} | High-level input voltage | 1.45 | | | V | |
| V _{IL} | Low-level input voltage | | | 0.46 | V | |
| V _{HYS} | Hysteresis voltage at an input | 0.4 | | | V | |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | | 8 | μA | |
| | Input leakage current, Receiver disabled, pullup enabled | | –161 | –100 | | –52 |
| | Input leakage current, Receiver disabled, pulldown enabled | | 52 | 100 | | 170 |
| TCK (VDDSHV6 = 3.3 V) | | | | | | |
| V _{IH} | High-level input voltage | 2.15 | | | V | |
| V _{IL} | Low-level input voltage | | | 0.46 | V | |
| V _{HYS} | Hysteresis voltage at an input | 0.4 | | | V | |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | | 18 | μA | |
| | Input leakage current, Receiver disabled, pullup enabled | | –243 | –100 | | –19 |
| | Input leakage current, Receiver disabled, pulldown enabled | | 51 | 110 | | 210 |
| PWRONRSTn (VDDSHV6 = 1.8 or 3.3 V)⁽²⁾ | | | | | | |
| V _{IH} | High-level input voltage | 1.35 | | | V | |
| V _{IL} | Low-level input voltage | | | 0.5 | V | |
| V _{HYS} | Hysteresis voltage at an input | 0.07 | | | V | |
| I _I | Input leakage current | V _I = 1.8 V | | 0.1 | μA | |
| | | V _I = 3.3 V | | 2 | | |
| RTC_PWRONRSTn | | | | | | |
| V _{IH} | High-level input voltage | 0.65 × VDDS_RTC | | | V | |

DC Electrical Characteristics (continued)over recommended ranges of supply voltage and operating temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--|--|------------------------|-----------------------------|-----------------------------|------|
| V _{IL} | Low-level input voltage | | | 0.35 × V _{DD5_RTC} | V |
| V _{HYS} | Hysteresis voltage at an input | 0.065 | | | V |
| I _I | Input leakage current | –1 | | 1 | μA |
| PMIC_POWER_EN | | | | | |
| V _{OH} | High-level output voltage, driver enabled, pullup or pulldown disabled | I _{OH} = 6 mA | V _{DD5_RTC} – 0.45 | | V |
| V _{OL} | Low-level output voltage, driver enabled, pullup or pulldown disabled | I _{OL} = 6 mA | | 0.45 | V |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | –1 | | 1 | μA |
| | Input leakage current, Receiver disabled, pullup enabled | –200 | | –40 | |
| | Input leakage current, Receiver disabled, pulldown enabled | 40 | | 200 | |
| I _{OZ} | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | –1 | | 1 | μA |
| EXT_WAKEUP | | | | | |
| V _{IH} | High-level input voltage | | 0.65 × V _{DD5_RTC} | | V |
| V _{IL} | Low-level input voltage | | | 0.35 × V _{DD5_RTC} | V |
| V _{HYS} | Hysteresis voltage at an input | 0.15 | | | V |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | –1 | | 1 | μA |
| | Input leakage current, Receiver disabled, pullup enabled | –200 | | –40 | |
| | Input leakage current, Receiver disabled, pulldown enabled | 40 | | 200 | |
| XTALIN (OSC0) | | | | | |
| V _{IH} | High-level input voltage | | 0.65 × V _{DD5_OSC} | | V |
| V _{IL} | Low-level input voltage | | | 0.35 × V _{DD5_OSC} | V |
| RTC_XTALIN (OSC1) | | | | | |
| V _{IH} | High-level input voltage | | 0.65 × V _{DD5_RTC} | | V |
| V _{IL} | Low-level input voltage | | | 0.35 × V _{DD5_RTC} | V |
| All other LVC MOS pins (V_{DDSHVx} = 1.8 V; x = 1 to 6) | | | | | |
| V _{IH} | High-level input voltage | | 0.65 × V _{DDSHVx} | | V |
| V _{IL} | Low-level input voltage | | | 0.35 × V _{DDSHVx} | V |
| V _{HYS} | Hysteresis voltage at an input | 0.18 | | 0.305 | V |
| V _{OH} | High-level output voltage, driver enabled, pullup or pulldown disabled | I _{OH} = 6 mA | V _{DDSHVx} – 0.45 | | V |
| V _{OL} | Low-level output voltage, driver enabled, pullup or pulldown disabled | I _{OL} = 6 mA | | 0.45 | V |
| I _I | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | | 8 | μA |
| | Input leakage current, Receiver disabled, pullup enabled | –161 | –100 | –52 | |
| | Input leakage current, Receiver disabled, pulldown enabled | 52 | 100 | 170 | |
| I _{OZ} | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | | 8 | μA |
| All other LVC MOS pins (V_{DDSHVx} = 3.3 V; x = 1 to 6) | | | | | |
| V _{IH} | High-level input voltage | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| V _{HYS} | Hysteresis voltage at an input | 0.265 | | 0.44 | V |
| V _{OH} | High-level output voltage, driver enabled, pullup or pulldown disabled | I _{OH} = 6 mA | V _{DDSHVx} – 0.45 | | V |
| V _{OL} | Low-level output voltage, driver enabled, pullup or pulldown disabled | I _{OL} = 6 mA | | 0.45 | V |

DC Electrical Characteristics *(continued)*

over recommended ranges of supply voltage and operating temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | MIN | NOM | MAX | UNIT |
|-----------|--|------|------|-----|---------------|
| I_i | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | | 18 | μA |
| | Input leakage current, Receiver disabled, pullup enabled | -243 | -100 | -19 | |
| | Input leakage current, Receiver disabled, pulldown enabled | 51 | 110 | 210 | |
| I_{OZ} | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | | 18 | μA |

- (1) The interfaces or signals described in this table correspond to the interfaces or signals available in multiplexing mode 0. All interfaces or signals multiplexed on the terminals described in this table have the same DC electrical characteristics.
- (2) The input voltage thresholds for this input are not a function of VDDSHV6.

5.8 Thermal Resistance Characteristics for ZCE and ZCZ Packages

Failure to maintain a junction temperature within the range specified in [Section 5.5](#) reduces operating lifetime, reliability, and performance—and may cause irreversible damage to the system. Therefore, the product design cycle should include thermal analysis to verify the maximum operating junction temperature of the device. It is important this thermal analysis is performed using specific system use cases and conditions. TI provides an application report to aid users in overcoming some of the existing challenges of producing a good thermal design. For more information, see [AM335x Thermal Considerations](#).

[Table 5-12](#) provides thermal characteristics for the packages used on this device.

NOTE

[Table 5-12](#) provides simulation data and may not represent actual use-case values.

Table 5-12. Thermal Resistance Characteristics (PBGA Package) [ZCE and ZCZ]

| | | ZCE (°C/W) ⁽¹⁾ (⁽²⁾) | ZCZ (°C/W) ⁽¹⁾ (⁽²⁾) | AIR FLOW (m/s) ⁽³⁾ |
|------------------|-------------------------|---|---|----------------------------------|
| R _{θJC} | Junction-to-case | 10.3 | 10.2 | N/A |
| R _{θJB} | Junction-to-board | 11.6 | 12.1 | N/A |
| R _{θJA} | Junction-to-free air | 24.7 | 24.2 | 0 |
| | | 20.5 | 20.1 | 1.0 |
| | | 19.7 | 19.3 | 2.0 |
| | | 19.2 | 18.8 | 3.0 |
| φ _{JT} | Junction-to-package top | 0.4 | 0.3 | 0.0 |
| | | 0.6 | 0.6 | 1.0 |
| | | 0.7 | 0.7 | 2.0 |
| | | 0.9 | 0.8 | 3.0 |
| φ _{JB} | Junction-to-board | 11.9 | 12.7 | 0.0 |
| | | 11.7 | 12.3 | 1.0 |
| | | 11.7 | 12.3 | 2.0 |
| | | 11.6 | 12.2 | 3.0 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the theta JC [R_{θJC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

(2) °C/W = degrees Celsius per watt.

(3) m/s = meters per second.

5.9 External Capacitors

To improve module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device, because this minimizes the inductance of the circuit board wiring and interconnects.

5.9.1 Voltage Decoupling Capacitors

Table 5-13 summarizes the Core voltage decoupling characteristics.

5.9.1.1 Core Voltage Decoupling Capacitors

To improve module performance, decoupling capacitors are required to suppress high-frequency switching noise and to stabilize the supply voltage. A decoupling capacitor is most effective when located close to the AM335x device, because this minimizes the inductance of the circuit board wiring and interconnects.

Table 5-13. Core Voltage Decoupling Characteristics

| PARAMETER | TYP | UNIT |
|--|-------|------|
| C _{VDD_CORE} ⁽¹⁾ | 10.08 | μF |
| C _{VDD_MPU} ⁽²⁾⁽³⁾ | 10.05 | μF |

(1) The typical value corresponds to one capacitor of 10 μF and eight capacitors of 10 nF.

(2) Not available on the ZCE package. VDD_MPU is merged with VDD_CORE on the ZCE package.

(3) The typical value corresponds to one capacitor of 10 μF and five capacitors of 10 nF.

5.9.1.2 I/O and Analog Voltage Decoupling Capacitors

Table 5-14 summarizes the power-supply decoupling capacitor recommendations.

Table 5-14. Power-Supply Decoupling Capacitor Characteristics

| PARAMETER | TYP | UNIT |
|---|----------------|------|
| C _{VDDA_ADC} | 10 | nF |
| C _{VDDA1P8V_USB0} | 10 | nF |
| C _{CVDDA3P3V_USB0} | 10 | nF |
| C _{VDDA1P8V_USB1} ⁽¹⁾ | 10 | nF |
| C _{VDDA3P3V_USB1} ⁽¹⁾ | 10 | nF |
| C _{VDDS} ⁽²⁾ | 10.04 | μF |
| C _{VDDS_DDR} | ⁽³⁾ | |
| C _{VDDS_OSC} | 10 | nF |
| C _{VDDS_PLL_DDR} | 10 | nF |
| C _{VDDS_PLL_CORE_LCD} | 10 | nF |
| C _{VDDS_SRAM_CORE_BG} ⁽⁴⁾ | 10.01 | μF |
| C _{VDDS_SRAM_MPU_BB} ⁽⁵⁾ | 10.01 | μF |
| C _{VDDS_PLL_MPU} | 10 | nF |
| C _{VDDS_RTC} | 10 | nF |
| C _{VDDSHV1} ⁽⁶⁾ | 10.02 | μF |
| C _{VDDSHV2} ⁽¹⁾⁽⁶⁾ | 10.02 | μF |
| C _{VDDSHV3} ⁽¹⁾⁽⁶⁾ | 10.02 | μF |
| C _{VDDSHV4} ⁽⁶⁾ | 10.02 | μF |
| C _{VDDSHV5} ⁽⁶⁾ | 10.02 | μF |
| C _{VDDSHV6} ⁽⁷⁾ | 10.06 | μF |

- (1) Not available on the ZCE package.
- (2) Typical values consist of one capacitor of 10 μ F and four capacitors of 10 nF.
- (3) For more details on decoupling capacitor requirements for the mDDR(LPDDR), DDR2, DDR3, DDR3L memory interface, see [Section 7.7.2.1.2.6](#) and [Section 7.7.2.1.2.7](#) when using mDDR(LPDDR) memory devices, [Section 7.7.2.2.2.6](#) and [Section 7.7.2.2.2.7](#) when using DDR2 memory devices, or [Section 7.7.2.3.3.6](#) and [Section 7.7.2.3.3.7](#) when using DDR3 or DDR3L memory devices.
- (4) VDDS_SRAM_CORE_BG supply powers an internal LDO for SRAM supplies. Inrush currents could cause voltage drop on the VDDS_SRAM_CORE_BG supplies when the SRAM LDO is enabled after powering up VDDS_SRAM_CORE_BG terminals. A 10 μ F is recommended to be placed close to the terminal and routed with widest traces possible to minimize the voltage drop on VDDS_SRAM_CORE_BG terminals.
- (5) VDDS_SRAM_MPU_BB supply powers an internal LDO for SRAM supplies. Inrush currents could cause voltage drop on the VDDS_SRAM_MPU_BB supplies when the SRAM LDO is enabled after powering up VDDS_SRAM_MPU_BB terminals. A 10 μ F is recommended to be placed close to the terminal and routed with widest traces possible to minimize the voltage drop on VDDS_SRAM_MPU_BB terminals.
- (6) Typical values consist of one capacitor of 10 μ F and two capacitors of 10 nF.
- (7) Typical values consist of one capacitor of 10 μ F and six capacitors of 10 nF.

5.9.2 Output Capacitors

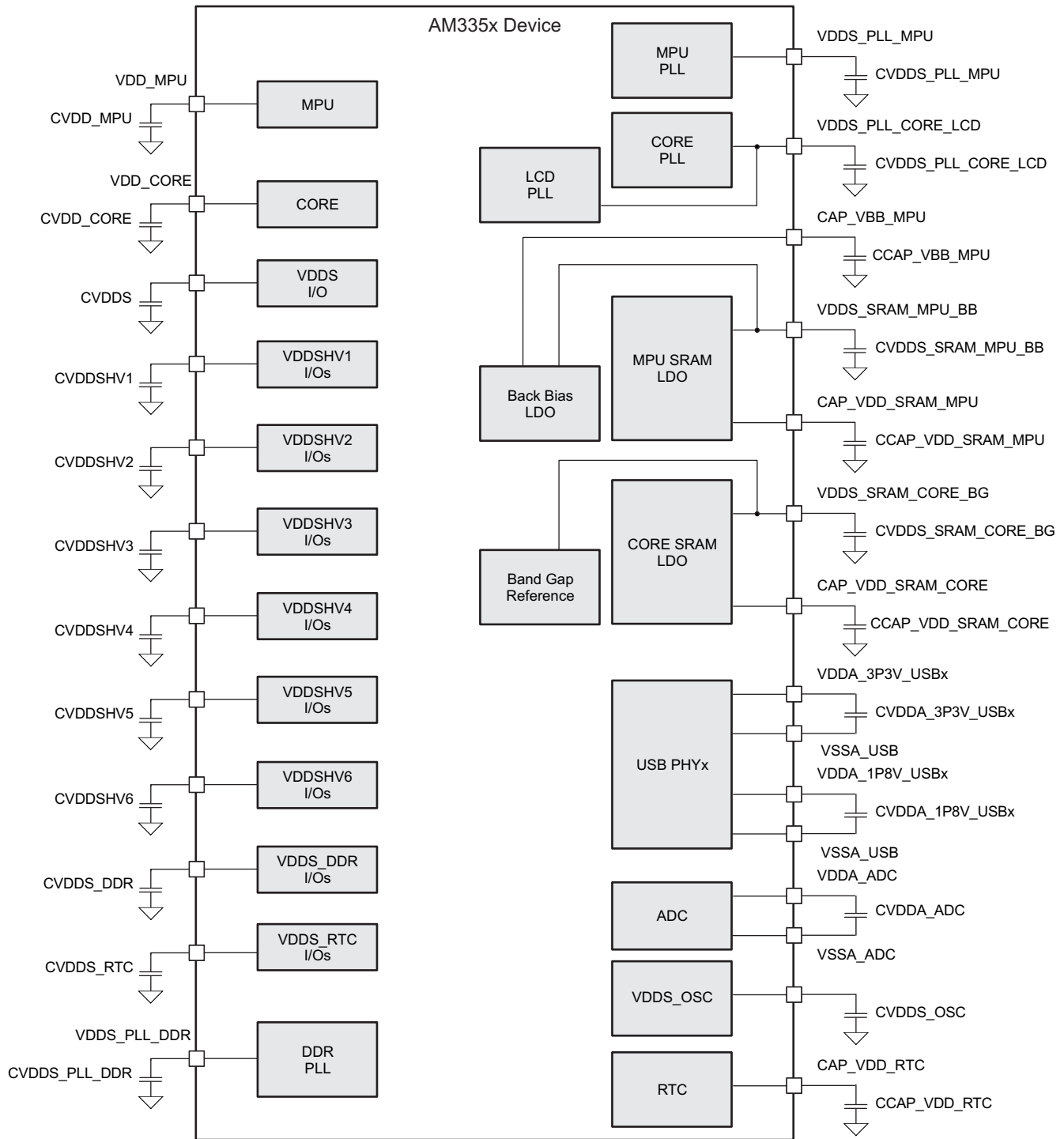
Internal low dropout output (LDO) regulators require external capacitors to stabilize their outputs. These capacitors should be placed as close as possible to the respective terminals of the AM335x device. [Table 5-15](#) summarizes the LDO output capacitor recommendations.

Table 5-15. Output Capacitor Characteristics

| PARAMETER | TYP | UNIT |
|---|-----|---------|
| C _{CAP_VDD_SRAM_CORE} ⁽¹⁾ | 1 | μ F |
| C _{CAP_VDD_RTC} ⁽¹⁾⁽²⁾ | 1 | μ F |
| C _{CAP_VDD_SRAM_MPU} ⁽¹⁾ | 1 | μ F |
| C _{CAP_VBB_MPU} ⁽¹⁾ | 1 | μ F |

- (1) LDO regulator outputs should not be used as a power source for any external components.
- (2) The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the RTC_KLDO_ENn terminal is high.

Figure 5-1 shows an example of the external capacitors.



- A. Decoupling capacitors must be placed as close as possible to the power terminal. Choose the ground closest to the power pin for each decoupling capacitor. In case of interconnecting powers, first insert the decoupling capacitor and then interconnect the powers.
- B. The decoupling capacitor value depends on the characteristics of the board.

Figure 5-1. External Capacitors

5.10 Touch Screen Controller and Analog-to-Digital Subsystem Electrical Parameters

The touch screen controller (TSC) and analog-to-digital converter (ADC) subsystem (TSC_ADC) is an 8-channel general-purpose ADC with optional support for interleaving TSC conversions for 4-wire, 5-wire, or 8-wire resistive panels. The TSC_ADC subsystem can be configured for use in one of the following applications:

- 8 general-purpose ADC channels
- 4-wire TSC with 4 general-purpose ADC channels
- 5-wire TSC with 3 general-purpose ADC channels
- 8-wire TSC.

Table 5-16 summarizes the TSC_ADC subsystem electrical parameters.

Table 5-16. TSC_ADC Electrical Parameters

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------------------|--|---------------------------------|---------------------------------|----------|------|
| Analog Input | | | | | |
| VREFP ⁽¹⁾ | | $(0.5 \times VDDA_ADC) + 0.25$ | | VDDA_ADC | V |
| VREFN ⁽¹⁾ | | 0 | $(0.5 \times VDDA_ADC) - 0.25$ | | V |
| VREFP + VREFN ⁽¹⁾ | | VDDA_ADC | | | V |
| Full-scale input range | Internal voltage reference | 0 | VDDA_ADC | | V |
| | External voltage reference | VREFN | | VREFP | |
| Differential nonlinearity (DNL) | Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V | –1 | 0.5 | 1 | LSB |
| Integral nonlinearity (INL) | Source impedance = 50 Ω Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V | –2 | ±1 | 2 | LSB |
| | Source impedance = 1 kΩ Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V | ±1 | | | |
| Gain error | Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V | ±2 | | | LSB |
| Offset error | Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V | ±2 | | | LSB |
| Input sampling capacitance | | | 5.5 | pF | |
| Signal-to-noise ratio (SNR) | Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V Input signal: 30-kHz sine wave at –0.5-dB full scale | 70 | | | dB |
| Total harmonic distortion (THD) | Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V Input signal: 30-kHz sine wave at –0.5-dB full scale | 75 | | | dB |

Table 5-16. TSC_ADC Electrical Parameters (continued)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|--|--|--|-----|-----|------------------|
| Spurious free dynamic range | Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V Input signal: 30-kHz sine wave at –0.5-dB full scale | | 80 | | dB |
| Signal-to-noise plus distortion | Internal voltage reference: VDDA_ADC = 1.8 V External voltage reference: VREFP – VREFN = 1.8 V Input signal: 30-kHz sine wave at –0.5-dB full scale | | 69 | | dB |
| VREFP and VREFN input impedance | | | 20 | | kΩ |
| Input impedance of AIN[7:0] ⁽²⁾ | f = Input frequency | [1 / ((65.97 × 10 ⁻¹²) × f)] | | | Ω |
| Sampling Dynamics | | | | | |
| Conversion time | | 15 | | | ADC clock cycles |
| Acquisition time | | 2 | | | ADC clock cycles |
| Sampling rate | ADC clock = 3 MHz | | 200 | | kSPS |
| Channel-to-channel isolation | | | 100 | | dB |
| Touch Screen Switch Drivers | | | | | |
| Pullup and pulldown switch ON resistance (Ron) | | | 2 | | Ω |
| Pullup and pulldown switch current leakage I _{leak} | Source impedance = 500 Ω | | | 0.5 | μA |
| Drive current | | | | 25 | mA |
| Touch screen resistance | | | | 6 | kΩ |
| Pen touch detect | | | | 2 | kΩ |

(1) VREFP and VREFN must be tied to ground if the internal voltage reference is used.

(2) This parameter is valid when the respective AIN terminal is configured to operate as a general-purpose ADC input.

6 Power and Clocking

6.1 Power Supplies

6.1.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate for powering on the supplies to be less than $1.0E + 5$ V/s. For instance, as shown in [Figure 6-1](#), TI recommends a value greater than $18 \mu\text{s}$ for the supply ramp slew for a 1.8-V supply.

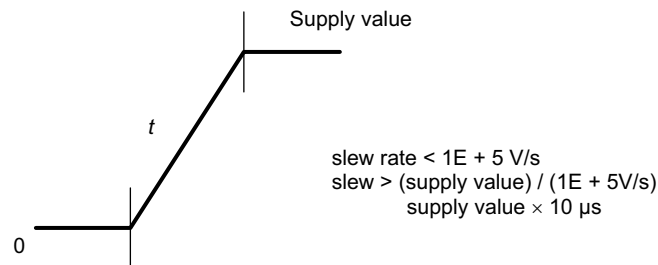
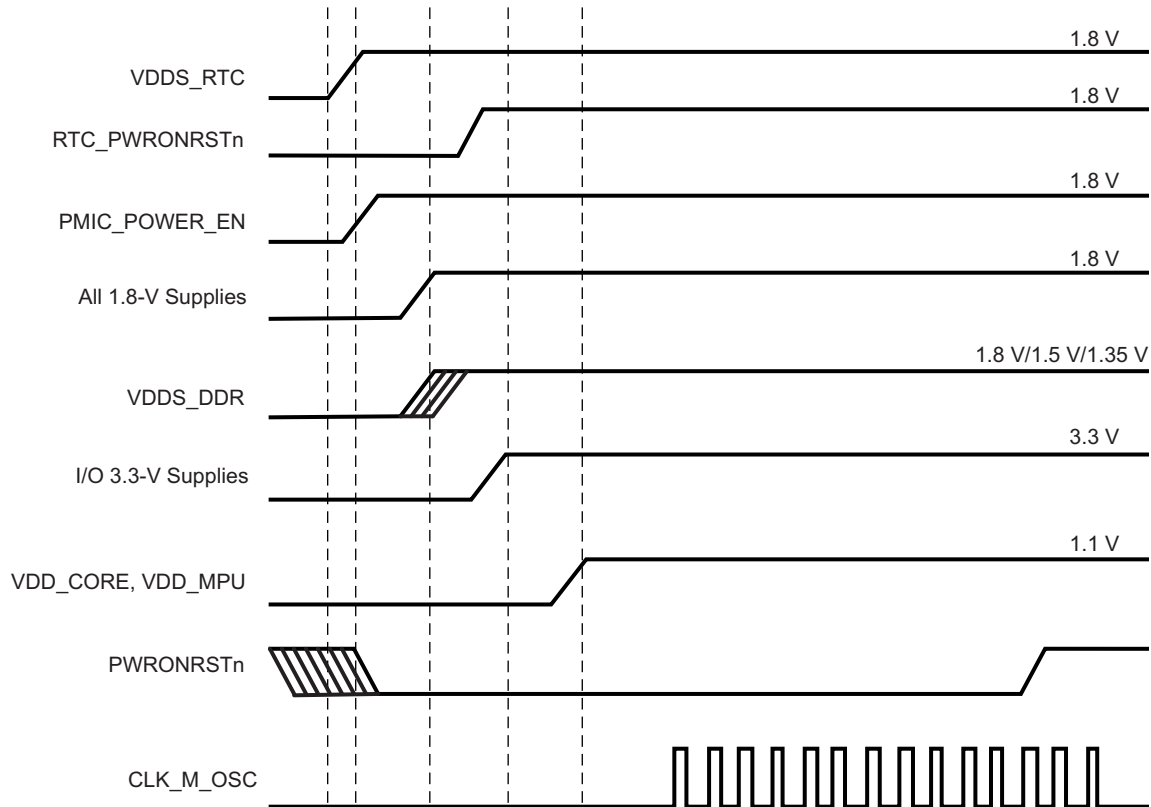
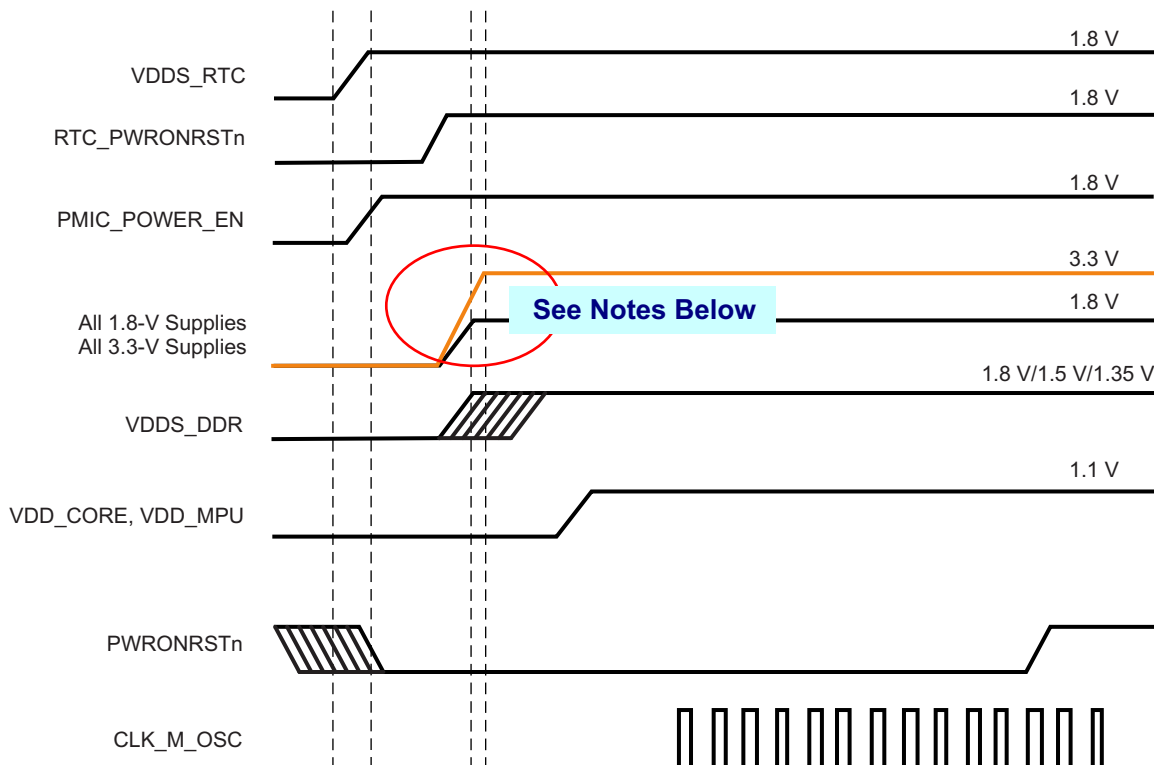


Figure 6-1. Power Supply Slew and Slew Rate



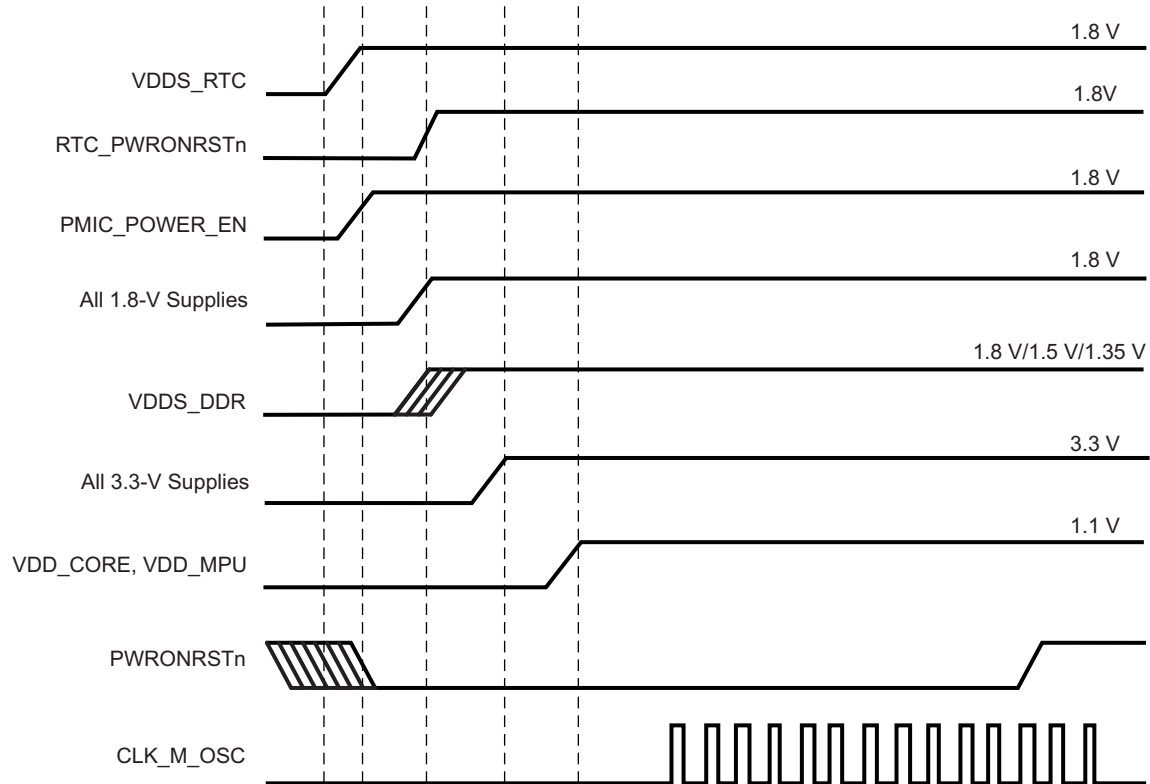
- A. RTC_PWRONRSTn should be asserted for at least 1 ms to provide enough time for the internal RTC LDO output to reach a valid level before RTC reset is released.
- B. When using the ZCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE. The ZCE package option has the VDD_MPU domain merged with the VDD_CORE domain.
- C. If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
- D. If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V I/O power supplies.
- E. VDDS_RTC can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
- F. To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

Figure 6-2. Preferred Power-Supply Sequencing With Dual-Voltage I/Os Configured as 3.3 V



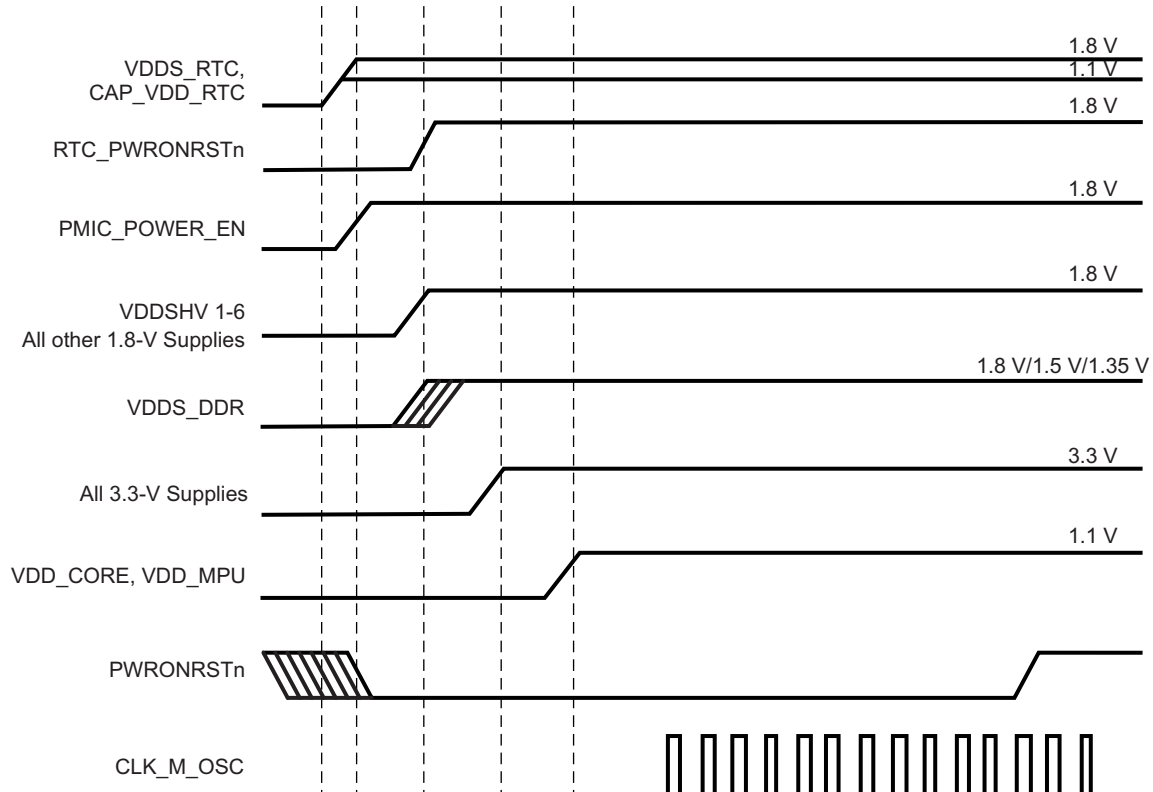
- RTC_PWRONRSTn should be asserted for at least 1 ms to provide enough time for the internal RTC LDO output to reach a valid level before RTC reset is released.
- The 3.3-V I/O power supplies may be ramped simultaneously with the 1.8-V I/O power supplies if the voltage sourced by any 3.3-V power supplies does not exceed the voltage sourced by any 1.8-V power supply by more than 2 V. Serious reliability issues may occur if the system power supply design allows any 3.3-V I/O power supplies to exceed any 1.8-V I/O power supplies by more than 2 V.
- When using the ZCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE. The ZCE package option has the VDD_MPU domain merged with the VDD_CORE domain.
- If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
- If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V I/O power supplies.
- VDDS_RTC can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
- To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

Figure 6-3. Alternate Power-Supply Sequencing With Dual-Voltage I/Os Configured as 3.3 V



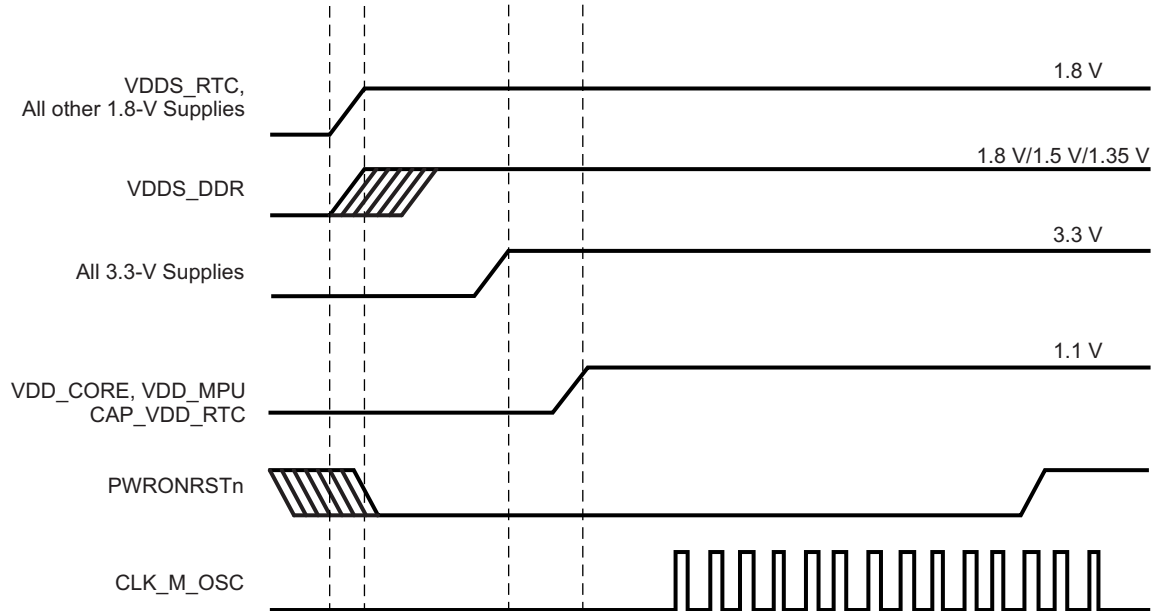
- A. RTC_PWRONRSTn should be asserted for at least 1 ms to provide enough time for the internal RTC LDO output to reach a valid level before RTC reset is released.
- B. When using the ZCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE. The ZCE package option has the VDD_MPU domain merged with the VDD_CORE domain.
- C. If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
- D. If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V I/O power supplies.
- E. VDDS_RTC can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
- F. To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

Figure 6-4. Power-Supply Sequencing With Dual-Voltage I/Os Configured as 1.8 V



- A. RTC_PWRONRSTn should be asserted for at least 1 ms to provide enough time for the internal RTC LDO output to reach a valid level before RTC reset is released.
- B. The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC. If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply.
- C. When using the ZCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE. The ZCE package option has the VDD_MPU domain merged with the VDD_CORE domain.
- D. If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
- E. If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V I/O power supplies.
- F. VDDS_RTC should be ramped at the same time or before CAP_VDD_RTC, but these power inputs can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
- G. To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

Figure 6-5. Power-Supply Sequencing With Internal RTC LDO Disabled



- CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC. If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply. The PMIC_POWER_EN output cannot be used when the RTC is disabled.
- When using the ZCZ package option, VDD_MPU and VDD_CORE power inputs may be powered from the same source if the application only uses operating performance points (OPPs) that define a common power supply voltage for VDD_MPU and VDD_CORE. The ZCE package option has the VDD_MPU domain merged with the VDD_CORE domain.
- If a USB port is not used, the respective VDDA1P8V_USB terminal may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
- If the system uses mDDR or DDR2 memory devices, VDDS_DDR can be ramped simultaneously with the other 1.8-V I/O power supplies.
- VDDS_RTC should be ramped at the same time or before CAP_VDD_RTC, but these power inputs can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE. The power sequence shown provides the lowest leakage option.
- To configure VDDSHVx [1-6] as 1.8 V, power up the respective VDDSHVx [1-6] to 1.8 V following the recommended sequence. To configure VDDSHVx [1-6] as 3.3 V, power up the respective VDDSHVx [1-6] to 3.3 V following the recommended sequence.

Figure 6-6. Power-Supply Sequencing With RTC Feature Disabled

6.1.2 Power-Down Sequencing

PWRONRSTn input terminal should be taken low, which stops all internal clocks before power supplies are turned off. All other external clocks to the device should be shut off.

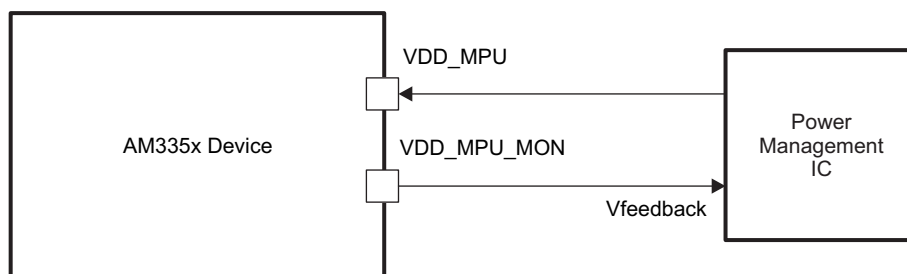
The preferred way to sequence power down is to have all the power supplies ramped down sequentially in the exact reverse order of the power-up sequencing. In other words, the power supply that has been ramped up first should be the last one that should be ramped down. This ensures there would be no spurious current paths during the power-down sequence. The VDDS power supply must ramp down after all 3.3-V VDDSHVx [1-6] power supplies.

If it is desired to ramp down VDDS and VDDSHVx [1-6] simultaneously, it should always be ensured that the difference between VDDS and VDDSHVx [1-6] during the entire power-down sequence is <2 V. Any violation of this could cause reliability risks for the device. TI recommends maintaining VDDS ≥ 1.5 V as all the other supplies fully ramp down to minimize in-rush currents.

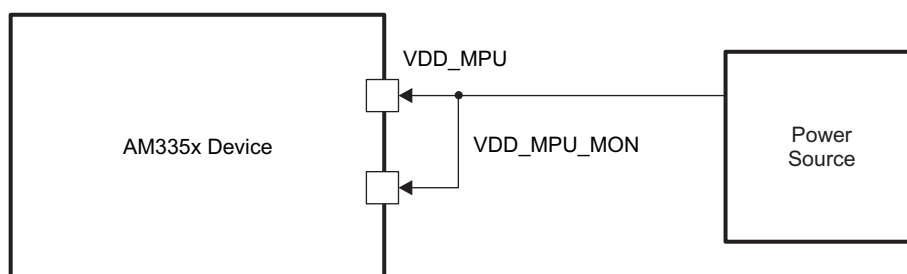
If none of the VDDSHVx [1-6] power supplies are configured as 3.3 V, the VDDS power supply may ramp down along with the VDDSHVx [1-6] supplies or after all the VDDSHVx [1-6] supplies have ramped down. TI recommends maintaining $V_{DDS} \geq 1.5V$ as all the other supplies fully ramp down to minimize in-rush currents.

6.1.3 VDD_MPU_MON Connections

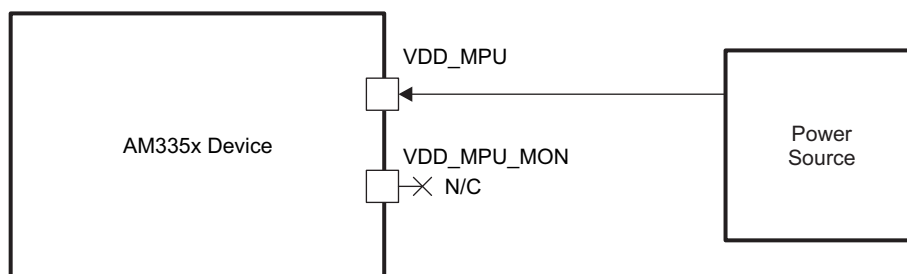
Figure 6-7 shows the VDD_MPU_MON connectivity. VDD_MPU_MON connectivity is available only on the ZCZ package.



Connection for VDD_MPU_MON if voltage monitoring is used



Preferred connection for VDD_MPU_MON if voltage monitoring is NOT used



Optional connection for VDD_MPU_MON if voltage monitoring is NOT used

Figure 6-7. VDD_MPU_MON Connectivity

6.1.4 Digital Phase-Locked Loop Power Supply Requirements

The digital phase-locked loop (DPLL) provides all interface clocks and functional clocks to the processor of the AM335x device. The AM335x device integrates five different DPLLs—Core DPLL, Per DPLL, LCD DPLL, DDR DPLL, MPU DPLL.

Figure 6-8 shows the power supply connectivity implemented in the AM335x device. Table 6-1 provides the power supply requirements for the DPLL.

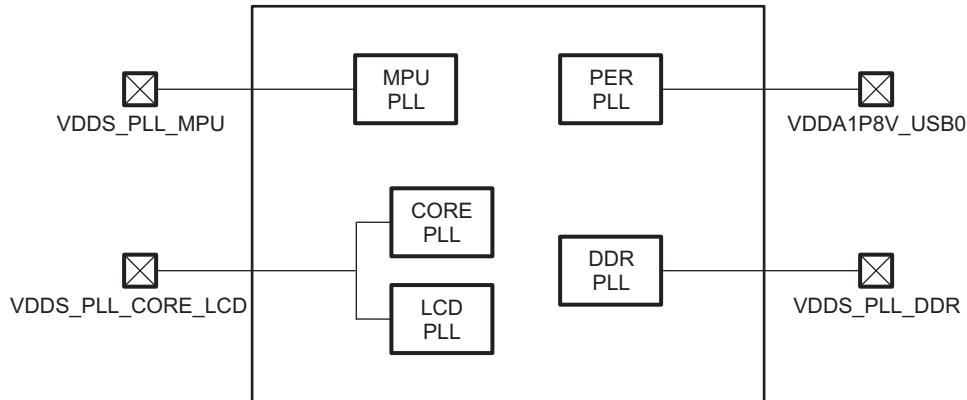


Figure 6-8. DPLL Power Supply Connectivity

Table 6-1. DPLL Power Supply Requirements

| SUPPLY NAME | DESCRIPTION | MIN | NOM | MAX | UNIT |
|-------------------|---|------|-----|------|----------|
| VDDA1P8V_USB0 | Supply voltage range for USBPHY and PER DPLL, Analog, 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | Max peak-to-peak supply noise | | | 50 | mV (p-p) |
| VDDS_PLL_MPU | Supply voltage range for DPLL MPU, analog | 1.71 | 1.8 | 1.89 | V |
| | Max peak-to-peak supply noise | | | 50 | mV (p-p) |
| VDDS_PLL_CORE_LCD | Supply voltage range for DPLL CORE and LCD, analog | 1.71 | 1.8 | 1.89 | V |
| | Max peak-to-peak supply noise | | | 50 | mV (p-p) |
| VDDS_PLL_DDR | Supply voltage range for DPLL DDR, analog | 1.71 | 1.8 | 1.89 | V |
| | Max peak-to-peak supply noise | | | 50 | mV (p-p) |

6.2 Clock Specifications

6.2.1 Input Clock Specifications

The AM335x device has two clock inputs. Each clock input passes through an internal oscillator which can be connected to an external crystal circuit (oscillator mode) or external LVCMOS square-wave digital clock source (bypass mode). The oscillators automatically operate in bypass mode when their input is connected to an external LVCMOS square-wave digital clock source. The oscillator associated with a specific clock input must be enabled when the clock input is being used in either oscillator mode or bypass mode.

The OSC1 oscillator provides a 32.768-kHz reference clock to the real-time clock (RTC) and is connected to the RTC_XTALIN and RTC_XTALOUT terminals. This clock source is referred to as the 32K oscillator (CLK_32K_RTC) in the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#). OSC1 is disabled by default after power is applied. This clock input is optional and may not be required if the RTC is configured to receive a clock from the internal 32k RC oscillator (CLK_RC32K) or peripheral PLL (CLK_32KHZ) which receives a reference clock from the OSC0 input.

The OSC0 oscillator provides a 19.2-MHz, 24-MHz, 25-MHz, or 26-MHz reference clock which is used to clock all non-RTC functions and is connected to the XTALIN and XTALOUT terminals. This clock source is referred to as the master oscillator (CLK_M_OSC) in the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#). OSC0 is enabled by default after power is applied.

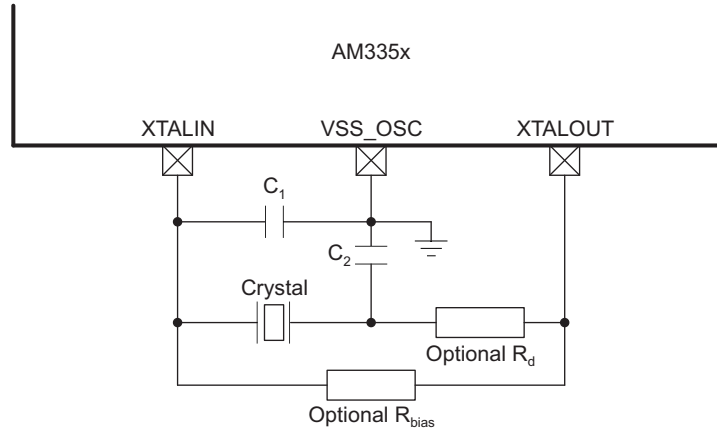
For more information related to recommended circuit topologies and crystal oscillator circuit requirements for these clock inputs, see [Section 6.2.2](#).

6.2.2 Input Clock Requirements

6.2.2.1 OSC0 Internal Oscillator Clock Source

[Figure 6-9](#) shows the recommended crystal circuit. TI recommends that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0- Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

The XTALIN terminal has a 15- to 40-k Ω internal pulldown resistor which is enabled when OSC0 is disabled. This internal resistor prevents the XTALIN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.



Copyright © 2016, Texas Instruments Incorporated

- A. Oscillator components (Crystal, C_1 , C_2 , optional R_{bias} and R_d) must be located close to the AM335x package. Parasitic capacitance to the VSS_OSC and respective crystal circuit component grounds should be connected directly to the nearest PCB digital ground (VSS).
- B. C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. The value of capacitors C_1 and C_2 should be selected to provide the total load capacitance, C_L , specified by the crystal manufacturer. The total load capacitance is $C_L = [(C_1 \times C_2) / (C_1 + C_2)] + C_{shunt}$, where C_{shunt} is the crystal shunt capacitance (C_0) specified by the crystal manufacturer plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the AM335x XTALIN and XTALOUT signals. For recommended values of crystal circuit components, see [Table 6-2](#).

Figure 6-9. OSC0 Crystal Circuit Schematic

Table 6-2. OSC0 Crystal Circuit Requirements

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|-------------|--|--|-----|---------------------|------|----------|
| f_{xtal} | Crystal parallel resonance frequency | Fundamental mode oscillation only | | 19.2, 24, 25, or 26 | | MHz |
| | Crystal frequency stability and tolerance ⁽¹⁾ | | -50 | | 50 | ppm |
| C_{C1} | C_1 capacitance | $C_{shunt} \leq 5$ pF | 12 | | 24 | pF |
| | | $C_{shunt} > 5$ pF | 18 | | 24 | |
| C_{C2} | C_2 capacitance | $C_{shunt} \leq 5$ pF | 12 | | 24 | pF |
| | | $C_{shunt} > 5$ pF | 18 | | 24 | |
| C_{shunt} | Shunt capacitance | | | | 7 | pF |
| ESR | Crystal effective series resistance | $f_{xtal} = 19.2$ MHz, oscillator has nominal negative resistance of 272 Ω and worst-case negative resistance of 163 Ω | | | 54.4 | Ω |
| | | $f_{xtal} = 24$ MHz, oscillator has nominal negative resistance of 240 Ω and worst-case negative resistance of 144 Ω | | | 48.0 | |
| | | $f_{xtal} = 25$ MHz, oscillator has nominal negative resistance of 233 Ω and worst-case negative resistance of 140 Ω | | | 46.6 | |
| | | $f_{xtal} = 26$ MHz, oscillator has nominal negative resistance of 227 Ω and worst-case negative resistance of 137 Ω | | | 45.3 | |

(1) Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.

Table 6-3. OSC0 Crystal Circuit Characteristics

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------------------|---|-------------|--|-----|------|
| C _{pkg} | Shunt capacitance of package | ZCE package | 0.01 | | pF |
| | | ZCZ package | 0.01 | | |
| P _{xtal} | The actual values of the ESR, f_{xtal} , and C _L should be used to yield a typical crystal power dissipation value. Using the maximum values specified for ESR, f_{xtal} , and C _L parameters yields a maximum power dissipation value. | | $P_{xtal} = 0.5 ESR (2 \pi f_{xtal} C_L V_{DD5_OSC})^2$ | | |
| t _{sx} | Start-up time | | 1.5 | | ms |

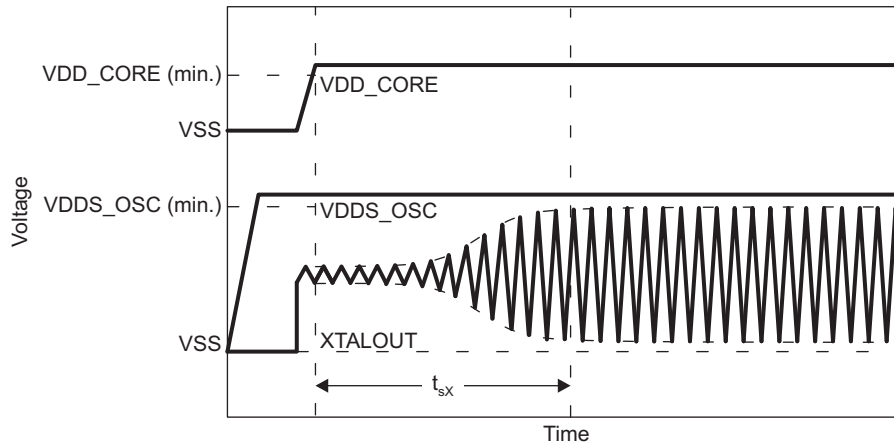
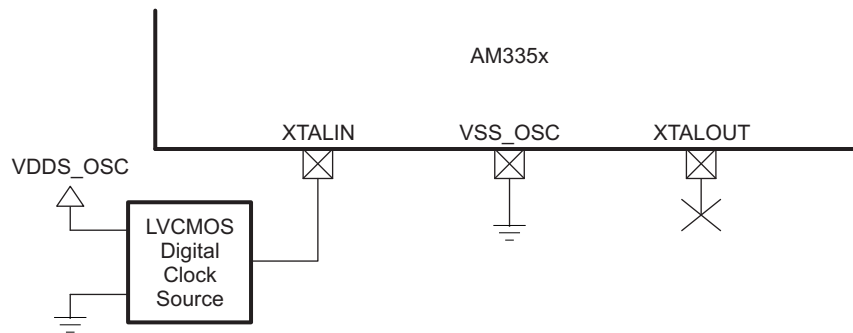


Figure 6-10. OSC0 Start-Up Time

6.2.2.2 OSC0 LVC MOS Digital Clock Source

Figure 6-11 shows the recommended oscillator connections when OSC0 is connected to an LVC MOS square-wave digital clock source. The LVC MOS clock source is connected to the XTALIN terminal. The ground for the LVC MOS clock source and VSS_ OSC should be connected directly to the nearest PCB digital ground (VSS). In this mode of operation, the XTALOUT terminal should not be used to source any external components. The PCB design should provide a mechanism to disconnect the XTALOUT terminal from any external components or signal traces that may couple noise into OSC0 via the XTALOUT terminal.

The XTALIN terminal has a 15- to 40-kΩ internal pulldown resistor which is enabled when OSC0 is disabled. This internal resistor prevents the XTALIN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.



Copyright © 2016, Texas Instruments Incorporated

Figure 6-11. OSC0 LVC MOS Circuit Schematic

Table 6-4. OSC0 LVC MOS Reference Clock Requirements

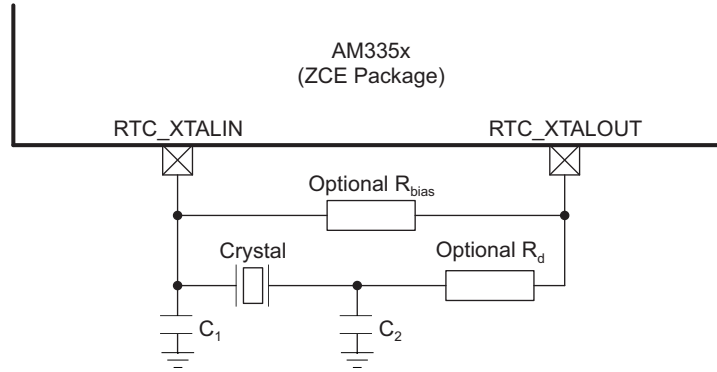
| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------------------|---|-----|---------------------|-----|------|
| $f_{(XTALIN)}$ | Frequency, LVC MOS reference clock | | 19.2, 24, 25, or 26 | | MHz |
| | Frequency, LVC MOS reference clock stability and tolerance ⁽¹⁾ | -50 | | 50 | ppm |
| $t_{dc(XTALIN)}$ | Duty cycle, LVC MOS reference clock period | 45% | | 55% | |
| $t_{jpp(XTALIN)}$ | Jitter peak-to-peak, LVC MOS reference clock period | -1% | | 1% | |
| $t_{R(XTALIN)}$ | Time, LVC MOS reference clock rise | | | 5 | ns |
| $t_{F(XTALIN)}$ | Time, LVC MOS reference clock fall | | | 5 | ns |

(1) Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.

6.2.2.3 OSC1 Internal Oscillator Clock Source

Figure 6-12 shows the recommended crystal circuit for OSC1 of the ZCE package and Figure 6-13 shows the recommended crystal circuit for OSC1 of the ZCZ package. TI recommends that preproduction PCB designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

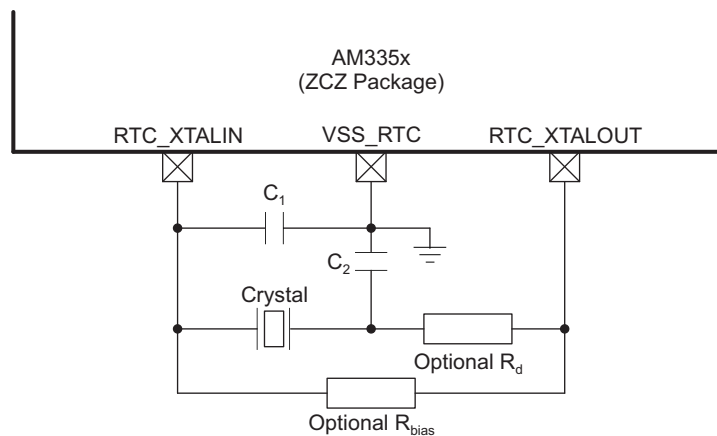
The RTC_XTALIN terminal has a 10- to 40-kΩ internal pullup resistor which is enabled when OSC1 is disabled. This internal resistor prevents the RTC_XTALIN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.



Copyright © 2016, Texas Instruments Incorporated

- A. Oscillator components (Crystal, C_1 , C_2 , optional R_{bias} and R_d) must be located close to the AM335x package. Parasitic capacitance to the PCB ground and other signals should be minimized to reduce noise coupled into the oscillator. VSS_RTC and respective crystal circuit component grounds should be connected directly to the nearest PCB digital ground (VSS).
- B. C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. The value of capacitors C_1 and C_2 should be selected to provide the total load capacitance, C_L , specified by the crystal manufacturer. The total load capacitance is $C_L = [(C_1 \times C_2) / (C_1 + C_2)] + C_{shunt}$, where C_{shunt} is the crystal shunt capacitance (C_0) specified by the crystal manufacturer plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the AM335x RTC_XTALIN and RTC_XTALOUT signals. For recommended values of crystal circuit components, see [Table 6-5](#).

Figure 6-12. OSC1 (ZCE Package) Crystal Circuit Schematic



Copyright © 2016, Texas Instruments Incorporated

- A. Oscillator components (Crystal, C_1 , C_2 , optional R_{bias} and R_d) must be located close to the AM335x package. Parasitic capacitance to the PCB ground and other signals should be minimized to reduce noise coupled into the oscillator. VSS_RTC and respective crystal circuit component grounds should be connected directly to the nearest PCB digital ground (VSS).
- B. C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. The value of capacitors C_1 and C_2 should be selected to provide the total load capacitance, C_L , specified by the crystal manufacturer. The total load capacitance is $C_L = [(C_1 \times C_2) / (C_1 + C_2)] + C_{shunt}$, where C_{shunt} is the crystal shunt capacitance (C_0) specified by the crystal manufacturer plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the AM335x RTC_XTALIN and RTC_XTALOUT signals. For recommended values of crystal circuit components, see [Table 6-5](#).

Figure 6-13. OSC1 (ZCZ Package) Crystal Circuit Schematic

Table 6-5. OSC1 Crystal Circuit Requirements

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|-------------|--|--|-------|--------|------|------------|
| f_{xtal} | Crystal parallel resonance frequency | Fundamental mode oscillation only | | 32.768 | | kHz |
| | Crystal frequency stability and tolerance ⁽¹⁾ | Maximum RTC error = 10.512 minutes per year | -20.0 | | 20.0 | ppm |
| | | Maximum RTC error = 26.28 minutes per year | -50.0 | | 50.0 | ppm |
| C_{C1} | C_1 capacitance | | 12.0 | | 24.0 | pF |
| C_{C2} | C_2 capacitance | | 12.0 | | 24.0 | pF |
| C_{shunt} | Shunt capacitance | | | | 1.5 | pF |
| ESR | Crystal effective series resistance | $f_{xtal} = 32.768$ kHz, oscillator has nominal negative resistance of 725 k Ω and worst-case negative resistance of 250 k Ω | | | 80 | k Ω |

(1) Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.

Table 6-6. OSC1 Crystal Circuit Characteristics

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|------------|---|-------------|---|------|-----|------|
| C_{pkg} | Shunt capacitance of package | ZCE package | | 0.17 | | pF |
| | | ZCZ package | | 0.01 | | pF |
| P_{xtal} | The actual values of the ESR, f_{xtal} , and C_L should be used to yield a typical crystal power dissipation value. Using the maximum values specified for ESR, f_{xtal} , and C_L parameters yields a maximum power dissipation value. | | $P_{xtal} = 0.5 ESR (2 \pi f_{xtal} C_L V_{DD_RTC})^2$ | | | |
| t_{sX} | Start-up time | | | 2 | | s |

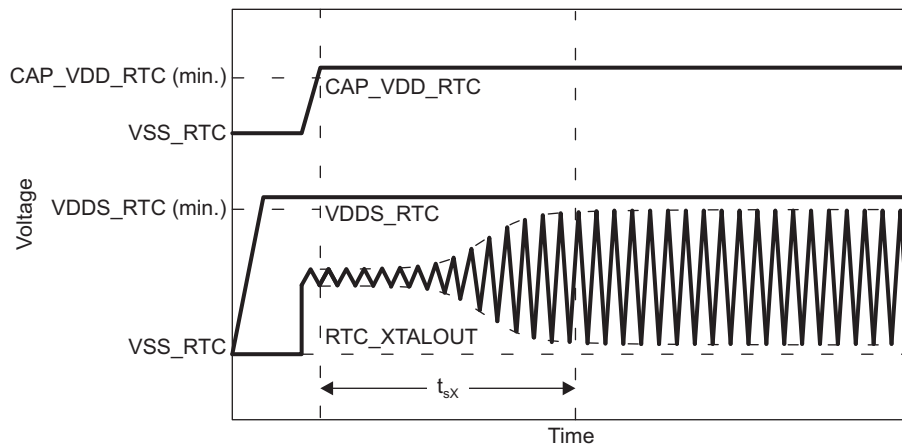
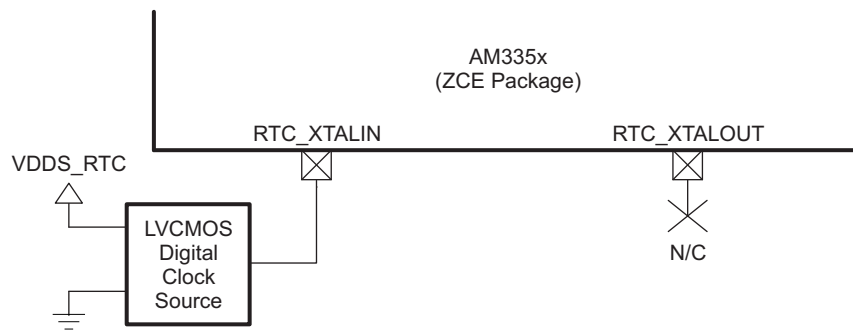


Figure 6-14. OSC1 Start-up Time

6.2.2.4 OSC1 LVC MOS Digital Clock Source

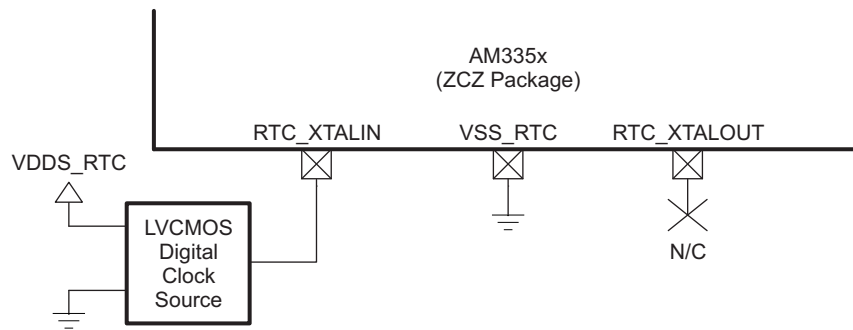
Figure 6-15 shows the recommended oscillator connections when OSC1 of the ZCE package is connected to an LVC MOS square-wave digital clock source and Figure 6-16 shows the recommended oscillator connections when OSC1 of the ZCZ package is connected to an LVC MOS square-wave digital clock source. The LVC MOS clock source is connected to the RTC_XTALIN terminal. The ground for the LVC MOS clock source and VSS_RTC of the ZCZ package should be connected directly to the nearest PCB digital ground (VSS). In this mode of operation, the RTC_XTALOUT terminal should not be used to source any external components. The PCB design should provide a mechanism to disconnect the RTC_XTALOUT terminal from any external components or signal traces that may couple noise into OSC1 through the RTC_XTALOUT terminal.

The RTC_XTALIN terminal has a 10- to 40-kΩ internal pullup resistor which is enabled when OSC1 is disabled. This internal resistor prevents the RTC_XTALIN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.



Copyright © 2016, Texas Instruments Incorporated

Figure 6-15. OSC1 (ZCE Package) LVC MOS Circuit Schematic



Copyright © 2016, Texas Instruments Incorporated

Figure 6-16. OSC1 (ZCZ Package) LVC MOS Circuit Schematic

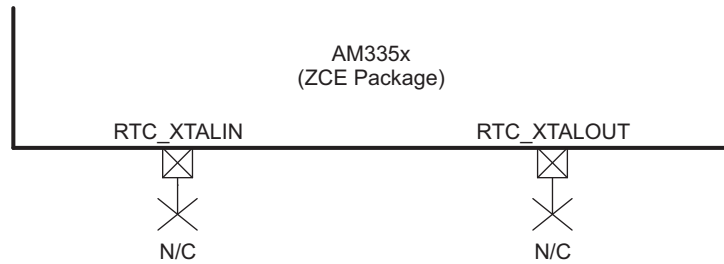
Table 6-7. OSC1 LVC MOS Reference Clock Requirements

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------------------------------|---|---|--------|-----|------|
| f _(RTC_XTALIN) | Frequency, LVC MOS reference clock | | 32.768 | | kHz |
| | Frequency, LVC MOS reference clock stability and tolerance ⁽¹⁾ | Maximum RTC error = 10.512 minutes/year | -20 | 20 | ppm |
| | | Maximum RTC error = 26.28 minutes/year | -50 | 50 | ppm |
| t _{dc} (RTC_XTALIN) | Duty cycle, LVC MOS reference clock period | 45% | | 55% | |
| t _{jpp} (RTC_XTALIN) | Jitter peak-to-peak, LVC MOS reference clock period | -1% | | 1% | |
| t _R (RTC_XTALIN) | Time, LVC MOS reference clock rise | | | 5 | ns |
| t _F (RTC_XTALIN) | Time, LVC MOS reference clock fall | | | 5 | ns |

(1) Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.

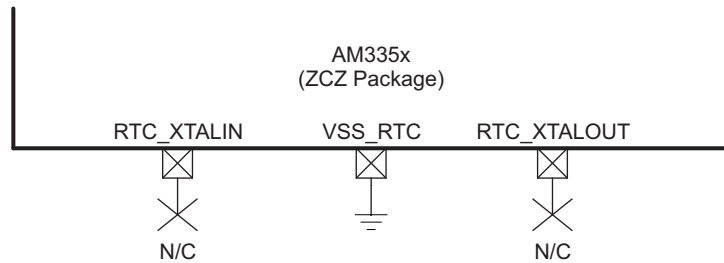
6.2.2.5 OSC1 Not Used

Figure 6-17 shows the recommended oscillator connections when OSC1 of the ZCE package is not used and Figure 6-18 shows the recommended oscillator connections when OSC1 of the ZCZ package is not used. An internal 10-kΩ pullup on the RTC_XTALIN terminal is turned on when OSC1 is disabled to prevent this input from floating to an invalid logic level which may increase leakage current through the oscillator input buffer. OSC1 is disabled by default after power is applied. Therefore, both RTC_XTALIN and RTC_XTALOUT terminals should be a no connect (NC) when OSC1 is not used.



Copyright © 2016, Texas Instruments Incorporated

Figure 6-17. OSC1 (ZCE Package) Not Used Schematic



Copyright © 2016, Texas Instruments Incorporated

Figure 6-18. OSC1 (ZCZ Package) Not Used Schematic

6.2.3 Output Clock Specifications

The AM335x device has two clock output signals. The CLKOUT1 signal is always a replica of the OSC0 input clock which is referred to as the master oscillator (CLK_M_OSC) in the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#). The CLKOUT2 signal can be configured to output the OSC1 input clock, which is referred to as the 32K oscillator (CLK_32K_RTC) in the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#), or four other internal clocks. For more information related to configuring these clock output signals, see the *CLKOUT Signals* section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

6.2.4 Output Clock Characteristics

NOTE

The AM335x CLKOUT1 and CLKOUT2 clock outputs should not be used as a synchronous clock for any of the peripheral interfaces because they were not timing closed to any other signals. These clock outputs also were not designed to source any time critical external circuits that require a low jitter reference clock. The jitter performance of these outputs is unpredictable due to complex combinations of many system variables. For example, CLKOUT2 may be sourced from several PLLs with each PLL supporting many configurations that yield different jitter performance. There are also other unpredictable contributors to jitter performance such as application specific noise or crosstalk into the clock circuits. Therefore, there are no plans to specify jitter performance for these outputs.

6.2.4.1 CLKOUT1

The CLKOUT1 signal can be output on the XDMA_EVENT_INTR0 terminal. This terminal connects to one of seven internal signals via configurable multiplexers. The XDMA_EVENT_INTR0 multiplexer must be configured for Mode 3 to connect the CLKOUT1 signal to the XDMA_EVENT_INTR0 terminal.

The default reset configuration of the XDMA_EVENT_INTR0 multiplexer is selected by the logic level applied to the LCD_DATA5 terminal on the rising edge of PWRONRSTn. The XDMA_EVENT_INTR0 multiplexer is configured to Mode 7 if the LCD_DATA5 terminal is low on the rising edge of PWRONRSTn or Mode 3 if the LCD_DATA5 terminal is high on the rising edge of PWRONRSTn. This allows the CLKOUT1 signal to be output on the XDMA_EVENT_INTR0 terminal without software intervention. In this mode, the output is held low while PWRONRSTn is active and begins to toggle after PWRONRSTn is released.

6.2.4.2 CLKOUT2

The CLKOUT2 signal can be output on the XDMA_EVENT_INTR1 terminal. This terminal connects to one of seven internal signals via configurable multiplexers. The XDMA_EVENT_INTR1 multiplexer must be configured for Mode 3 to connect the CLKOUT2 signal to the XDMA_EVENT_INTR1 terminal.

The default reset configuration of the XDMA_EVENT_INTR1 multiplexer is always Mode 7. Software must configure the XDMA_EVENT_INTR1 multiplexer to Mode 3 for the CLKOUT2 signal to be output on the XDMA_EVENT_INTR1 terminal.

7 Peripheral Information and Timings

The AM335x device contains many peripheral interfaces. In order to reduce package size and lower overall system cost while maintaining maximum functionality, many of the AM335x terminals can multiplex up to eight signal functions. Although there are many combinations of pin multiplexing that are possible, only a certain number of sets, called I/O Sets, are valid due to timing limitations. These valid I/O Sets were carefully chosen to provide many possible application scenarios for the user.

Texas Instruments has developed a Windows-based application called Pin Mux Utility that helps a system designer select the appropriate pin-multiplexing configuration for their AM335x-based product design. The Pin Mux Utility provides a way to select valid I/O Sets of specific peripheral interfaces to ensure the pin-multiplexing configuration selected for a design only uses valid I/O Sets supported by the AM335x device.

7.1 Parameter Information

The data provided in the following Timing Requirements and Switching Characteristics tables assumes the device is operating within the Recommended Operating Conditions defined in [Section 5](#), unless otherwise noted.

7.1.1 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing or decreasing such delays. TI recommends using the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

The timing parameter values specified in this data manual assume the SLEWCTRL bit in each pad control register is configured for fast mode (0b).

For the mDDR(LPDDR), DDR2, DDR3, DDR3L memory interface, it is *not* necessary to use the IBIS models to analyze timing characteristics. TI provides a PCB routing rules solution that describes the routing rules to ensure the mDDR(LPDDR), DDR2, DDR3, DDR3L memory interface timings are met.

7.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals *must* transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

7.3 OPP50 Support

Some peripherals and features have limited support when the device is operating in OPP50. A complete list of these limitations follows.

Not supported when operating in OPP50:

- CPSW
- DDR3
- DEBUGSS-Trace
- GPMC Asynchronous Mode
- LCDL LIDD Mode
- MDIO
- PRU-ICSS MII

Reduced performance when operating in OPP50:

- DDR2
- DEBUGSS-JTAG
- GPMC Synchronous Mode
- LCDL Raster Mode
- LPDDR
- McASP
- McSPI
- MMCSD

7.4 Controller Area Network (CAN)

For more information, see the Controller Area Network (CAN) section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

7.4.1 DCAN Electrical Data and Timing

Table 7-1. Timing Requirements for DCANx Receive

(see [Figure 7-1](#))

| NO. | | MIN | MAX | UNIT |
|-----|-------------------------|--------------------------------|---------------|------|
| | $f_{\text{baud(baud)}}$ | Maximum programmable baud rate | | 1 |
| 1 | $t_{w(\text{RX})}$ | $H - 2^{(1)}$ | $H + 2^{(1)}$ | ns |

(1) H = Period of baud rate, 1 / programmed baud rate

Table 7-2. Switching Characteristics for DCANx Transmit

(see [Figure 7-1](#))

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|-------------------------|--------------------------------|---------------|------|
| | $f_{\text{baud(baud)}}$ | Maximum programmable baud rate | | 1 |
| 2 | $t_{w(\text{TX})}$ | $H - 2^{(1)}$ | $H + 2^{(1)}$ | ns |

(1) H = Period of baud rate, 1 / programmed baud rate

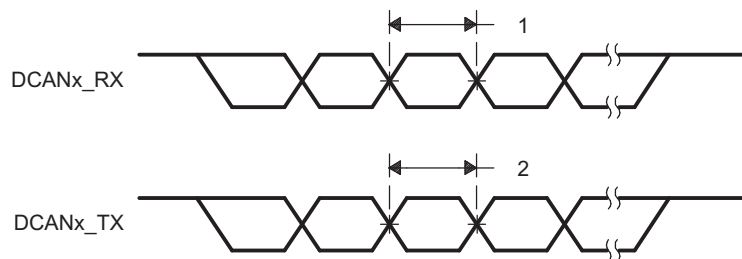


Figure 7-1. DCANx Timings

7.5 DMTimer

7.5.1 DMTimer Electrical Data and Timing

Table 7-3. Timing Requirements for DMTimer [1-7]

(see Figure 7-2)

| NO. | | | MIN | MAX | UNIT |
|-----|-----------------|--------------------|----------------|-----|------|
| 1 | $t_{c(TCLKIN)}$ | Cycle time, TCLKIN | $4P + 1^{(1)}$ | | ns |

(1) P = Period of PICKOCP (interface clock).

Table 7-4. Switching Characteristics for DMTimer [4-7]

(see Figure 7-2)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|------------------|----------------------|----------------|-----|------|
| 2 | $t_{w(TIMERxH)}$ | Pulse duration, high | $4P - 3^{(1)}$ | | ns |
| 3 | $t_{w(TIMERxL)}$ | Pulse duration, low | $4P - 3^{(1)}$ | | ns |

(1) P = Period of PICKTIMER (functional clock).

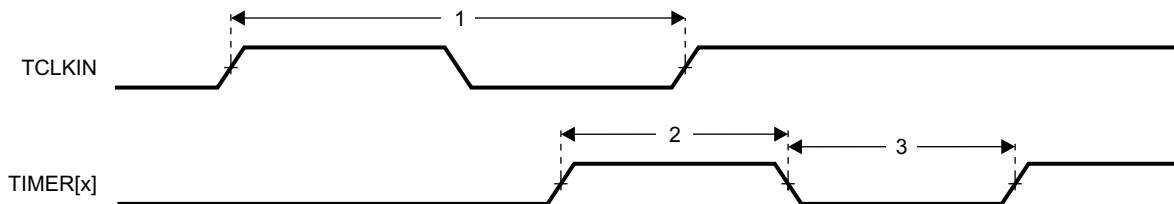


Figure 7-2. Timer Timing

7.6 Ethernet Media Access Controller (EMAC) and Switch

7.6.1 EMAC and Switch Electrical Data and Timing

The EMAC and Switch implemented in the AM335x device supports GMII mode, but the AM335x design does not pin out 9 of the 24 GMII signals. This was done to reduce the total number of package terminals. Therefore, the AM335x device does not support GMII mode. MII mode is supported with the remaining GMII signals.

The *AM335x and AMIC110 Sitara Processors Technical Reference Manual* and this document may reference internal signal names when discussing peripheral input and output signals because many of the AM335x package terminals can be multiplexed to one of several peripheral signals. For example, the AM335x terminal names for port 1 of the EMAC and switch have been changed from GMII to MII to indicate their Mode 0 function, but the internal signal is named GMII. However, documents that describe the Ethernet switch reference these signals by their internal signal name. For a cross-reference of internal signal names to terminal names, see [Table 4-2](#).

Operation of the EMAC and switch is not supported for OPP50.

Table 7-5. EMAC and Switch Timing Conditions

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|------------------|-----|------------------|------|
| Input Conditions | | | | | |
| t_R | Input signal rise time | 1 ⁽¹⁾ | | 5 ⁽¹⁾ | ns |
| t_F | Input signal fall time | 1 ⁽¹⁾ | | 5 ⁽¹⁾ | ns |
| Output Condition | | | | | |
| C_{LOAD} | Output load capacitance | 3 | | 30 | pF |

(1) Except when specified otherwise.

7.6.1.1 EMAC/Switch MDIO Electrical Data and Timing

Table 7-6. Timing Requirements for MDIO_DATA

(see [Figure 7-3](#))

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|--------------------|--|-----|-----|-----|------|
| 1 | $t_{su}(MDIO-MDC)$ | Setup time, MDIO valid before MDC high | 90 | | | ns |
| 2 | $t_h(MDIO-MDC)$ | Hold time, MDIO valid from MDC high | 0 | | | ns |

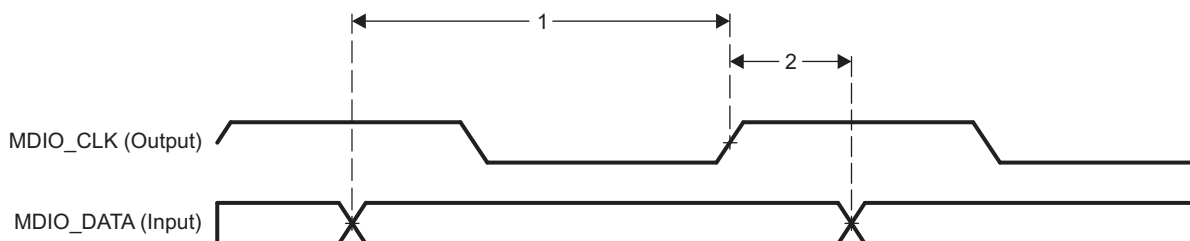


Figure 7-3. MDIO_DATA Timing - Input Mode

Table 7-7. Switching Characteristics for MDIO_CLK

(see [Figure 7-4](#))

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|-------------|--------------------------|-----|-----|-----|------|
| 1 | $t_c(MDC)$ | Cycle time, MDC | 400 | | | ns |
| 2 | $t_w(MDCH)$ | Pulse duration, MDC high | 160 | | | ns |
| 3 | $t_w(MDCL)$ | Pulse duration, MDC low | 160 | | | ns |
| 4 | $t_t(MDC)$ | Transition time, MDC | | | 5 | ns |

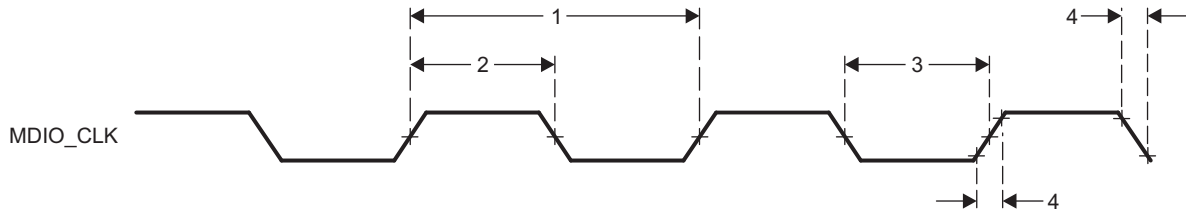


Figure 7-4. MDIO_CLK Timing

Table 7-8. Switching Characteristics for MDIO_DATA

(see Figure 7-5)

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|-------------------|------------------------------------|-----|-----|-----|------|
| 1 | $t_{d(MDC-MDIO)}$ | Delay time, MDC high to MDIO valid | 10 | | 390 | ns |

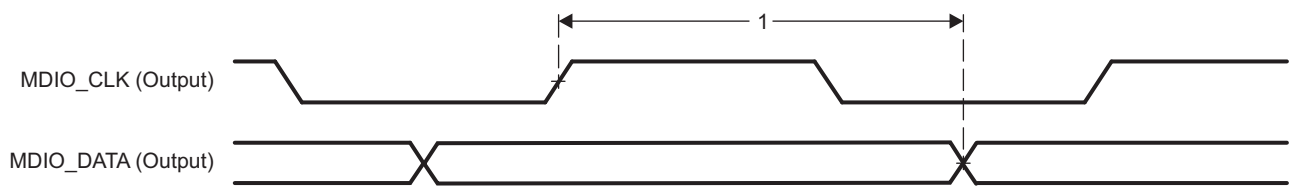


Figure 7-5. MDIO_DATA Timing - Output Mode

7.6.1.2 EMAC and Switch MII Electrical Data and Timing

Table 7-9. Timing Requirements for GMII[x]_RXCLK - MII Mode

(see Figure 7-6)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|-----|-----------------|-----------------------------|---------|-----|--------|----------|-----|--------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_c(RX_CLK)$ | Cycle time, RX_CLK | 399.96 | | 400.04 | 39.996 | | 40.004 | ns |
| 2 | $t_w(RX_CLKH)$ | Pulse duration, RX_CLK high | 140 | | 260 | 14 | | 26 | ns |
| 3 | $t_w(RX_CLKL)$ | Pulse duration, RX_CLK low | 140 | | 260 | 14 | | 26 | ns |
| 4 | $t_t(RX_CLK)$ | Transition time, RX_CLK | | | 5 | | | 5 | ns |

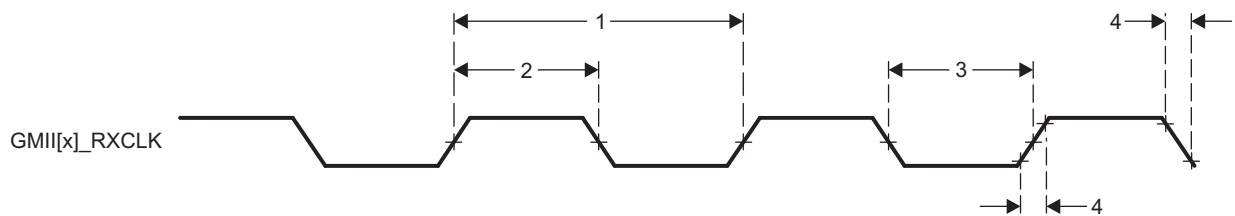


Figure 7-6. GMII[x]_RXCLK Timing - MII Mode

Table 7-10. Timing Requirements for GMII[x]_TXCLK - MII Mode

(see [Figure 7-7](#))

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|-----|-------------------|-----------------------------|---------|-----|--------|----------|-----|--------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(TX_CLK)}$ | Cycle time, TX_CLK | 399.96 | | 400.04 | 39.996 | | 40.004 | ns |
| 2 | $t_{w(TX_CLKH)}$ | Pulse duration, TX_CLK high | 140 | | 260 | 14 | | 26 | ns |
| 3 | $t_{w(TX_CLKL)}$ | Pulse duration, TX_CLK low | 140 | | 260 | 14 | | 26 | ns |
| 4 | $t_{t(TX_CLK)}$ | Transition time, TX_CLK | | | 5 | | | 5 | ns |

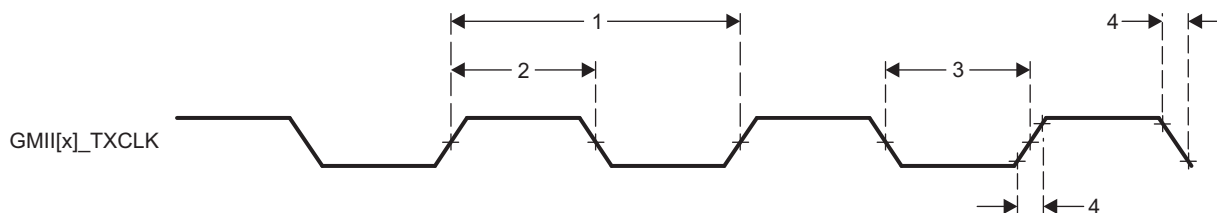


Figure 7-7. GMII[x]_TXCLK Timing - MII Mode

Table 7-11. Timing Requirements for GMII[x]_RXD[3:0], GMII[x]_RXDV, and GMII[x]_RXER - MII Mode

(see [Figure 7-8](#))

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|-----|--------------------------|--|---------|-----|-----|----------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su(RXD-RX_CLK)}$ | Setup time, RXD[3:0] valid before RX_CLK | 8 | | | 8 | | | ns |
| | $t_{su(RX_DV-RX_CLK)}$ | Setup time, RX_DV valid before RX_CLK | | | | | | | |
| | $t_{su(RX_ER-RX_CLK)}$ | Setup time, RX_ER valid before RX_CLK | | | | | | | |
| 2 | $t_{h(RX_CLK-RXD)}$ | Hold time RXD[3:0] valid after RX_CLK | 8 | | | 8 | | | ns |
| | $t_{h(RX_CLK-RX_DV)}$ | Hold time RX_DV valid after RX_CLK | | | | | | | |
| | $t_{h(RX_CLK-RX_ER)}$ | Hold time RX_ER valid after RX_CLK | | | | | | | |

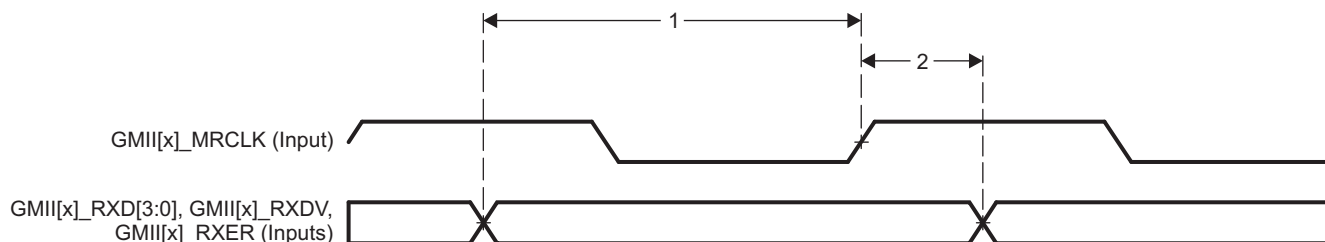


Figure 7-8. GMII[x]_RXD[3:0], GMII[x]_RXDV, GMII[x]_RXER Timing - MII Mode

Table 7-12. Switching Characteristics for GMII[x]_TXD[3:0], and GMII[x]_TXEN - MII Mode

(see [Figure 7-9](#))

| NO. | PARAMETER | | 10 Mbps | | | 100 Mbps | | | UNIT |
|-----|-------------------------|---|---------|-----|-----|----------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{d(TX_CLK-TXD)}$ | Delay time, TX_CLK high to TXD[3:0] valid | 5 | | 25 | 5 | | 25 | ns |
| | $t_{d(TX_CLK-TX_EN)}$ | Delay time, TX_CLK to TX_EN valid | | | | | | | |

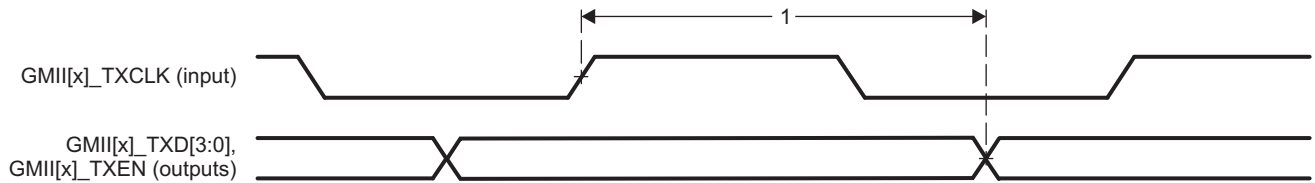


Figure 7-9. GMII[x]_TXD[3:0], GMII[x]_TXEN Timing - MII Mode

7.6.1.3 EMAC and Switch RMIIElectrical Data and Timing

Table 7-13. Timing Requirements for RMII[x]_REFCLK - RMIIE Mode

(see Figure 7-10)

| NO. | | | MIN | TYP | MAX | UNIT |
|-----|--------------------|------------------------------|--------|-----|--------|------|
| 1 | $t_{c(REF_CLK)}$ | Cycle time, REF_CLK | 19.999 | | 20.001 | ns |
| 2 | $t_{w(REF_CLKH)}$ | Pulse duration, REF_CLK high | 7 | | 13 | ns |
| 3 | $t_{w(REF_CLKL)}$ | Pulse duration, REF_CLK low | 7 | | 13 | ns |

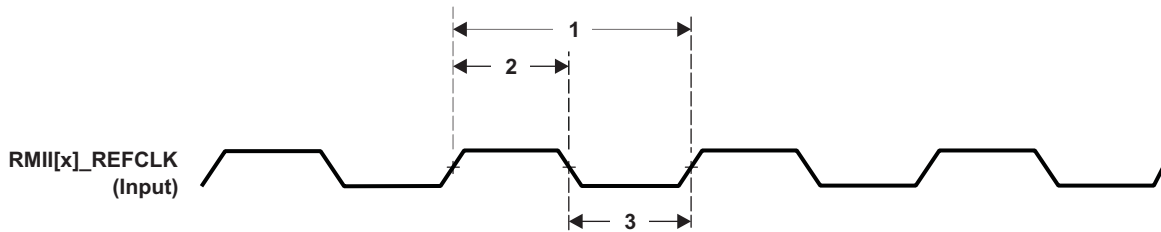


Figure 7-10. RMII[x]_REFCLK Timing - RMIIE Mode

Table 7-14. Timing Requirements for RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RXER - RMIIE Mode

(see Figure 7-11)

| NO. | | | MIN | TYP | MAX | UNIT |
|-----|----------------------------|---|-----|-----|-----|------|
| 1 | $t_{su(RXD-REF_CLK)}$ | Setup time, RXD[1:0] valid before REF_CLK | 4 | | | ns |
| | $t_{su(CRS_DV-REF_CLK)}$ | Setup time, CRS_DV valid before REF_CLK | | | | |
| | $t_{su(RX_ER-REF_CLK)}$ | Setup time, RX_ER valid before REF_CLK | | | | |
| 2 | $t_{h(REF_CLK-RXD)}$ | Hold time RXD[1:0] valid after REF_CLK | 2 | | | ns |
| | $t_{h(REF_CLK-CRS_DV)}$ | Hold time, CRS_DV valid after REF_CLK | | | | |
| | $t_{h(REF_CLK-RX_ER)}$ | Hold time, RX_ER valid after REF_CLK | | | | |

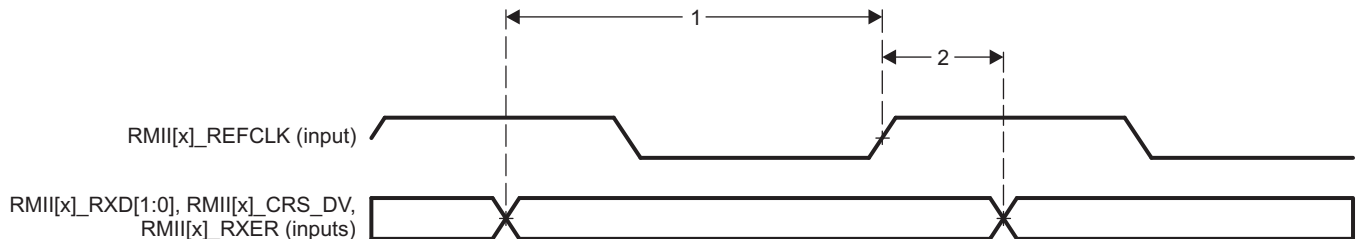


Figure 7-11. RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RXER Timing - RMIIE Mode

Table 7-15. Switching Characteristics for RMII[x]_TXD[1:0], and RMII[x]_TXEN - RMII Mode

(see Figure 7-12)

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|------------------------|--|-----|-----|-----|------|
| 1 | $t_{d(REF_CLK-TXD)}$ | Delay time, REF_CLK high to TXD[1:0] valid | 2 | | 13 | ns |
| | $t_{d(REF_CLK-TXEN)}$ | Delay time, REF_CLK to TXEN valid | | | | |
| 2 | $t_r(TXD)$ | Rise time, TXD outputs | 1 | | 5 | ns |
| | $t_r(TX_EN)$ | Rise time, TX_EN output | | | | |
| 3 | $t_f(TXD)$ | Fall time, TXD outputs | 1 | | 5 | ns |
| | $t_f(TX_EN)$ | Fall time, TX_EN output | | | | |

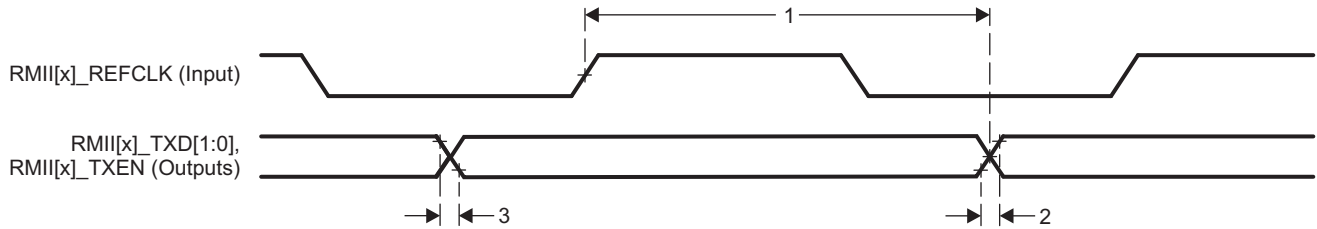


Figure 7-12. RMII[x]_TXD[1:0], RMII[x]_TXEN Timing - RMII Mode

7.6.1.4 EMAC and Switch RGMII Electrical Data and Timing

Table 7-16. Timing Requirements for RGMII[x]_RCLK - RGMII Mode

(see Figure 7-13)

| NO. | | | 10 Mbps | | | 100 Mbps | | | 1000 Mbps | | | UNIT |
|-----|---------------|--------------------------|---------|-----|------|----------|-----|------|-----------|-----|------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(RXC)}$ | Cycle time, RXC | 360 | | 440 | 36 | | 44 | 7.2 | | 8.8 | ns |
| 2 | $t_{w(RXCH)}$ | Pulse duration, RXC high | 160 | | 240 | 16 | | 24 | 3.6 | | 4.4 | ns |
| 3 | $t_{w(RXCL)}$ | Pulse duration, RXC low | 160 | | 240 | 16 | | 24 | 3.6 | | 4.4 | ns |
| 4 | $t_t(RXC)$ | Transition time, RXC | | | 0.75 | | | 0.75 | | | 0.75 | ns |

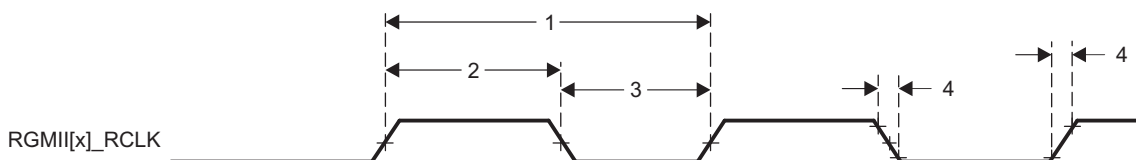
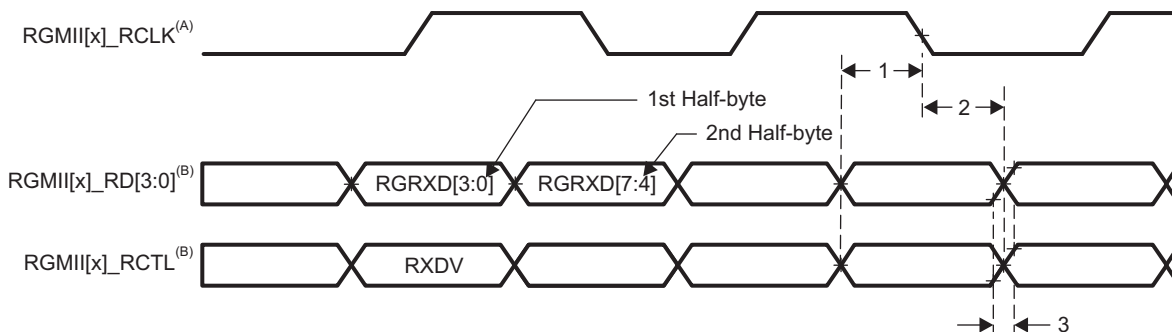


Figure 7-13. RGMII[x]_RCLK Timing - RGMII Mode

Table 7-17. Timing Requirements for RGMII[x]_RD[3:0], and RGMII[x]_RCTL - RGMII Mode

(see Figure 7-14)

| NO. | | | 10 Mbps | | | 100 Mbps | | | 1000 Mbps | | | UNIT |
|-----|-----------------------|--|---------|-----|------|----------|-----|------|-----------|-----|------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su(RD-RXC)}$ | Setup time, RD[3:0] valid before RXC high or low | 1 | | | 1 | | | 1 | | | ns |
| | $t_{su(RX_CTL-RXC)}$ | Setup time, RX_CTL valid before RXC high or low | 1 | | | 1 | | | 1 | | | |
| 2 | $t_h(RXC-RD)$ | Hold time, RD[3:0] valid after RXC high or low | 1 | | | 1 | | | 1 | | | ns |
| | $t_h(RXC-RX_CTL)$ | Hold time, RX_CTL valid after RXC high or low | 1 | | | 1 | | | 1 | | | |
| 3 | $t_t(RD)$ | Transition time, RD | | | 0.75 | | | 0.75 | | | 0.75 | ns |
| | $t_t(RX_CTL)$ | Transition time, RX_CTL | | | 0.75 | | | 0.75 | | | 0.75 | |



- A. RGMII[x]_RCLK must be externally delayed relative to the RGMII[x]_RD[3:0] and RGMII[x]_RCTL signals to meet the respective timing requirements.
- B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RCLK and data bits 7-4 on the falling edge of RGMII[x]_RCLK. Similarly, RGMII[x]_RCTL carries RXDV on rising edge of RGMII[x]_RCLK and RXERR on falling edge of RGMII[x]_RCLK.

Figure 7-14. RGMII[x]_RD[3:0], RGMII[x]_RCTL Timing - RGMII Mode

Table 7-18. Switching Characteristics for RGMII[x]_TCLK - RGMII Mode

(see Figure 7-15)

| NO. | PARAMETER | | 10 Mbps | | | 100 Mbps | | | 1000 Mbps | | | UNIT |
|-----|---------------|--------------------------|---------|-----|------|----------|-----|------|-----------|-----|------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(TXC)}$ | Cycle time, TXC | 360 | | 440 | 36 | | 44 | 7.2 | | 8.8 | ns |
| 2 | $t_{w(TXCH)}$ | Pulse duration, TXC high | 160 | | 240 | 16 | | 24 | 3.6 | | 4.4 | ns |
| 3 | $t_{w(TXCL)}$ | Pulse duration, TXC low | 160 | | 240 | 16 | | 24 | 3.6 | | 4.4 | ns |
| 4 | $t_t(TXC)$ | Transition time, TXC | | | 0.75 | | | 0.75 | | | 0.75 | ns |

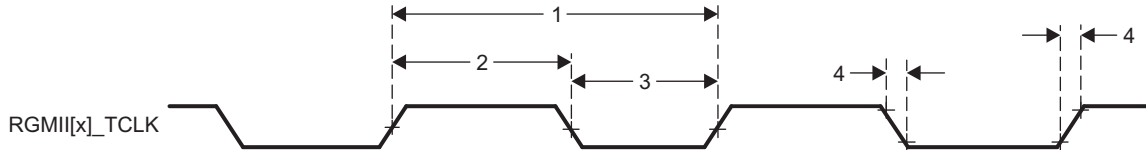
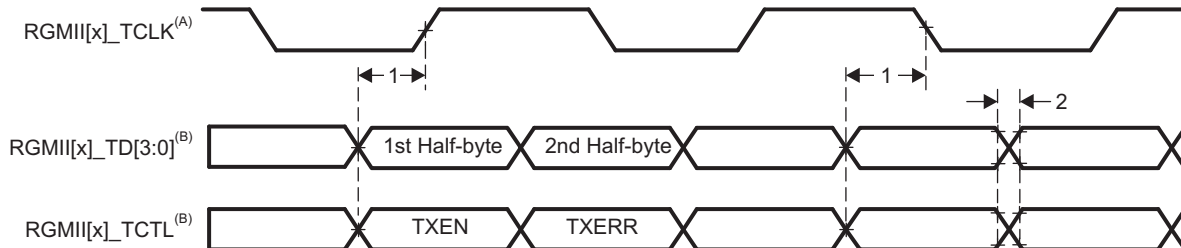


Figure 7-15. RGMII[x]_TCLK Timing - RGMII Mode

Table 7-19. Switching Characteristics for RGMII[x]_TD[3:0], and RGMII[x]_TCTL - RGMII Mode

(see Figure 7-16)

| NO. | PARAMETER | | 10 Mbps | | | 100 Mbps | | | 1000 Mbps | | | UNIT |
|-----|-----------------------|---------------------------|---------|-----|------|----------|-----|------|-----------|-----|------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{sk(TD-TXC)}$ | TD to TXC output skew | -0.5 | | 0.5 | -0.5 | | 0.5 | -0.5 | | 0.5 | ns |
| | $t_{sk(TX_CTL-TXC)}$ | TX_CTL to TXC output skew | -0.5 | | 0.5 | -0.5 | | 0.5 | -0.5 | | 0.5 | |
| 2 | $t_t(TD)$ | Transition time, TD | | | 0.75 | | | 0.75 | | | 0.75 | ns |
| | $t_t(TX_CTL)$ | Transition time, TX_CTL | | | 0.75 | | | 0.75 | | | 0.75 | |



- A. The EMAC and switch implemented in the AM335x device supports internal delay mode, but timing closure was not performed for this mode of operation. Therefore, the AM335x device does not support internal delay mode.
- B. Data and control information is transmitted using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TCLK and data bits 7-4 on the falling edge of RGMII[x]_TCLK. Similarly, RGMII[x]_TCTL carries TXEN on rising edge of RGMII[x]_TCLK and TXERR of falling edge of RGMII[x]_TCLK.

Figure 7-16. RGMII[x]_TD[3:0], RGMII[x]_TCTL Timing - RGMII Mode

7.7 External Memory Interfaces

The device includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface (EMIF)

7.7.1 General-Purpose Memory Controller (GPMC)

NOTE

For more information, see the Memory Subsystem and General-Purpose Memory Controller section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

The GPMC is the unified memory controller used to interface external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

7.7.1.1 GPMC and NOR Flash—Synchronous Mode

[Table 7-21](#) and [Table 7-22](#) assume testing over the recommended operating conditions and electrical characteristic conditions shown in [Table 7-20](#) (see [Figure 7-17](#) through [Figure 7-21](#)).

Table 7-20. GPMC and NOR Flash Timing Conditions—Synchronous Mode

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input signal rise time | 1 | | 5 | ns |
| t_F | Input signal fall time | 1 | | 5 | ns |
| Output Condition | | | | | |
| C_{LOAD} | Output load capacitance | 3 | | 30 | pF |

Table 7-21. GPMC and NOR Flash Timing Requirements—Synchronous Mode

| NO. | | | OPP100 | | OPP50 | | UNIT |
|-----|----------------------|--|--|------|-------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| F12 | $t_{su(dV-clkH)}$ | Setup time, input data gpmc_ad[15:0] valid before output clock gpmc_clk high | 3.2 | | 13.2 | | ns |
| F13 | $t_h(clkH-dV)$ | Hold time, input data gpmc_ad[15:0] valid after output clock gpmc_clk high | Industrial extended temperature (-40°C to 125°C) | 4.74 | 4.74 | ns | |
| | | | All other temperature ranges | 4.74 | 2.75 | | |
| F21 | $t_{su(waitV-clkH)}$ | Setup time, input wait gpmc_wait[x] ⁽¹⁾ valid before output clock gpmc_clk high | 3.2 | | 13.2 | | ns |
| F22 | $t_h(clkH-waitV)$ | Hold time, input wait gpmc_wait[x] ⁽¹⁾ valid after output clock gpmc_clk high | Industrial extended temperature (-40°C to 125°C) | 4.74 | 4.74 | ns | |
| | | | All other temperature ranges | 4.74 | 2.75 | | |

(1) In gpmc_wait[x], x is equal to 0 or 1.

Table 7-22. GPMC and NOR Flash Switching Characteristics—Synchronous Mode⁽²⁾

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-------------------------------|--|-------------------------|-------------------------|-------------------------|--------------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| F0 | $1 / t_{c(\text{clk})}$ | Frequency ⁽¹⁸⁾ , output clock gpmc_clk | 100 | | 50 | | MHz |
| F1 | $t_{w(\text{clkH})}$ | Typical pulse duration, output clock gpmc_clk high | 0.5P ⁽¹⁵⁾ | 0.5P ⁽¹⁵⁾ | 0.5P ⁽¹⁵⁾ | 0.5P ⁽¹⁵⁾ | ns |
| F1 | $t_{w(\text{clkL})}$ | Typical pulse duration, output clock gpmc_clk low | 0.5P ⁽¹⁵⁾ | 0.5P ⁽¹⁵⁾ | 0.5P ⁽¹⁵⁾ | 0.5P ⁽¹⁵⁾ | ns |
| | $t_{dc(\text{clk})}$ | Duty cycle error, output clock gpmc_clk | -500 | 500 | -500 | 500 | ps |
| | $t_{j(\text{clk})}$ | Jitter standard deviation ⁽¹⁹⁾ , output clock gpmc_clk | 33.33 | | 33.33 | | ps |
| | $t_{R(\text{clk})}$ | Rise time, output clock gpmc_clk | 2 | | 2 | | ns |
| | $t_{F(\text{clk})}$ | Fall time, output clock gpmc_clk | 2 | | 2 | | ns |
| | $t_{R(\text{do})}$ | Rise time, output data gpmc_ad[15:0] | 2 | | 2 | | ns |
| | $t_{F(\text{do})}$ | Fall time, output data gpmc_ad[15:0] | 2 | | 2 | | ns |
| F2 | $t_{d(\text{clkH-csnV})}$ | Delay time, output clock gpmc_clk rising edge to output chip select gpmc_csn[x] ⁽¹⁴⁾ transition | F ⁽⁶⁾ - 2.2 | F ⁽⁶⁾ + 4.5 | F ⁽⁶⁾ - 3.2 | F ⁽⁶⁾ + 9.5 | ns |
| F3 | $t_{d(\text{clkH-csnIV})}$ | Delay time, output clock gpmc_clk rising edge to output chip select gpmc_csn[x] ⁽¹⁴⁾ invalid | E ⁽⁵⁾ - 2.2 | E ⁽⁵⁾ + 4.5 | E ⁽⁵⁾ - 3.2 | E ⁽⁵⁾ + 9.5 | ns |
| F4 | $t_{d(\text{aV-clk})}$ | Delay time, output address gpmc_a[27:1] valid to output clock gpmc_clk first edge | B ⁽²⁾ - 4.5 | B ⁽²⁾ + 2.3 | B ⁽²⁾ - 5.5 | B ⁽²⁾ + 12.3 | ns |
| F5 | $t_{d(\text{clkH-aIV})}$ | Delay time, output clock gpmc_clk rising edge to output address gpmc_a[27:1] invalid | -2.3 | 4.5 | -3.3 | 14.5 | ns |
| F6 | $t_{d(\text{be[x]nV-clk})}$ | Delay time, output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n valid to output clock gpmc_clk first edge | B ⁽²⁾ - 1.9 | B ⁽²⁾ + 2.3 | B ⁽²⁾ - 2.9 | B ⁽²⁾ + 12.3 | ns |
| F7 | $t_{d(\text{clkH-be[x]nIV})}$ | Delay time, output clock gpmc_clk rising edge to output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n invalid ⁽¹¹⁾ | D ⁽⁴⁾ - 2.3 | D ⁽⁴⁾ + 1.9 | D ⁽⁴⁾ - 3.3 | D ⁽⁴⁾ + 6.9 | ns |
| F7 | $t_{d(\text{clkL-be[x]nIV})}$ | Delay time, gpmc_clk falling edge to gpmc_nbe0_cle, gpmc_nbe1 invalid ⁽¹²⁾ | D ⁽⁴⁾ - 2.3 | D ⁽⁴⁾ + 1.9 | D ⁽⁴⁾ - 3.3 | D ⁽⁴⁾ + 6.9 | ns |
| F7 | $t_{d(\text{clkL-be[x]nIV})}$ | Delay time, gpmc_clk falling edge to gpmc_nbe0_cle, gpmc_nbe1 invalid ⁽¹³⁾ | D ⁽⁴⁾ - 2.3 | D ⁽⁴⁾ + 1.9 | D ⁽⁴⁾ - 3.3 | D ⁽⁴⁾ + 11.9 | ns |
| F8 | $t_{d(\text{clkH-advn})}$ | Delay time, output clock gpmc_clk rising edge to output address valid and address latch enable gpmc_advn_ale transition | G ⁽⁷⁾ - 2.3 | G ⁽⁷⁾ + 4.5 | G ⁽⁷⁾ - 3.3 | G ⁽⁷⁾ + 9.5 | ns |
| F9 | $t_{d(\text{clkH-advnIV})}$ | Delay time, output clock gpmc_clk rising edge to output address valid and address latch enable gpmc_advn_ale invalid | D ⁽⁴⁾ - 2.3 | D ⁽⁴⁾ + 3.5 | D ⁽⁴⁾ - 3.3 | D ⁽⁴⁾ + 9.5 | ns |
| F10 | $t_{d(\text{clkH-oen})}$ | Delay time, output clock gpmc_clk rising edge to output enable gpmc_oen transition | H ⁽⁸⁾ - 2.3 | H ⁽⁸⁾ + 3.5 | H ⁽⁸⁾ - 3.3 | H ⁽⁸⁾ + 8.5 | ns |
| F11 | $t_{d(\text{clkH-oenIV})}$ | Delay time, output clock gpmc_clk rising edge to output enable gpmc_oen invalid | E ⁽⁸⁾ - 2.3 | E ⁽⁸⁾ + 3.5 | E ⁽⁸⁾ - 3.3 | E ⁽⁸⁾ + 8.5 | ns |
| F14 | $t_{d(\text{clkH-wen})}$ | Delay time, output clock gpmc_clk rising edge to output write enable gpmc_wen transition | I ⁽⁹⁾ - 2.3 | I ⁽⁹⁾ + 4.5 | I ⁽⁹⁾ - 3.3 | I ⁽⁹⁾ + 9.5 | ns |
| F15 | $t_{d(\text{clkH-do})}$ | Delay time, output clock gpmc_clk rising edge to output data gpmc_ad[15:0] transition ⁽¹¹⁾ | J ⁽¹⁰⁾ - 2.3 | J ⁽¹⁰⁾ + 1.9 | J ⁽¹⁰⁾ - 3.3 | J ⁽¹⁰⁾ + 6.9 | ns |
| F15 | $t_{d(\text{clkL-do})}$ | Delay time, gpmc_clk falling edge to gpmc_ad[15:0] data bus transition ⁽¹²⁾ | J ⁽¹⁰⁾ - 2.3 | J ⁽¹⁰⁾ + 1.9 | J ⁽¹⁰⁾ - 3.3 | J ⁽¹⁰⁾ + 6.9 | ns |
| F15 | $t_{d(\text{clkL-do})}$ | Delay time, gpmc_clk falling edge to gpmc_ad[15:0] data bus transition ⁽¹³⁾ | J ⁽¹⁰⁾ - 2.3 | J ⁽¹⁰⁾ + 1.9 | J ⁽¹⁰⁾ - 3.3 | J ⁽¹⁰⁾ + 11.9 | ns |
| F17 | $t_{d(\text{clkH-be[x]n})}$ | Delay time, output clock gpmc_clk rising edge to output lower byte enable and command latch enable gpmc_be0n_cle transition ⁽¹¹⁾ | J ⁽¹⁰⁾ - 2.3 | J ⁽¹⁰⁾ + 1.9 | J ⁽¹⁰⁾ - 3.3 | J ⁽¹⁰⁾ + 6.9 | ns |
| F17 | $t_{d(\text{clkL-be[x]n})}$ | Delay time, gpmc_clk falling edge to gpmc_nbe0_cle, gpmc_nbe1 transition ⁽¹²⁾ | J ⁽¹⁰⁾ - 2.3 | J ⁽¹⁰⁾ + 1.9 | J ⁽¹⁰⁾ - 3.3 | J ⁽¹⁰⁾ + 6.9 | ns |
| F17 | $t_{d(\text{clkL-be[x]n})}$ | Delay time, gpmc_clk falling edge to gpmc_nbe0_cle, gpmc_nbe1 transition ⁽¹³⁾ | J ⁽¹⁰⁾ - 2.3 | J ⁽¹⁰⁾ + 1.9 | J ⁽¹⁰⁾ - 3.3 | J ⁽¹⁰⁾ + 11.9 | ns |

Table 7-22. GPMC and NOR Flash Switching Characteristics—Synchronous Mode⁽²⁾ (continued)

| NO. | PARAMETER | | | OPP100 | | OPP50 | | UNIT |
|-----|------------------|---|-------|-------------------|-----|-------------------|-----|------|
| | | | | MIN | MAX | MIN | MAX | |
| F18 | $t_{w(csnV)}$ | Pulse duration, output chip select gpmc_csn[x] ⁽¹⁴⁾ low | Read | A ⁽¹⁾ | | A ⁽¹⁾ | | ns |
| | | | Write | A ⁽¹⁾ | | A ⁽¹⁾ | | ns |
| F19 | $t_{w(be[x]nV)}$ | Pulse duration, output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n low | Read | C ⁽³⁾ | | C ⁽³⁾ | | ns |
| | | | Write | C ⁽³⁾ | | C ⁽³⁾ | | ns |
| F20 | $t_{w(advnV)}$ | Pulse duration, output address valid and address latch enable gpmc_advn_ale low | Read | K ⁽¹⁶⁾ | | K ⁽¹⁶⁾ | | ns |
| | | | Write | K ⁽¹⁶⁾ | | K ⁽¹⁶⁾ | | ns |

(1) For single read: $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 For burst read: $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 For burst write: $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 With n being the page burst access number.

(2) $B = ClkActivationTime \times GPMC_FCLK^{(17)}$

(3) For single read: $C = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 For burst read: $C = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 For burst write: $C = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 With n being the page burst access number.

(4) For single read: $D = (RdCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 For burst read: $D = (RdCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 For burst write: $D = (WrCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$

(5) For single read: $E = (CSRdOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 For burst read: $E = (CSRdOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
 For burst write: $E = (CSWrOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$

(6) For csn falling edge (CS activated):

- Case GpmcFCLKDivider = 0:
 - $F = 0.5 \times CSExtraDelay \times GPMC_FCLK^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $F = 0.5 \times CSExtraDelay \times GPMC_FCLK^{(17)}$ if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
 - $F = (1 + 0.5 \times CSExtraDelay) \times GPMC_FCLK^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $F = 0.5 \times CSExtraDelay \times GPMC_FCLK^{(17)}$ if ((CSOnTime - ClkActivationTime) is a multiple of 3)
 - $F = (1 + 0.5 \times CSExtraDelay) \times GPMC_FCLK^{(17)}$ if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
 - $F = (2 + 0.5 \times CSExtraDelay) \times GPMC_FCLK^{(17)}$ if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):

- Case GpmcFCLKDivider = 0:
 - $G = 0.5 \times ADVExtraDelay \times GPMC_FCLK^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $G = 0.5 \times ADVExtraDelay \times GPMC_FCLK^{(17)}$ if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
 - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC_FCLK^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $G = 0.5 \times ADVExtraDelay \times GPMC_FCLK^{(17)}$ if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
 - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC_FCLK^{(17)}$ if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
 - $G = (2 + 0.5 \times ADVExtraDelay) \times GPMC_FCLK^{(17)}$ if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

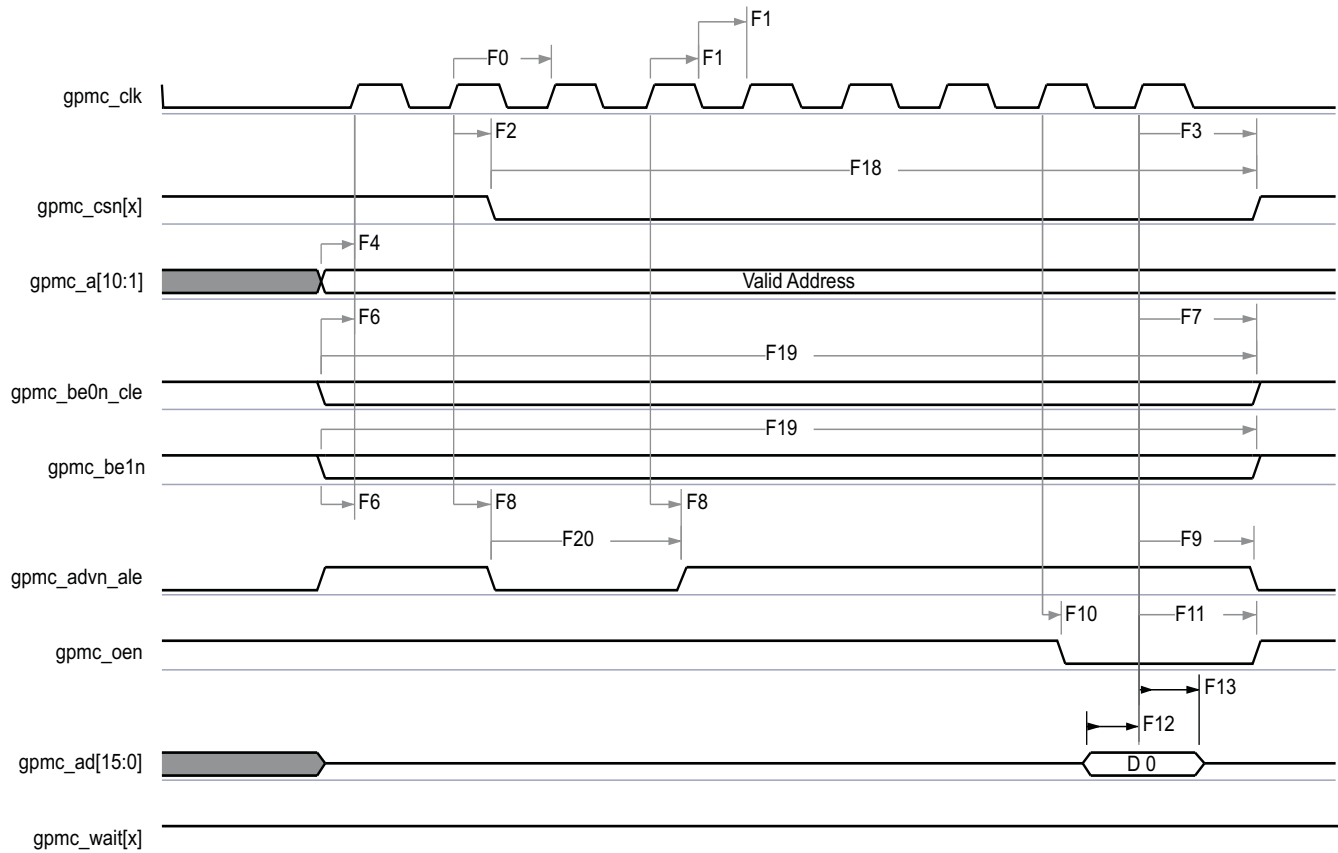
For ADV rising edge (ADV deactivated) in Reading mode:

- Case GpmcFCLKDivider = 0:
 - $G = 0.5 \times ADVExtraDelay \times GPMC_FCLK^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $G = 0.5 \times ADVExtraDelay \times GPMC_FCLK^{(17)}$ if (ClkActivationTime and ADVrOffTime are odd) or (ClkActivationTime and ADVrOffTime are even)
 - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC_FCLK^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $G = 0.5 \times ADVExtraDelay \times GPMC_FCLK^{(17)}$ if ((ADVrOffTime - ClkActivationTime) is a multiple of 3)
 - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC_FCLK^{(17)}$ if ((ADVrOffTime - ClkActivationTime - 1) is a multiple of 3)
 - $G = (2 + 0.5 \times ADVExtraDelay) \times GPMC_FCLK^{(17)}$ if ((ADVrOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

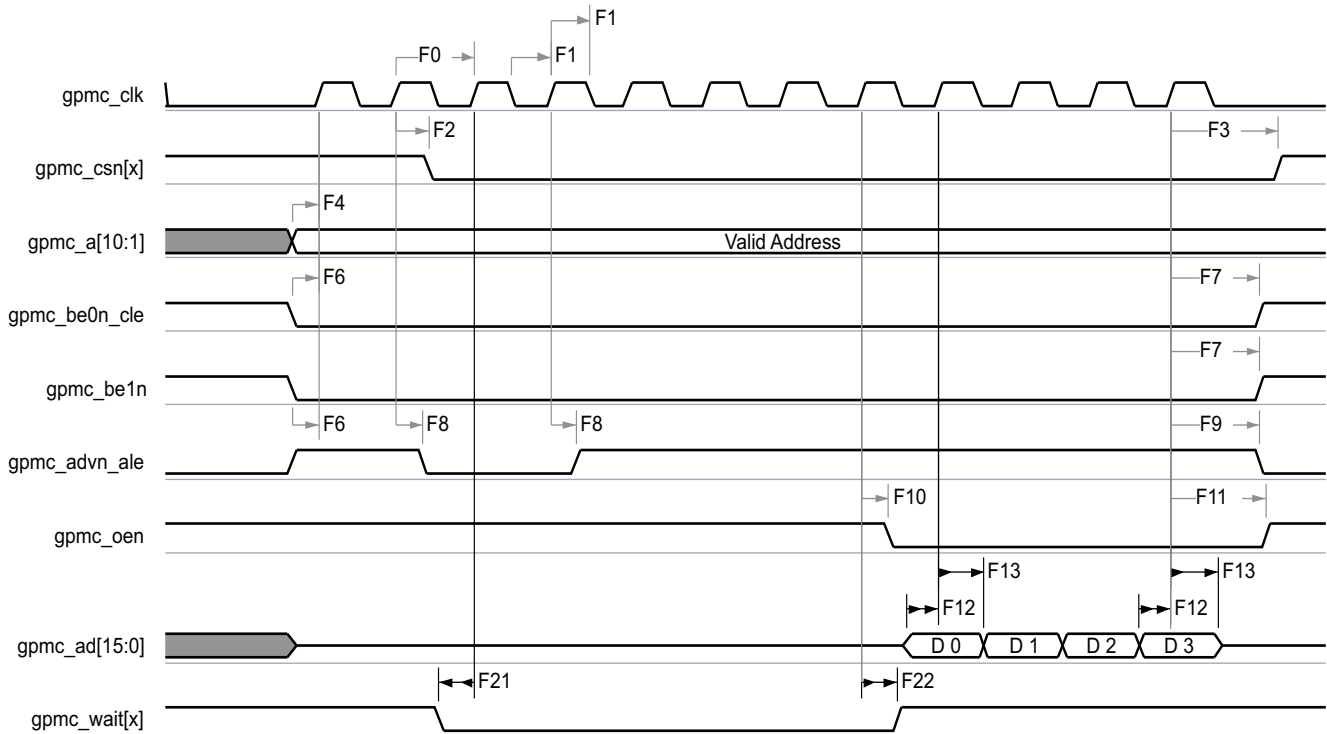
- Case GpmcFCLKDivider = 0:
 - $G = 0.5 \times ADVExtraDelay \times GPMC_FCLK^{(17)}$
- Case GpmcFCLKDivider = 1:

- $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
 - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
 - Case GpmcFCLKDivider = 2:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
 - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
 - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)
- (8) For OE falling edge (OE activated) and I/O DIR rising edge (Data Bus input direction):
- Case GpmcFCLKDivider = 0:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
 - Case GpmcFCLKDivider = 1:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
 - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
 - Case GpmcFCLKDivider = 2:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((OEOnTime – ClkActivationTime) is a multiple of 3)
 - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
 - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)
- For OE rising edge (OE deactivated):
- Case GpmcFCLKDivider = 0:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
 - Case GpmcFCLKDivider = 1:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
 - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
 - Case GpmcFCLKDivider = 2:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((OEOffTime – ClkActivationTime) is a multiple of 3)
 - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
 - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)
- (9) For WE falling edge (WE activated):
- Case GpmcFCLKDivider = 0:
 - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
 - Case GpmcFCLKDivider = 1:
 - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
 - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
 - Case GpmcFCLKDivider = 2:
 - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((WEOnTime – ClkActivationTime) is a multiple of 3)
 - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
 - $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)
- For WE rising edge (WE deactivated):
- Case GpmcFCLKDivider = 0:
 - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
 - Case GpmcFCLKDivider = 1:
 - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
 - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
 - Case GpmcFCLKDivider = 2:
 - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((WEOffTime – ClkActivationTime) is a multiple of 3)
 - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
 - $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)
- (10) $J = \text{GPMC_FCLK}^{(17)}$
- (11) First transfer only for CLK DIV 1 mode.
- (12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
- (13) Half cycle of GPMC_CLK_OUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLK_OUT divide down from GPMC_FCLK.
- (14) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
- (15) P = gpmc_clk period in ns
- (16) For read: $K = (\text{ADVRdOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For write: $K = (\text{ADVWrOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
- (17) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
- (18) Related to the gpmc_clk output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_CSx configuration register bit field GpmcFCLKDivider.
- (19) The jitter probability density can be approximated by a Gaussian function.



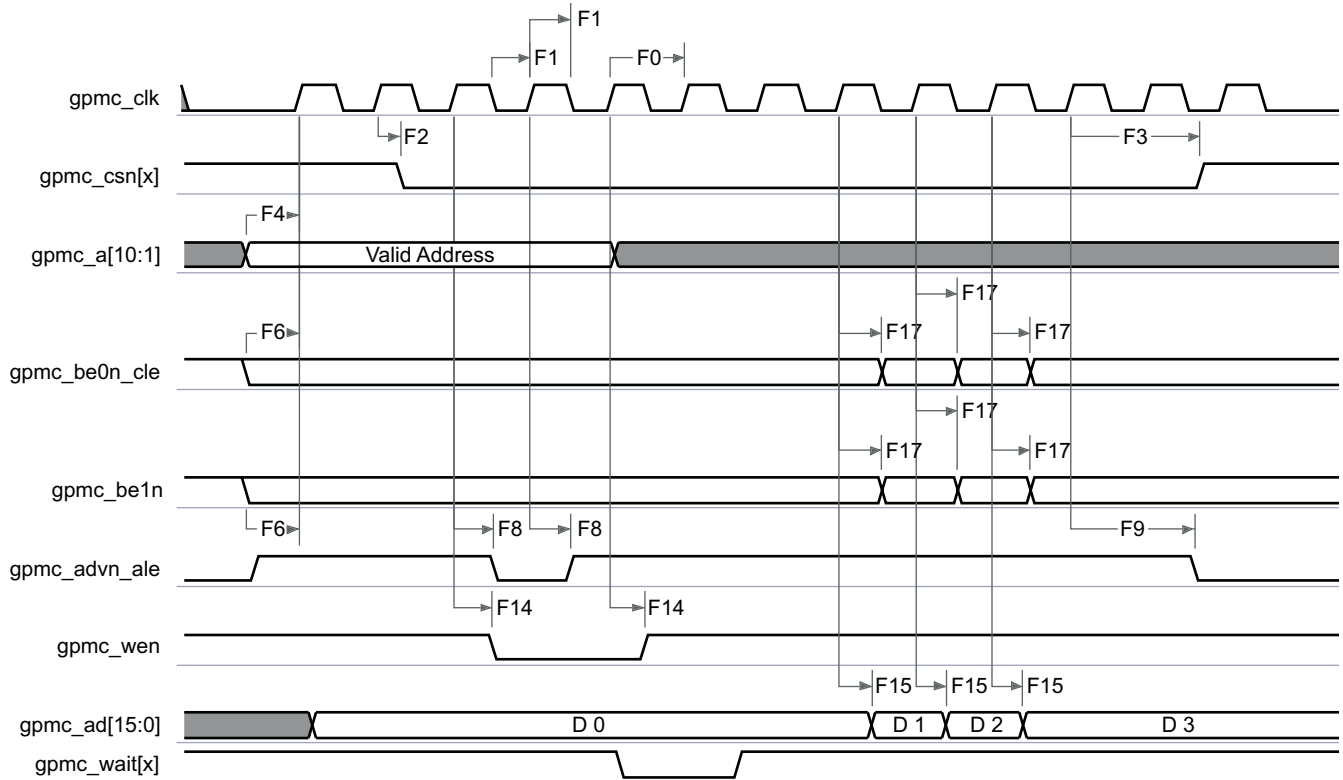
- A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
- B. In gpmc_wait[x], x is equal to 0 or 1.

Figure 7-17. GPMC and NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0)



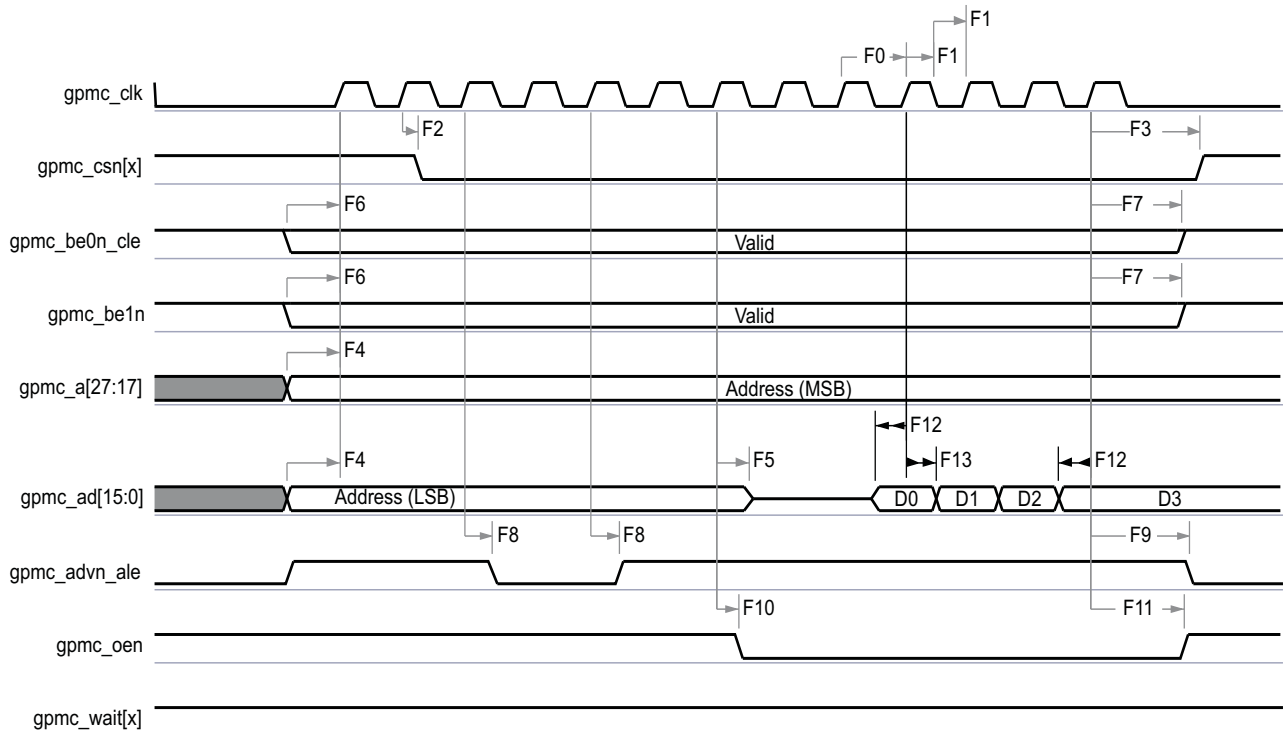
- A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
- B. In gpmc_wait[x], x is equal to 0 or 1.

Figure 7-18. GPMC and NOR Flash—Synchronous Burst Read—4x16-Bit (GpmcFCLKDivider = 0)



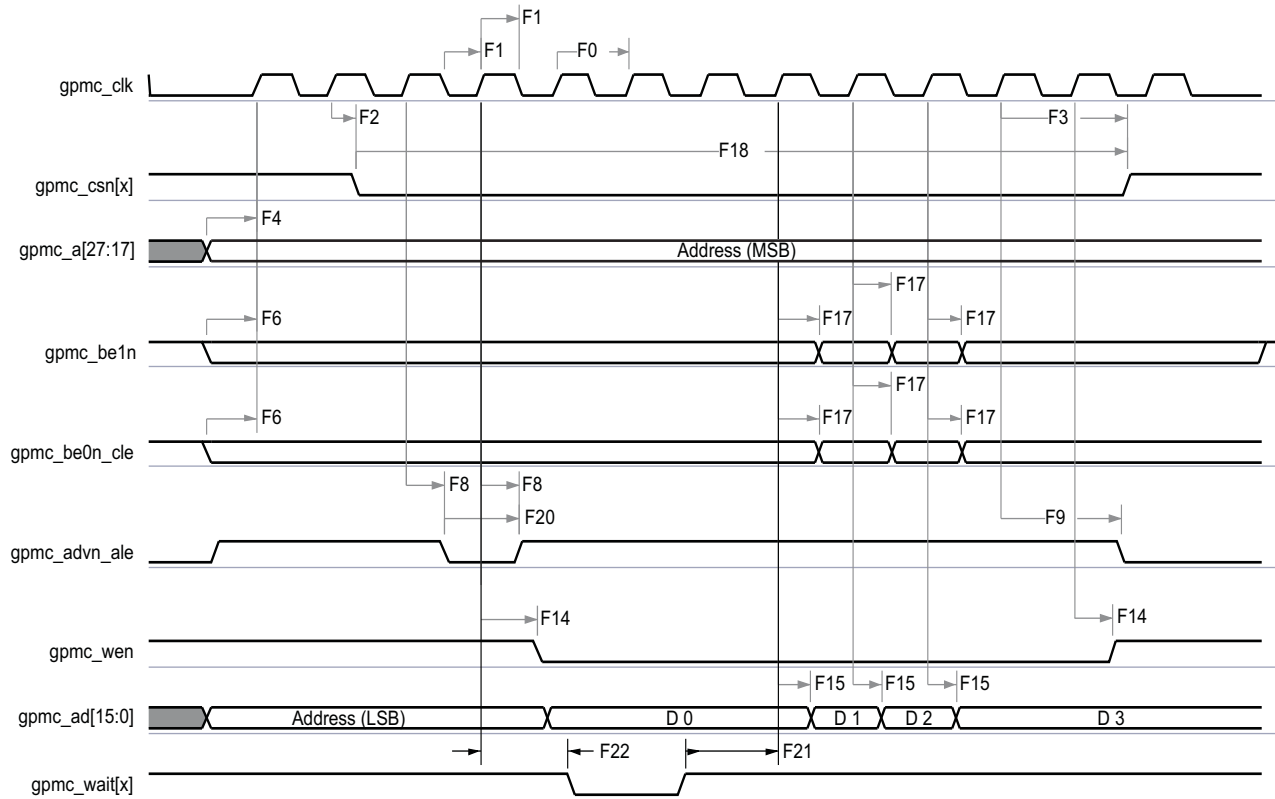
- A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
- B. In gpmc_wait[x], x is equal to 0 or 1.

Figure 7-19. GPMC and NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0)



- A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
- B. In gpmc_wait[x], x is equal to 0 or 1.

Figure 7-20. GPMC and Multiplexed NOR Flash—Synchronous Burst Read



- A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
- B. In gpmc_wait[x], x is equal to 0 or 1.

Figure 7-21. GPMC and Multiplexed NOR Flash—Synchronous Burst Write

7.7.1.2 GPMC and NOR Flash—Asynchronous Mode

Table 7-24 and Table 7-25 assume testing over the recommended operating conditions and electrical characteristic conditions shown in Table 7-23 (see Figure 7-22 through Figure 7-27).

Table 7-23. GPMC and NOR Flash Timing Conditions—Asynchronous Mode

| | | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input signal rise time | 1 | | 5 | ns |
| t_F | Input signal fall time | 1 | | 5 | ns |
| Output Condition | | | | | |
| C_{LOAD} | Output load capacitance | 3 | | 30 | pF |

Table 7-24. GPMC and NOR Flash Internal Timing Requirements—Asynchronous Mode⁽¹⁾⁽²⁾

| NO. | | OPP100 | | OPP50 | | UNIT |
|-----|--|--------|-----|-------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| F11 | Delay time, output data gpmc_ad[15:0] generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| F12 | Delay time, input data gpmc_ad[15:0] capture from internal functional clock GPMC_FCLK ⁽³⁾ | | 4 | | 4 | ns |
| F13 | Delay time, output chip select gpmc_csn[x] generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| F14 | Delay time, output address gpmc_a[27:1] generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| F15 | Delay time, output address gpmc_a[27:1] valid from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| F16 | Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| F17 | Delay time, output enable gpmc_oen generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| F18 | Delay time, output write enable gpmc_wen generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| F19 | Skew, internal functional clock GPMC_FCLK ⁽³⁾ | | 100 | | 100 | ps |

(1) The internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.

(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

(3) GPMC_FCLK is general-purpose memory controller internal functional clock.

Table 7-25. GPMC and NOR Flash Timing Requirements—Asynchronous Mode

| NO. | | | OPP100 | | OPP50 | | UNIT |
|---------------------|-----------------------------|---------------------------------------|--------|------------------|-------|------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| FA5 ⁽¹⁾ | t _{acc(d)} | Data access time | | H ⁽⁵⁾ | | H ⁽⁵⁾ | ns |
| FA20 ⁽²⁾ | t _{acc1-pgmode(d)} | Page mode successive data access time | | P ⁽⁴⁾ | | P ⁽⁴⁾ | ns |
| FA21 ⁽³⁾ | t _{acc2-pgmode(d)} | Page mode first data access time | | H ⁽⁵⁾ | | H ⁽⁵⁾ | ns |

- (1) The FA5 parameter shows the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2) The FA20 parameter shows amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
- (3) The FA21 parameter shows amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
- (4) $P = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(6)}$
- (5) $H = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(6)}$
- (6) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

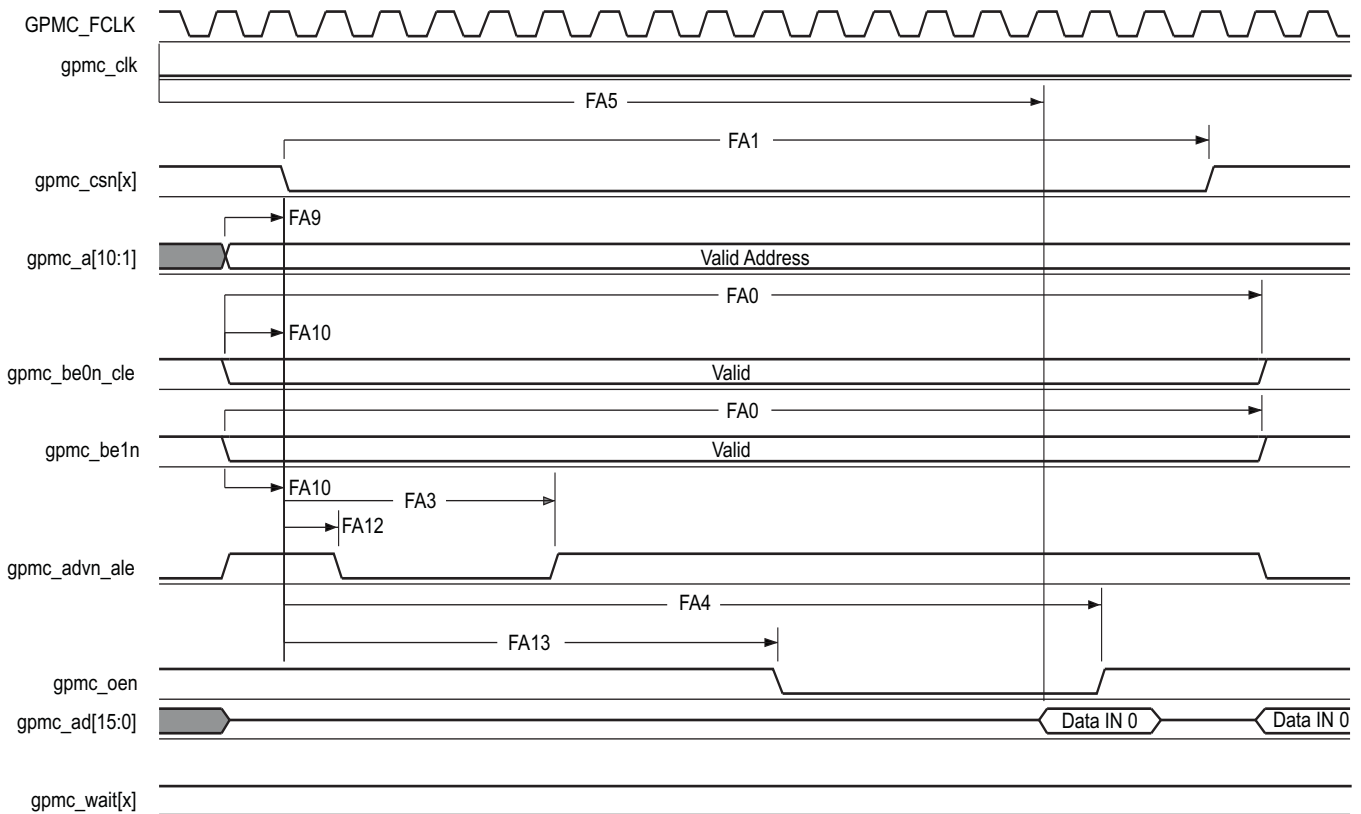
Table 7-26. GPMC and NOR Flash Switching Characteristics—Asynchronous Mode

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT | |
|------|------------------------------|---|--------|-------------------------|-------------------------|-----------------------|-----------------------|----|
| | | | MIN | MAX | MIN | MAX | | |
| | t _{R(d)} | Rise time, output data gpmc_ad[15:0] | | 2 | | 2 | ns | |
| | t _{F(d)} | Fall time, output data gpmc_ad[15:0] | | 2 | | 2 | ns | |
| FA0 | t _{w(be[x]nV)} | Pulse duration, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n valid time | Read | | N ⁽¹²⁾ | | N ⁽¹²⁾ | ns |
| | | | Write | | N ⁽¹²⁾ | | N ⁽¹²⁾ | |
| FA1 | t _{w(csnV)} | Pulse duration, output chip select gpmc_csn[x] ⁽¹³⁾ low | Read | | A ⁽¹⁾ | | A ⁽¹⁾ | ns |
| | | | Write | | A ⁽¹⁾ | | A ⁽¹⁾ | |
| FA3 | t _{d(csnV-advnIV)} | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output address valid and address latch enable gpmc_advn_ale invalid | Read | B ⁽²⁾ – 0.2 | B ⁽²⁾ + 2.0 | B ⁽²⁾ – 5 | B ⁽²⁾ + 5 | ns |
| | | | Write | B ⁽²⁾ – 0.2 | B ⁽²⁾ + 2.0 | B ⁽²⁾ – 5 | B ⁽²⁾ + 5 | |
| FA4 | t _{d(csnV-oenIV)} | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output enable gpmc_oen invalid (Single read) | | C ⁽³⁾ – 0.2 | C ⁽³⁾ + 2.0 | C ⁽³⁾ – 5 | C ⁽³⁾ + 5 | ns |
| FA9 | t _{d(aV-csnV)} | Delay time, output address gpmc_a[27:1] valid to output chip select gpmc_csn[x] ⁽¹³⁾ valid | | J ⁽⁹⁾ – 0.2 | J ⁽⁹⁾ + 2.0 | J ⁽⁹⁾ – 5 | J ⁽⁹⁾ + 5 | ns |
| FA10 | t _{d(be[x]nV-csnV)} | Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n valid to output chip select gpmc_csn[x] ⁽¹³⁾ valid | | J ⁽⁹⁾ – 0.2 | J ⁽⁹⁾ + 2.0 | J ⁽⁹⁾ – 5 | J ⁽⁹⁾ + 5 | ns |
| FA12 | t _{d(csnV-advnV)} | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output address valid and address latch enable gpmc_advn_ale valid | | K ⁽¹⁰⁾ – 0.2 | K ⁽¹⁰⁾ + 2.0 | K ⁽¹⁰⁾ – 5 | K ⁽¹⁰⁾ + 5 | ns |
| FA13 | t _{d(csnV-oenV)} | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output enable gpmc_oen valid | | L ⁽¹¹⁾ – 0.2 | L ⁽¹¹⁾ + 2.0 | L ⁽¹¹⁾ – 5 | L ⁽¹¹⁾ + 5 | ns |
| FA16 | t _{w(aIV)} | Pulse durationm output address gpmc_a[26:1] invalid between 2 successive read and write accesses | | G ⁽⁷⁾ | | G ⁽⁷⁾ | | ns |
| FA18 | t _{d(csnV-oenIV)} | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output enable gpmc_oen invalid (Burst read) | | I ⁽⁸⁾ – 0.2 | I ⁽⁸⁾ + 2.0 | I ⁽⁸⁾ – 5 | I ⁽⁸⁾ + 5 | ns |
| FA20 | t _{w(aV)} | Pulse duration, output address gpmc_a[27:1] valid - 2nd, 3rd, and 4th accesses | | D ⁽⁴⁾ | | D ⁽⁴⁾ | | ns |
| FA25 | t _{d(csnV-wenV)} | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output write enable gpmc_wen valid | | E ⁽⁵⁾ – 0.2 | E ⁽⁵⁾ + 2.0 | E ⁽⁵⁾ – 5 | E ⁽⁵⁾ + 5 | ns |

Table 7-26. GPMC and NOR Flash Switching Characteristics—Asynchronous Mode (continued)

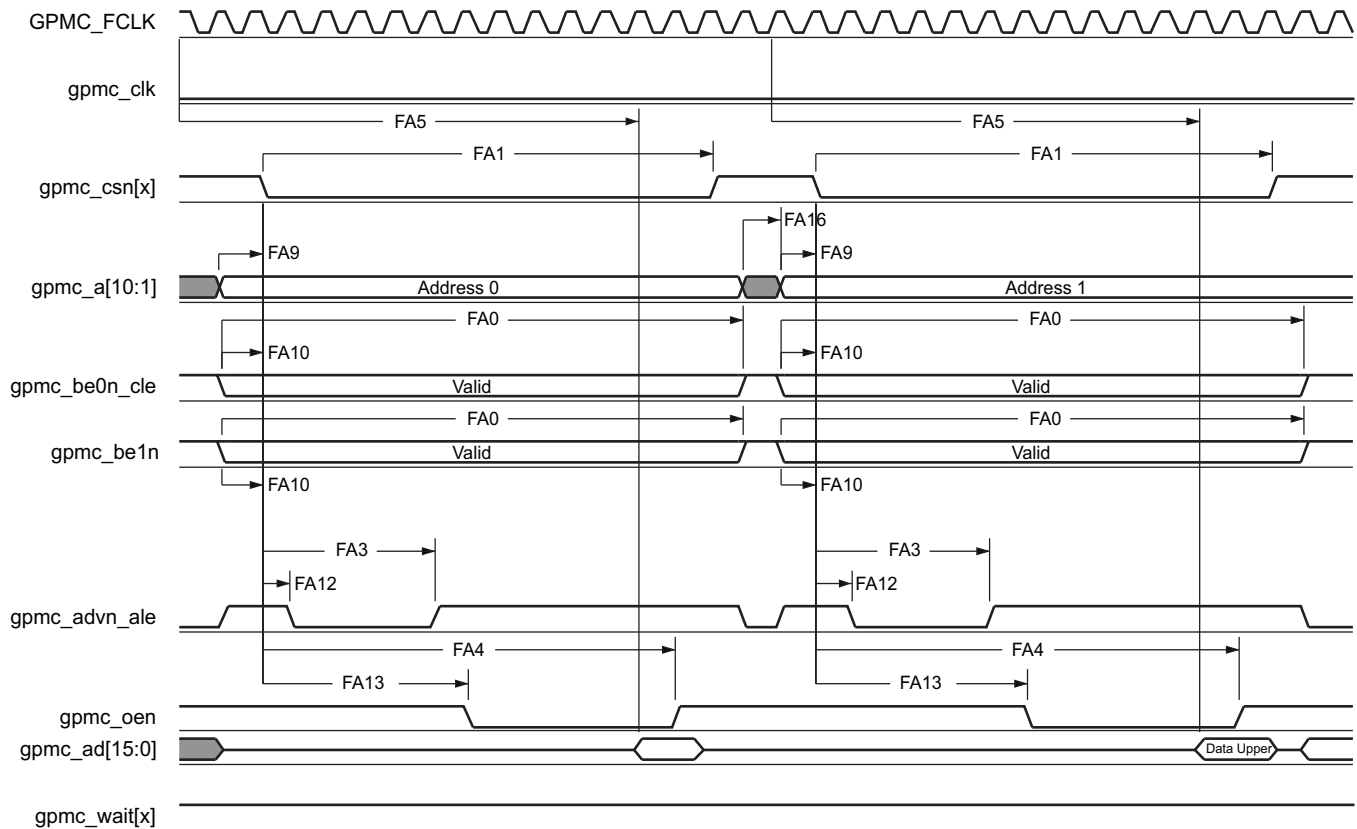
| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|------|--------------------|--|------------------------|------------------------|----------------------|----------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| FA27 | $t_{d(csnV-wenV)}$ | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output write enable gpmc_wen invalid | F ⁽⁶⁾ – 0.2 | F ⁽⁶⁾ + 2.0 | F ⁽⁶⁾ – 5 | F ⁽⁶⁾ + 5 | ns |
| FA28 | $t_{d(wenV-dV)}$ | Delay time, output write enable gpmc_wen valid to output data gpmc_ad[15:0] valid | | 2.0 | | 5 | ns |
| FA29 | $t_{d(dV-csnV)}$ | Delay time, output data gpmc_ad[15:0] valid to output chip select gpmc_csn[x] ⁽¹³⁾ valid | J ⁽⁹⁾ – 0.2 | J ⁽⁹⁾ + 2.0 | J ⁽⁹⁾ – 5 | J ⁽⁹⁾ + 5 | ns |
| FA37 | $t_{d(oenV-alV)}$ | Delay time, output enable gpmc_oen valid to output address gpmc_ad[15:0] phase end | | 2.0 | | 5 | ns |

- (1) For single read: $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
For single write: $A = (CSWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
For burst read: $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
For burst write: $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
with n being the page burst access number
- (2) For reading: $B = ((ADVrdOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
For writing: $B = ((ADVwrOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (3) $C = ((OEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (4) $D = PageBurstAccessTime \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
- (5) $E = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (6) $F = ((WEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (7) $G = Cycle2CycleDelay \times GPMC_FCLK^{(14)}$
- (8) $I = ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (9) $J = (CSOnTime \times (TimeParaGranularity + 1) + 0.5 \times CSEExtraDelay) \times GPMC_FCLK^{(14)}$
- (10) $K = ((ADVOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (11) $L = ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (12) For single read: $N = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
For single write: $N = WrCycleTime \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
For burst read: $N = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
For burst write: $N = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
- (13) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.
- (14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.



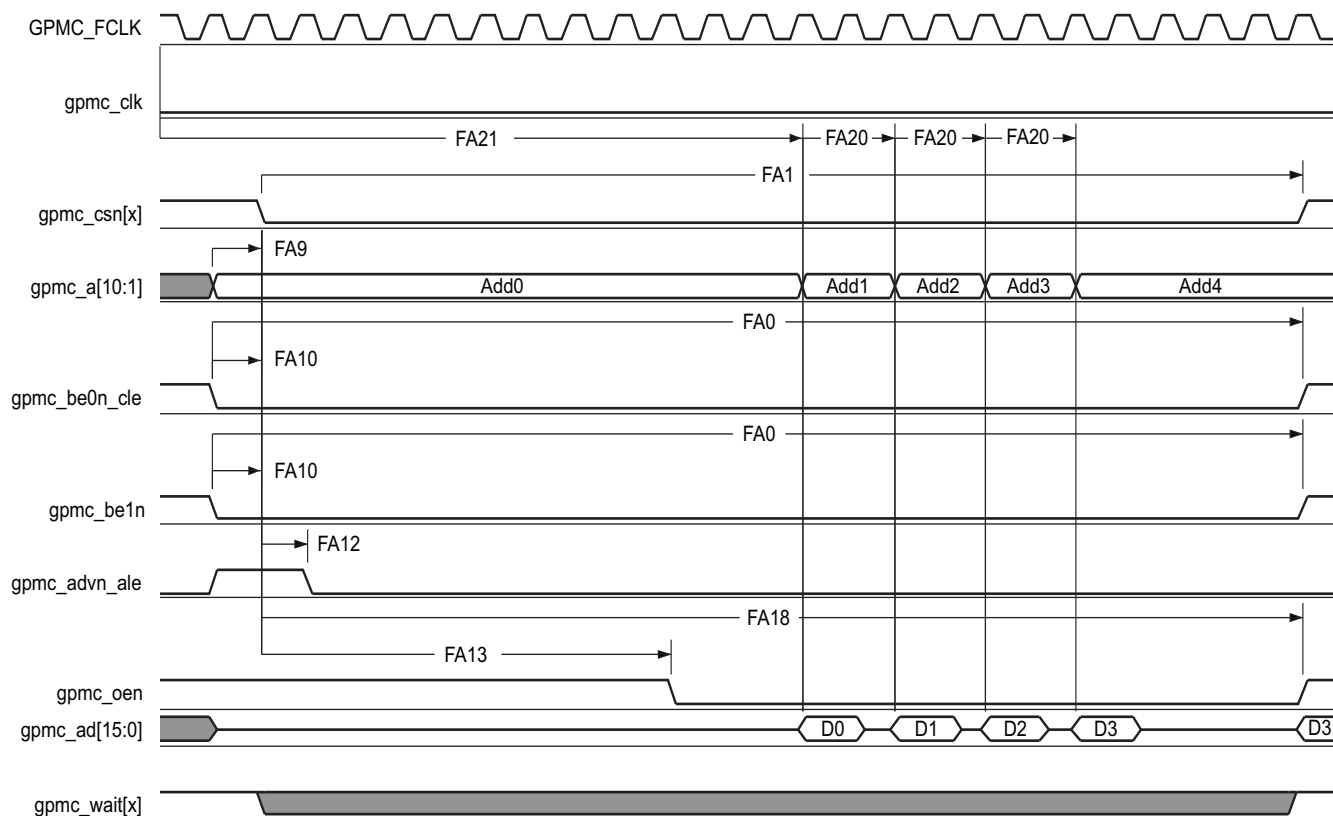
- A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 7-22. GPMC and NOR Flash—Asynchronous Read—Single Word



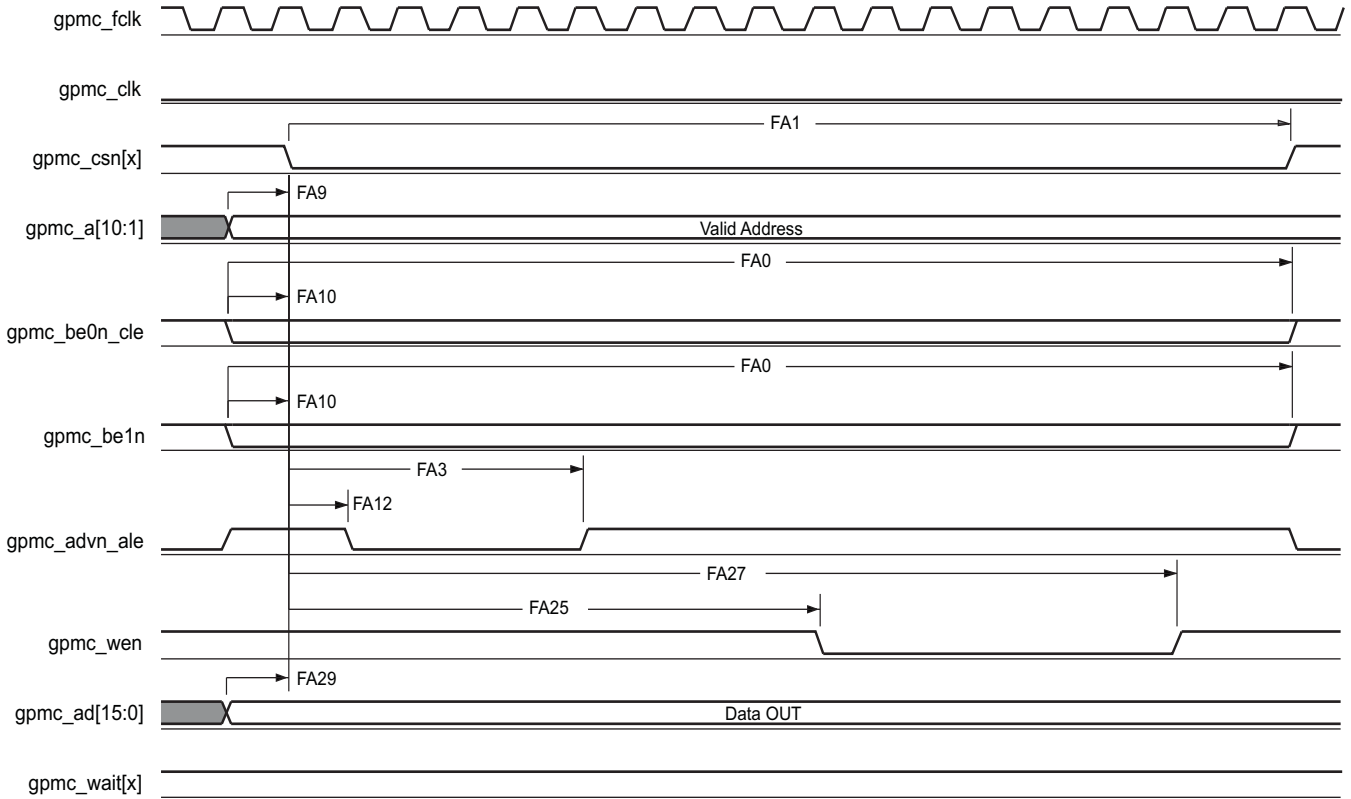
- A. In `gpmc_csn[x]`, `x` is equal to 0, 1, 2, 3, 4, or 5. In `gpmc_wait[x]`, `x` is equal to 0 or 1.
- B. `FA5` parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after `FA5` functional clock cycles, input data will be internally sampled by active functional clock edge. `FA5` value must be stored inside `AccessTime` register bits field.
- C. `GPMC_FCLK` is an internal clock (GPMC functional clock) not provided externally.

Figure 7-23. GPMC and NOR Flash—Asynchronous Read—32-Bit



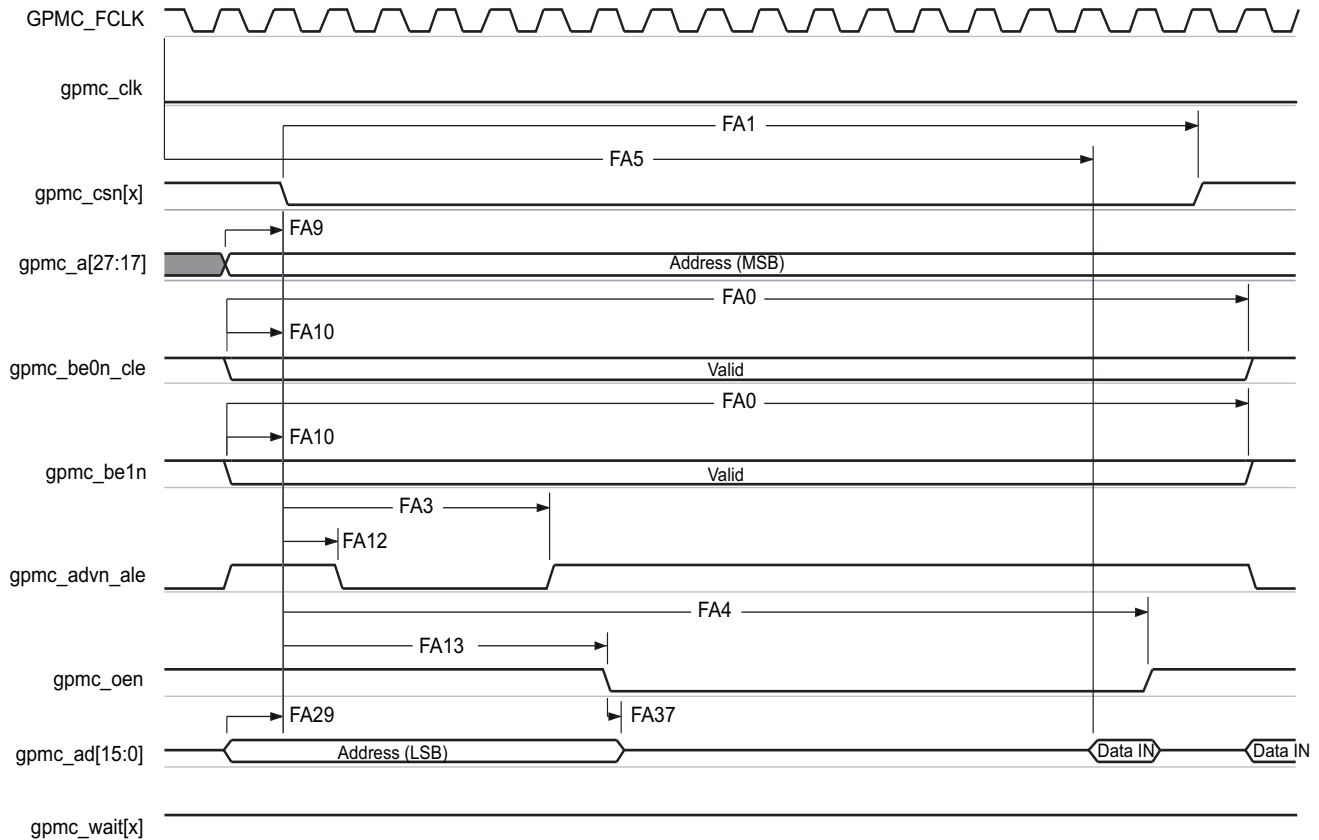
- A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
- B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 7-24. GPMC and NOR Flash—Asynchronous Read—Page Mode 4x16-Bit



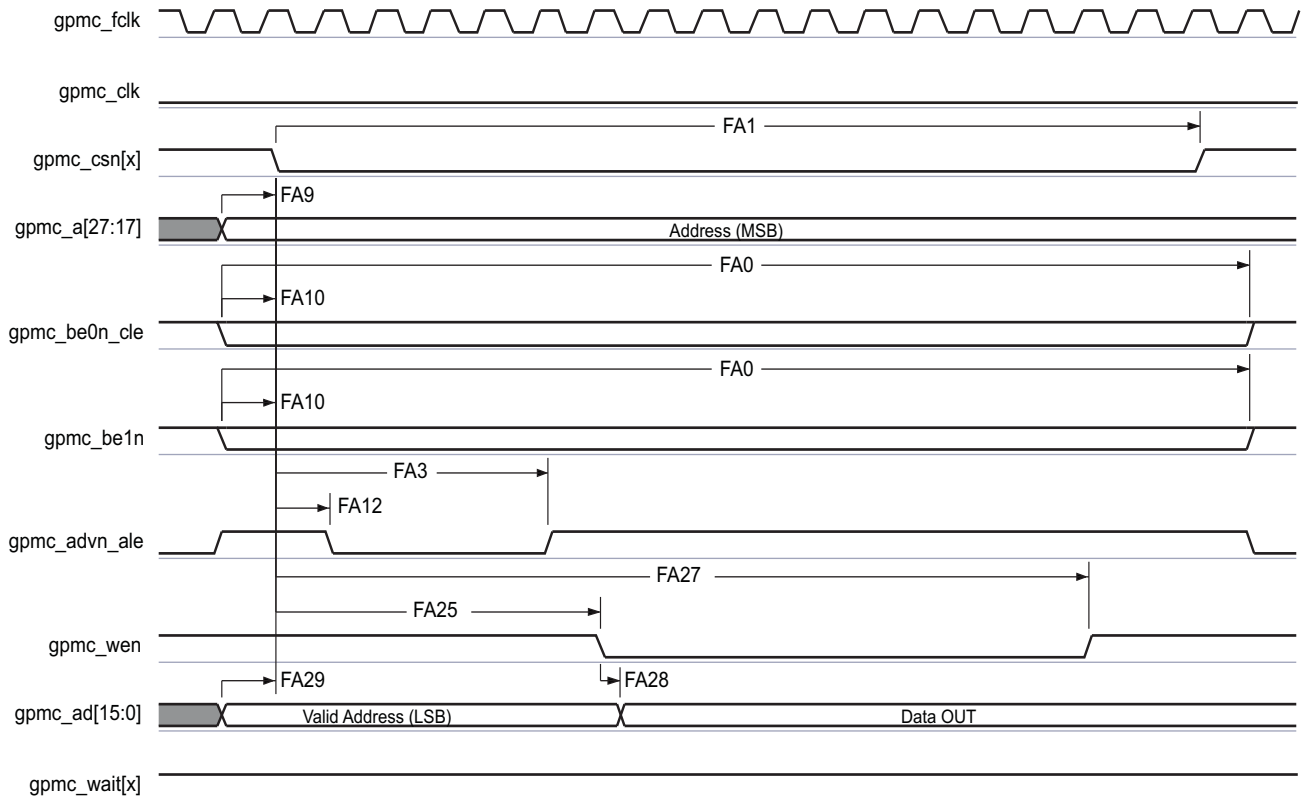
A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.

Figure 7-25. GPMC and NOR Flash—Asynchronous Write—Single Word



- A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 7-26. GPMC and Multiplexed NOR Flash—Asynchronous Read—Single Word



A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.

Figure 7-27. GPMC and Multiplexed NOR Flash—Asynchronous Write—Single Word

7.7.1.3 GPMC and NAND Flash—Asynchronous Mode

Table 7-28 and Table 7-29 assume testing over the recommended operating conditions and electrical characteristic conditions shown in Table 7-27 (see Figure 7-28 through Figure 7-31).

Table 7-27. GPMC and NAND Flash Timing Conditions—Asynchronous Mode

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input signal rise time | 1 | | 5 | ns |
| t_F | Input signal fall time | 1 | | 5 | ns |
| Output Condition | | | | | |
| C_{LOAD} | Output load capacitance | 3 | | 30 | pF |

Table 7-28. GPMC and NAND Flash Internal Timing Requirements—Asynchronous Mode⁽¹⁾⁽²⁾

| NO. | | OPP100 | | OPP50 | | UNIT |
|-------|--|--------|-----|-------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| GNFI1 | Delay time, output data gpmc_ad[15:0] generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| GNFI2 | Delay time, input data gpmc_ad[15:0] capture from internal functional clock GPMC_FCLK ⁽³⁾ | | 4.0 | | 4.0 | ns |
| GNFI3 | Delay time, output chip select gpmc_csn[x] generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| GNFI4 | Delay time, output address valid and address latch enable gpmc_advn_ale generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| GNFI5 | Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| GNFI6 | Delay time, output enable gpmc_oen generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| GNFI7 | Delay time, output write enable gpmc_wen generation from internal functional clock GPMC_FCLK ⁽³⁾ | | 6.5 | | 6.5 | ns |
| GNFI8 | Skew, functional clock GPMC_FCLK ⁽³⁾ | | 100 | | 100 | ps |

- (1) Internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.
- (2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.
- (3) GPMC_FCLK is general-purpose memory controller internal functional clock.

Table 7-29. GPMC and NAND Flash Timing Requirements—Asynchronous Mode

| NO. | | OPP100 | | OPP50 | | UNIT |
|----------------------|--|--------|------------------|-------|------------------|------|
| | | MIN | MAX | MIN | MAX | |
| GNF12 ⁽¹⁾ | $t_{acc(d)}$ Access time, input data gpmc_ad[15:0] | | J ⁽²⁾ | | J ⁽²⁾ | ns |

- (1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
- (2) $J = AccessTime \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(3)}$
- (3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

Table 7-30. GPMC and NAND Flash Switching Characteristics—Asynchronous Mode

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-------|----------------------|---|-------------------------|-------------------------|-----------------------|-----------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{R(d)}$ | Rise time, output data gpmc_ad[15:0] | 2 | | 2 | | ns |
| | $t_{F(d)}$ | Fall time, output data gpmc_ad[15:0] | 2 | | 2 | | ns |
| GNF0 | $t_{w(wenV)}$ | Pulse duration, output write enable gpmc_wen valid | A ⁽¹⁾ | | A ⁽¹⁾ | | ns |
| GNF1 | $t_{d(csnV-wenV)}$ | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output write enable gpmc_wen valid | B ⁽²⁾ – 0.2 | B ⁽²⁾ + 2.0 | B ⁽²⁾ – 5 | B ⁽²⁾ + 5 | ns |
| GNF2 | $t_{w(cleH-wenV)}$ | Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle high to output write enable gpmc_wen valid | C ⁽³⁾ – 0.2 | C ⁽³⁾ + 2.0 | C ⁽³⁾ – 5 | C ⁽³⁾ + 5 | ns |
| GNF3 | $t_{w(wenV-dV)}$ | Delay time, output data gpmc_ad[15:0] valid to output write enable gpmc_wen valid | D ⁽⁴⁾ – 0.2 | D ⁽⁴⁾ + 2.0 | D ⁽⁴⁾ – 5 | D ⁽⁴⁾ + 5 | ns |
| GNF4 | $t_{w(wenIV-dIV)}$ | Delay time, output write enable gpmc_wen invalid to output data gpmc_ad[15:0] invalid | E ⁽⁵⁾ – 0.2 | E ⁽⁵⁾ + 5 | E ⁽⁵⁾ – 5 | E ⁽⁵⁾ + 5 | ns |
| GNF5 | $t_{w(wenIV-cleIV)}$ | Delay time, output write enable gpmc_wen invalid to output lower-byte enable and command latch enable gpmc_be0n_cle invalid | F ⁽⁶⁾ – 0.2 | F ⁽⁶⁾ + 2.0 | F ⁽⁶⁾ – 5 | F ⁽⁶⁾ + 5 | ns |
| GNF6 | $t_{w(wenIV-csnIV)}$ | Delay time, output write enable gpmc_wen invalid to output chip select gpmc_csn[x] ⁽¹³⁾ invalid | G ⁽⁷⁾ – 0.2 | G ⁽⁷⁾ + 2.0 | G ⁽⁷⁾ – 5 | G ⁽⁷⁾ + 5 | ns |
| GNF7 | $t_{w(aleH-wenV)}$ | Delay time, output address valid and address latch enable gpmc_advn_ale high to output write enable gpmc_wen valid | C ⁽³⁾ – 0.2 | C ⁽³⁾ + 2.0 | C ⁽³⁾ – 5 | C ⁽³⁾ + 5 | ns |
| GNF8 | $t_{w(wenIV-aleIV)}$ | Delay time, output write enable gpmc_wen invalid to output address valid and address latch enable gpmc_advn_ale invalid | F ⁽⁶⁾ – 0.2 | F ⁽⁶⁾ + 2.0 | F ⁽⁶⁾ – 5 | F ⁽⁶⁾ + 5 | ns |
| GNF9 | $t_{c(wen)}$ | Cycle time, write | H ⁽⁸⁾ | | H ⁽⁸⁾ | | ns |
| GNF10 | $t_{d(csnV-oenV)}$ | Delay time, output chip select gpmc_csn[x] ⁽¹³⁾ valid to output enable gpmc_oen valid | I ⁽⁹⁾ – 0.2 | I ⁽⁹⁾ + 2.0 | I ⁽⁹⁾ – 5 | I ⁽⁹⁾ + 5 | ns |
| GNF13 | $t_{w(oenV)}$ | Pulse duration, output enable gpmc_oen valid | K ⁽¹⁰⁾ | | K ⁽¹⁰⁾ | | ns |
| GNF14 | $t_{c(oen)}$ | Cycle time, read | L ⁽¹¹⁾ | | L ⁽¹¹⁾ | | ns |
| GNF15 | $t_{w(oenIV-csnIV)}$ | Delay time, output enable gpmc_oen invalid to output chip select gpmc_csn[x] ⁽¹³⁾ invalid | M ⁽¹²⁾ – 0.2 | M ⁽¹²⁾ + 2.0 | M ⁽¹²⁾ – 5 | M ⁽¹²⁾ + 5 | ns |

(1) $A = (WEOffTime - WEOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$

(2) $B = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$

(3) $C = ((WEOnTime - ADVOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEExtraDelay - ADVExtraDelay)) \times GPMC_FCLK^{(14)}$

(4) $D = (WEOnTime \times (TimeParaGranularity + 1) + 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(14)}$

(5) $E = ((WRCycleTime - WEOffTime) \times (TimeParaGranularity + 1) - 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(14)}$

(6) $F = ((ADVWROffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - WEEExtraDelay)) \times GPMC_FCLK^{(14)}$

(7) $G = ((CSWROffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - WEEExtraDelay)) \times GPMC_FCLK^{(14)}$

(8) $H = WRCycleTime \times (1 + TimeParaGranularity) \times GPMC_FCLK^{(14)}$

(9) $I = ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$

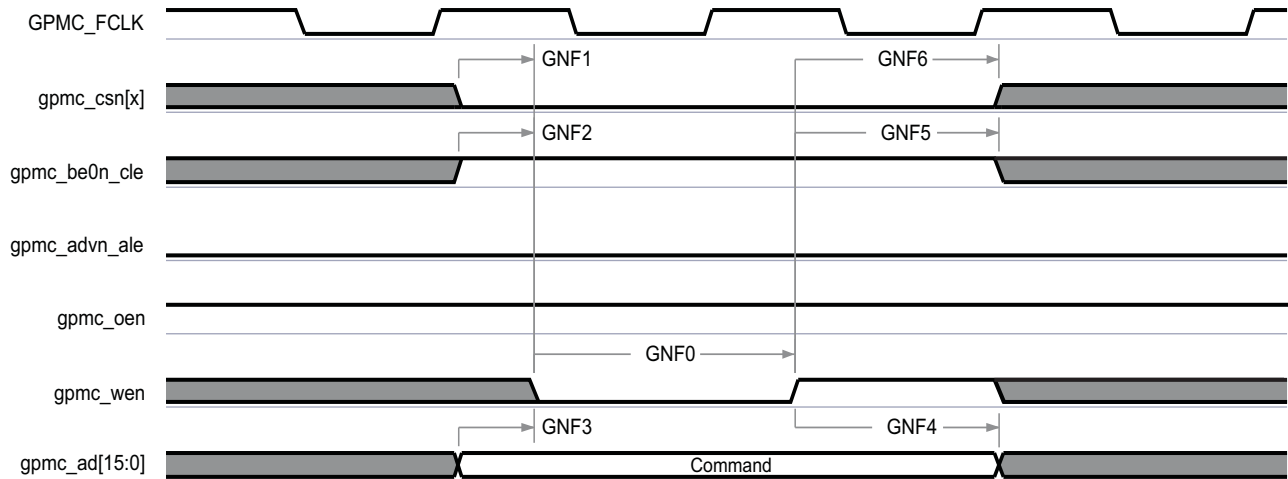
(10) $K = (OEOffTime - OEOnTime) \times (1 + TimeParaGranularity) \times GPMC_FCLK^{(14)}$

(11) $L = RdCycleTime \times (1 + TimeParaGranularity) \times GPMC_FCLK^{(14)}$

(12) $M = ((CSRdOffTime - OEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - OEExtraDelay)) \times GPMC_FCLK^{(14)}$

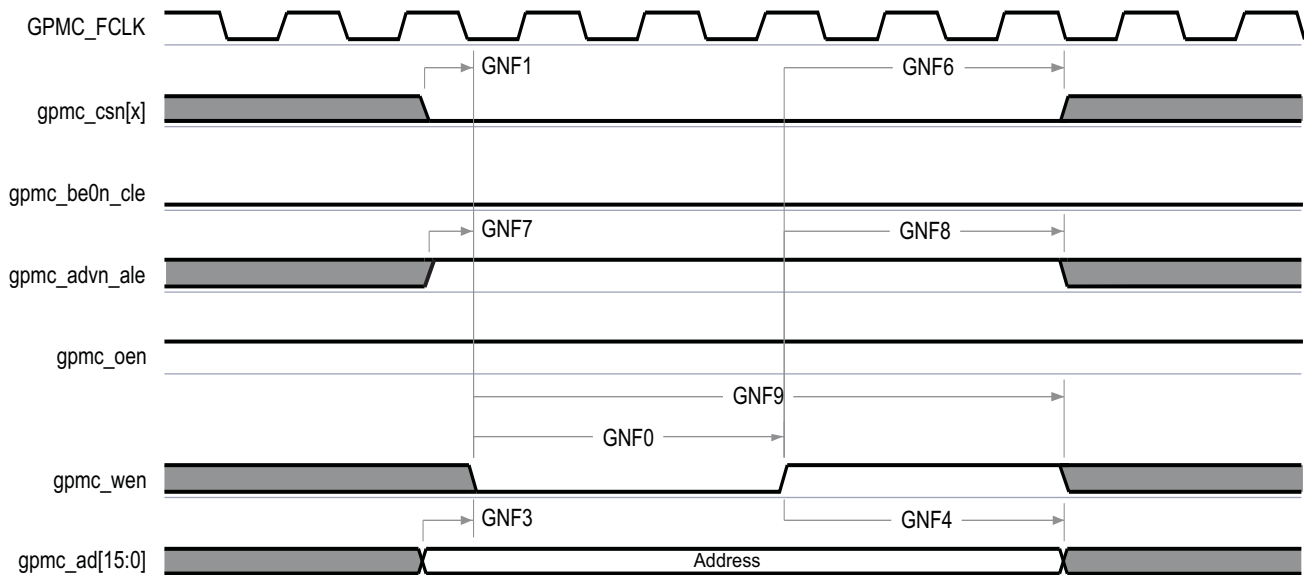
(13) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.

(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.



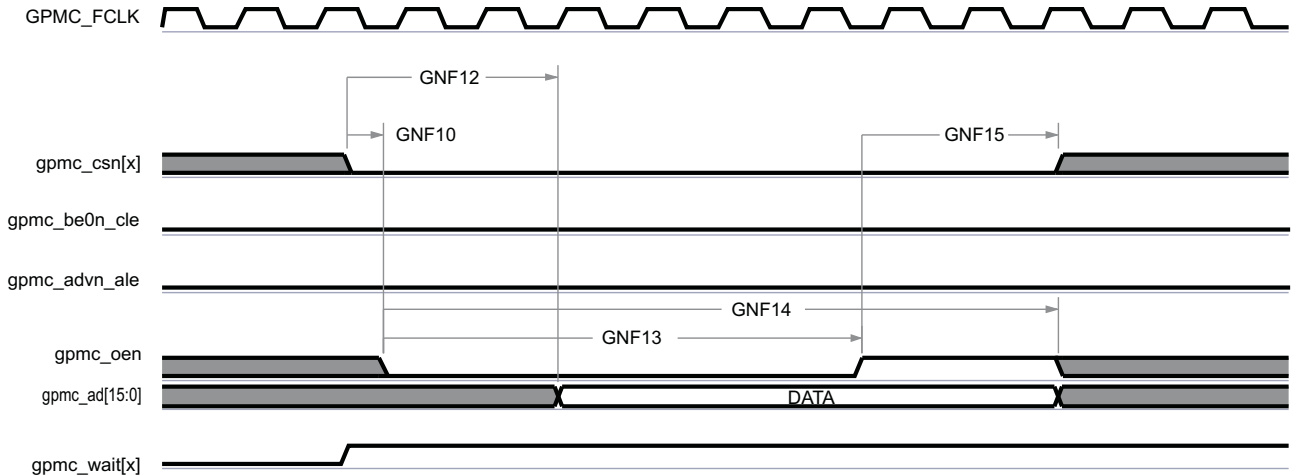
(1) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.

Figure 7-28. GPMC and NAND Flash—Command Latch Cycle



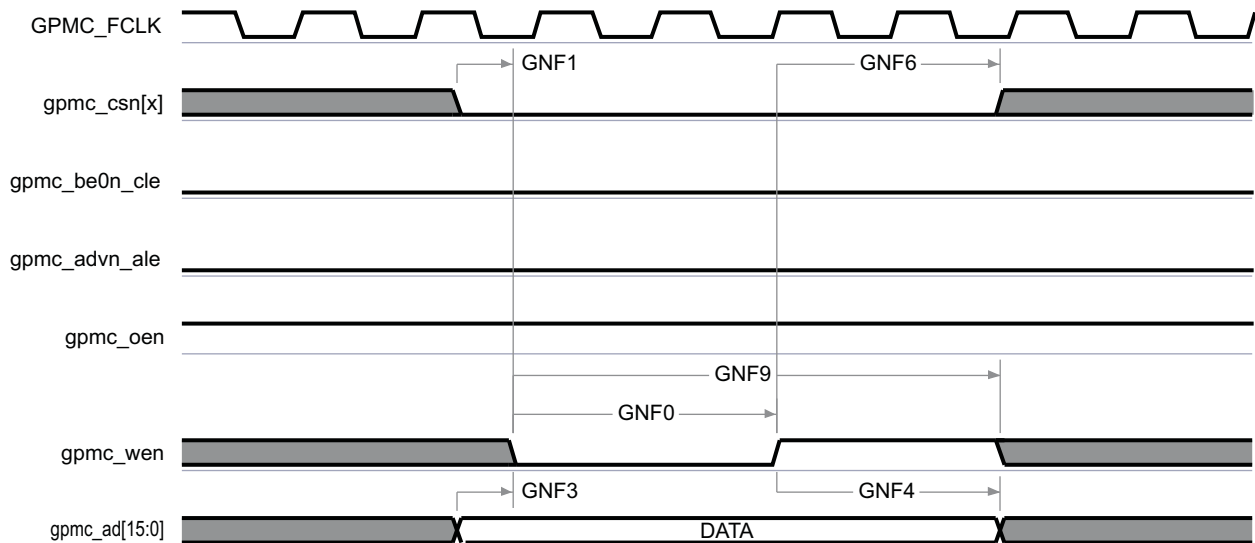
(1) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.

Figure 7-29. GPMC and NAND Flash—Address Latch Cycle



- (1) GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- (2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (3) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5. In gpmc_wait[x], x is equal to 0 or 1.

Figure 7-30. GPMC and NAND Flash—Data Read Cycle



- (1) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, or 5.

Figure 7-31. GPMC and NAND Flash—Data Write Cycle

7.7.2 mDDR(LPDDR), DDR2, DDR3, DDR3L Memory Interface

The device has a dedicated interface to mDDR(LPDDR), DDR2, DDR3, and DDR3L SDRAM. It supports JEDEC standard compliant mDDR(LPDDR), DDR2, DDR3, and DDR3L SDRAM devices with a 16-bit data path to external SDRAM memory.

For more details on the mDDR(LPDDR), DDR2, DDR3, and DDR3L memory interface, see the EMIF section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

7.7.2.1 mDDR (LPDDR) Routing Guidelines

It is common to find industry references to mobile double data rate (mDDR) when discussing JEDEC defined low-power double-data rate (LPDDR) memory devices. The following guidelines use LPDDR when referencing JEDEC defined low-power double-data rate memory devices.

7.7.2.1.1 Board Designs

TI only supports board designs that follow the guidelines outlined in this document. The switching characteristics and the timing diagram for the LPDDR memory interface are shown in [Table 7-31](#) and [Figure 7-32](#).

Table 7-31. Switching Characteristics for LPDDR Memory Interface

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---------------------------------------|-----|-----|------|
| 1 | $t_{c(DDR_CK)}$ $t_{c(DDR_CKn)}$ | 5 | (1) | ns |

(1) The JEDEC JESD209B specification only defines the maximum clock period for LPDDR333 and faster speed bin LPDDR memory devices. To determine the maximum clock period, see the respective LPDDR memory data sheet.

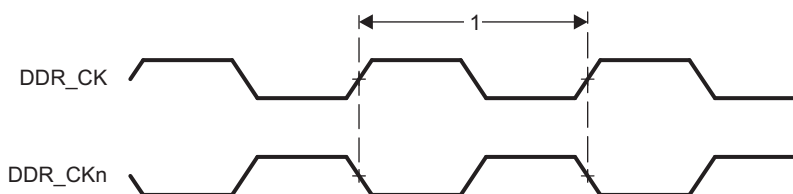


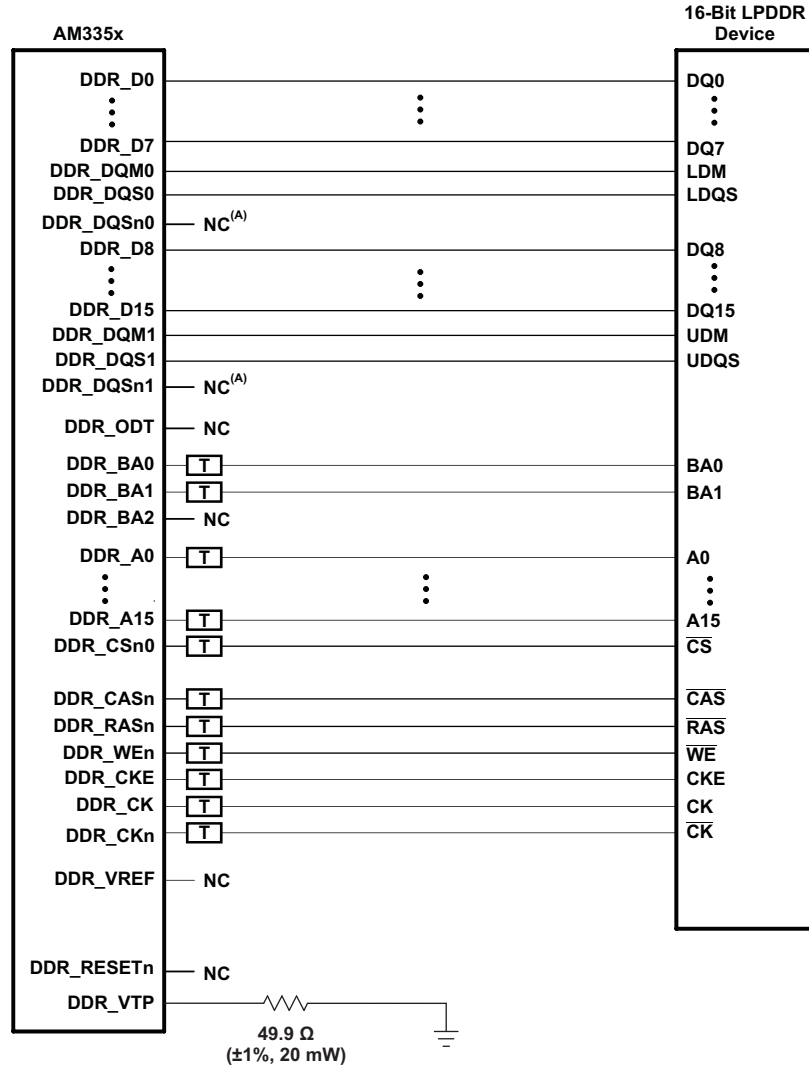
Figure 7-32. LPDDR Memory Interface Clock Timing

7.7.2.1.2 LPDDR Interface

This section provides the timing specification for the LPDDR interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable LPDDR memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this LPDDR specification, see [Understanding TI's PCB Routing Rule-Based DDR Timing Specification](#). This application report provides generic guidelines and approach. All the specifications provided in the data manual take precedence over the generic guidelines and must be adhered to for a reliable LPDDR interface operation.

7.7.2.1.2.1 LPDDR Interface Schematic

[Figure 7-33](#) shows the schematic connections for 16-bit interface on the AM335x device using one x16 LPDDR device. The AM335x LPDDR memory interface only supports 16-bit-wide mode of operation. The AM335x device can only source one load connected to the DQS[x] and DQ[x] net class signals and one load connected to the CK and ADDR_CTRL net class signals. For more information related to net classes, see [Section 7.7.2.1.2.8](#).



- A. Enable internal weak pulldown on these pins. For details, see the EMIF section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).
- B. For all the termination requirements, see [Section 7.7.2.1.2.9](#).

Figure 7-33. 16-Bit LPDDR Interface Using One 16-Bit LPDDR Device

7.7.2.1.2.2 Compatible JEDEC LPDDR Devices

Table 7-32 shows the parameters of the JEDEC LPDDR devices that are compatible with this interface. Generally, the LPDDR interface is compatible with x16 LPDDR400 speed grade LPDDR devices.

Table 7-32. Compatible JEDEC LPDDR Devices (Per Interface)⁽¹⁾

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|-----------------------------------|----------|-----|-----------|
| 1 | JEDEC LPDDR device speed grade | LPDDR400 | | |
| 2 | JEDEC LPDDR device bit width | x16 | x16 | Bits |
| 3 | JEDEC LPDDR device count | | 1 | Devices |
| 4 | JEDEC LPDDR device terminal count | | 60 | Terminals |

(1) If the LPDDR interface is operated with a clock frequency less than 200 MHz, lower-speed grade LPDDR devices may be used if the minimum clock period specified for the LPDDR device is less than or equal to the minimum clock period selected for the AM335x LPDDR interface.

7.7.2.1.2.3 PCB Stackup

The minimum stackup required for routing the AM335x device is a 4-layer stackup as shown in Table 7-33. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance signal integrity and electromagnetic interference performance, or to reduce the size of the PCB footprint.

Table 7-33. Minimum PCB Stackup⁽¹⁾

| LAYER | TYPE | DESCRIPTION |
|-------|--------|-----------------------|
| 1 | Signal | Top signal routing |
| 2 | Plane | Ground |
| 3 | Plane | Split Power Plane |
| 4 | Signal | Bottom signal routing |

(1) All signals that have critical signal integrity requirements should be routed first on layer 1. It may not be possible to route all of these signals on layer 1, therefore requiring routing of some signals on layer 4. When this is done, the signal routes on layer 4 must not cross splits in the power plane.

Complete stackup specifications are provided in [Table 7-34](#).

Table 7-34. PCB Stackup Specifications⁽¹⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|---|---------|-------|---------|----------|
| 1 | PCB routing and plane layers | 4 | | | |
| 2 | Signal routing layers | 2 | | | |
| 3 | Full ground layers under LPDDR routing region | 1 | | | |
| 4 | Number of ground plane cuts allowed within LPDDR routing region | | | 0 | |
| 5 | Full VDDS_DDR power reference layers under LPDDR routing region | 1 | | | |
| 6 | Number of layers between LPDDR routing layer and reference ground plane | | | 0 | |
| 7 | PCB routing feature size | | 4 | | mils |
| 8 | PCB trace width, w | | 4 | | mils |
| 9 | PCB BGA escape via pad size ⁽²⁾ | | 18 | 20 | mils |
| 10 | PCB BGA escape via hole size ⁽²⁾ | | 10 | | mils |
| 11 | Single-ended impedance, Z_0 ⁽³⁾ | | 50 | 75 | Ω |
| 12 | Impedance control ⁽⁴⁾⁽⁵⁾ | Z_0-5 | Z_0 | Z_0+5 | Ω |

(1) For the LPDDR device BGA pad size, see the LPDDR device manufacturer documentation.

(2) A 20-10 via may be used if enough power routing resources are available. An 18-10 via allows for more flexible power routing to the AM335x device.

(3) Z_0 is the nominal single-ended impedance selected for the PCB.

(4) This parameter specifies the AC characteristic impedance tolerance for each segment of a PCB signal trace relative to the chosen Z_0 defined by the single-ended impedance parameter.

(5) Tighter impedance control is required to ensure flight time skew is minimal.

7.7.2.1.2.4 Placement

Figure 7-34 shows the required placement for the LPDDR devices. The dimensions for this figure are defined in Table 7-35. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For single-memory LPDDR systems, the second LPDDR device is omitted from the placement.

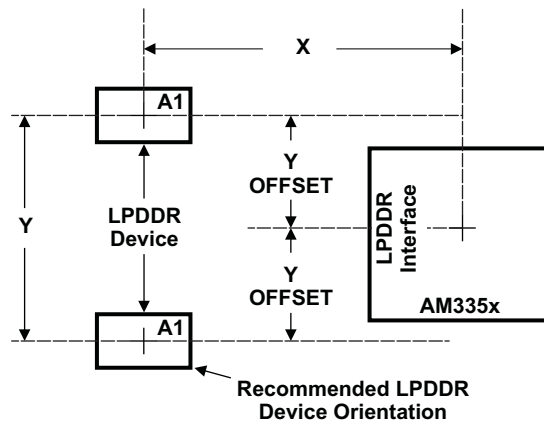


Figure 7-34. AM335x Device and LPDDR Device Placement

Table 7-35. Placement Specifications⁽¹⁾

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|------|------|
| 1 | X ⁽²⁾⁽³⁾ | | 1750 | mils |
| 2 | Y ⁽²⁾⁽³⁾ | | 1280 | mils |
| 3 | Y Offset ⁽²⁾⁽³⁾⁽⁴⁾ | | 650 | mils |
| 4 | Clearance from non-LPDDR signal to LPDDR keepout region ⁽⁵⁾⁽⁶⁾ | 4 | | w |

- (1) LPDDR keepout region to encompass entire LPDDR routing area.
- (2) For dimension definitions, see Figure 7-34.
- (3) Measurements from center of the AM335x device to center of LPDDR device.
- (4) For single-memory systems, TI recommends that Y offset be as small as possible.
- (5) w is defined as the signal trace width.
- (6) Non-LPDDR signals allowed within LPDDR keepout region provided they are separated from LPDDR routing layers by a ground plane.

7.7.2.1.2.5 LPDDR Keepout Region

The region of the PCB used for the LPDDR circuitry must be isolated from other signals. The LPDDR keepout region is defined for this purpose and is shown in Figure 7-35. This region should encompass all LPDDR circuitry and the region size varies with component placement and LPDDR routing. Additional clearances required for the keepout region are shown in Table 7-35. Non-LPDDR signals must not be routed on the same signal layer as LPDDR signals within the LPDDR keepout region. Non-LPDDR signals may be routed in the region provided they are routed on layers separated from LPDDR signal layers by a ground layer. No breaks should be allowed in the reference ground or VDDS_DDR power plane in this region. In addition, the VDDS_DDR power plane should cover the entire keepout region.

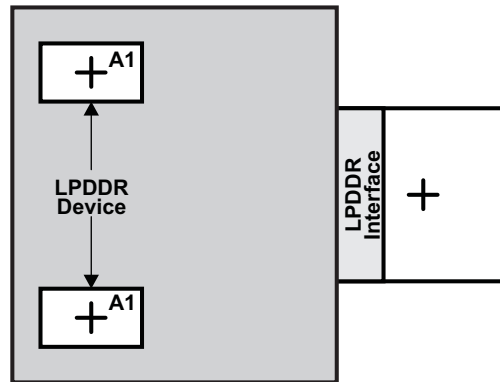


Figure 7-35. LPDDR Keepout Region

7.7.2.1.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the LPDDR and other circuitry. Table 7-36 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the AM335x LPDDR interface and LPDDR devices. Additional bulk bypass capacitance may be needed for other circuitry.

Table 7-36. Bulk Bypass Capacitors⁽¹⁾

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|-----|-----|---------|
| 1 | AM335x VDDS_DDR bulk bypass capacitor count | 1 | | Devices |
| 2 | AM335x VDDS_DDR bulk bypass total capacitance | 10 | | μF |
| 3 | LPDDR#1 bulk bypass capacitor count | 1 | | Devices |
| 4 | LPDDR#1 bulk bypass total capacitance | 10 | | μF |
| 5 | LPDDR#2 bulk bypass capacitor count ⁽²⁾ | 1 | | Devices |
| 6 | LPDDR#2 bulk bypass total capacitance ⁽²⁾ | 10 | | μF |

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors.

(2) Only used when two LPDDR devices are used.

7.7.2.1.2.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper LPDDR interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, the AM335x device LPDDR power, and the AM335x device LPDDR ground connections. [Table 7-37](#) contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

Table 7-37. High-Speed Bypass Capacitors

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|-----|------|---------|
| 1 | HS bypass capacitor package size ⁽¹⁾ | | 0402 | 10 mils |
| 2 | Distance from HS bypass capacitor to device being bypassed | | 250 | mils |
| 3 | Number of connection vias for each HS bypass capacitor ⁽²⁾ | 2 | | Vias |
| 4 | Trace length from bypass capacitor contact to connection via | | 30 | mils |
| 5 | Number of connection vias for each AM335x VDDS_DDR and VSS terminal | 1 | | Vias |
| 6 | Trace length from AM335x VDDS_DDR and VSS terminal to connection via | | 35 | mils |
| 7 | Number of connection vias for each LPDDR device power and ground terminal | 1 | | Vias |
| 8 | Trace length from LPDDR device power and ground terminal to connection via | | 35 | mils |
| 9 | AM335x VDDS_DDR HS bypass capacitor count ⁽³⁾ | 10 | | Devices |
| 10 | AM335x VDDS_DDR HS bypass capacitor total capacitance | 0.6 | | μF |
| 11 | LPDDR device HS bypass capacitor count ⁽³⁾⁽⁴⁾ | 8 | | Devices |
| 12 | LPDDR device HS bypass capacitor total capacitance ⁽⁴⁾ | 0.4 | | μF |

(1) LxW, 10-mil units; for example, a 0402 is a 40x20-mil surface-mount capacitor.

(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.

(3) These devices should be placed as close as possible to the device being bypassed.

(4) Per LPDDR device.

7.7.2.1.2.8 Net Classes

[Table 7-38](#) lists the clock net classes for the LPDDR interface. [Table 7-39](#) lists the signal net classes, and associated clock net classes, for the signals in the LPDDR interface. These net classes are used for the termination and routing rules that follow.

Table 7-38. Clock Net Class Definitions

| CLOCK NET CLASS | AM335x PIN NAMES |
|-----------------|--------------------|
| CK | DDR_CK and DDR_CKn |
| DQS0 | DDR_DQS0 |
| DQS1 | DDR_DQS1 |

Table 7-39. Signal Net Class Definitions

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | AM335x PIN NAMES |
|------------------|----------------------------|--|
| ADDR_CTRL | CK | DDR_BA[1:0], DDR_A[15:0], DDR_CSn0, DDR_CASn, DDR_RASn, DDR_WEn, DDR_CKE |
| DQ0 | DQS0 | DDR_D[7:0], DDR_DQM0 |
| DQ1 | DQS1 | DDR_D[15:8], DDR_DQM1 |

7.7.2.1.2.9 LPDDR Signal Termination

There is no specific need for adding terminations on the LPDDR interface. However, system designers may evaluate the need for serial terminators for EMI and overshoot reduction. Placement of serial terminations for DQS[x] and DQ[x] net class signals should be determined based on PCB analysis. Placement of serial terminations for ADDR_CTRL net class signals should be close to the AM335x device. [Table 7-40](#) shows the specifications for the serial terminators in such cases.

Table 7-40. LPDDR Signal Terminations

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|-----|-----|-------------------------------|------|
| 1 | CK net class ⁽¹⁾ | 0 | 22 | Z _o ⁽²⁾ | Ω |
| 2 | ADDR_CTRL net class ⁽¹⁾⁽³⁾⁽⁴⁾ | 0 | 22 | Z _o ⁽²⁾ | Ω |
| 3 | DQS0, DQS1, DQ0, and DQ1 net classes | 0 | 22 | Z _o ⁽²⁾ | Ω |

(1) Only series termination is permitted.

(2) Z_o is the LPDDR PCB trace characteristic impedance.

(3) Series termination values larger than typical only recommended to address EMI issues.

(4) Series termination values should be uniform across net class.

7.7.2.1.3 LPDDR CK and ADDR_CTRL Routing

Figure 7-36 shows the topology of the routing for the CK and ADDR_CTRL net classes. The length of signal path AB and AC should be minimized with emphasis to minimize lengths C and D such that length A is the majority of the total length of signal path AB and AC.

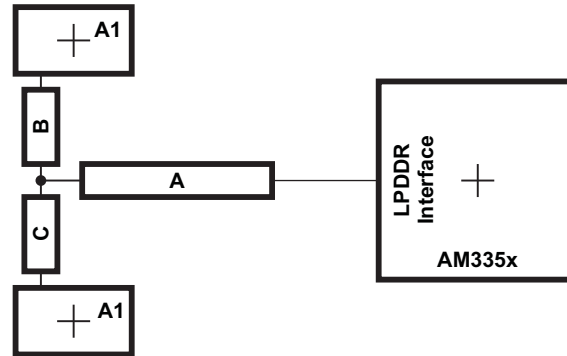


Figure 7-36. CK and ADDR_CTRL Routing and Topology

Table 7-41. CK and ADDR_CTRL Routing Specification⁽¹⁾⁽²⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|----------|-------|----------|------|
| 1 | Center-to-center CK spacing | | | 2w | |
| 2 | CK differential pair skew length mismatch ⁽²⁾⁽³⁾ | | | 25 | mils |
| 3 | CK B-to-CK C skew length mismatch | | | 25 | mils |
| 4 | Center-to-center CK to other LPDDR trace spacing ⁽⁴⁾ | 4w | | | |
| 5 | CK and ADDR_CTRL nominal trace length ⁽⁵⁾ | CACLM-50 | CACLM | CACLM+50 | mils |
| 6 | ADDR_CTRL-to-CK skew length mismatch | | | 100 | mils |
| 7 | ADDR_CTRL-to-ADDR_CTRL skew length mismatch | | | 100 | mils |
| 8 | Center-to-center ADDR_CTRL to other LPDDR trace spacing ⁽⁴⁾ | 4w | | | |
| 9 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing ⁽⁴⁾ | 3w | | | |
| 10 | ADDR_CTRL A-to-B and ADDR_CTRL A-to-C skew length mismatch ⁽²⁾ | | | 100 | mils |
| 11 | ADDR_CTRL B-to-C skew length mismatch | | | 100 | mils |

- (1) CK represents the clock net class, and ADDR_CTRL represents the address and control signal net class.
- (2) Series terminator, if used, should be located closest to the AM335x device.
- (3) Differential impedance should be $Z_o \times 2$, where Z_o is the single-ended impedance defined in Table 7-34.
- (4) Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
- (5) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

Figure 7-37 shows the topology and routing for the DQS[x] and DQ[x] net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

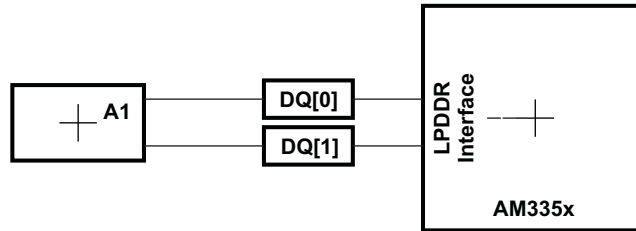


Figure 7-37. DQS[x] and DQ[x] Routing and Topology

Table 7-42. DQS[x] and DQ[x] Routing Specification⁽¹⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|---|---------|------|---------|------|
| 1 | Center-to-center DQS[x] spacing | | | 2w | |
| 2 | Center-to-center DDR_DQS[x] to other LPDDR trace spacing ⁽²⁾ | 4w | | | |
| 3 | DQS[x] and DQ[x] nominal trace length ⁽³⁾ | DQLM-50 | DQLM | DQLM+50 | mils |
| 4 | DQ[x]-to-DQS[x] skew length mismatch ⁽³⁾ | | | 100 | mils |
| 5 | DQ[x]-to-DQ[x] skew length mismatch ⁽³⁾ | | | 100 | mils |
| 6 | Center-to-center DQ[x] to other LPDDR trace spacing ⁽²⁾⁽⁴⁾ | 4w | | | |
| 7 | Center-to-center DQ[x] to other DQ[x] trace spacing ⁽²⁾⁽⁵⁾ | 3w | | | |

- (1) DQS[x] represents the DQS0 and DQS1 clock net classes, and DQ[x] represents the DQ0 and DQ1 signal net classes.
- (2) Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
- (3) There is no requirement for skew matching between data bytes; that is, from net classes DQS0 and DQ0 to net classes DQS1 and DQ1.
- (4) Signals from one DQ net class should be considered other LPDDR traces to another DQ net class.
- (5) DQLM is the longest Manhattan distance of each of the DQS[x] and DQ[x] net classes.

7.7.2.2 DDR2 Routing Guidelines

7.7.2.2.1 Board Designs

TI only supports board designs that follow the guidelines outlined in this document. [Table 7-43](#) and [Figure 7-38](#) show the switching characteristics and timing diagram for the DDR2 memory interface.

Table 7-43. Switching Characteristics for DDR2 Memory Interface

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|------|------------------|------|
| 1 | $t_{c(DDR_CK)}$ $t_{c(DDR_CKn)}$ Cycle time, DDR_CK and DDR_CKn | 3.75 | 8 ⁽¹⁾ | ns |

(1) The JEDEC JESD79-2F specification defines the maximum clock period of 8 ns for all standard-speed bin DDR2 memory devices. Therefore, all standard-speed bin DDR2 memory devices are required to operate at 125 MHz.

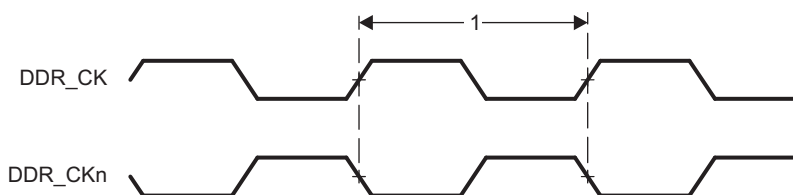


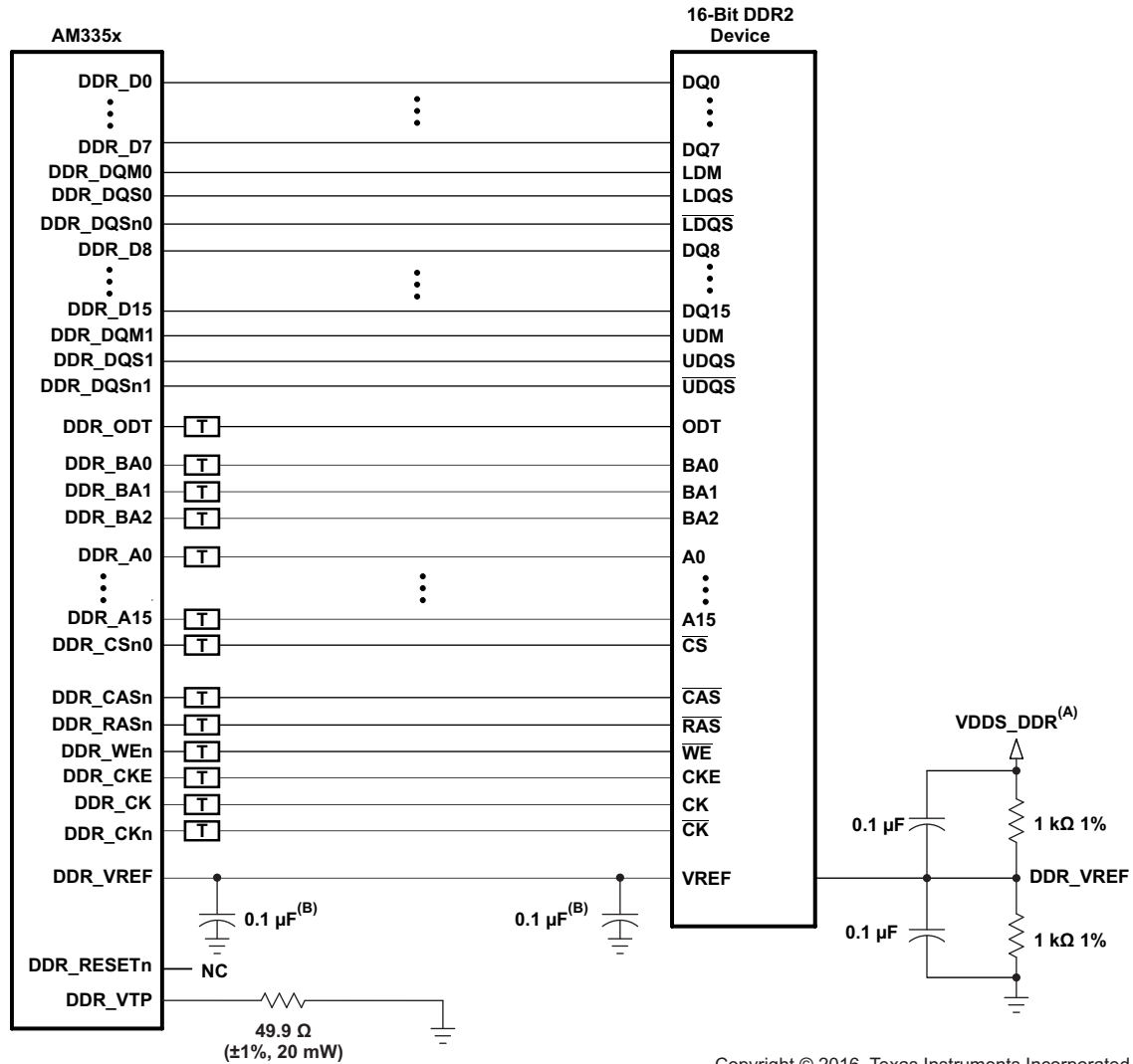
Figure 7-38. DDR2 Memory Interface Clock Timing

7.7.2.2.2 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR2 specification, see [Understanding TI's PCB Routing Rule-Based DDR Timing Specification](#). This application report provides generic guidelines and approach. All the specifications provided in the data manual take precedence over the generic guidelines and must be adhered to for a reliable DDR2 interface operation.

7.7.2.2.2.1 DDR2 Interface Schematic

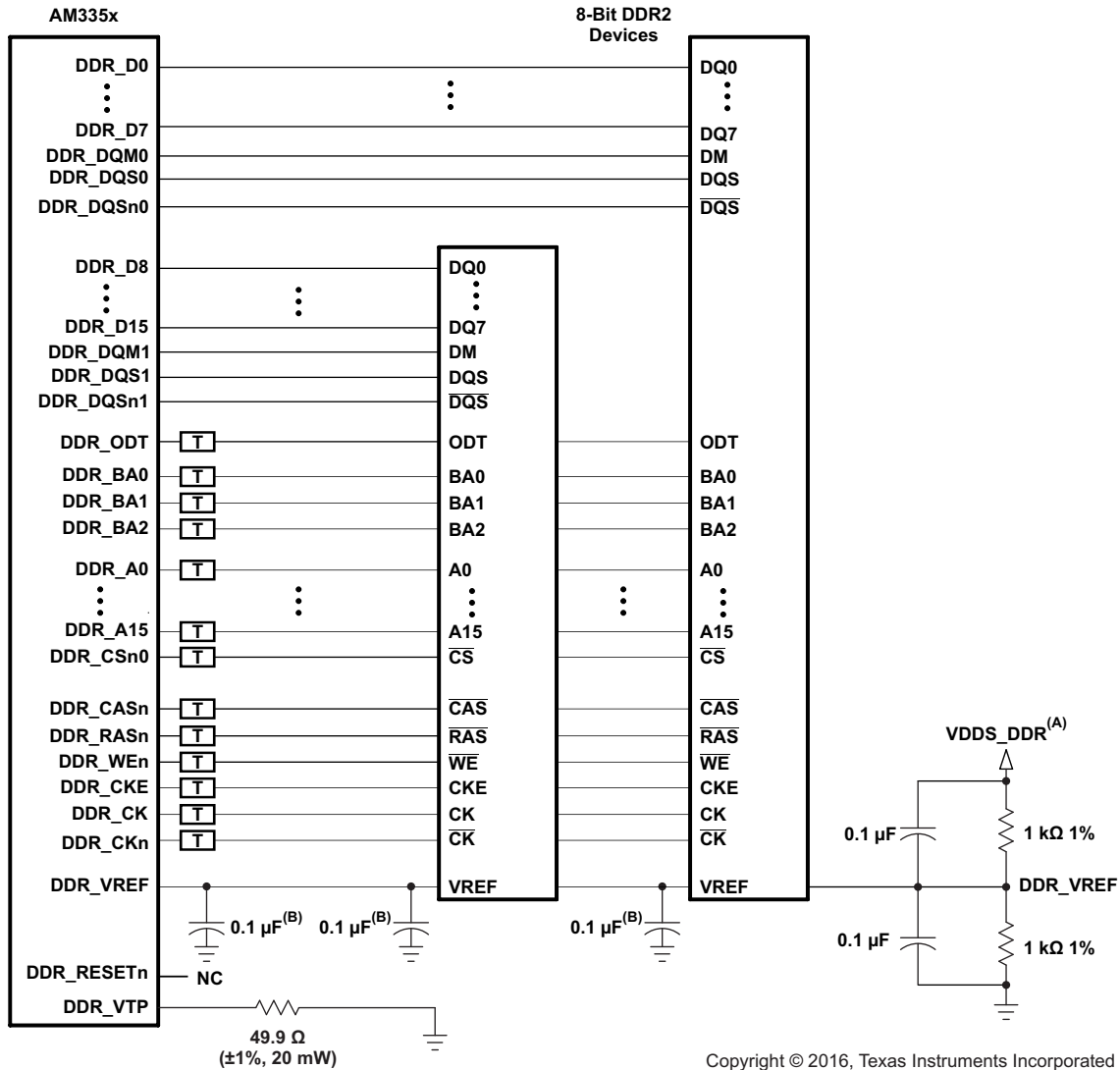
[Figure 7-39](#) shows the schematic connections for 16-bit interface on the AM335x device using one x16 DDR2 device and [Figure 7-40](#) shows the schematic connections for 16-bit interface on the AM335x device using two x8 DDR2 devices. The AM335x DDR2 memory interface only supports 16-bit-wide mode of operation. The AM335x device can only source one load connected to the DQS[x] and DQ[x] net class signals and two loads connected to the CK and ADDR_CTRL net class signals. For more information related to net classes, see [Section 7.7.2.2.8](#).



Copyright © 2016, Texas Instruments Incorporated

- A. VDDSDDDR is the power supply for the DDR2 memories and the AM335x DDR2 interface.
- B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a DDR_VREF pin.
- C. For all the termination requirements, see [Section 7.7.2.2.2.9](#).

Figure 7-39. 16-Bit DDR2 Interface Using One 16-Bit DDR2 Device



Copyright © 2016, Texas Instruments Incorporated

- A. VDDSDDR is the power supply for the DDR2 memories and the AM335x DDR2 interface.
- B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a DDR_VREF pin.
- C. For all the termination requirements, see [Section 7.7.2.2.2.9](#).

Figure 7-40. 16-Bit DDR2 Interface Using Two 8-Bit DDR2 Devices

7.7.2.2.2 Compatible JEDEC DDR2 Devices

Table 7-44 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 or x8 DDR2-533 speed grade DDR2 devices.

Table 7-44. Compatible JEDEC DDR2 Devices (Per Interface)⁽¹⁾

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|----------|-----|-----------|
| 1 | JEDEC DDR2 device speed grade ⁽²⁾ | DDR2-533 | | |
| 2 | JEDEC DDR2 device bit width | x8 | x16 | bits |
| 3 | JEDEC DDR2 device count | 1 | 2 | devices |
| 4 | JEDEC DDR2 device terminal count ⁽³⁾ | 60 | 84 | terminals |

(1) If the DDR2 interface is operated with a clock frequency less than 266 MHz, lower-speed grade DDR2 devices may be used if the minimum clock period specified for the DDR2 device is less than or equal to the minimum clock period selected for the AM335x DDR2 interface.

(2) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backward compatibility.

(3) 92-terminal devices are also supported for legacy reasons. New designs will migrate to 84-terminal DDR2 devices. Electrically, the 92- and 84-terminal DDR2 devices are the same.

7.7.2.2.3 PCB Stackup

The minimum stackup required for routing the AM335x device is a 4-layer stackup as shown in Table 7-45. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance signal integrity and electromagnetic interference performance, or to reduce the size of the PCB footprint.

Table 7-45. Minimum PCB Stackup⁽¹⁾

| LAYER | TYPE | DESCRIPTION |
|-------|--------|-----------------------|
| 1 | Signal | Top signal routing |
| 2 | Plane | Ground |
| 3 | Plane | Split power plane |
| 4 | Signal | Bottom signal routing |

(1) All signals that have critical signal integrity requirements should be routed first on layer 1. It may not be possible to route all of these signals on layer 1, therefore requiring routing of some signals on layer 4. When this is done, the signal routes on layer 4 must not cross splits in the power plane.

Complete stackup specifications are provided in [Table 7-46](#).

Table 7-46. PCB Stackup Specifications⁽¹⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|---------|-------|---------|----------|
| 1 | PCB routing and plane layers | 4 | | | |
| 2 | Signal routing layers | 2 | | | |
| 3 | Full ground layers under DDR2 routing region | 1 | | | |
| 4 | Number of ground plane cuts allowed within DDR2 routing region | | | 0 | |
| 5 | Full VDDS_DDR power reference layers under DDR2 routing region | 1 | | | |
| 6 | Number of layers between DDR2 routing layer and reference ground plane | | | 0 | |
| 7 | PCB routing feature size | | 4 | | mils |
| 8 | PCB trace width, w | | 4 | | mils |
| 9 | PCB BGA escape via pad size ⁽²⁾ | | 18 | 20 | mils |
| 10 | PCB BGA escape via hole size ⁽²⁾ | | 10 | | mils |
| 11 | Single-ended impedance, Z_0 ⁽³⁾ | | 50 | 75 | Ω |
| 12 | Impedance control ⁽⁴⁾⁽⁵⁾ | Z_0-5 | Z_0 | Z_0+5 | Ω |

(1) For the DDR2 device BGA pad size, see the DDR2 device manufacturer documentation.

(2) A 20-10 via may be used if enough power routing resources are available. An 18-10 via allows for more flexible power routing to the AM335x device.

(3) Z_0 is the nominal single-ended impedance selected for the PCB.

(4) This parameter specifies the AC characteristic impedance tolerance for each segment of a PCB signal trace relative to the chosen Z_0 defined by the single-ended impedance parameter.

(5) Tighter impedance control is required to ensure flight time skew is minimal.

7.7.2.2.4 Placement

Figure 7-41 shows the required placement for the DDR2 devices. The dimensions for this figure are defined in Table 7-47. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For single-memory DDR2 systems, the second DDR2 device is omitted from the placement.

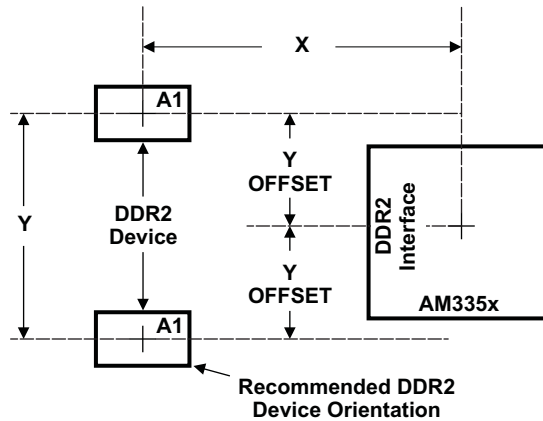


Figure 7-41. AM335x Device and DDR2 Device Placement

Table 7-47. Placement Specifications⁽¹⁾

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|------|------|
| 1 | X ⁽²⁾⁽³⁾ | | 1750 | mils |
| 2 | Y ⁽²⁾⁽³⁾ | | 1280 | mils |
| 3 | Y Offset ⁽²⁾⁽³⁾⁽⁴⁾ | | 650 | mils |
| 4 | Clearance from non-DDR2 signal to DDR2 keepout region ⁽⁵⁾⁽⁶⁾ | 4 | | w |

(1) DDR2 keepout region to encompass entire DDR2 routing area.

(2) For dimension definitions, see Figure 7-41.

(3) Measurements from center of the AM335x device to center of the DDR2 device.

(4) For single-memory systems, it is recommended that Y offset be as small as possible.

(5) w is defined as the signal trace width.

(6) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

7.7.2.2.5 DDR2 Keepout Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keepout region is defined for this purpose and is shown in Figure 7-42. This region should encompass all DDR2 circuitry and the region size varies with component placement and DDR2 routing. Additional clearances required for the keepout region are shown in Table 7-47. Non-DDR2 signals must not be routed on the same signal layer as DDR2 signals within the DDR2 keepout region. Non-DDR2 signals may be routed in the region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground or VDDS_DDR power plane in this region. In addition, the VDDS_DDR power plane should cover the entire keepout region.

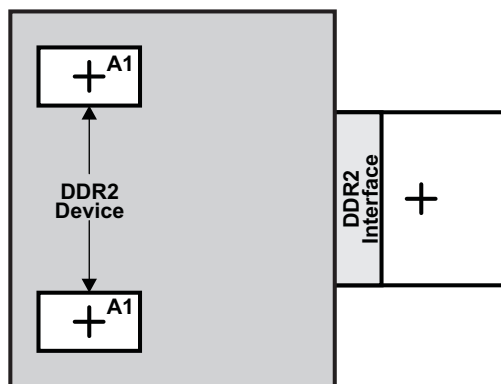


Figure 7-42. DDR2 Keepout Region

7.7.2.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 7-48 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the AM335x DDR2 interface and DDR2 devices. Additional bulk bypass capacitance may be needed for other circuitry.

Table 7-48. Bulk Bypass Capacitors⁽¹⁾

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|-----|-----|---------|
| 1 | AM335x VDDS_DDR bulk bypass capacitor count | 1 | | devices |
| 2 | AM335x VDDS_DDR bulk bypass total capacitance | 10 | | μF |
| 3 | DDR2 number 1 bulk bypass capacitor count | 1 | | devices |
| 4 | DDR2 number 1 bulk bypass total capacitance | 10 | | μF |
| 5 | DDR2 number 2 bulk bypass capacitor count ⁽²⁾ | 1 | | devices |
| 6 | DDR2 number 2 bulk bypass total capacitance ⁽²⁾ | 10 | | μF |

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors.

(2) Only used when two DDR2 devices are used.

7.7.2.2.7 High-Speed (HS) Bypass Capacitors

HS bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, the AM335x device DDR2 power, and the AM335x device DDR2 ground connections. [Table 7-49](#) contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

Table 7-49. HS Bypass Capacitors

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|------|---------|
| 1 | HS bypass capacitor package size ⁽¹⁾ | | 0402 | 10 mils |
| 2 | Distance from HS bypass capacitor to device being bypassed | | 250 | mils |
| 3 | Number of connection vias for each HS bypass capacitor ⁽²⁾ | 2 | | vias |
| 4 | Trace length from bypass capacitor contact to connection via | | 30 | mils |
| 5 | Number of connection vias for each AM335x VDDS_DDR and VSS terminal | 1 | | vias |
| 6 | Trace length from AM335x VDDS_DDR and VSS terminal to connection via | | 35 | mils |
| 7 | Number of connection vias for each DDR2 device power and ground terminal | 1 | | vias |
| 8 | Trace length from DDR2 device power and ground terminal to connection via | | 35 | mils |
| 9 | AM335x VDDS_DDR HS bypass capacitor count ⁽³⁾ | 10 | | devices |
| 10 | AM335x VDDS_DDR HS bypass capacitor total capacitance | 0.6 | | μF |
| 11 | DDR2 device HS bypass capacitor count ⁽³⁾⁽⁴⁾ | 8 | | devices |
| 12 | DDR2 device HS bypass capacitor total capacitance ⁽⁴⁾ | 0.4 | | μF |

(1) LxW, 10-mil units; for example, a 0402 is a 40x20-mil surface-mount capacitor.

(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.

(3) These devices should be placed as close as possible to the device being bypassed.

(4) Per DDR2 device.

7.7.2.2.8 Net Classes

[Table 7-50](#) lists the clock net classes for the DDR2 interface. [Table 7-51](#) lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

Table 7-50. Clock Net Class Definitions

| CLOCK NET CLASS | AM335x PIN NAMES |
|-----------------|------------------------|
| CK | DDR_CK and DDR_CKn |
| DQS0 | DDR_DQS0 and DDR_DQSn0 |
| DQS1 | DDR_DQS1 and DDR_DQSn1 |

Table 7-51. Signal Net Class Definitions

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | AM335x PIN NAMES |
|------------------|----------------------------|---|
| ADDR_CTRL | CK | DDR_BA[2:0], DDR_A[15:0], DDR_CSn0, DDR_CASn, DDR_RASn, DDR_WEn, DDR_CKE, DDR_ODT |
| DQ0 | DQS0 | DDR_D[7:0], DDR_DQM0 |
| DQ1 | DQS1 | DDR_D[15:8], DDR_DQM1 |

7.7.2.2.9 DDR2 Signal Termination

Signal terminations are required on the CK and ADDR_CTRL net class signals. Serial terminations should be used on the CK and ADDR_CTRL lines and is the preferred termination scheme. On-device terminations (ODTs) are required on the DQS[x] and DQ[x] net class signals. They should be enabled to ensure signal integrity. Table 7-52 shows the specifications for the series terminators. Placement of serial terminations for ADDR_CTRL net class signals should be close to the AM335x device.

Table 7-52. DDR2 Signal Terminations

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|---|-----|-----|-------------------|----------|
| 1 | CK net class ⁽¹⁾ | 0 | | 10 | Ω |
| 2 | ADDR_CTRL net class ⁽¹⁾⁽²⁾⁽³⁾ | 0 | 22 | Zo ⁽⁴⁾ | Ω |
| 3 | DQS0, DQS1, DQ0, and DQ1 net classes ⁽⁵⁾ | N/A | | N/A | Ω |

- (1) Only series termination is permitted.
 (2) Series termination values larger than typical only recommended to address EMI issues.
 (3) Series termination values should be uniform across net class.
 (4) Zo is the DDR2 PCB trace characteristic impedance.
 (5) No external termination resistors are allowed and ODT must be used for these net classes.

If the DDR2 interface is operated at a lower frequency (<200-MHz clock rate), on-device terminations are not specifically required for the DQS[x] and DQ[x] net class signals and serial terminations for the CK and ADDR_CTRL net class signals are not mandatory. System designers may evaluate the need for serial terminators for EMI and overshoot reduction. Placement of serial terminations for DQS[x] and DQ[x] net class signals should be determined based on PCB analysis. Placement of serial terminations for ADDR_CTRL net class signals should be close to the AM335x device. Table 7-53 shows the specifications for the serial terminators in such cases.

Table 7-53. Lower-Frequency DDR2 Signal Terminations

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|-----|-----|-------------------|----------|
| 1 | CK net class ⁽¹⁾ | 0 | 22 | Zo ⁽²⁾ | Ω |
| 2 | ADDR_CTRL net class ⁽¹⁾⁽³⁾⁽⁴⁾ | 0 | 22 | Zo ⁽²⁾ | Ω |
| 3 | DQS0, DQS1, DQ0, and DQ1 net classes | 0 | 22 | Zo ⁽²⁾ | Ω |

- (1) Only series termination is permitted.
 (2) Zo is the DDR2 PCB trace characteristic impedance.
 (3) Series termination values larger than typical only recommended to address EMI issues.
 (4) Series termination values should be uniform across net class.

7.7.2.2.10 DDR_VREF Routing

DDR_VREF is used as a reference by the input buffers of the DDR2 memories as well as the AM335x device. DDR_VREF is intended to be half the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 7-39 and Figure 7-40. TI does not recommend other methods of creating DDR_VREF. Figure 7-43 shows the layout guidelines for DDR_VREF.

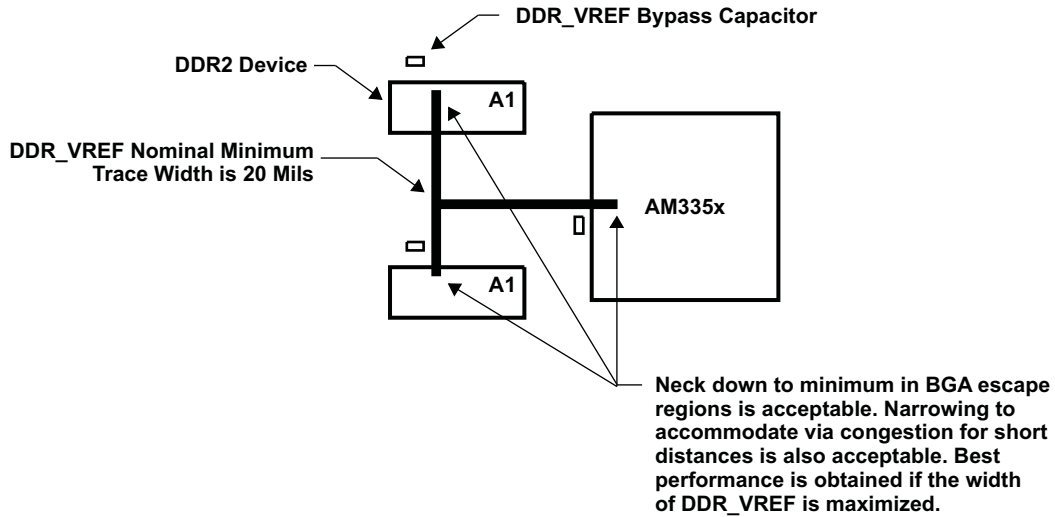


Figure 7-43. DDR_VREF Routing and Topology

7.7.2.2.3 DDR2 CK and ADDR_CTRL Routing

Figure 7-44 shows the topology of the routing for the CK and ADDR_CTRL net classes. The length of signal path AB and AC should be minimized with emphasis to minimize lengths C and D such that length A is the majority of the total length of signal path AB and AC.

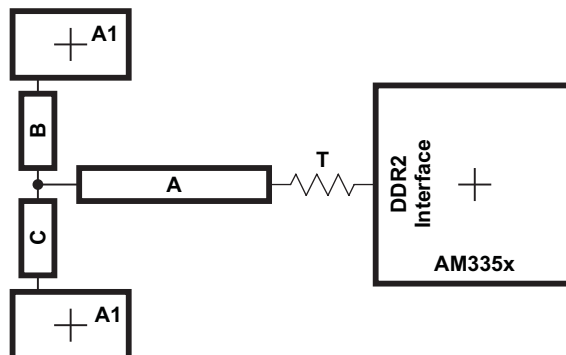


Figure 7-44. CK and ADDR_CTRL Routing and Topology

Table 7-54. CK and ADDR_CTRL Routing Specification⁽¹⁾⁽²⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|----------|-------|----------|------|
| 1 | Center-to-center CK spacing | | | 2w | |
| 2 | CK differential pair skew length mismatch ⁽²⁾⁽³⁾ | | | 25 | mils |
| 3 | CK B-to-CK C skew length mismatch | | | 25 | mils |
| 4 | Center-to-center CK to other DDR2 trace spacing ⁽⁴⁾ | 4w | | | |
| 5 | CK and ADDR_CTRL nominal trace length ⁽⁵⁾ | CACLM-50 | CACLM | CACLM+50 | mils |
| 6 | ADDR_CTRL-to-CK skew length mismatch | | | 100 | mils |
| 7 | ADDR_CTRL-to-ADDR_CTRL skew length mismatch | | | 100 | mils |
| 8 | Center-to-center ADDR_CTRL to other DDR2 trace spacing ⁽⁴⁾ | 4w | | | |
| 9 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing ⁽⁴⁾ | 3w | | | |
| 10 | ADDR_CTRL A-to-B and ADDR_CTRL A-to-C skew length mismatch ⁽²⁾ | | | 100 | mils |
| 11 | ADDR_CTRL B-to-C skew length mismatch | | | 100 | mils |

- (1) CK represents the clock net class, and ADDR_CTRL represents the address and control signal net class.
- (2) Series terminator, if used, should be located closest to the AM335x device.
- (3) Differential impedance should be $Z_o \times 2$, where Z_o is the single-ended impedance defined in Table 7-46.
- (4) Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
- (5) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

Figure 7-45 shows the topology and routing for the DQS[x] and DQ[x] net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

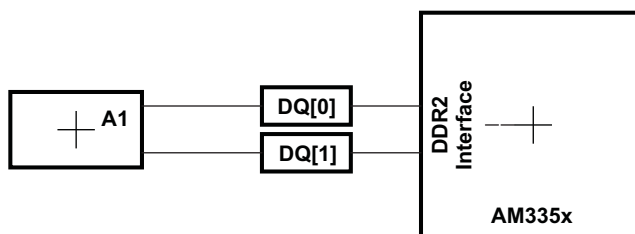


Figure 7-45. DQS[x] and DQ[x] Routing and Topology

Table 7-55. DQS[x] and DQ[x] Routing Specification⁽¹⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|---------|------|---------|------|
| 1 | Center-to-center DQS[x] spacing | | | 2w | |
| 2 | DQS[x] differential pair skew length mismatch ⁽²⁾ | | | 25 | mils |
| 3 | Center-to-center DDR_DQS[x] to other DDR2 trace spacing ⁽³⁾ | 4w | | | |
| 4 | DQS[x] and DQ[x] nominal trace length ⁽⁴⁾ | DQLM-50 | DQLM | DQLM+50 | mils |
| 5 | DQ[x]-to-DQS[x] skew length mismatch ⁽⁴⁾ | | | 100 | mils |
| 6 | DQ[x]-to-DQ[x] skew length mismatch ⁽⁴⁾ | | | 100 | mils |
| 7 | Center-to-center DQ[x] to other DDR2 trace spacing ⁽³⁾⁽⁵⁾ | 4w | | | |
| 8 | Center-to-center DQ[x] to other DQ[x] trace spacing ⁽³⁾⁽⁶⁾ | 3w | | | |

(1) DQS[x] represents the DQS0 and DQS1 clock net classes, and DQ[x] represents the DQ0 and DQ1 signal net classes.

(2) Differential impedance should be $Z_o \times 2$, where Z_o is the single-ended impedance defined in [Table 7-46](#).

(3) Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(4) There is no requirement for skew matching between data bytes; that is, from net classes DQS0 and DQ0 to net classes DQS1 and DQ1.

(5) Signals from one DQ net class should be considered other DDR2 traces to another DQ net class.

(6) DQLM is the longest Manhattan distance of each of the DQS[x] and DQ[x] net classes.

7.7.2.3 DDR3 and DDR3L Routing Guidelines

NOTE

All references to DDR3 in this section apply to DDR3 and DDR3L devices, unless otherwise noted.

7.7.2.3.1 Board Designs

TI only supports board designs using DDR3 memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3 memory interface are shown in [Table 7-56](#) and [Figure 7-46](#).

Table 7-56. Switching Characteristics for DDR3 Memory Interface

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---------------------------------------|-----|--------------------|------|
| 1 | $t_{c(DDR_CK)}$ $t_{c(DDR_CKn)}$ | 2.5 | 3.3 ⁽¹⁾ | ns |

(1) The JEDEC JESD79-3F Standard defines the maximum clock period of 3.3 ns for all standard-speed bin DDR3 and DDR3L memory devices. Therefore, all standard-speed bin DDR3 and DDR3L memory devices are required to operate at 303 MHz.

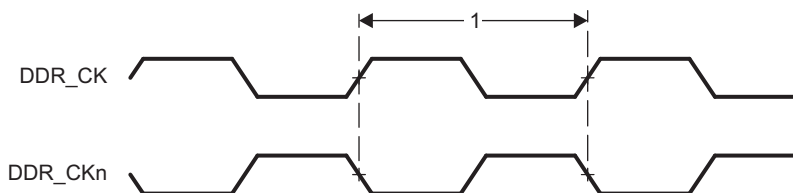


Figure 7-46. DDR3 Memory Interface Clock Timing

7.7.2.3.1.1 DDR3 versus DDR2

This specification only covers AM335x PCB designs that use DDR3 memory. Designs using DDR2 memory should use the DDR2 routing guidelines described in [Section 7.7.2.2](#). While similar, the two memory systems have different requirements. It is currently not possible to design one PCB that meets the requirements of both DDR2 and DDR3.

7.7.2.3.2 DDR3 Device Combinations

Because there are several possible combinations of device counts and single-side or dual-side mounting, [Table 7-57](#) summarizes the supported device configurations.

Table 7-57. Supported DDR3 Device Combinations

| NUMBER OF DDR3 DEVICES | DDR3 DEVICE WIDTH (BITS) | MIRRORED? | DDR3 EMIF WIDTH (BITS) |
|------------------------|--------------------------|------------------|------------------------|
| 1 | 16 | N | 16 |
| 2 | 8 | Y ⁽¹⁾ | 16 |

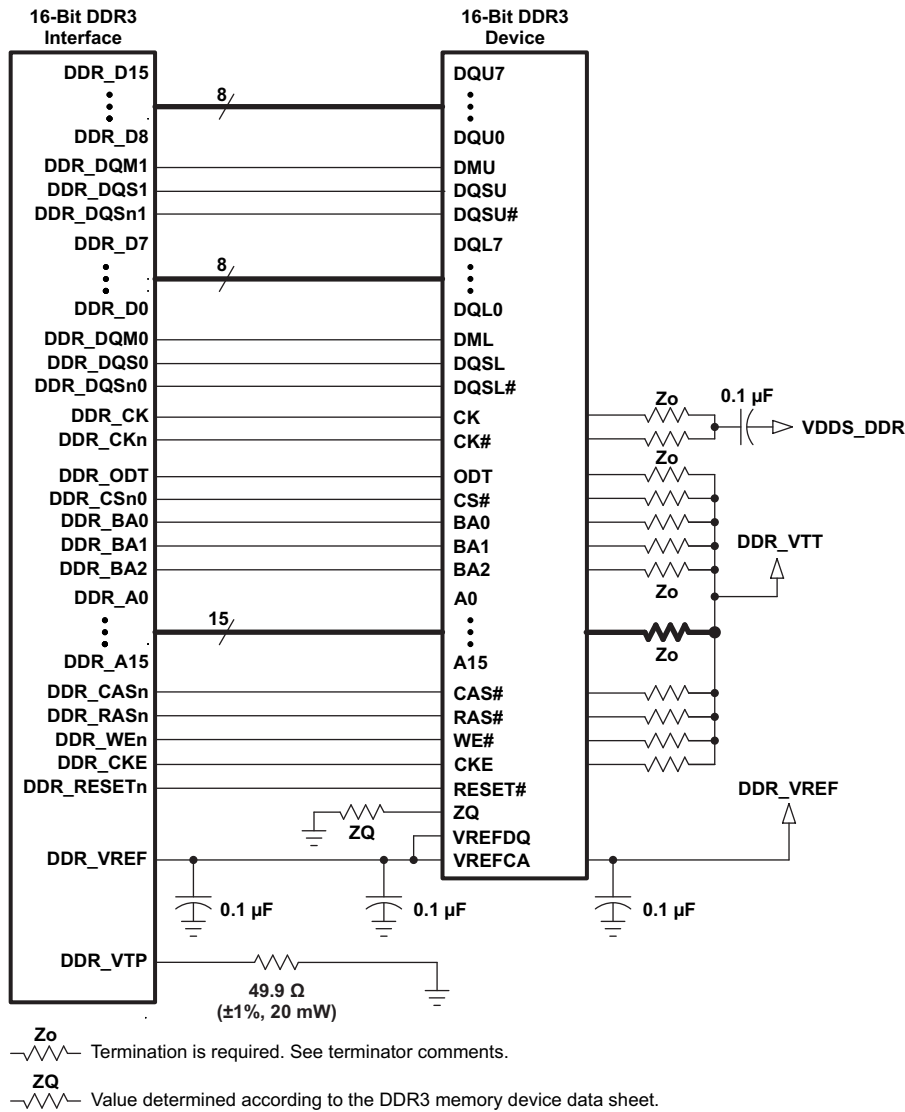
(1) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.

7.7.2.3.3 DDR3 Interface

This section provides the timing specification for the DDR3 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR3 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR3 specification, see [Understanding TI's PCB Routing Rule-Based DDR Timing Specification](#). This application report provides generic guidelines and approach. All the specifications provided in the data manual take precedence over the generic guidelines and must be adhered to for a reliable DDR3 interface operation.

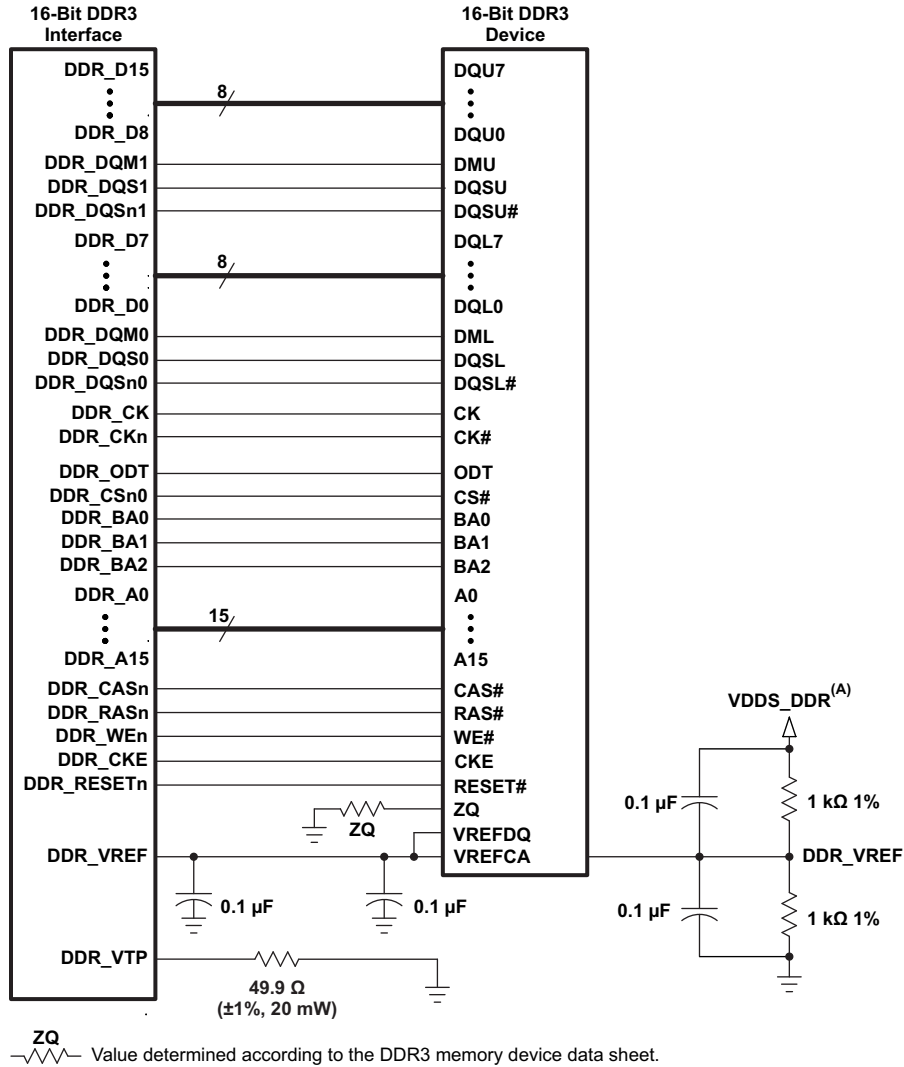
7.7.2.3.3.1 DDR3 Interface Schematic

The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used. Figure 7-47 shows the schematic connections for 16-bit interface on the AM335x device using one x16 DDR3 device and Figure 7-49 shows the schematic connections for 16-bit interface on the AM335x device using two x8 DDR3 devices. The AM335x DDR3 memory interface only supports 16-bit wide mode of operation. The AM335x device can only source one load connected to the DQS[x] and DQ[x] net class signals and two loads connected to the CK and ADDR_CTRL net class signals. For more information related to net classes, see Section 7.7.2.3.3.8.



Copyright © 2016, Texas Instruments Incorporated

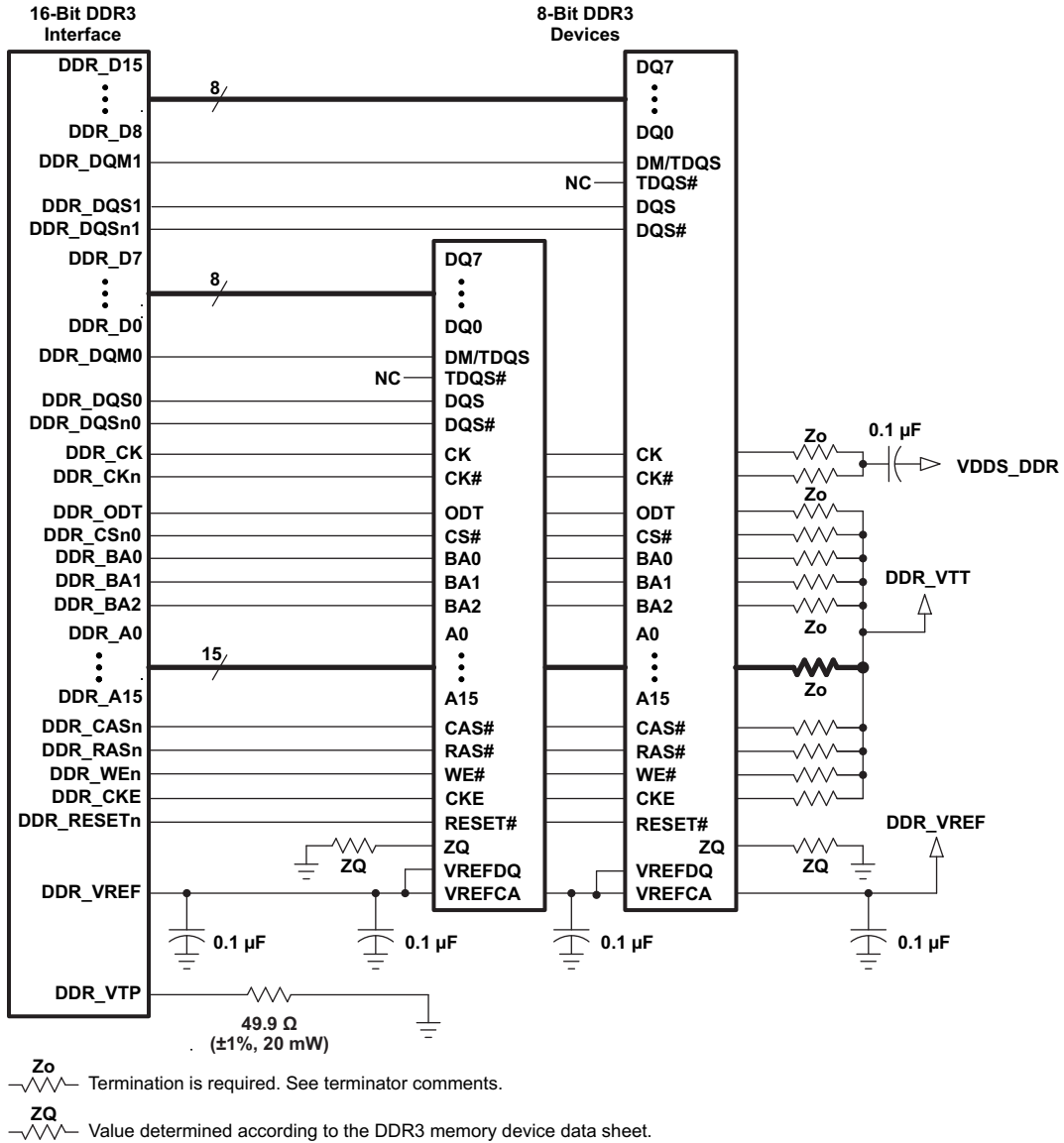
Figure 7-47. 16-Bit DDR3 Interface Using One 16-Bit DDR3 Device with V_{TT} Termination



Copyright © 2016, Texas Instruments Incorporated

A. VDDSDDR is the power supply for the DDR3 memories and the AM335x DDR3 interface.

Figure 7-48. 16-Bit DDR3 Interface Using One 16-Bit DDR3 Device without V_{TT} Termination



Copyright © 2016, Texas Instruments Incorporated

Figure 7-49. 16-Bit DDR3 Interface Using Two 8-Bit DDR3 Devices

7.7.2.3.3.2 Compatible JEDEC DDR3 Devices

Table 7-58 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface.

Table 7-58. Compatible JEDEC DDR3 Devices (Per Interface)

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|-----|--|--|-----------|-----|---------|
| 1 | JEDEC DDR3 device speed grade | $t_{C(DDR_CK)}$ and $t_{C(DDR_CKn)}$ = 3.3 ns | DDR3-800 | | |
| | | $t_{C(DDR_CK)}$ and $t_{C(DDR_CKn)}$ = 2.5 ns | DDR3-1600 | | |
| 2 | JEDEC DDR3 device bit width | | x8 | x16 | bits |
| 3 | JEDEC DDR3 device count ⁽¹⁾ | | 1 | 2 | devices |

(1) For valid DDR3 device configurations and device counts, see Section 7.7.2.3.3.1, Figure 7-47, and Figure 7-49.

7.7.2.3.3.3 PCB Stackup

The minimum stackup for routing the DDR3 interface is a four-layer stack up as shown in Table 7-59. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance signal integrity and electromagnetic interference performance, or to reduce the size of the PCB footprint.

Table 7-59. Minimum PCB Stackup⁽¹⁾

| LAYER | TYPE | DESCRIPTION |
|-------|--------|-----------------------|
| 1 | Signal | Top signal routing |
| 2 | Plane | Ground |
| 3 | Plane | Split Power Plane |
| 4 | Signal | Bottom signal routing |

(1) All signals that have critical signal integrity requirements should be routed first on layer 1. It may not be possible to route all of these signals on layer 1, therefore requiring routing of some signals on layer 4. When this is done, the signal routes on layer 4 must not cross splits in the power plane.

Table 7-60. PCB Stackup Specifications⁽¹⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|---|---------|-------|---------|----------|
| 1 | PCB routing and plane layers | 4 | | | |
| 2 | Signal routing layers | 2 | | | |
| 3 | Full ground reference layers under DDR3 routing region ⁽²⁾ | 1 | | | |
| 4 | Full VDDS_DDR power reference layers under the DDR3 routing region ⁽²⁾ | 1 | | | |
| 5 | Number of reference plane cuts allowed within DDR3 routing region ⁽³⁾ | | | 0 | |
| 6 | Number of layers between DDR3 routing layer and reference plane ⁽⁴⁾ | | | 0 | |
| 7 | PCB routing feature size | | 4 | | mils |
| 8 | PCB trace width, w | | 4 | | mils |
| 9 | PCB BGA escape via pad size ⁽⁵⁾ | | 18 | 20 | mils |
| 10 | PCB BGA escape via hole size | | 10 | | mils |
| 11 | Single-ended impedance, Z_0 ⁽⁶⁾ | | 50 | 75 | Ω |
| 12 | Impedance control ⁽⁷⁾⁽⁸⁾ | Z_0-5 | Z_0 | Z_0+5 | Ω |

(1) For the DDR3 device BGA pad size, see the DDR3 device manufacturer documentation.

(2) Ground reference layers are preferred over power reference layers. Be sure to include bypass capacitors to accommodate reference layer return current as the trace routes switch routing layers.

(3) No traces should cross reference plane cuts within the DDR3 routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(4) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(5) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.

(6) Z_0 is the nominal single-ended impedance selected for the PCB.

(7) This parameter specifies the AC characteristic impedance tolerance for each segment of a PCB signal trace relative to the chosen Z_0 defined by the single-ended impedance parameter.

(8) Tighter impedance control is required to ensure flight time skew is minimal.

7.7.2.3.3.4 Placement

Figure 7-50 shows the required placement for the AM335x device as well as the DDR3 devices. The dimensions for this figure are defined in Table 7-61. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space.

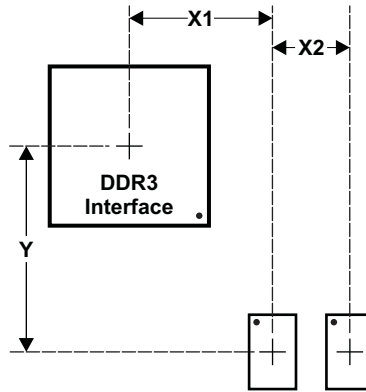


Figure 7-50. Placement Specifications

Table 7-61. Placement Specifications⁽¹⁾

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|------|------|
| 1 | X1 ⁽²⁾⁽³⁾⁽⁴⁾ | | 1000 | mils |
| 2 | X2 ⁽²⁾⁽³⁾ | | 600 | mils |
| 3 | Y Offset ⁽²⁾⁽³⁾⁽⁴⁾ | | 1500 | mils |
| 4 | Clearance from non-DDR3 signal to DDR3 keepout region ⁽⁵⁾⁽⁶⁾ | 4 | | w |

- (1) DDR3 keepout region to encompass entire DDR3 routing area.
- (2) For dimension definitions, see Figure 7-50.
- (3) Measurements from center of the AM335x device to center of the DDR3 device.
- (4) Minimizing X1 and Y improves timing margins.
- (5) w is defined as the signal trace width.
- (6) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.

7.7.2.3.3.5 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in Figure 7-51. This region should encompass all DDR3 circuitry and the region size varies with component placement and DDR3 routing. Additional clearances required for the keepout region are shown in Table 7-61. Non-DDR3 signals must not be routed on the same signal layer as DDR3 signals within the DDR3 keepout region. Non-DDR3 signals may be routed in the region provided they are routed on layers separated from DDR3 signal layers by a ground layer. No breaks should be allowed in the reference ground or VDDS_DDR power plane in this region. In addition, the VDDS_DDR power plane should cover the entire keepout region.

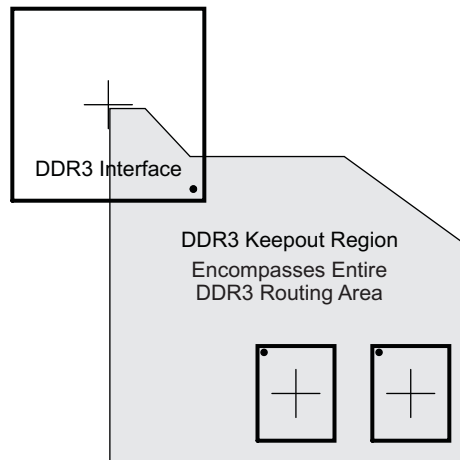


Figure 7-51. DDR3 Keepout Region

7.7.2.3.3.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. Table 7-62 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the AM335x DDR3 interface and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry.

Table 7-62. Bulk Bypass Capacitors⁽¹⁾

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|-----|-----|---------|
| 1 | AM335x VDDS_DDR bulk bypass capacitor count | 2 | | devices |
| 2 | AM335x VDDS_DDR bulk bypass total capacitance | 20 | | μF |
| 3 | DDR3 number 1 bulk bypass capacitor count | 2 | | devices |
| 4 | DDR3 number 1 bulk bypass total capacitance | 20 | | μF |
| 5 | DDR3 number 2 bulk bypass capacitor count ⁽²⁾ | 2 | | devices |
| 6 | DDR3 number 2 bulk bypass total capacitance ⁽²⁾ | 20 | | μF |

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

(2) Only used when two DDR3 devices are used.

7.7.2.3.3.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, the AM335x device DDR3 power, and the AM335x device DDR3 ground connections. [Table 7-63](#) contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

- Fit as many HS bypass capacitors as possible.
- Minimize the distance from the bypass capacitor to the power terminals being bypassed.
- Use the smallest physical sized capacitors possible with the highest capacitance readily available.
- Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
- Minimize via sharing. Note the limits on via sharing shown in [Table 7-63](#).

Table 7-63. High-Speed Bypass Capacitors

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|------|------|------|---------|
| 1 | HS bypass capacitor package size ⁽¹⁾ | | 0201 | 0402 | 10 mils |
| 2 | Distance, HS bypass capacitor to AM335x VDDSD_DDR and VSS terminal being bypassed ⁽²⁾⁽³⁾⁽⁴⁾ | | | 400 | mils |
| 3 | AM335x VDDSD_DDR HS bypass capacitor count | 20 | | | devices |
| 4 | AM335x VDDSD_DDR HS bypass capacitor total capacitance | 1 | | | μF |
| 5 | Trace length from AM335x VDDSD_DDR and VSS terminal to connection via ⁽²⁾ | | 35 | 70 | mils |
| 6 | Distance, HS bypass capacitor to DDR3 device being bypassed ⁽⁵⁾ | | | 150 | mils |
| 7 | DDR3 device HS bypass capacitor count ⁽⁶⁾ | 12 | | | devices |
| 8 | DDR3 device HS bypass capacitor total capacitance ⁽⁶⁾ | 0.85 | | | μF |
| 9 | Number of connection vias for each HS bypass capacitor ⁽⁷⁾⁽⁸⁾ | 2 | | | vias |
| 10 | Trace length from bypass capacitor connect to connection via ⁽²⁾⁽⁸⁾ | | 35 | 100 | mils |
| 11 | Number of connection vias for each DDR3 device power and ground terminal ⁽⁹⁾ | 1 | | | vias |
| 12 | Trace length from DDR3 device power and ground terminal to connection via ⁽²⁾⁽⁷⁾ | | 35 | 60 | mils |

(1) LxW, 10-mil units; for example, a 0402 is a 40x20-mil surface-mount capacitor.

(2) Closer and shorter is better.

(3) Measured from the nearest AM335x VDDSD_DDR and ground terminal to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the AM335x device, between the cluster of VDDSD_DDR and ground terminals, between the DDR3 interfaces on the package.

(5) Measured from the DDR3 device power and ground terminal to the center of the capacitor package.

(6) Per DDR3 device.

(7) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(8) An HS bypass capacitor may share a via with a DDR3 device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR3 device pad should be less than 150 mils.

(9) Up to two pairs of DDR3 power and ground terminals may share a via.

7.7.2.3.3.7.1 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Because these are returns for signal current, the signal via size may be used for these capacitors.

7.7.2.3.3.8 Net Classes

Table 7-64 lists the clock net classes for the DDR3 interface. Table 7-65 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

Table 7-64. Clock Net Class Definitions

| CLOCK NET CLASS | AM335x PIN NAMES |
|-----------------|------------------------|
| CK | DDR_CK and DDR_CKn |
| DQS0 | DDR_DQS0 and DDR_DQSn0 |
| DQS1 | DDR_DQS1 and DDR_DQSn1 |

Table 7-65. Signal Net Class Definitions

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | AM335x PIN NAMES |
|------------------|----------------------------|---|
| ADDR_CTRL | CK | DDR_BA[2:0], DDR_A[15:0], DDR_CSn0, DDR_CASn, DDR_RASn, DDR_WEn, DDR_CKE, DDR_ODT |
| DQ0 | DQS0 | DDR_D[7:0], DDR_DQM0 |
| DQ1 | DQS1 | DDR_D[15:8], DDR_DQM1 |

7.7.2.3.3.9 DDR3 Signal Termination

Signal terminations are required for the CK and ADDR_CTRL net class signals. On-device terminations (ODTs) are required on the DQS[x] and DQ[x] net class signals. Detailed termination specifications are covered in the routing rules in the following sections.

Figure 7-48 provides an example DDR3 schematic with a single 16-bit DDR3 memory device that does not have V_{TT} termination on the address and control signals. A typical DDR3 point-to-point topology may provide acceptable signal integrity without V_{TT} termination. System performance should be verified by performing signal integrity analysis using specific PCB design details before implementing this topology.

7.7.2.3.3.10 DDR_VREF Routing

DDR_VREF is used as a reference by the input buffers of the DDR3 memories as well as the AM335x device. DDR_VREF is intended to be half the DDR3 power supply voltage and is typically generated with a voltage divider connected to the VDDSD_DDR power supply. It should be routed as a nominal 20-mil wide trace with 0.1 μ F bypass capacitors near each device connection. Narrowing of DDR_VREF is allowed to accommodate routing congestion.

7.7.2.3.3.11 VTT

Like DDR_VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike DDR_VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

7.7.2.3.4 DDR3 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in Table 7-66.

7.7.2.3.4.1 Two DDR3 Devices

Two DDR3 devices are supported on the DDR3 interface consisting of two x8 DDR3 devices arranged as one 16-bit bank. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

7.7.2.3.4.1.1 CK and ADDR_CTRL Topologies, Two DDR3 Devices

Figure 7-52 shows the topology of the CK net classes and Figure 7-53 shows the topology for the corresponding ADDR_CTRL net classes.

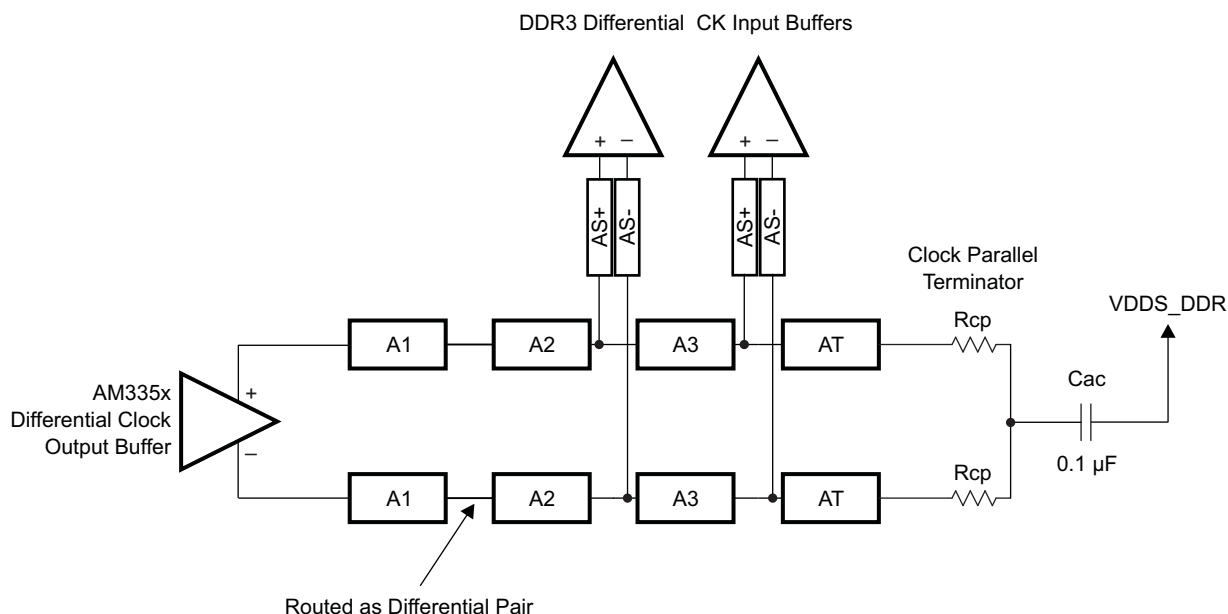


Figure 7-52. CK Topology for Two DDR3 Devices

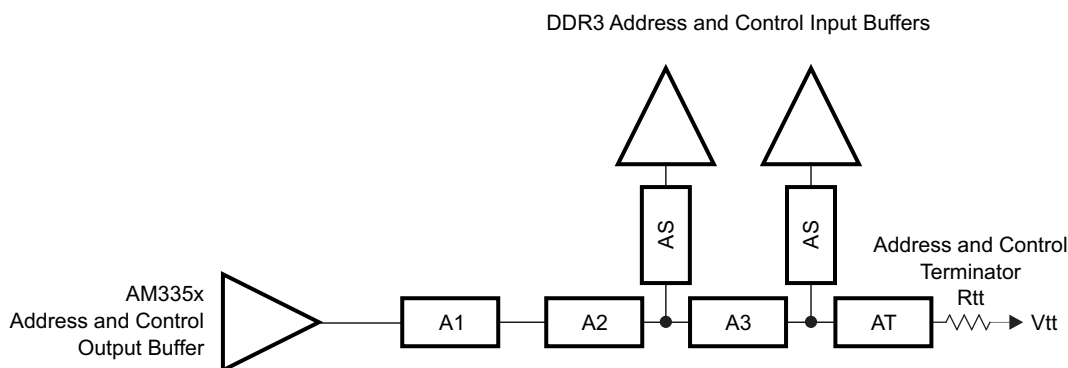


Figure 7-53. ADDR_CTRL Topology for Two DDR3 Devices

7.7.2.3.4.1.2 CK and ADDR_CTRL Routing, Two DDR3 Devices

Figure 7-54 shows the CK routing for two DDR3 devices placed on the same side of the PCB. Figure 7-55 shows the corresponding ADDR_CTRL routing.

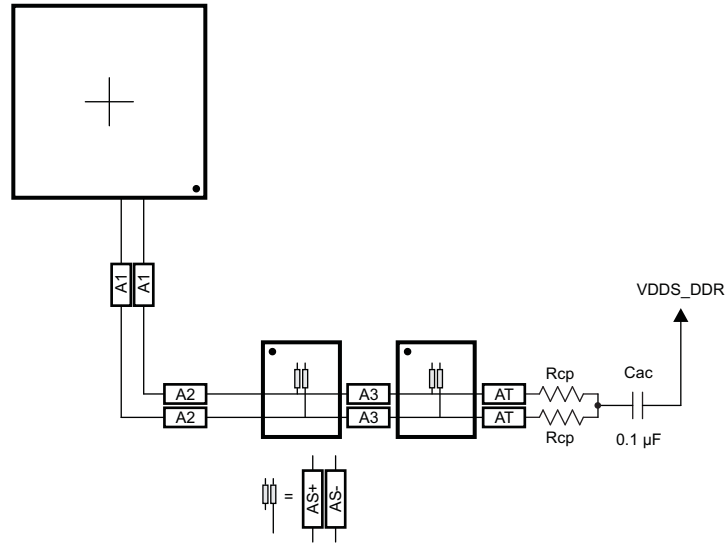


Figure 7-54. CK Routing for Two Single-Sided DDR3 Devices

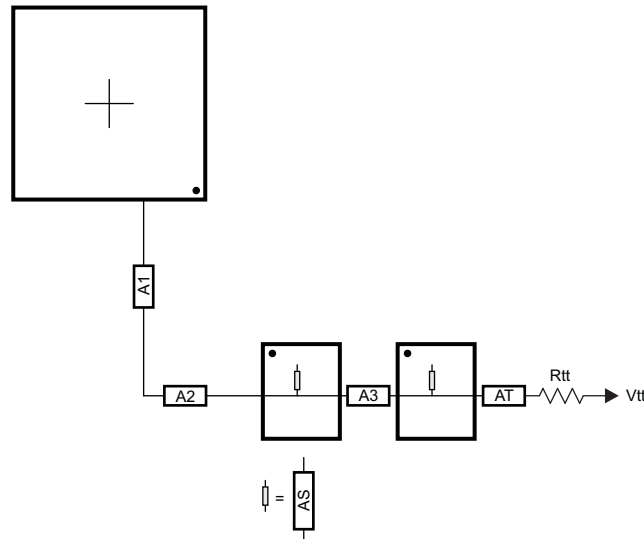


Figure 7-55. ADDR_CTRL Routing for Two Single-Sided DDR3 Devices

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. [Figure 7-56](#) and [Figure 7-57](#) show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.

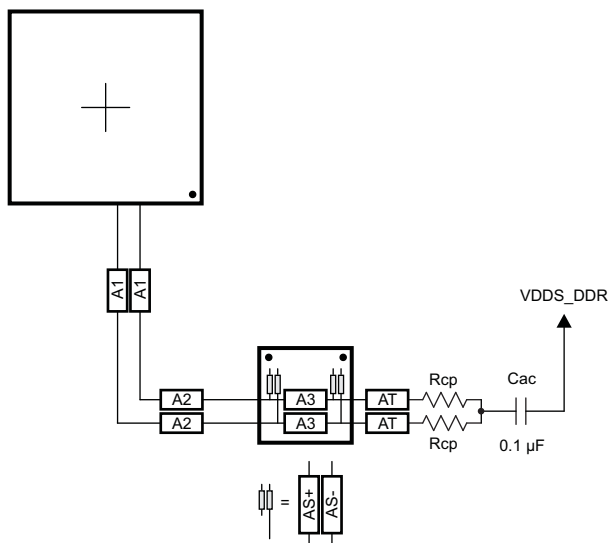


Figure 7-56. CK Routing for Two Mirrored DDR3 Devices

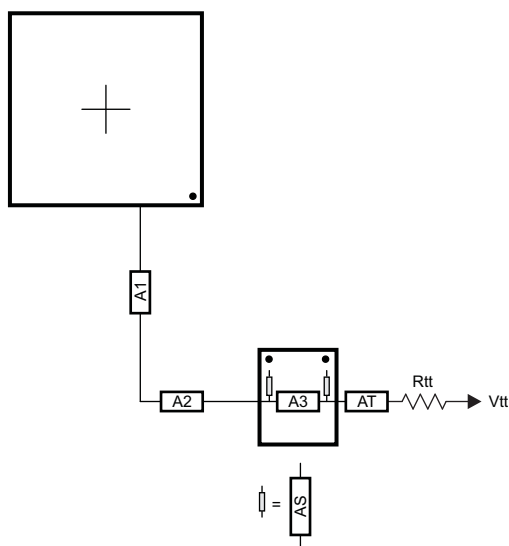


Figure 7-57. ADDR_CTRL Routing for Two Mirrored DDR3 Devices

7.7.2.3.4.2 One DDR3 Device

One DDR3 device is supported on the DDR3 interface consisting of one x16 DDR3 device arranged as one 16-bit bank.

7.7.2.3.4.2.1 CK and ADDR_CTRL Topologies, One DDR3 Device

Figure 7-58 shows the topology of the CK net classes and Figure 7-59 shows the topology for the corresponding ADDR_CTRL net classes.

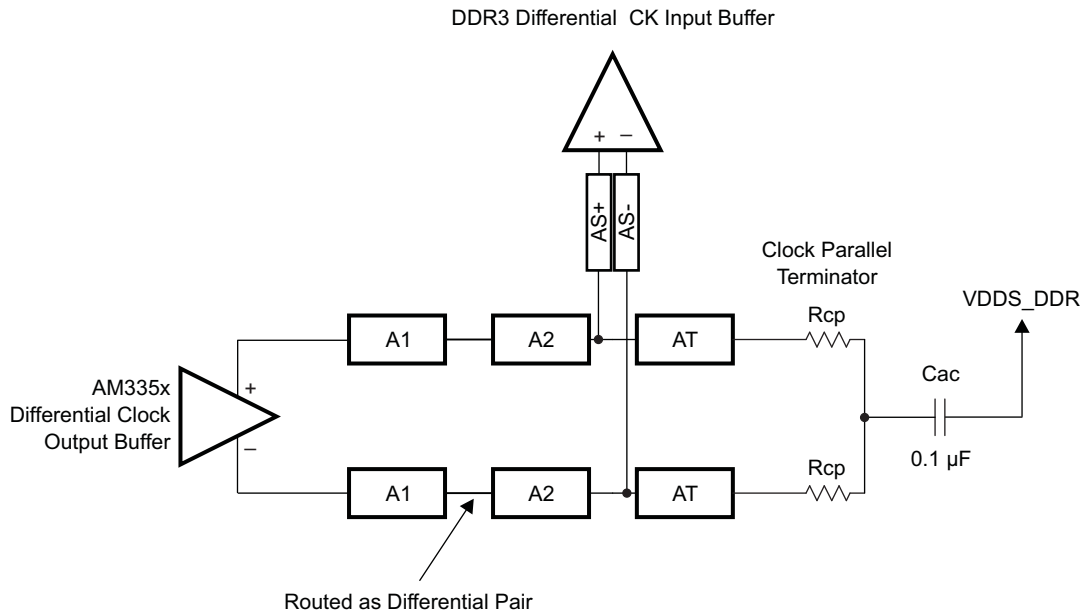


Figure 7-58. CK Topology for One DDR3 Device

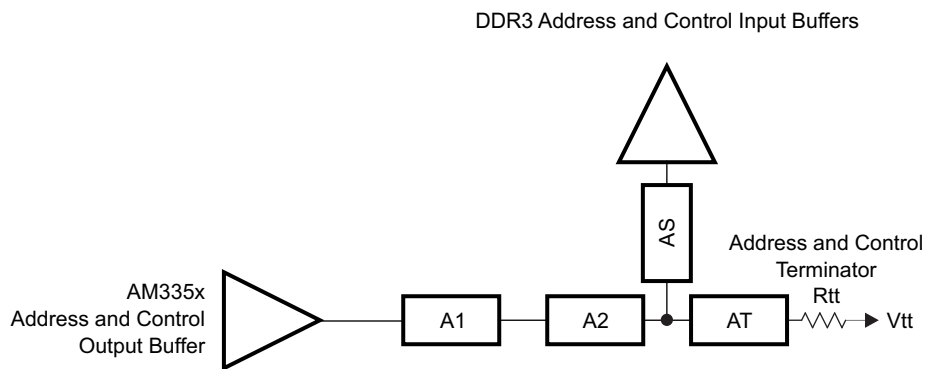


Figure 7-59. ADDR_CTRL Topology for One DDR3 Device

7.7.2.3.4.2 CK and ADDR_CTRL Routing, One DDR3 Device

Figure 7-60 shows the CK routing for one DDR3 device. Figure 7-61 shows the corresponding ADDR_CTRL routing.

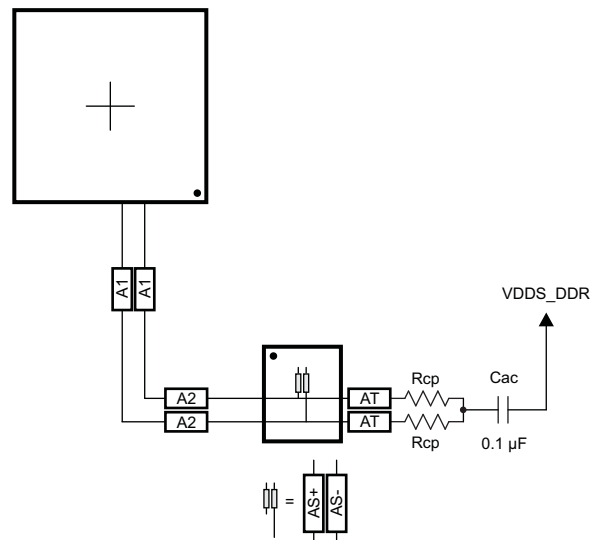


Figure 7-60. CK Routing for One DDR3 Device

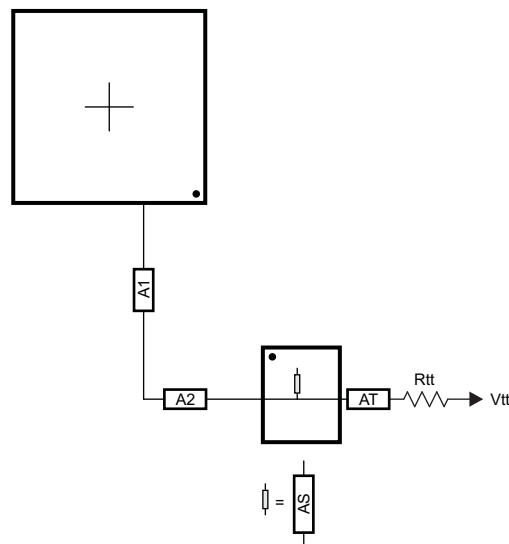


Figure 7-61. ADDR_CTRL Routing for One DDR3 Device

7.7.2.3.5 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

7.7.2.3.5.1 DQS[x] and DQ[x] Topologies, Any Number of Allowed DDR3 Devices

DQS[x] lines are point-to-point differential, and DQ[x] lines are point-to-point single-ended. Figure 7-62 and Figure 7-63 show these topologies.

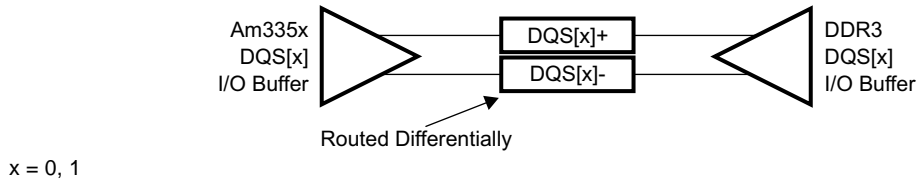


Figure 7-62. DQS[x] Topology

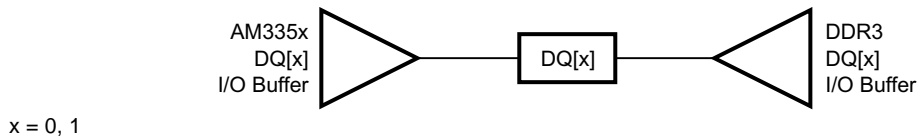


Figure 7-63. DQ[x] Topology

7.7.2.3.5.2 DQS[x] and DQ[x] Routing, Any Number of Allowed DDR3 Devices

Figure 7-64 and Figure 7-65 show the DQS[x] and DQ[x] routing.

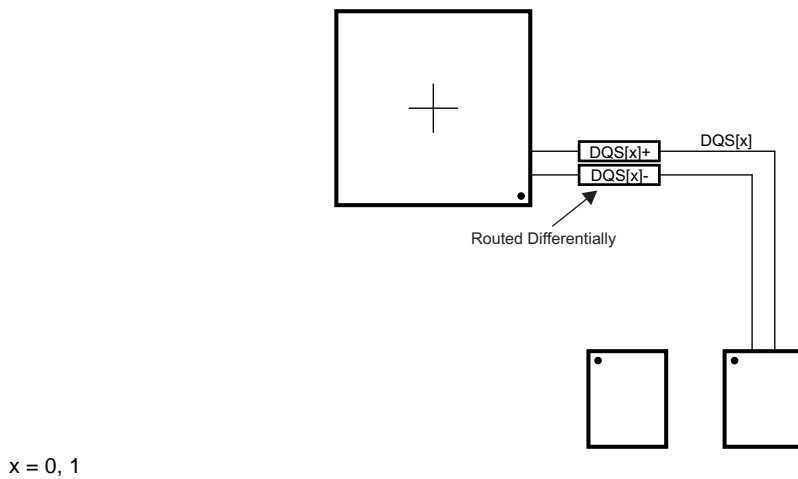


Figure 7-64. DQS[x] Routing With Any Number of Allowed DDR3 Devices

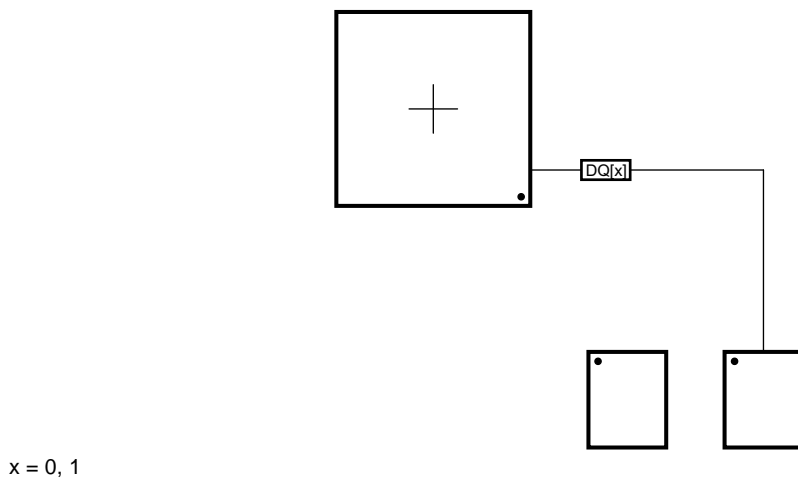


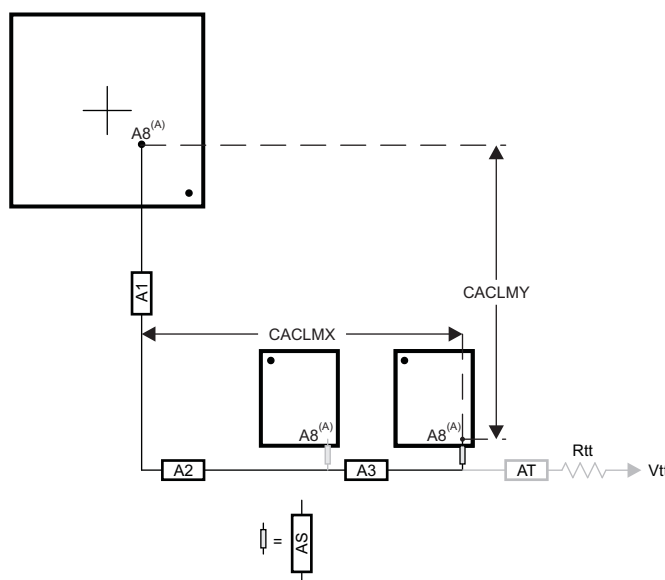
Figure 7-65. DQ[x] Routing With Any Number of Allowed DDR3 Devices

7.7.2.3.6 Routing Specification

7.7.2.3.6.1 CK and ADDR_CTRL Routing Specification

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the AM335x device and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 7-66 shows this distance for two loads. The specifications on the lengths of the transmission lines for the address bus are determined from this distance. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK and ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 7-66.



- A. It is very likely that the longest CK and ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK and ADDR_CTRL skew matching and length control.

The length of shorter CK and ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Nonincluded lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 7-66. CACLM for Two Address Loads on One Side of PCB

Table 7-66. CK and ADDR_CTRL Routing Specification⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|------------------------|-----|-----|------|------|
| 1 | A1 + A2 length | | | 2500 | mils |
| 2 | A1 + A2 skew | | | 25 | mils |
| 3 | A3 length | | | 660 | mils |
| 4 | A3 skew ⁽⁴⁾ | | | 25 | mils |
| 5 | A3 skew ⁽⁵⁾ | | | 125 | mils |
| 6 | AS length | | | 100 | mils |

Table 7-66. CK and ADDR_CTRL Routing Specification⁽¹⁾⁽²⁾⁽³⁾ (continued)

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|---|-------------------|----------------|-------------------|------|
| 7 | AS skew | | | 25 | mils |
| 8 | AS+ and AS– length | | | 70 | mils |
| 9 | AS+ and AS– skew | | | 5 | mils |
| 10 | AT length ⁽⁶⁾ | | 500 | | mils |
| 11 | AT skew ⁽⁷⁾ | | 100 | | mils |
| 12 | AT skew ⁽⁸⁾ | | | 5 | mils |
| 13 | CK and ADDR_CTRL nominal trace length ⁽⁹⁾ | CACLM-50 | CACLM | CACLM+50 | mils |
| 14 | Center-to-center CK to other DDR3 trace spacing ⁽¹⁰⁾ | 4w | | | |
| 15 | Center-to-center ADDR_CTRL to other DDR3 trace spacing ⁽¹⁰⁾⁽¹¹⁾ | 4w | | | |
| 16 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing ⁽¹⁰⁾ | 3w | | | |
| 17 | CK center-to-center spacing ⁽¹²⁾ | | | | |
| 18 | CK spacing to other net ⁽¹⁰⁾ | 4w | | | |
| 19 | Rcp ⁽¹³⁾ | Z _o -1 | Z _o | Z _o +1 | Ω |
| 20 | Rtt ⁽¹³⁾⁽¹⁴⁾ | Z _o -5 | Z _o | Z _o +5 | Ω |

(1) CK represents the clock net class, and ADDR_CTRL represents the address and control signal net class.

(2) The use of vias should be minimized.

(3) Additional bypass capacitors are required when using the VDDS_DDR plane as the reference plane to allow the return current to jump between the VDDS_DDR plane and the ground plane when the net class switches layers at a via.

(4) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).

(5) Nonmirrored configuration (all DDR3 memories on same side of PCB).

(6) While this length can be increased for convenience, its length should be minimized.

(7) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.

(8) CK net class only.

(9) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes + 300 mils. For definition, see [Section 7.7.2.3.6.1](#) and [Figure 7-66](#).

(10) Center-to-center spacing is allowed to fall to minimum (w) for up to 1250 mils of routed length.

(11) Signals from one DQ net class should be considered other DDR3 traces to another DQ net class.

(12) CK spacing set to ensure proper differential impedance. Differential impedance should be Z_o x 2, where Z_o is the single-ended impedance defined in [Table 7-60](#).

(13) Source termination (series resistor at driver) is specifically not allowed.

(14) Termination values should be uniform across the net class.

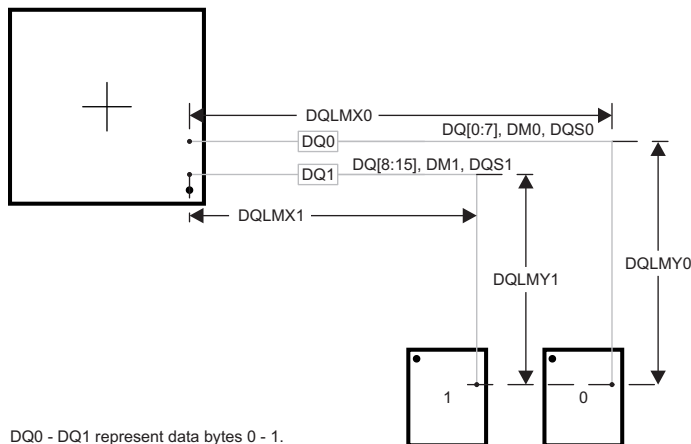
7.7.2.3.6.2 DQS[x] and DQ[x] Routing Specification

Skew within the DQS[x] and DQ[x] net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. DQLM_n is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

NOTE

Matching the lengths across all bytes is not required, nor is it recommended. Length matching is only required within each byte.

Given the DQS[x] and DQ[x] pin locations on the AM335x device and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. [Figure 7-67](#) shows this distance for a two-load case. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS[x] and DQ[x] routing, these specifications are contained in [Table 7-67](#).



DQ0 - DQ1 represent data bytes 0 - 1.

There are two DQLMs, one for each byte (16-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:

$$DQLM0 = DQLMX0 + DQLMY0$$

$$DQLM1 = DQLMX1 + DQLMY1$$

Figure 7-67. DQLM for Any Number of Allowed DDR3 Devices

Table 7-67. DQS[x] and DQ[x] Routing Specification⁽¹⁾⁽²⁾

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|-----|-----|-------|------|
| 1 | DQ0 nominal length ⁽³⁾⁽⁴⁾ | | | DQLM0 | mils |
| 2 | DQ1 nominal length ⁽³⁾⁽⁵⁾ | | | DQLM1 | mils |
| 3 | DQ[x] skew ⁽⁶⁾ | | | 25 | mils |
| 4 | DQS[x] skew | | | 5 | mils |
| 5 | DQS[x]-to-DQ[x] skew ⁽⁶⁾⁽⁷⁾ | | | 25 | mils |
| 6 | Center-to-center DQ[x] to other DDR3 trace spacing ⁽⁸⁾⁽⁹⁾ | 4w | | | |
| 7 | Center-to-center DQ[x] to other DQ[x] trace spacing ⁽⁸⁾⁽¹⁰⁾ | 3w | | | |
| 8 | DQS[x] center-to-center spacing ⁽¹¹⁾ | | | | |
| 9 | DQS[x] center-to-center spacing to other net ⁽⁸⁾ | 4w | | | |

- (1) DQS[x] represents the DQS0 and DQS1 clock net classes, and DQ[x] represents the DQ0 and DQ1 signal net classes.
- (2) External termination disallowed. Data termination should use built-in ODT functionality.
- (3) DQLMn is the longest Manhattan distance of a byte. For definition, see [Section 7.7.2.3.6.2](#) and [Figure 7-67](#).
- (4) DQLM0 is the longest Manhattan length for the DQ0 net class.
- (5) DQLM1 is the longest Manhattan length for the DQ1 net class.
- (6) Length matching is only done within a byte. Length matching across bytes is not required.
- (7) Each DQS clock net class is length matched to its associated DQ signal net class.
- (8) Center-to-center spacing is allowed to fall to minimum for up to 1250 mils of routed length.
- (9) Other DDR3 trace spacing means signals that are not part of the same DQ[x] signal net class.
- (10) This applies to spacing within same DQ[x] signal net class.
- (11) DQS[x] pair spacing is set to ensure proper differential impedance. Differential impedance should be $Z_o \times 2$, where Z_o is the single-ended impedance defined in [Table 7-60](#).

7.8 I²C

For more information, see the Inter-Integrated Circuit (I²C) section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

7.8.1 I²C Electrical Data and Timing

Table 7-68. I²C Timing Conditions – Slave Mode

| PARAMETER | | STANDARD MODE | | FAST MODE | | UNIT |
|-------------------------|-----------------------------------|---------------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| Output Condition | | | | | | |
| C _b | Capacitive load for each bus line | | 400 | | 400 | pF |

Table 7-69. Timing Requirements for I²C Input Timings

(see [Figure 7-68](#))

| NO. | | | STANDARD MODE | | FAST MODE | | UNIT |
|-----|----------------------------|---|------------------|---------------------|--------------------|--------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | t _{c(SCL)} | Cycle time, SCL | 10 | | 2.5 | | μs |
| 2 | t _{su(SCLH-SDAL)} | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μs |
| 3 | t _{h(SDAL-SCLL)} | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | μs |
| 4 | t _{w(SCLL)} | Pulse duration, SCL low | 4.7 | | 1.3 | | μs |
| 5 | t _{w(SCLH)} | Pulse duration, SCL high | 4 | | 0.6 | | μs |
| 6 | t _{su(SDAV-SCLH)} | Setup time, SDA valid before SCL high | 250 | | 100 ⁽¹⁾ | | ns |
| 7 | t _{h(SCLL-SDAV)} | Hold time, SDA valid after SCL low | 0 ⁽²⁾ | 3.45 ⁽³⁾ | 0 ⁽²⁾ | 0.9 ⁽³⁾ | μs |
| 8 | t _{w(SDAH)} | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μs |
| 9 | t _{r(SDA)} | Rise time, SDA | | 1000 | | 300 | ns |
| 10 | t _{r(SCL)} | Rise time, SCL | | 1000 | | 300 | ns |
| 11 | t _{f(SDA)} | Fall time, SDA | | 300 | | 300 | ns |
| 12 | t _{f(SCL)} | Fall time, SCL | | 300 | | 300 | ns |
| 13 | t _{su(SCLH-SDAH)} | Setup time, high before SDA high (for STOP condition) | 4 | | 0.6 | | μs |
| 14 | t _{w(SP)} | Pulse duration, spike (must be suppressed) | 0 | 50 | 0 | 50 | ns |

(1) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement t_{su(SDA-SCLH)} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device stretches the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{r max} + t_{su(SDA-SCLH)} = 1000 + 250 = 1250 ns (according to the standard-mode I²C-Bus Specification) before the SCL line is released.

(2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

(3) The maximum t_{h(SDA-SCLL)} has only to be met if the device does not stretch the low period [t_{w(SCLL)}] of the SCL signal.

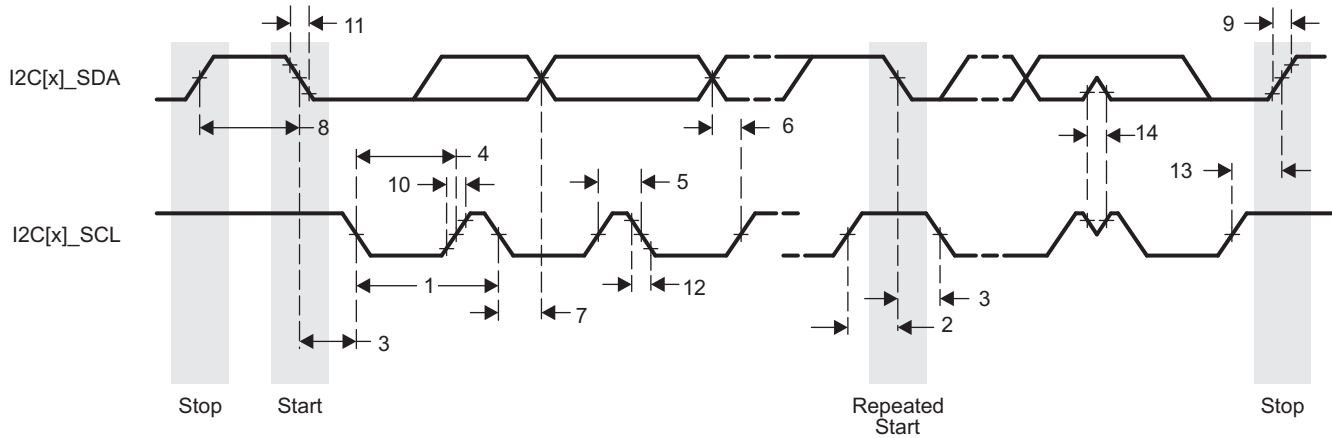


Figure 7-68. I²C Receive Timing

Table 7-70. Switching Characteristics for I²C Output Timings

(see [Figure 7-69](#))

| NO. | PARAMETER | | STANDARD MODE | | FAST MODE | | UNIT |
|-----|---------------------|---|---------------|------|-----------|-----|---------|
| | | | MIN | MAX | MIN | MAX | |
| 15 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | μ s |
| 16 | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μ s |
| 17 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | μ s |
| 18 | $t_w(SCLL)$ | Pulse duration, SCL low | 4.7 | | 1.3 | | μ s |
| 19 | $t_w(SCLH)$ | Pulse duration, SCL high | 4 | | 0.6 | | μ s |
| 20 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| 21 | $t_{h(SCLL-SDAV)}$ | Hold time, SDA valid after SCL low | 0 | 3.45 | 0 | 0.9 | μ s |
| 22 | $t_w(SDAH)$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μ s |
| 23 | $t_r(SDA)$ | Rise time, SDA | | 1000 | | 300 | ns |
| 24 | $t_r(SCL)$ | Rise time, SCL | | 1000 | | 300 | ns |
| 25 | $t_f(SDA)$ | Fall time, SDA | | 300 | | 300 | ns |
| 26 | $t_f(SCL)$ | Fall time, SCL | | 300 | | 300 | ns |
| 27 | $t_{su(SCLH-SDAH)}$ | Setup time, high before SDA high (for STOP condition) | 4 | | 0.6 | | μ s |

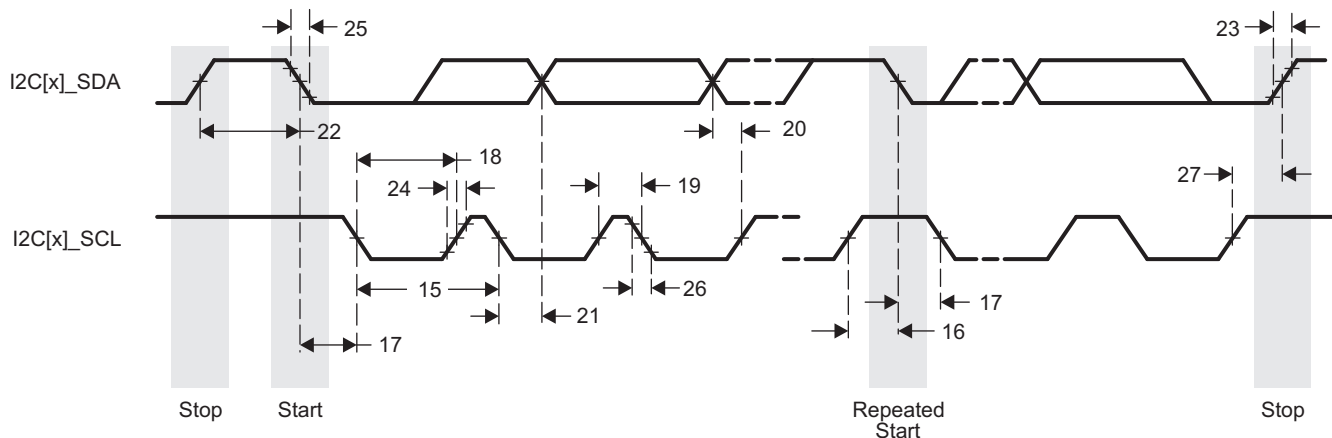


Figure 7-69. I²C Transmit Timing

7.9 JTAG Electrical Data and Timing

Table 7-71. Timing Requirements for JTAG

(see Figure 7-70)

| NO. | | | OPP100 | | OPP50 | | UNIT |
|-----|---------------------------|--|--------|-----|-------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_c(\text{TCK})$ | Cycle time, TCK | 81.5 | | 104.5 | | ns |
| 1a | $t_w(\text{TCKH})$ | Pulse duration, TCK high (40% of t_c) | 32.6 | | 41.8 | | ns |
| 1b | $t_w(\text{TCKL})$ | Pulse duration, TCK low (40% of t_c) | 32.6 | | 41.8 | | ns |
| 3 | $t_{su}(\text{TDI-TCKH})$ | Input setup time, TDI valid to TCK high | 3 | | 3 | | ns |
| | $t_{su}(\text{TMS-TCKH})$ | Input setup time, TMS valid to TCK high | 3 | | 3 | | ns |
| 4 | $t_h(\text{TCKH-TDI})$ | Input hold time, TDI valid from TCK high | 8.05 | | 8.05 | | ns |
| | $t_h(\text{TCKH-TMS})$ | Input hold time, TMS valid from TCK high | 8.05 | | 8.05 | | ns |

Table 7-72. Switching Characteristics for JTAG

(see Figure 7-70)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|------------------------|----------------------------------|--------|------|-------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| 2 | $t_d(\text{TCKL-TDO})$ | Delay time, TCK low to TDO valid | 3 | 27.6 | 4 | 36.8 | ns |

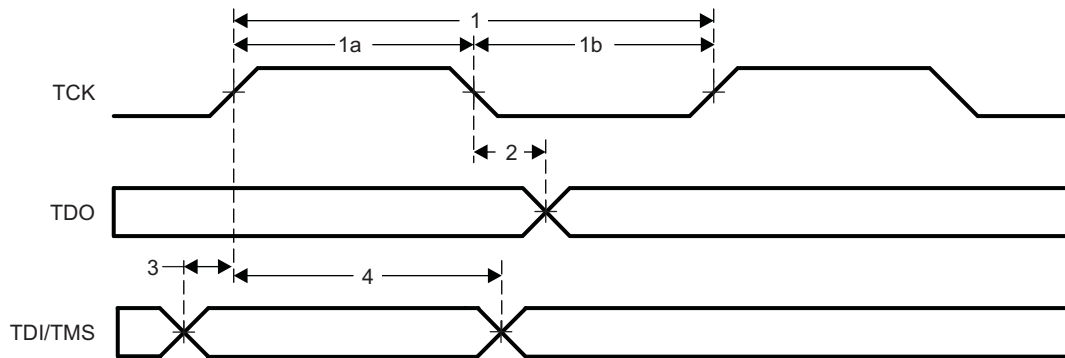


Figure 7-70. JTAG Timing

7.10 LCD Controller (LCDC)

The LCDC consists of two independent controllers, the raster controller and the LCD interface display driver (LIDD) controller. Each controller operates independently from the other and only one of them is active at any given time.

- The raster controller handles the synchronous LCD interface. It provides timing and data for constant graphics refresh to a passive display. It supports a wide variety of monochrome and full-color display types and sizes by use of programmable timing controls, a built-in palette, and a gray-scale and serializer. Graphics data is processed and stored in frame buffers. A frame buffer is a contiguous memory block in the system. A built-in DMA engine supplies the graphics data to the raster engine which, in turn, outputs to the external LCD device.
- The LIDD controller supports the asynchronous LCD interface. It provides full-timing programmability of control signals (CS, WE, OE, ALE) and output data.

The maximum resolution for the LCD controller is 2048 × 2048 pixels. The maximum frame rate is determined by the image size in combination with the pixel clock rate.

Table 7-73. LCD Controller Timing Conditions

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|-------------|-----|-----|-----|------|
| Output Condition | | | | | | |
| C _{LOAD} | Output load capacitance | LIDD mode | 5 | | 60 | pF |
| | | Raster mode | 3 | | 30 | |

7.10.1 LCD Interface Display Driver (LIDD Mode)

Table 7-74. Timing Requirements for LCD LIDD Mode

(see [Figure 7-72](#) through [Figure 7-80](#))

| NO. | PARAMETER | DESCRIPTION | OPP100 | | UNIT |
|-----|---|---|--------|-----|------|
| | | | MIN | MAX | |
| 16 | t _{su} (LCD_DATA-LCD_MEMORY_CLK) | Setup time, LCD_DATA[15:0] valid before LCD_MEMORY_CLK high | 18 | | ns |
| 17 | t _h (LCD_MEMORY_CLK-LCD_DATA) | Hold time, LCD_DATA[15:0] valid after LCD_MEMORY_CLK high | 0 | | ns |
| 18 | t _t (LCD_DATA) | Transition time, LCD_DATA[15:0] | 1 | 3 | ns |

Table 7-75. Switching Characteristics for LCD LIDD Mode

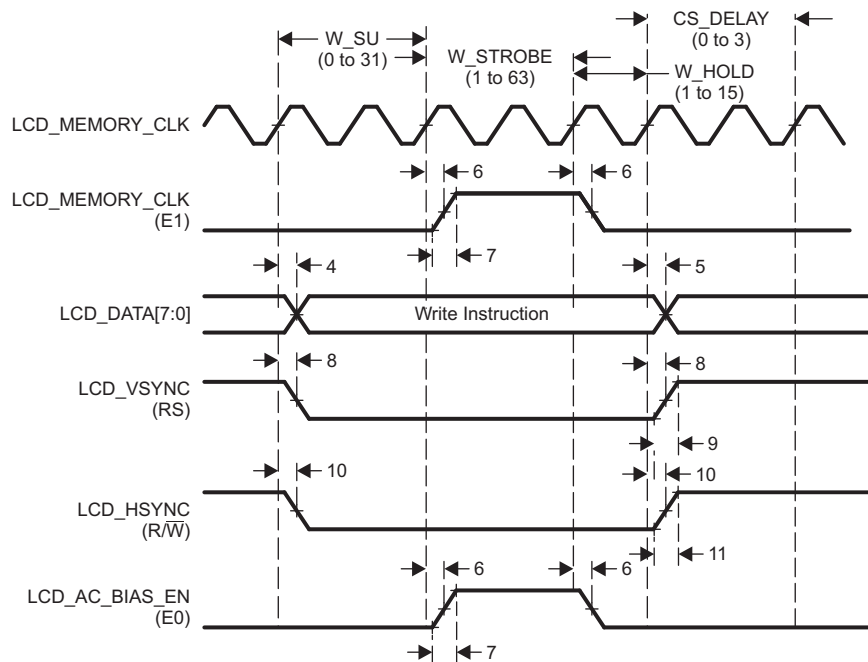
(see [Figure 7-72](#) through [Figure 7-80](#))

| NO. | PARAMETER | DESCRIPTION | OPP100 | | UNIT |
|-----|--|---|--------------------|--------------------|------|
| | | | MIN | MAX | |
| 1 | t _c (LCD_MEMORY_CLK) | Cycle time, LCD_MEMORY_CLK | 23.7 | | ns |
| 2 | t _w (LCD_MEMORY_CLKH) | Pulse duration, LCD_MEMORY_CLK high | 0.45t _c | 0.55t _c | ns |
| 3 | t _w (LCD_MEMORY_CLKL) | Pulse duration, LCD_MEMORY_CLK low | 0.45t _c | 0.55t _c | ns |
| 4 | t _d (LCD_MEMORY_CLK-LCD_DATAV) | Delay time, LCD_MEMORY_CLK high to LCD_DATA[15:0] valid (write) | | 7 | ns |
| 5 | t _d (LCD_MEMORY_CLK-LCD_DATAI) | Delay time, LCD_MEMORY_CLK high to LCD_DATA[15:0] invalid (write) | 0 | | ns |
| 6 | t _d (LCD_MEMORY_CLK-LCD_AC_BIAS_EN) | Delay time, LCD_MEMORY_CLK high to LCD_AC_BIAS_EN | 0 | 6.8 | ns |
| 7 | t _t (LCD_AC_BIAS_EN) | Transition time, LCD_AC_BIAS_EN | 1 | 10 | ns |
| 8 | t _d (LCD_MEMORY_CLK-LCD_VSYNC) | Delay time, LCD_MEMORY_CLK high to LCD_VSYNC | 0 | 7 | ns |
| 9 | t _t (LCD_VSYNC) | Transition time, LCD_VSYNC | 1 | 10 | ns |
| 10 | t _d (LCD_MEMORY_CLK-LCD_HSYNC) | Delay time, LCD_MEMORY_CLK high to LCD_HSYNC | 0 | 7 | ns |

Table 7-75. Switching Characteristics for LCD LIDD Mode (continued)

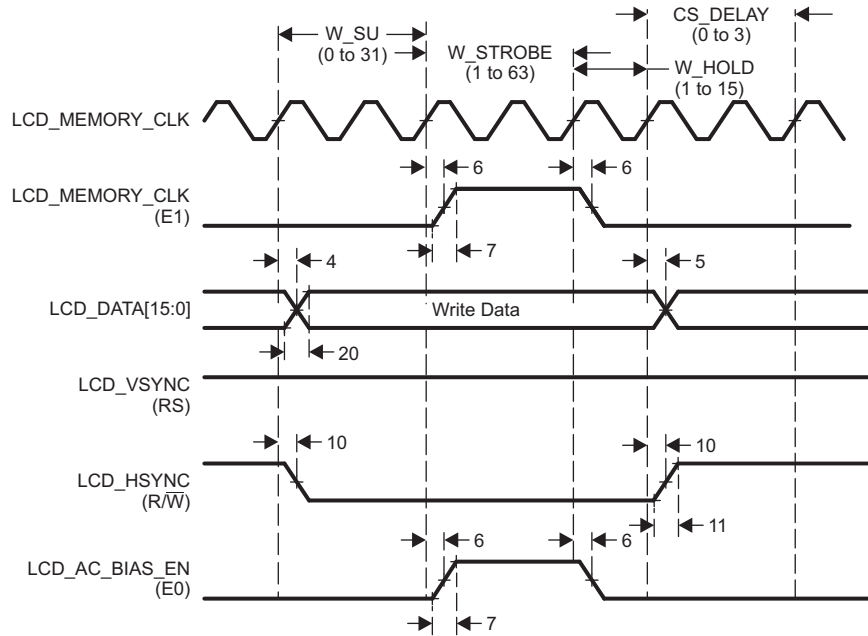
(see [Figure 7-72](#) through [Figure 7-80](#))

| NO. | PARAMETER | OPP100 | | UNIT |
|-----|--------------------------------------|--------|-----|------|
| | | MIN | MAX | |
| 11 | $t_{f(LCD_HSYNC)}$ | 1 | 10 | ns |
| 12 | $t_{d(LCD_MEMORY_CLK-LCD_PCLK)}$ | 0 | 7 | ns |
| 13 | $t_{f(LCD_PCLK)}$ | 1 | 10 | ns |
| 14 | $t_{d(LCD_MEMORY_CLK-LCD_DATAZ)}$ | 0 | 7 | ns |
| 15 | $t_{d(LCD_MEMORY_CLK-LCD_DATA)}$ | 0 | 7 | ns |
| 19 | $t_{f(LCD_MEMORY_CLK)}$ | 1 | 2.5 | ns |
| 20 | $t_{f(LCD_DATA)}$ | 1 | 10 | ns |



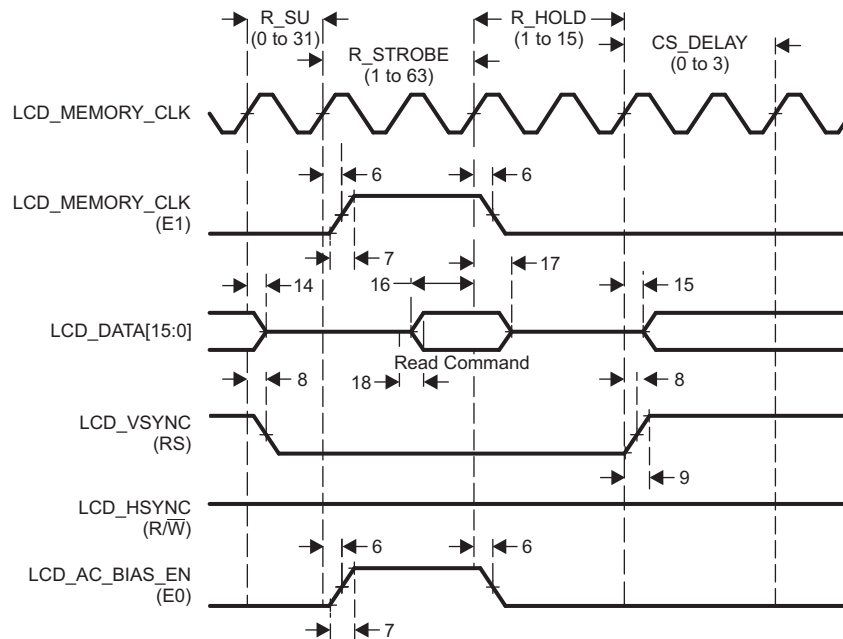
- A. Hitachi mode performs asynchronous operations that do not require an external LCD_MEMORY_CLK. The first LCD_MEMORY_CLK waveform is only shown as a reference of the internal clock that sequences the other signals. The second LCD_MEMORY_CLK waveform is shown as E1 because the LCD_MEMORY_CLK signal is used to implement the E1 function in Hitachi mode.

Figure 7-71. Command Write in Hitachi Mode



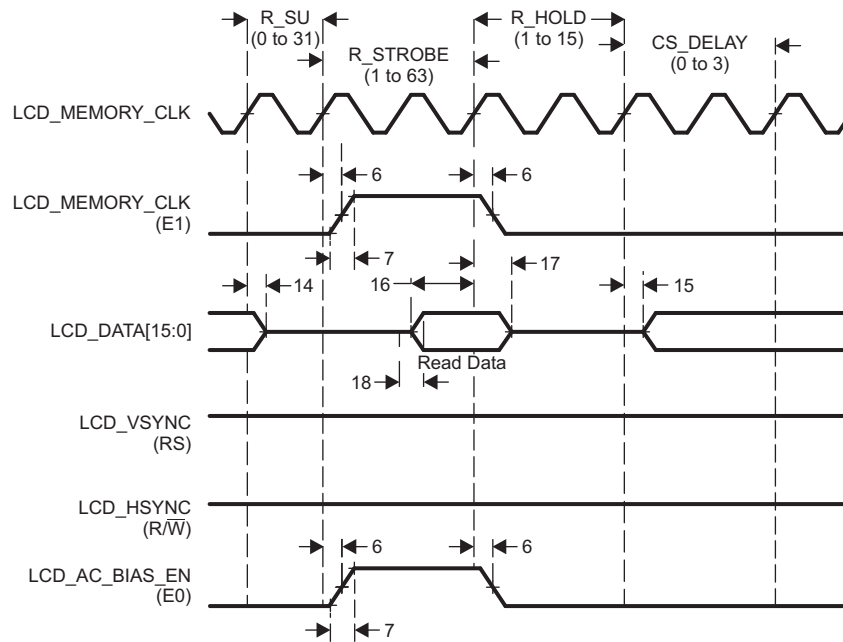
- A. Hitachi mode performs asynchronous operations that do not require an external LCD_MEMORY_CLK. The first LCD_MEMORY_CLK waveform is only shown as a reference of the internal clock that sequences the other signals. The second LCD_MEMORY_CLK waveform is shown as E1 because the LCD_MEMORY_CLK signal is used to implement the E1 function in Hitachi mode.

Figure 7-72. Data Write in Hitachi Mode



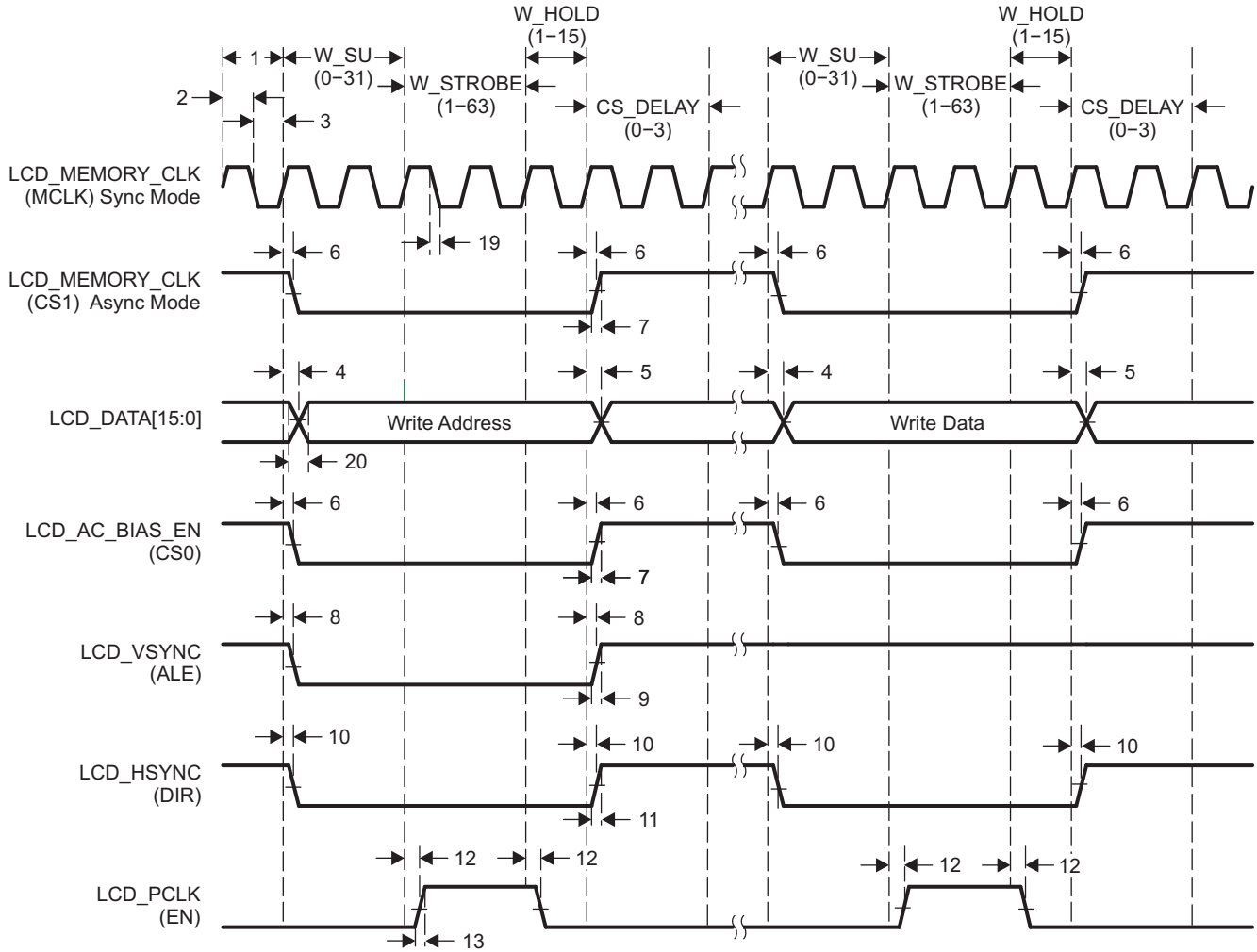
- A. Hitachi mode performs asynchronous operations that do not require an external LCD_MEMORY_CLK. The first LCD_MEMORY_CLK waveform is only shown as a reference of the internal clock that sequences the other signals. The second LCD_MEMORY_CLK waveform is shown as E1 because the LCD_MEMORY_CLK signal is used to implement the E1 function in Hitachi mode.

Figure 7-73. Command Read in Hitachi Mode



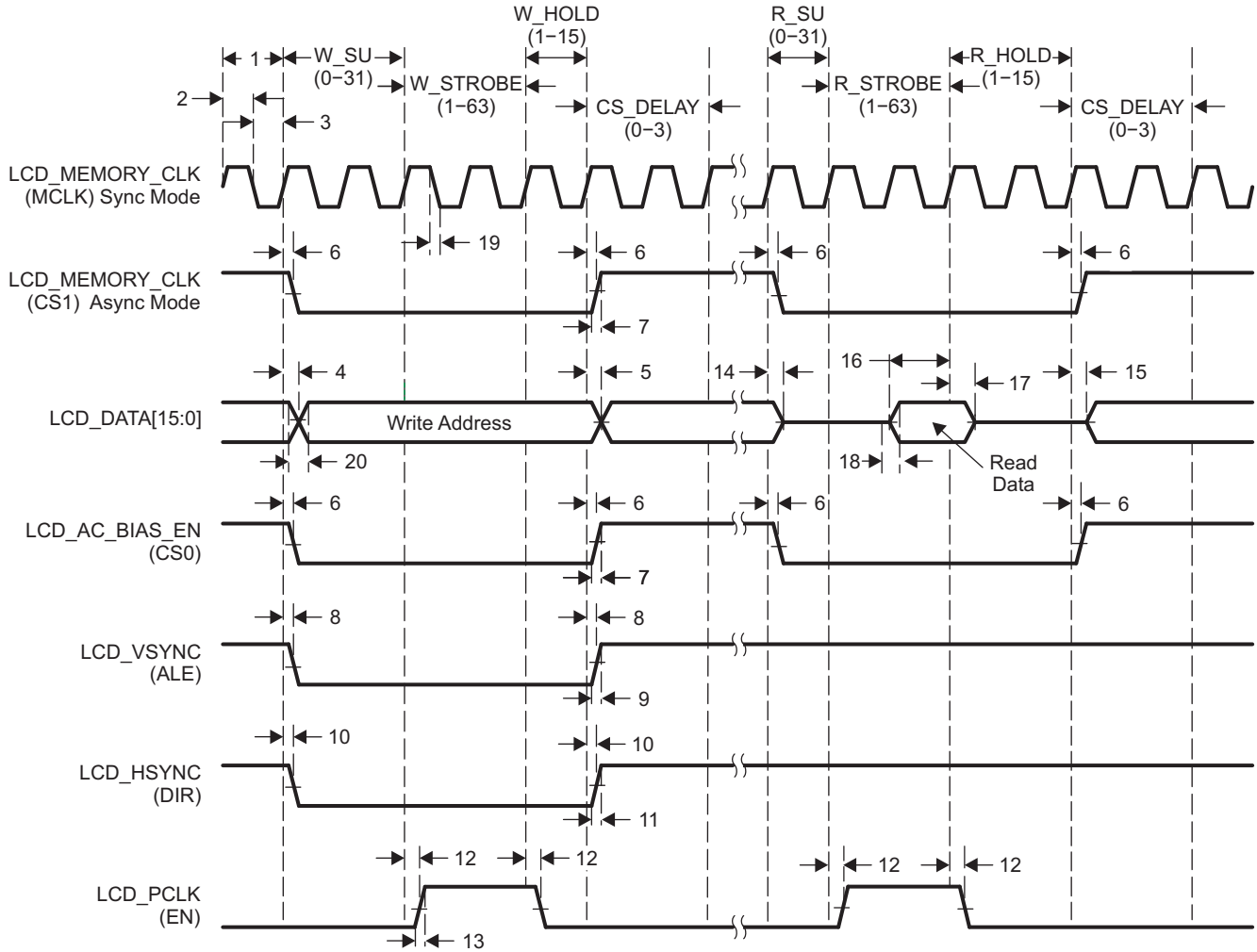
- A. Hitachi mode performs asynchronous operations that do not require an external LCD_MEMORY_CLK. The first LCD_MEMORY_CLK waveform is only shown as a reference of the internal clock that sequences the other signals. The second LCD_MEMORY_CLK waveform is shown as E1 because the LCD_MEMORY_CLK signal is used to implement the E1 function in Hitachi mode.

Figure 7-74. Data Read in Hitachi Mode



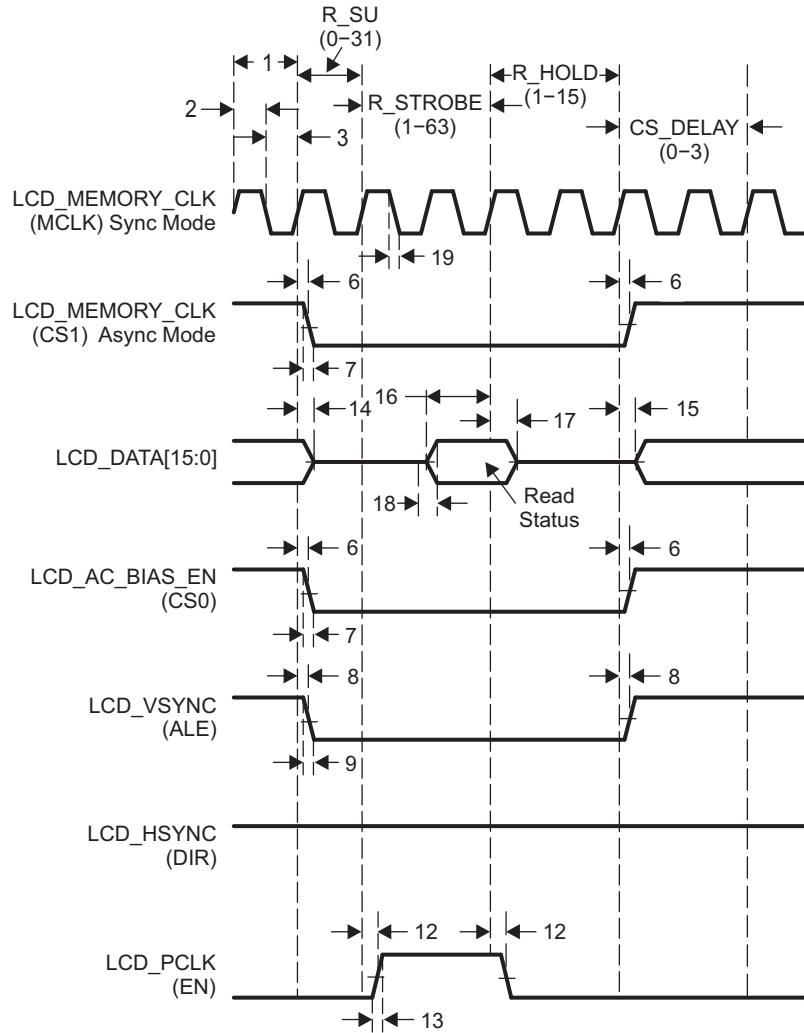
- A. Motorola mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

Figure 7-75. Micro-Interface Graphic Display Motorola Write



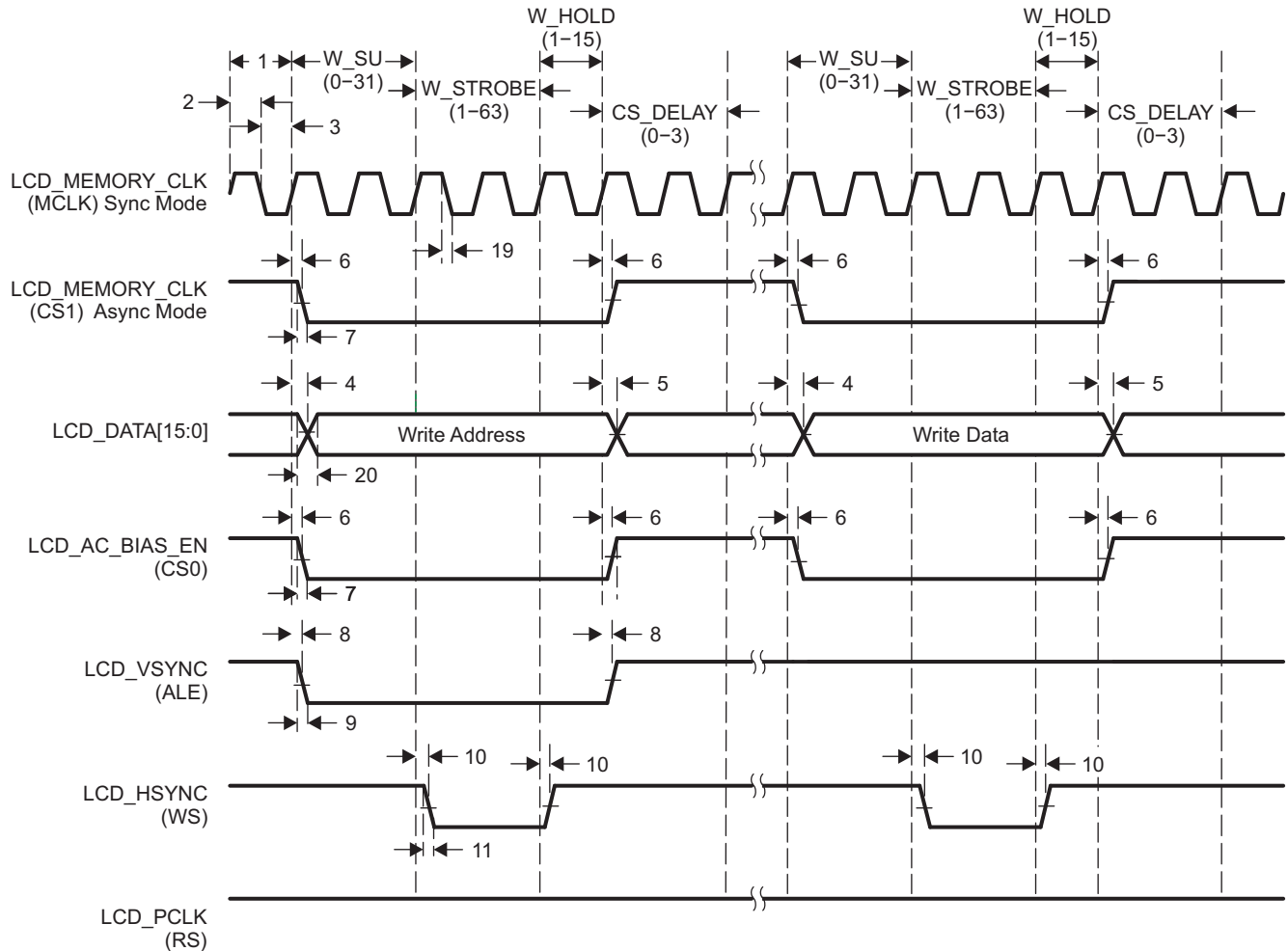
- A. Motorola mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

Figure 7-76. Micro-Interface Graphic Display Motorola Read



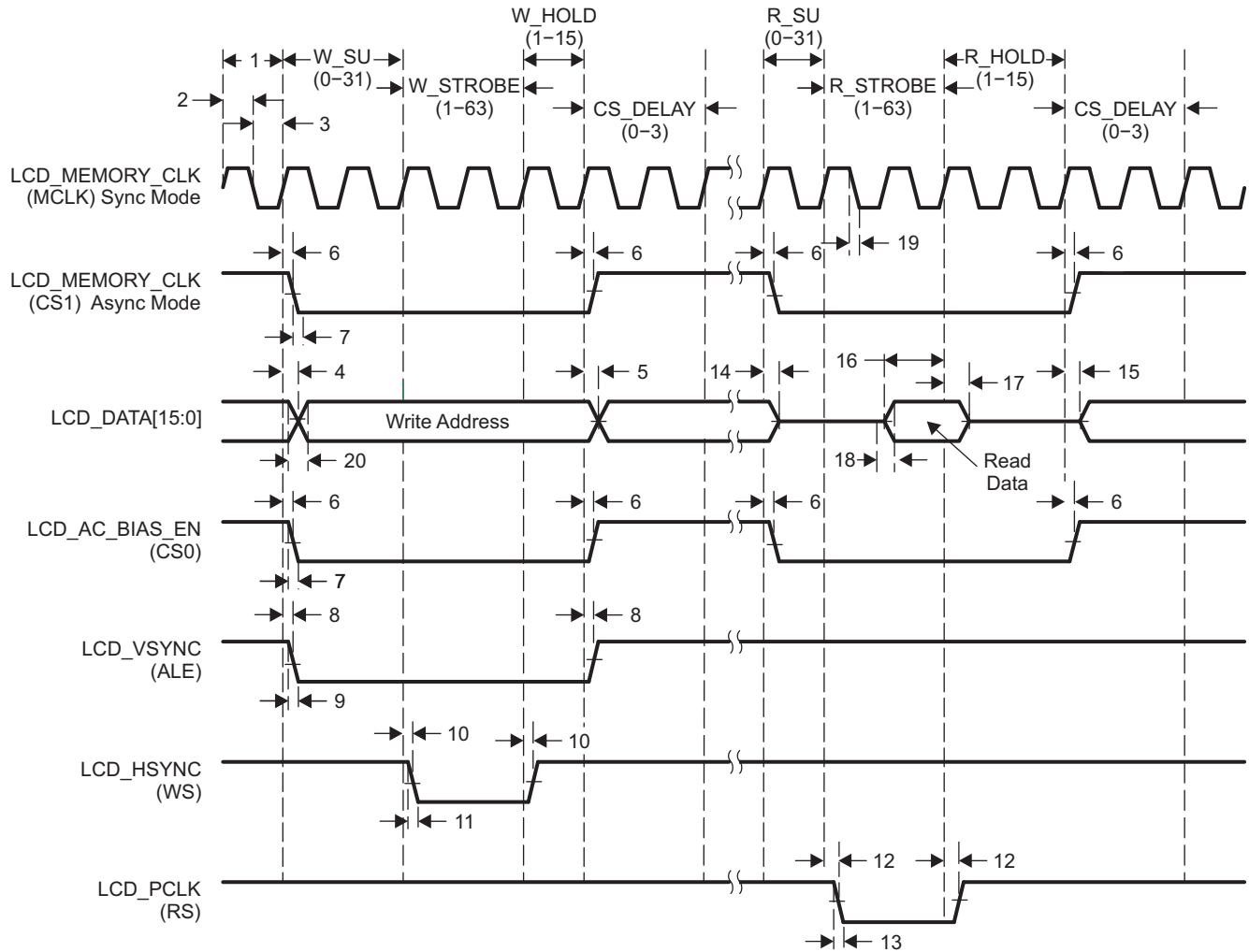
- A. Motorola mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

Figure 7-77. Micro-Interface Graphic Display Motorola Status



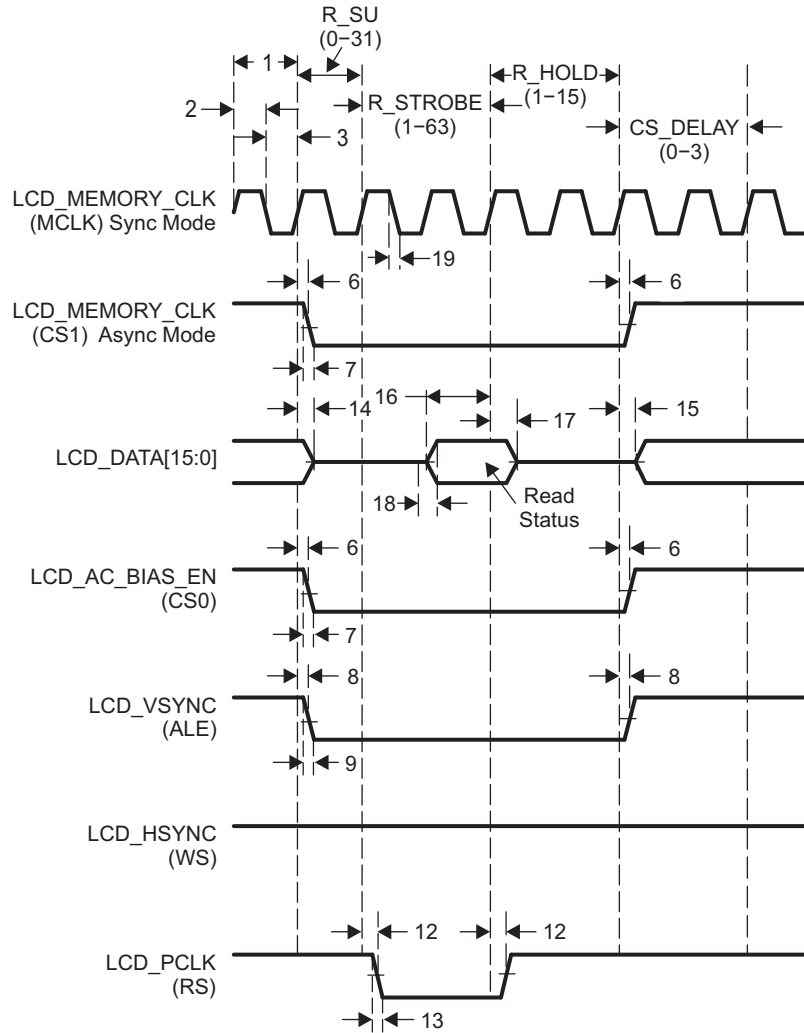
- A. Intel mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

Figure 7-78. Micro-Interface Graphic Display Intel Write



- A. Intel mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

Figure 7-79. Micro-Interface Graphic Display Intel Read



- A. Intel mode can be configured to perform asynchronous operations or synchronous operations. When configured in asynchronous mode, LCD_MEMORY_CLK is not required, so it performs the CS1 function. When configured in synchronous mode, LCD_MEMORY_CLK performs the MCLK function. LCD_MEMORY_CLK is also shown as a reference of the internal clock that sequences the other signals.

Figure 7-80. Micro-Interface Graphic Display Intel Status

7.10.2 LCD Raster Mode

Table 7-76. Switching Characteristics for LCD Raster Mode

(see [Figure 7-82](#) through [Figure 7-85](#))

| NO. | PARAMETER | OPP50 | | OPP100 | | UNIT |
|-----|---|-----------|-----------|-----------|-----------|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_c(\text{LCD_PCLK})$ Cycle time, pixel clock | 15.8 | | 7.9 | | ns |
| 2 | $t_w(\text{LCD_PCLKH})$ Pulse duration, pixel clock high | $0.45t_c$ | $0.55t_c$ | $0.45t_c$ | $0.55t_c$ | ns |
| 3 | $t_w(\text{LCD_PCLKL})$ Pulse duration, pixel clock low | $0.45t_c$ | $0.55t_c$ | $0.45t_c$ | $0.55t_c$ | ns |
| 4 | $t_d(\text{LCD_PCLK-LCD_DATAV})$ Delay time, LCD_PCLK to LCD_DATA[23:0] valid (write) | | 3.0 | | 1.9 | ns |
| 5 | $t_d(\text{LCD_PCLK-LCD_DATAI})$ Delay time, LCD_PCLK to LCD_DATA[23:0] invalid (write) | -3.0 | | -1.7 | | ns |
| 6 | $t_d(\text{LCD_PCLK-LCD_AC_BIAS_EN})$ Delay time, LCD_PCLK to LCD_AC_BIAS_EN | -3.0 | 3.0 | -1.7 | 1.9 | ns |
| 7 | $t_t(\text{LCD_AC_BIAS_EN})$ Transition time, LCD_AC_BIAS_EN | 0.5 | 2.4 | 0.5 | 2.4 | ns |
| 8 | $t_d(\text{LCD_PCLK-LCD_VSYNC})$ Delay time, LCD_PCLK to LCD_VSYNC | -3.0 | 3.0 | -1.7 | 1.9 | ns |
| 9 | $t_t(\text{LCD_VSYNC})$ Transition time, LCD_VSYNC | 0.5 | 2.4 | 0.5 | 2.4 | ns |
| 10 | $t_d(\text{LCD_PCLK-LCD_HSYNC})$ Delay time, LCD_PCLK to LCD_HSYNC | -3.0 | 3.0 | -1.7 | 1.9 | ns |
| 11 | $t_t(\text{LCD_HSYNC})$ Transition time, LCD_HSYNC | 0.5 | 2.4 | 0.5 | 2.4 | ns |
| 12 | $t_t(\text{LCD_PCLK})$ Transition time, LCD_PCLK | 0.5 | 2.4 | 0.5 | 2.4 | ns |
| 13 | $t_t(\text{LCD_DATA})$ Transition time, LCD_DATA | 0.5 | 2.4 | 0.5 | 2.4 | ns |

Frame-to-frame timing is derived through the following parameters in the LCD (RASTER_TIMING_1) register:

- Vertical front porch (VFP)
- Vertical sync pulse width (VSW)
- Vertical back porch (VBP)
- Lines per panel (LPP_B10 + LPP)

Line-to-line timing is derived through the following parameters in the LCD (RASTER_TIMING_0) register:

- Horizontal front porch (HFP)
- Horizontal sync pulse width (HSW)
- Horizontal back porch (HBP)
- Pixels per panel (PPLMSB + PPLLSB)

LCD_AC_BIAS_EN timing is derived through the following parameter in the LCD (RASTER_TIMING_2) register:

- AC bias frequency (ACB)

The display format produced in raster mode is shown in [Figure 7-81](#). An entire frame is delivered one line at a time. The first line delivered starts at data pixel (1, 1) and ends at data pixel (P, 1). The last line delivered starts at data pixel (1, L) and ends at data pixel (P, L). The beginning of each new frame is denoted by the activation of I/O signal LCD_VSYNC. The beginning of each new line is denoted by the activation of I/O signal LCD_HSYNC.

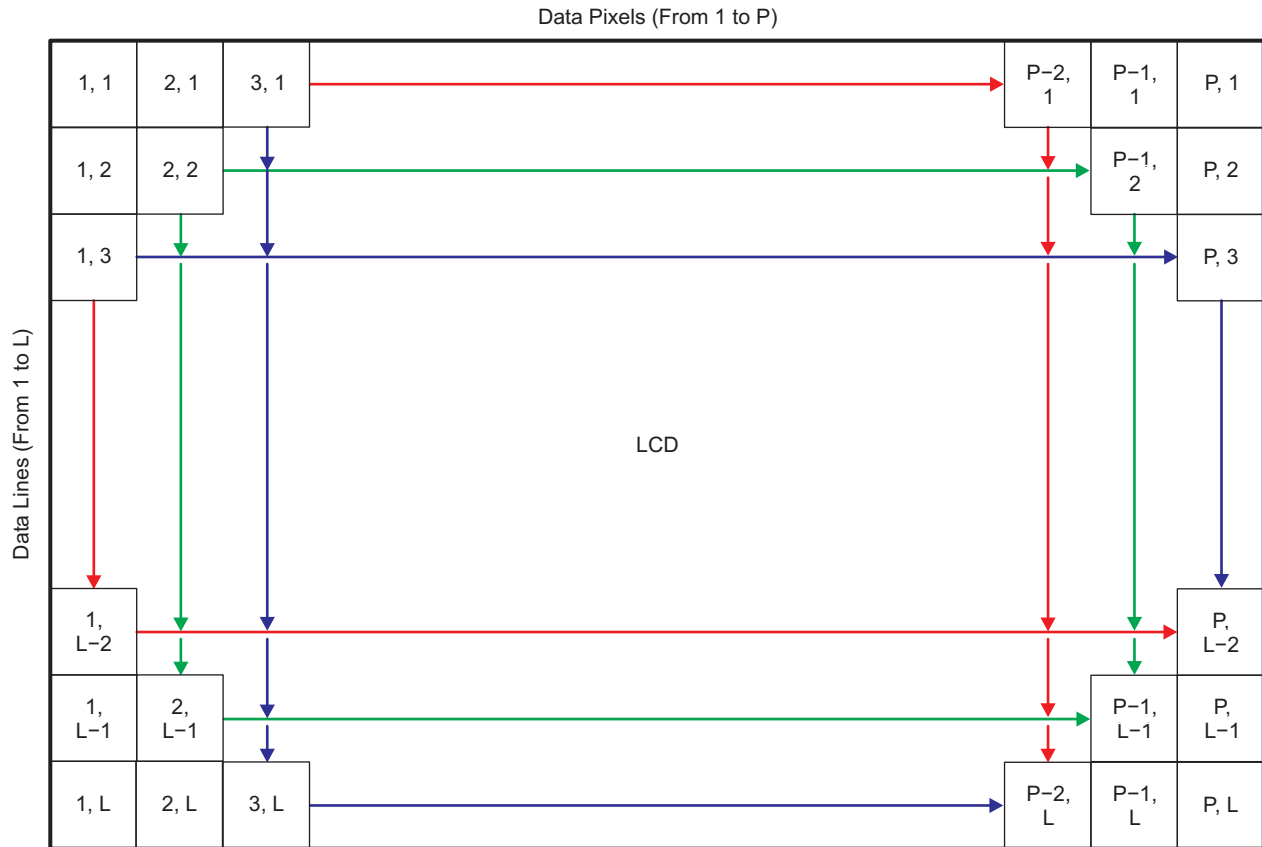


Figure 7-81. LCD Raster-Mode Display Format

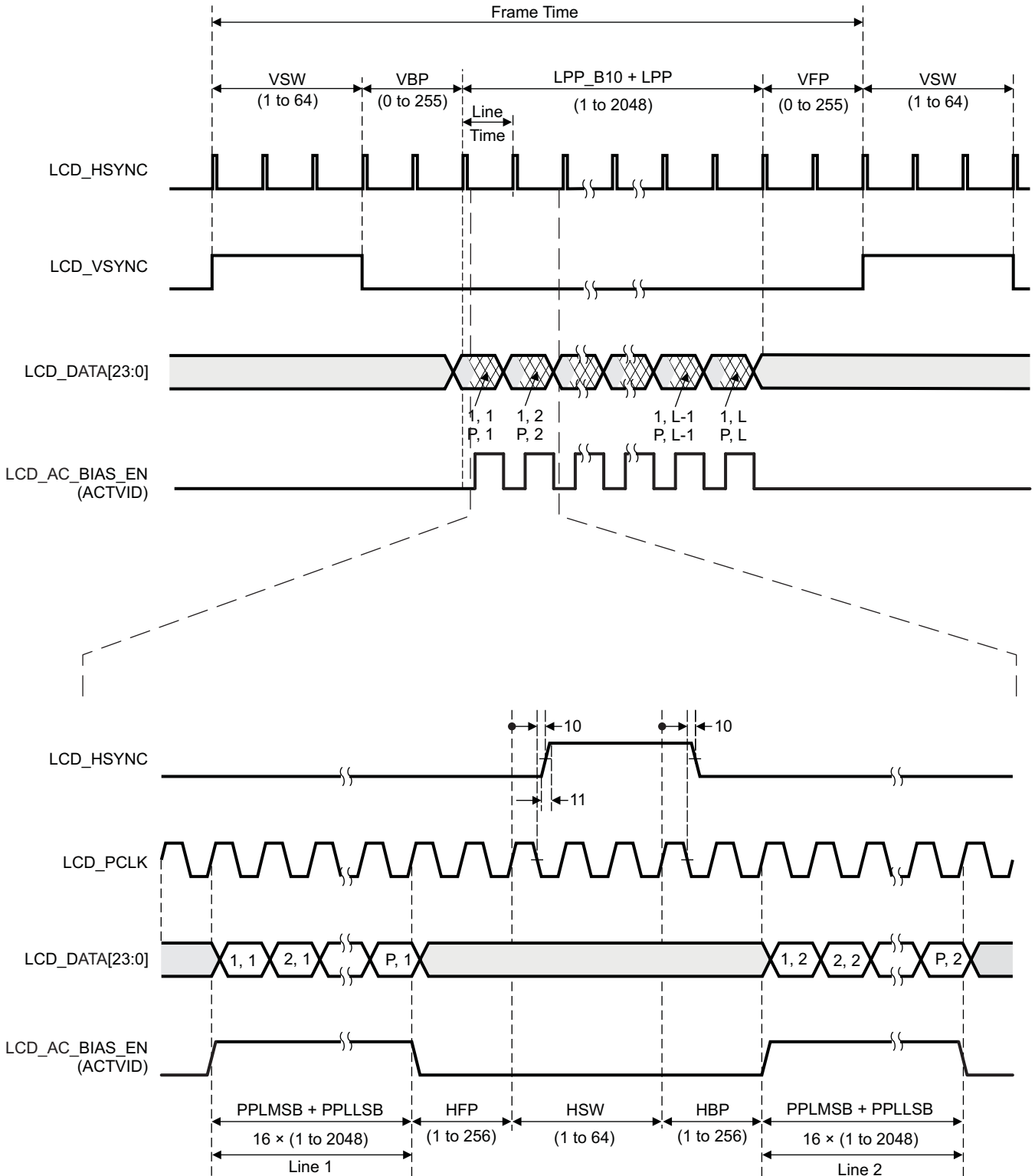
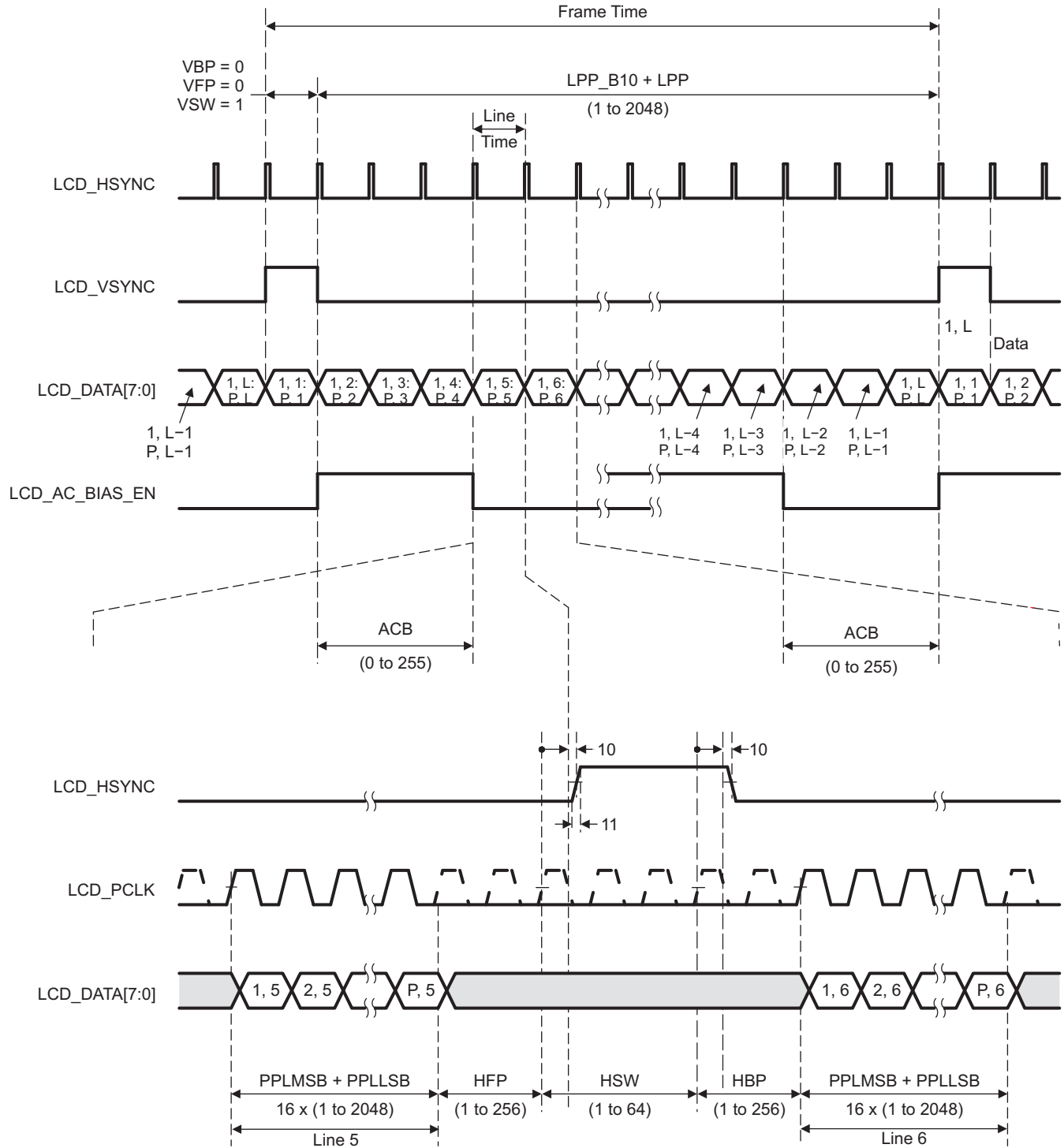
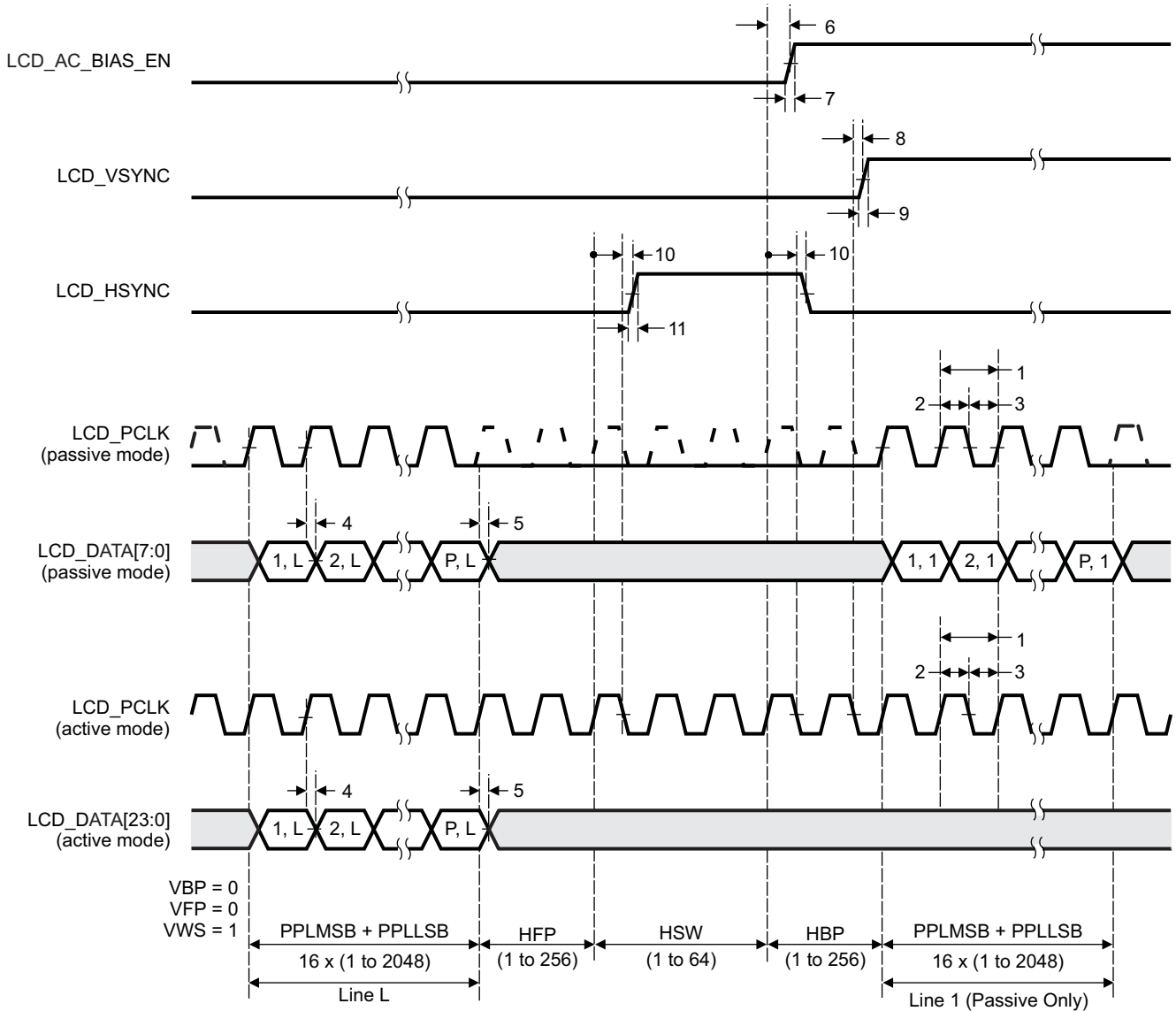


Figure 7-82. LCD Raster-Mode Active



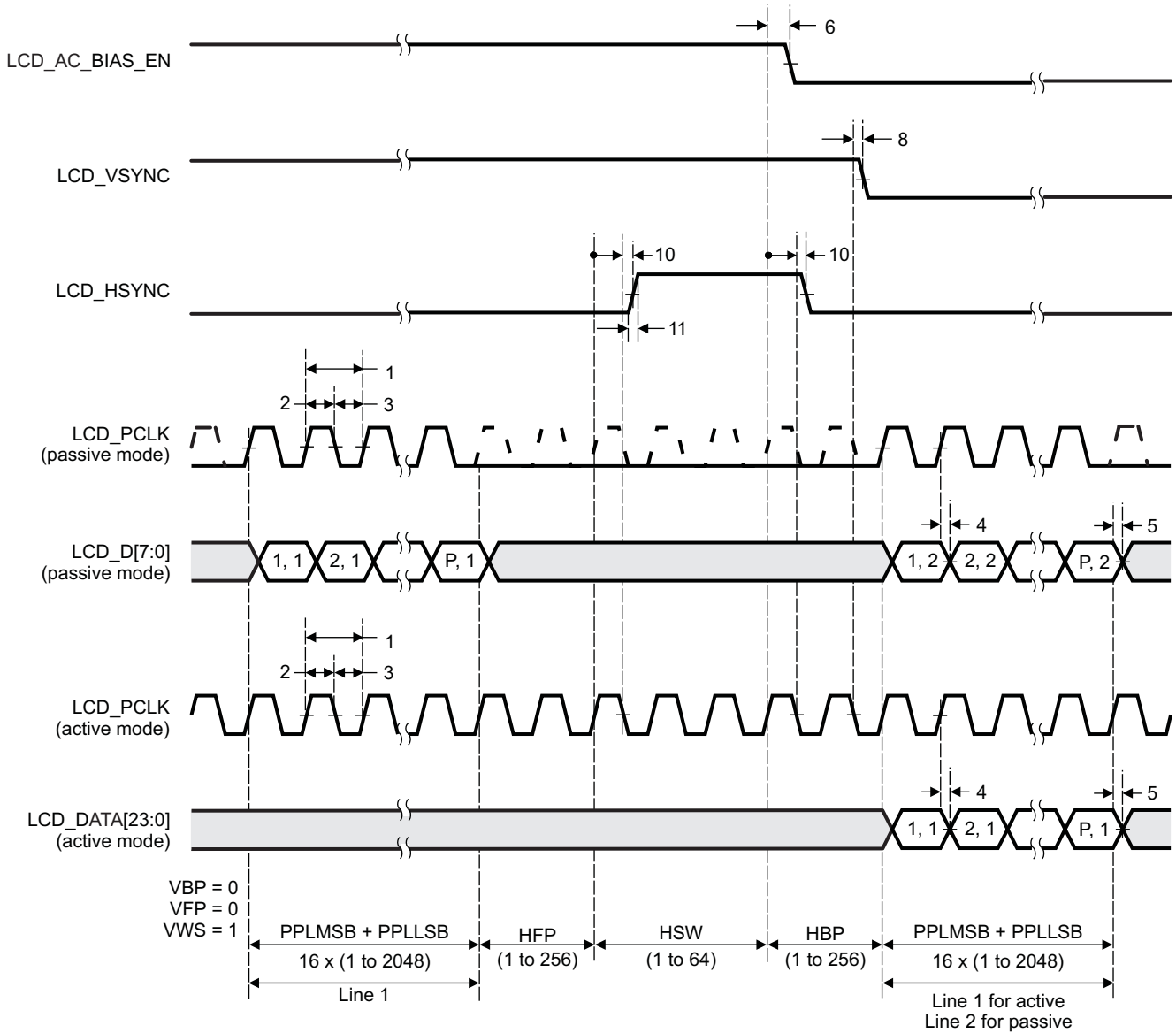
A. The dashed portion of LCD_PCLK is only shown as a reference of the internal clock that sequences the other signals.

Figure 7-83. LCD Raster-Mode Passive



A. The dashed portion of LCD_PCLK is only shown as a reference of the internal clock that sequences the other signals.

Figure 7-84. LCD Raster-Mode Control Signal Activation



A. The dashed portion of LCD_PCLK is only shown as a reference of the internal clock that sequences the other signals.

Figure 7-85. LCD Raster-Mode Control Signal Deactivation

7.11 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I²S) protocols, and inter-component digital audio interface transmission (DIT).

7.11.1 McASP Device-Specific Information

The device includes two multichannel audio serial port (McASP) interface peripherals (McASP0 and McASP1). The McASP module consists of a transmit and receive section. These sections can operate completely independently with different data formats, separate master clocks, bit clocks, and frame syncs or, alternatively, the transmit and receive sections may be synchronized. The McASP module also includes shift registers that may be configured to operate as either transmit data or receive data.

The transmit section of the McASP can transmit data in either a time-division-multiplexed (TDM) synchronous serial format or in a digital audio interface (DIT) format where the bit stream is encoded for SPDIF, AES-3, IEC-60958, CP-430 transmission. The receive section of the McASP peripheral supports the TDM synchronous serial format.

The McASP module can support one transmit data format (either a TDM format or DIT format) and one receive format at a time. All transmit shift registers use the same format and all receive shift registers use the same format; however, the transmit and receive formats need not be the same. Both the transmit and receive sections of the McASP also support burst mode, which is useful for nonaudio data (for example, passing control information between two devices).

The McASP peripheral has additional capability for flexible clock generation and error detection/handling, as well as error management.

The device McASP0 and McASP1 modules have up to four serial data pins each. The McASP FIFO size is 256 bytes and two DMA and two interrupt requests are supported. Buffers are used transparently to better manage DMA, which can be leveraged to manage data flow more efficiently.

For more detailed information on and the functionality of the McASP peripheral, see the Multichannel Audio Serial Port (McASP) section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

7.11.2 McASP Electrical Data and Timing

Table 7-77. McASP Timing Conditions

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|------------------|-----|------------------|------|
| Input Conditions | | | | | |
| t_R | Input signal rise time | 1 ⁽¹⁾ | | 4 ⁽¹⁾ | ns |
| t_F | Input signal fall time | 1 ⁽¹⁾ | | 4 ⁽¹⁾ | ns |
| Output Condition | | | | | |
| C_{LOAD} | Output load capacitance | 15 | | 30 | pF |

(1) Except when specified otherwise.

Table 7-78. Timing Requirements for McASP⁽¹⁾

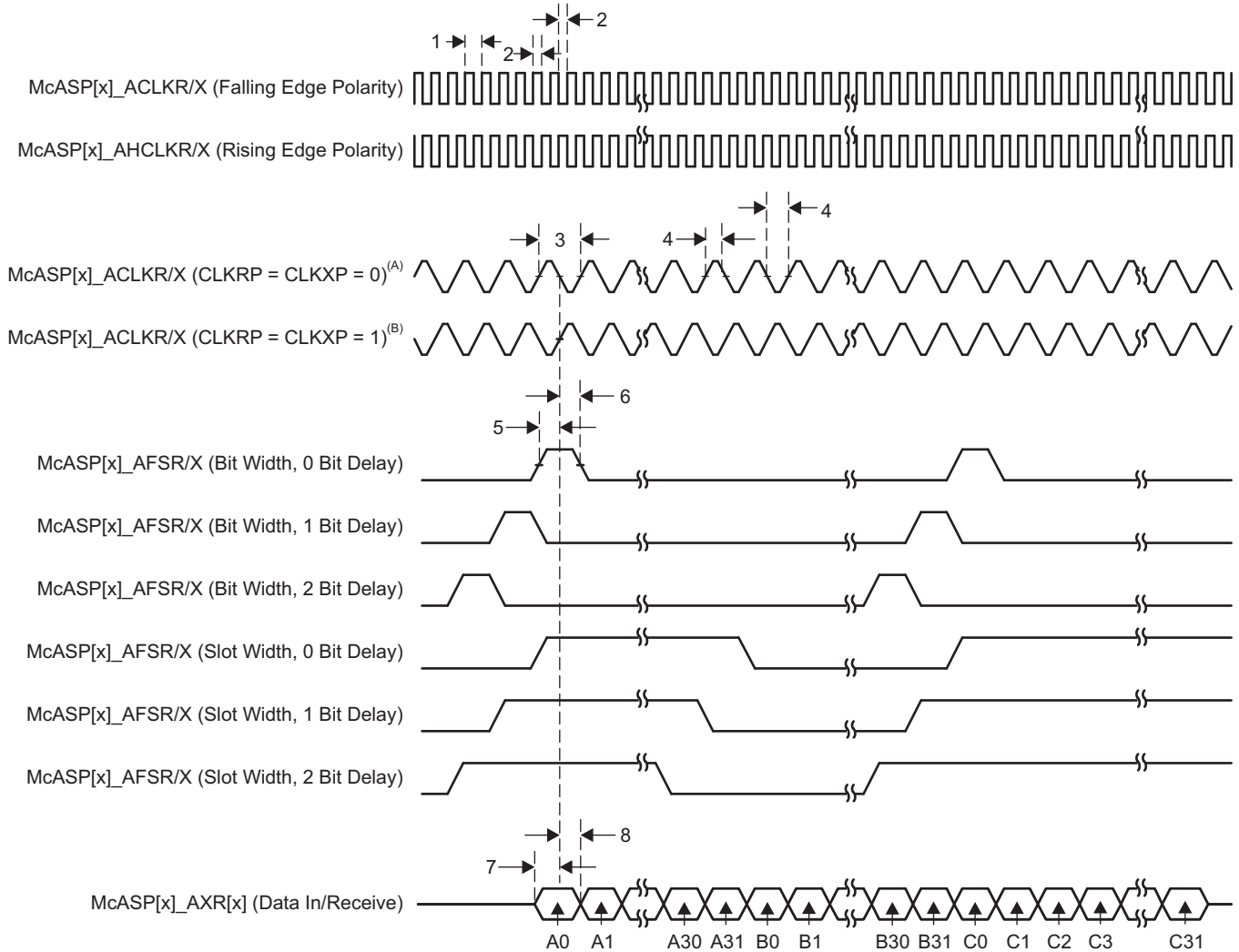
(see Figure 7-86)

| NO. | | | OPP100 | | OPP50 | | UNIT |
|-----|------------------------|--|---------------------------|------|---------------------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, McASP[x]_AHCLKR and McASP[x]_AHCLKX | 20 | | 40 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, McASP[x]_AHCLKR and McASP[x]_AHCLKX high or low | 0.5P - 2.5 ⁽²⁾ | | 0.5P - 2.5 ⁽²⁾ | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, McASP[x]_ACLKR and McASP[x]_ACLKX | 20 | | 40 | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, McASP[x]_ACLKR and McASP[x]_ACLKX high or low | 0.5R - 2.5 ⁽³⁾ | | 0.5R - 2.5 ⁽³⁾ | | ns |
| 5 | $t_{su(AFSRX-ACLKRX)}$ | Setup time, McASP[x]_AFSR and McASP[x]_AFSX input valid before McASP[x]_ACLKR and McASP[x]_ACLKX | ACLKR and ACLKX int | 11.5 | | 15.5 | ns |
| | | | ACLKR and ACLKX ext in | 4 | | 6 | |
| | | | ACLKR and ACLKX ext out | 4 | | 6 | |
| 6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, McASP[x]_AFSR and McASP[x]_AFSX input valid after McASP[x]_ACLKR and McASP[x]_ACLKX | ACLKR and ACLKX int | -1 | | -1 | ns |
| | | | ACLKR and ACLKX ext in | 0.4 | | 0.4 | |
| | | | ACLKR and ACLKX ext out | 0.4 | | 0.4 | |
| 7 | $t_{su(AXR-ACLKRX)}$ | Setup time, McASP[x]_AXR input valid before McASP[x]_ACLKR and McASP[x]_ACLKX | ACLKR and ACLKX int | 11.5 | | 15.5 | ns |
| | | | ACLKR and ACLKX ext in | 4 | | 6 | |
| | | | ACLKR and ACLKX ext out | 4 | | 6 | |
| 8 | $t_{h(ACLKRX-AXR)}$ | Hold time, McASP[x]_AXR input valid after McASP[x]_ACLKR and McASP[x]_ACLKX | ACLKR and ACLKX int | -1 | | -1 | ns |
| | | | ACLKR and ACLKX ext in | 0.4 | | 0.4 | |
| | | | ACLKR and ACLKX ext out | 0.4 | | 0.4 | |

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
 ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
 ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
 ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
 ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = McASP[x]_AHCLKR and McASP[x]_AHCLKX period in nanoseconds (ns).

(3) R = McASP[x]_ACLKR and McASP[x]_ACLKX period in ns.



- A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).
- B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

Figure 7-86. McASP Input Timing

Table 7-79. Switching Characteristics for McASP⁽¹⁾

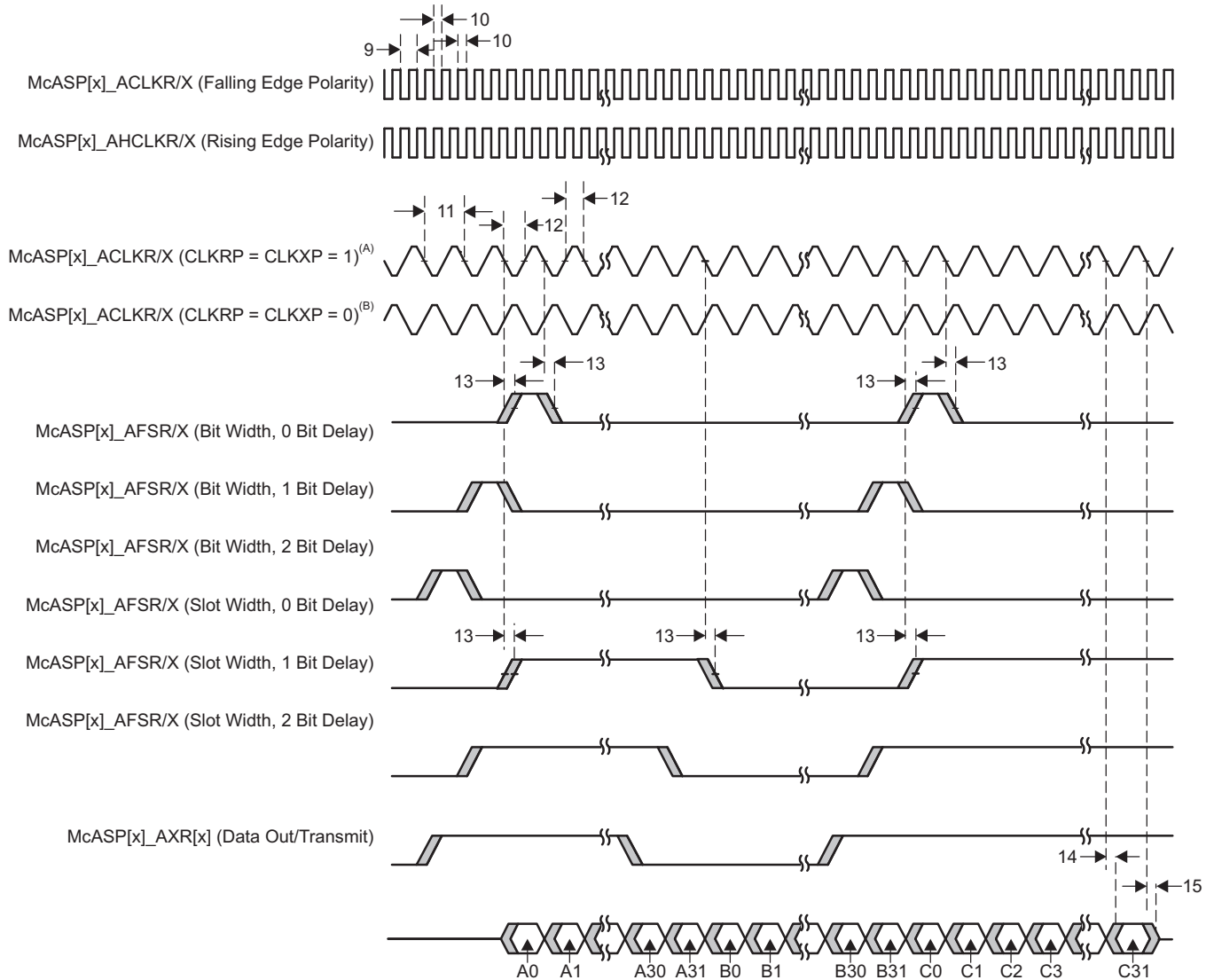
(see Figure 7-87)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT | |
|-----|-----------------------|---|---------------------------|-----|---------------------------|-----|------|----|
| | | | MIN | MAX | MIN | MAX | | |
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, McASP[x]_AHCLKR and McASP[x]_AHCLKX | 20 ⁽²⁾ | | 40 | | ns | |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, McASP[x]_AHCLKR and McASP[x]_AHCLKX high or low | 0.5P – 2.5 ⁽³⁾ | | 0.5P – 2.5 ⁽³⁾ | | ns | |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, McASP[x]_ACLKR and McASP[x]_ACLKX | 20 | | 40 | | ns | |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, McASP[x]_ACLKR and McASP[x]_ACLKX high or low | 0.5P – 2.5 ⁽³⁾ | | 0.5P – 2.5 ⁽³⁾ | | ns | |
| 13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, McASP[x]_ACLKR and McASP[x]_ACLKX transmit edge to McASP[x]_AFSR and McASP[x]_AFSX output valid | ACLKR and ACLKX int | 0 | 6 | 0 | 6 | ns |
| | | | ACLKR and ACLKX ext in | 2 | 13.5 | 2 | 18 | |
| | | Delay time, McASP[x]_ACLKR and McASP[x]_ACLKX transmit edge to McASP[x]_AFSR and McASP[x]_AFSX output valid with Pad Loopback | ACLKR and ACLKX ext out | 2 | 13.5 | 2 | 18 | |
| 14 | $t_{d(ACLKX-AXR)}$ | Delay time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output valid | ACLKX int | 0 | 6 | 0 | 6 | ns |
| | | | ACLKX ext in | 2 | 13.5 | 2 | 18 | |
| | | Delay time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output valid with Pad Loopback | ACLKX ext out | 2 | 13.5 | 2 | 18 | |
| 15 | $t_{dis(ACLKX-AXR)}$ | Disable time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output high impedance | ACLKX int | 0 | 6 | 0 | 6 | ns |
| | | | ACLKX ext in | 2 | 13.5 | 2 | 18 | |
| | | Disable time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output high impedance with pad loopback | ACLKX ext out | 2 | 13.5 | 2 | 18 | |

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
 ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
 ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
 ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
 ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) 50 MHz

(3) P = AHCLKR and AHCLKX period.



- A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).
- B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 7-87. McASP Output Timing

7.12 Multichannel Serial Port Interface (McSPI)

For more information, see the Multichannel Serial Port Interface (McSPI) section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

7.12.1 McSPI Electrical Data and Timing

The following timings are applicable to the different configurations of McSPI in master or slave mode for any McSPI and any channel (n).

7.12.1.1 McSPI—Slave Mode

Table 7-80. McSPI Timing Conditions – Slave Mode

| PARAMETER | | MIN | MAX | UNIT |
|-------------------------|-------------------------|-----|-----|------|
| Input Conditions | | | | |
| t_r | Input signal rise time | | 5 | ns |
| t_f | Input signal fall time | | 5 | ns |
| Output Condition | | | | |
| C_{load} | Output load capacitance | | 20 | pF |

Table 7-81. Timing Requirements for McSPI Input Timings—Slave Mode

(see [Figure 7-88](#))

| NO. | PARAMETER | OPP100 | | OPP50 | | UNIT |
|-----|-----------------------|--|----------------------------|----------------------------|----------------------------|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK | | 124.8 | | ns |
| 2 | $t_{w(SPICLKL)}$ | 0.5P – 3.12 ⁽¹⁾ | 0.5P + 3.12 ⁽¹⁾ | 0.5P – 3.12 ⁽¹⁾ | 0.5P + 3.12 ⁽¹⁾ | ns |
| 3 | $t_{w(SPICLKH)}$ | 0.5P – 3.12 ⁽¹⁾ | 0.5P + 3.12 ⁽¹⁾ | 0.5P – 3.12 ⁽¹⁾ | 0.5P + 3.12 ⁽¹⁾ | ns |
| 4 | $t_{su(SIMO-SPICLK)}$ | Setup time, SPI_D[x] (SIMO) valid before SPI_CLK active edge ⁽²⁾⁽³⁾ | | 12.92 | | ns |
| 5 | $t_{h(SPICLK-SIMO)}$ | Hold time, SPI_D[x] (SIMO) valid after SPI_CLK active edge ⁽²⁾⁽³⁾ | | 12.92 | | ns |
| 8 | $t_{su(CS-SPICLK)}$ | Setup time, SPI_CS valid before SPI_CLK first edge ⁽²⁾ | | 12.92 | | ns |
| 9 | $t_{h(SPICLK-CS)}$ | Hold time, SPI_CS valid after SPI_CLK last edge ⁽²⁾ | | 12.92 | | ns |

(1) P = SPI_CLK period.

(2) This timing applies to all configurations regardless of MCSPIX_CLK polarity and which clock edges are used to drive output data and capture input data.

(3) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

Table 7-82. Switching Characteristics for McSPI Output Timings—Slave Mode

(see [Figure 7-89](#))

| NO. | PARAMETER | OPP100 | | OPP50 | | UNIT |
|-----|----------------------|---|-----|-------|-------|------|
| | | MIN | MAX | MIN | MAX | |
| 6 | $t_{d(SPICLK-SOMI)}$ | Delay time, SPI_CLK active edge to SPI_D[x] (SOMI) transition ⁽¹⁾⁽²⁾ | | –4.00 | 17.12 | ns |
| 7 | $t_{d(CS-SOMI)}$ | Delay time, SPI_CS active edge to SPI_D[x] (SOMI) transition ⁽¹⁾⁽²⁾ | | | 17.12 | ns |

(1) This timing applies to all configurations regardless of MCSPIX_CLK polarity and which clock edges are used to drive output data and capture input data.

(2) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

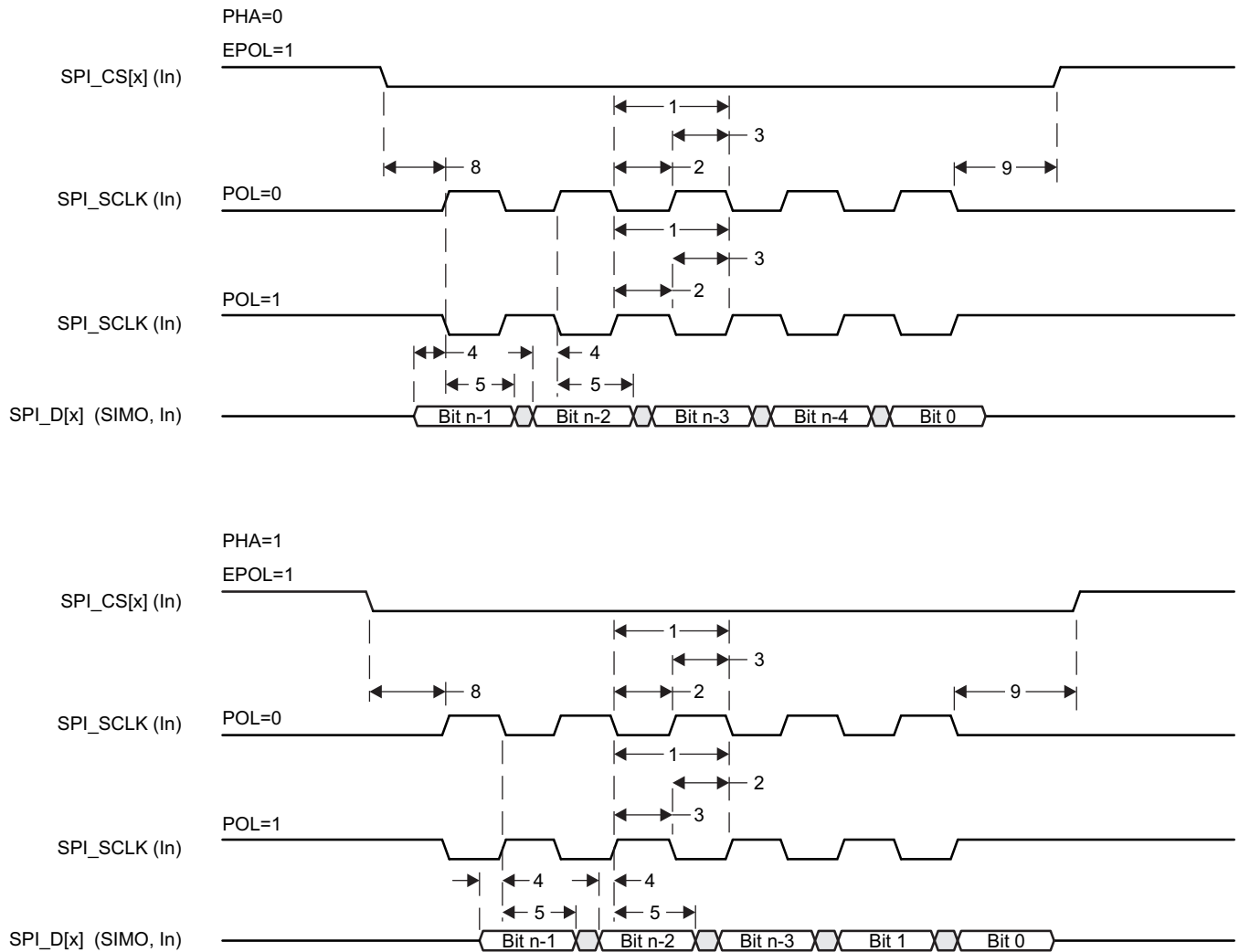


Figure 7-88. SPI Slave Mode Receive Timing

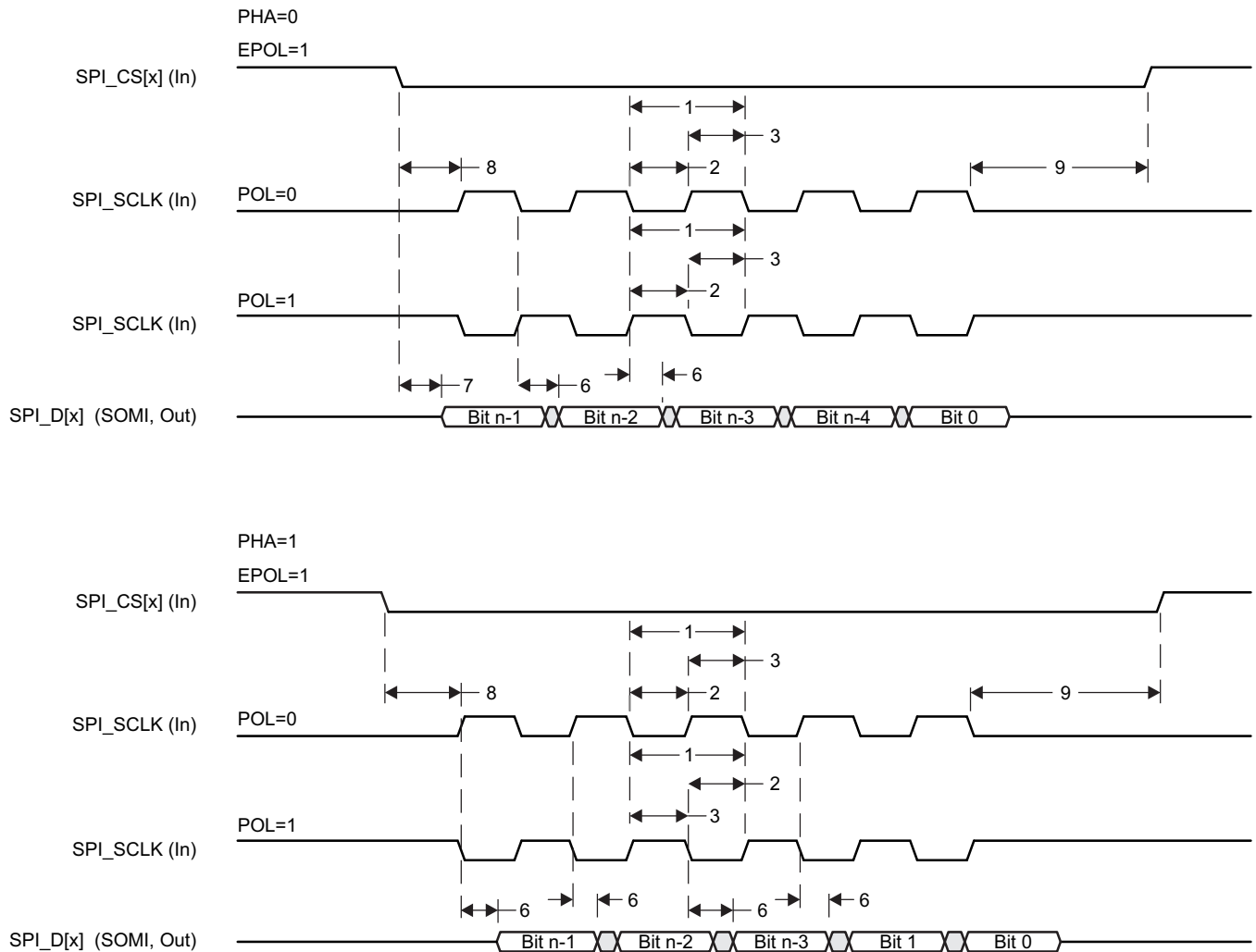


Figure 7-89. SPI Slave Mode Transmit Timing

7.12.1.2 McSPI—Master Mode

Table 7-83. McSPI Timing Conditions – Master Mode

| PARAMETER | LOW LOAD | | HIGH LOAD | | UNIT |
|-------------------------|-------------------------|-----|-----------|-----|------|
| | MIN | MAX | MIN | MAX | |
| Input Conditions | | | | | |
| t _r | Input signal rise time | | 8 | 8 | ns |
| t _f | Input signal fall time | | 8 | 8 | ns |
| Output Condition | | | | | |
| C _{load} | Output load capacitance | | 5 | 25 | pF |

Table 7-84. Timing Requirements for McSPI Input Timings – Master Mode

(see Figure 7-90)

| NO. | PARAMETER | DESCRIPTION | OPP100 | | | | OPP50 | | | | UNIT |
|-----|------------------------------|---|--|-----|-----------|-----|----------|-----|-----------|-----|------|
| | | | LOW LOAD | | HIGH LOAD | | LOW LOAD | | HIGH LOAD | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 4 | t _{su(SOMI-SPICKH)} | Setup time, SPI_D[x] (SOMI) valid before SPI_CLK active edge ⁽¹⁾ | 2.29 | | 3.02 | | 2.29 | | 3.02 | ns | |
| 5 | t _{h(SPICLKH-SOMI)} | Hold time, SPI_D[x] (SOMI) valid after SPI_CLK active edge ⁽¹⁾ | Industrial extended temperature (-40°C to 125°C) | | 7.1 | | 7.1 | | 7.1 | ns | |
| | | | All other temperature ranges | | 4.7 | | 4.7 | | 4.7 | | |

(1) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

Table 7-85. Switching Characteristics for McSPI Output Timings – Master Mode

(see Figure 7-91)

| NO. | PARAMETER | DESCRIPTION | OPP100 | | | | OPP50 | | | | UNIT |
|-----|-----------------------------|--|-----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|------|
| | | | LOW LOAD | | HIGH LOAD | | LOW LOAD | | HIGH LOAD | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | t _{c(SPICLK)} | Cycle time, SPI_CLK | 20.8 | | 20.8 | | 41.6 | | 41.6 | | ns |
| 2 | t _{w(SPICLK)} | Typical pulse duration, SPI_CLK low | 0.5P – 1.04 ⁽¹⁾ | 0.5P + 1.04 ⁽¹⁾ | 0.5P – 2.08 ⁽¹⁾ | 0.5P + 2.08 ⁽¹⁾ | 0.5P – 1.04 ⁽¹⁾ | 0.5P + 1.04 ⁽¹⁾ | 0.5P – 2.08 ⁽¹⁾ | 0.5P + 2.08 ⁽¹⁾ | ns |
| 3 | t _{w(SPICLKH)} | Typical pulse duration, SPI_CLK high | 0.5P – 1.04 ⁽¹⁾ | 0.5P + 1.04 ⁽¹⁾ | 0.5P – 2.08 ⁽¹⁾ | 0.5P + 2.08 ⁽¹⁾ | 0.5P – 1.04 ⁽¹⁾ | 0.5P + 1.04 ⁽¹⁾ | 0.5P – 2.08 ⁽¹⁾ | 0.5P + 2.08 ⁽¹⁾ | ns |
| | t _{r(SPICLK)} | Rising time, SPI_CLK | 3.82 | | 3.82 | | 3.82 | | 3.82 | | ns |
| | t _{f(SPICLK)} | Falling time, SPI_CLK | 3.44 | | 3.44 | | 3.44 | | 3.44 | | ns |
| 6 | t _{d(SPICLK-SIMO)} | Delay time, SPI_CLK active edge to SPI_D[x] (SIMO) transition ⁽²⁾ | -3.57 | 3.57 | -4.62 | 4.62 | -3.57 | 3.57 | -4.62 | 4.62 | ns |
| 7 | t _{d(CS-SIMO)} | Delay time, SPI_CS active edge to SPI_D[x] (SIMO) transition ⁽²⁾ | 3.57 | | 4.62 | | 3.57 | | 4.62 | | ns |
| 8 | t _{d(CS-SPICLK)} | Delay time, SPI_CS active to SPI_CLK first edge | Mode 1 and 3 ⁽³⁾ | A – 4.2 ⁽⁴⁾ | A – 2.54 ⁽⁴⁾ | | A – 4.2 ⁽⁴⁾ | | A – 2.54 ⁽⁴⁾ | | ns |
| | | | Mode 0 and 2 ⁽³⁾ | B – 4.2 ⁽⁵⁾ | B – 2.54 ⁽⁵⁾ | | B – 4.2 ⁽⁵⁾ | | B – 2.54 ⁽⁵⁾ | | ns |
| 9 | t _{d(SPICLK-CS)} | Delay time, SPI_CLK last edge to SPI_CS inactive | Mode 1 and 3 ⁽³⁾ | B – 4.2 ⁽⁵⁾ | B – 2.54 ⁽⁵⁾ | | B – 4.2 ⁽⁵⁾ | | B – 2.54 ⁽⁵⁾ | | ns |
| | | | Mode 0 and 2 ⁽³⁾ | A – 4.2 ⁽⁴⁾ | A – 2.54 ⁽⁴⁾ | | A – 4.2 ⁽⁴⁾ | | A – 2.54 ⁽⁴⁾ | | ns |

(1) P = SPI_CLK period.

(2) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

(3) The polarity of SPIx_CLK and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable:

- SPIx_CLK(1) phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 1 (Modes 1 and 3).
- SPIx_CLK(1) phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 0 (Modes 0 and 2).

- (4) Case P = 20.8 ns, A = (TCS + 1) × TSPICLKREF (TCS is a bit field of MCSPI_CH(i)CONF register).
 Case P > 20.8 ns, A = (TCS + 0.5) × Fratio × TSPICLKREF (TCS is a bit field of MCSPI_CH(i)CONF register).
 Note: P = SPI_CLK clock period.
- (5) B = (TCS + 0.5) × TSPICLKREF × Fratio (TCS is a bit field of MCSPI_CH(i)CONF register, Fratio: Even ≥ 2).

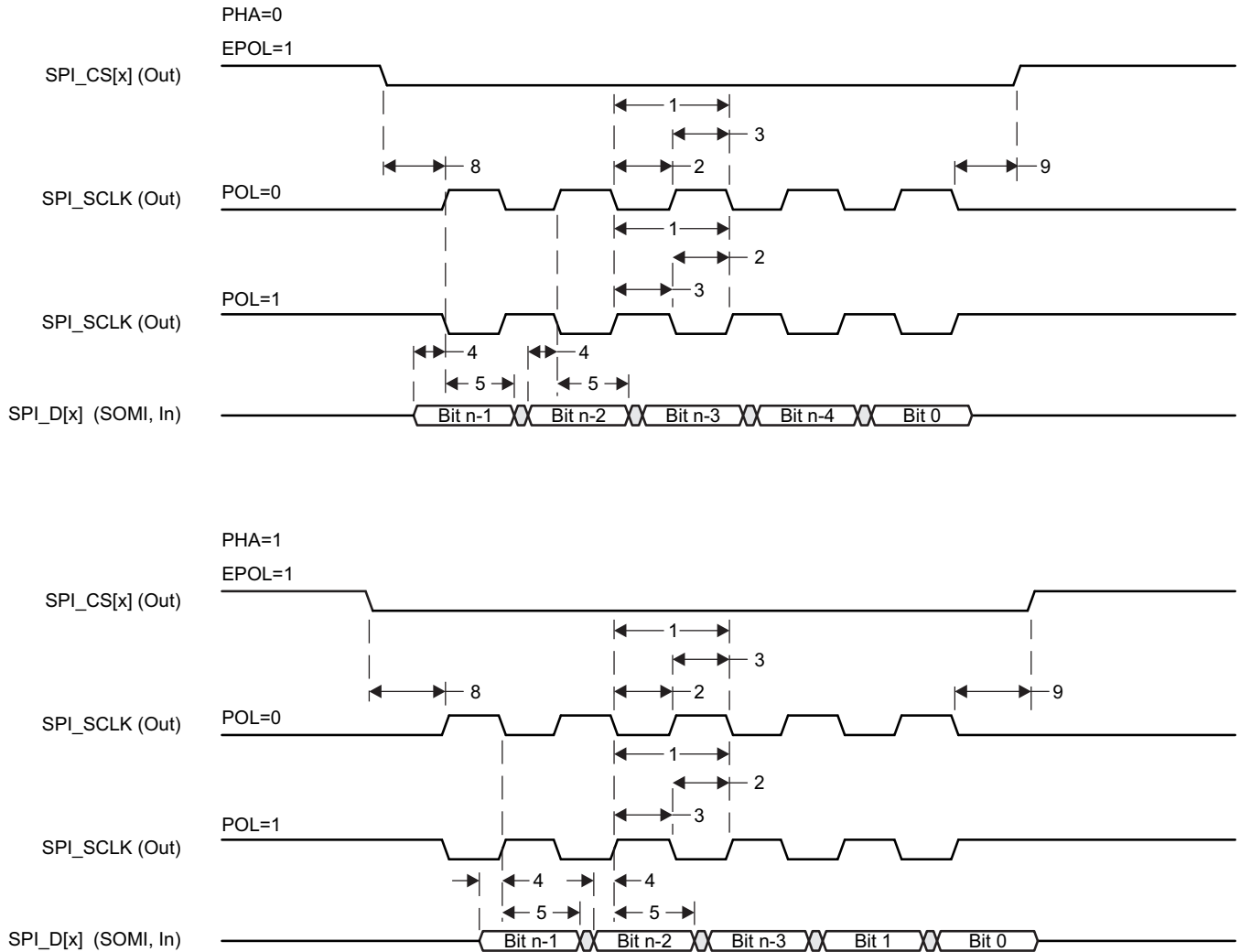


Figure 7-90. SPI Master Mode Receive Timing

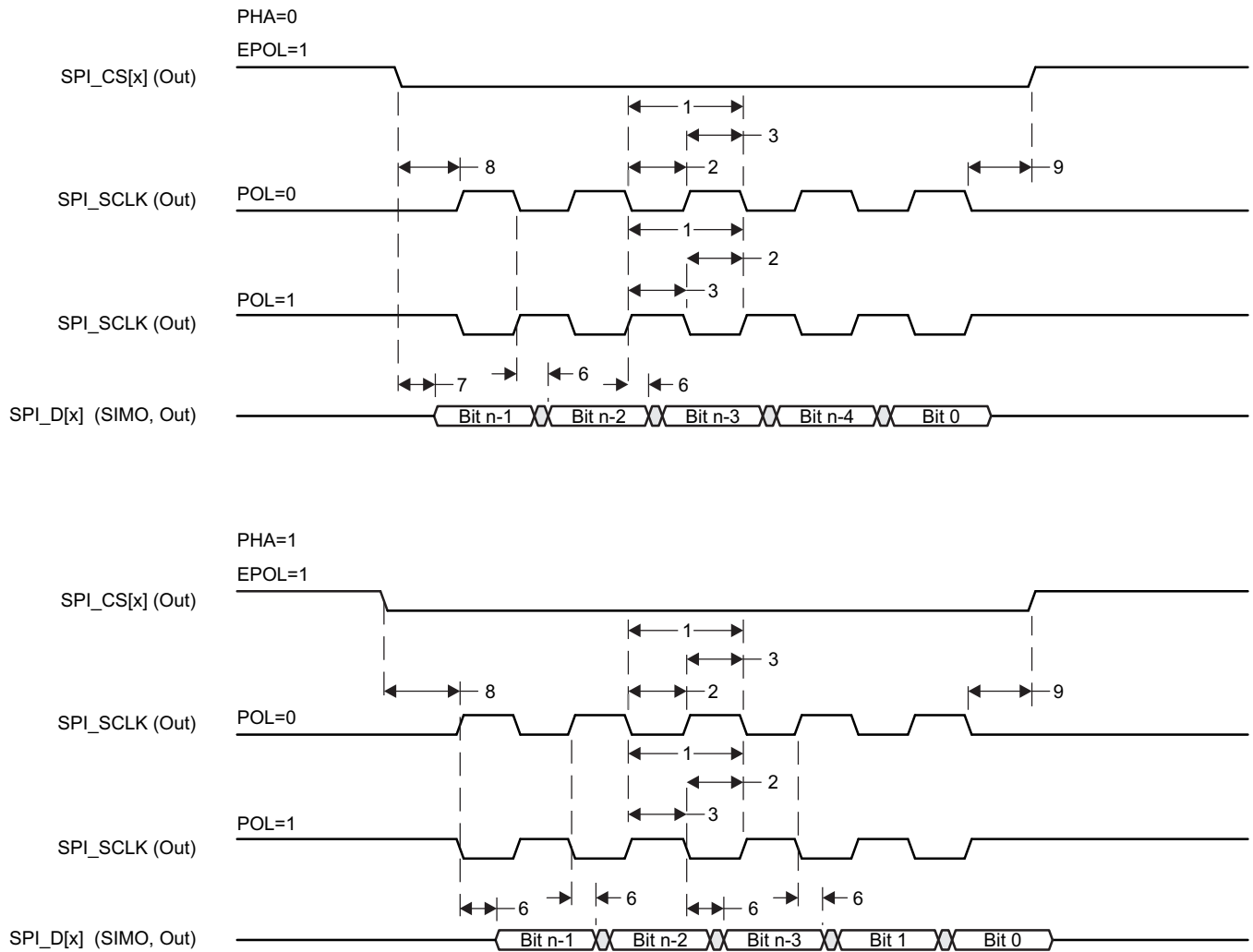


Figure 7-91. SPI Master Mode Transmit Timing

7.13 Multimedia Card (MMC) Interface

For more information, see the Multimedia Card (MMC) section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

7.13.1 MMC Electrical Data and Timing

Table 7-86. MMC Timing Conditions

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_r | Input signal rise time | 1 | | 5 | ns |
| t_f | Input signal fall time | 1 | | 5 | ns |
| Output Condition | | | | | |
| C_{load} | Output load capacitance | 3 | | 30 | pF |

Table 7-87. Timing Requirements for MMC[x]_CMD and MMC[x]_DAT[7:0]

(see Figure 7-92)

| NO. | | | 1.8-V MODE | | | 3.3-V MODE | | | UNIT |
|-----|---------------------|---|--|--------|------|------------|------|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su}(CMDV-CLKH)$ | Setup time, MMC_CMD valid before MMC_CLK rising clock edge | 4.1 | | | 4.1 | | | ns |
| 2 | $t_h(CLKH-CMDV)$ | Hold time, MMC_CMD valid after MMC_CLK rising clock edge | Industrial extended temperature (-40°C to 125°C) | MMC0-2 | 3.76 | | 3.76 | | ns |
| | | | All other temperature ranges | MMC0 | 3.76 | | 2.52 | | |
| | | | | MMC1 | 3.76 | | 3.03 | | |
| 3 | $t_{su}(DATV-CLKH)$ | Setup time, MMC_DATx valid before MMC_CLK rising clock edge | 4.1 | | | 4.1 | | | ns |
| 4 | $t_h(CLKH-DATV)$ | Hold time, MMC_DATx valid after MMC_CLK rising clock edge | Industrial extended temperature (-40°C to 125°C) | MMC0-2 | 3.76 | | 3.76 | | ns |
| | | | All other temperature ranges | MMC0 | 3.76 | | 2.52 | | |
| | | | | MMC1 | 3.76 | | 3.03 | | |
| | | | | MMC2 | 3.76 | | 3.0 | | |

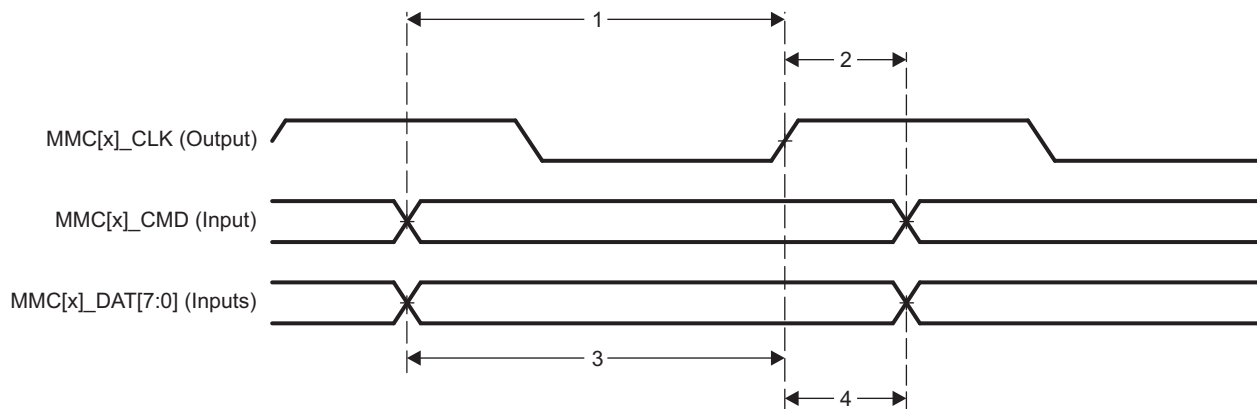


Figure 7-92. MMC[x]_CMD and MMC[x]_DAT[7:0] Input Timing

Table 7-88. Switching Characteristics for MMC[x]_CLK

(see Figure 7-93)

| NO. | PARAMETER | | STANDARD MODE | | | HIGH-SPEED MODE | | | UNIT |
|-----|----------------|--|-------------------------------------|-----|-----|-------------------------------------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 5 | $f_{op}(CLK)$ | Operating frequency, MMC_CLK | | | 24 | | | 48 | MHz |
| | $t_{cop}(CLK)$ | Operating period: MMC_CLK | 41.7 | | | 20.8 | | | ns |
| | $f_{id}(CLK)$ | Identification mode frequency, MMC_CLK | | | 400 | | | 400 | kHz |
| | $t_{cid}(CLK)$ | Identification mode period: MMC_CLK | 2500 | | | 2500 | | | ns |
| 6 | $t_{w}(CLKL)$ | Pulse duration, MMC_CLK low | $(0.5 \times P) - t_{r}(CLK)^{(1)}$ | | | $(0.5 \times P) - t_{r}(CLK)^{(1)}$ | | | ns |
| 7 | $t_{w}(CLKH)$ | Pulse duration, MMC_CLK high | $(0.5 \times P) - t_{r}(CLK)^{(1)}$ | | | $(0.5 \times P) - t_{r}(CLK)^{(1)}$ | | | ns |
| 8 | $t_{r}(CLK)$ | Rise time, all signals (10% to 90%) | | | 2.2 | | | 2.2 | ns |
| 9 | $t_{f}(CLK)$ | Fall time, all signals (10% to 90%) | | | 2.2 | | | 2.2 | ns |

(1) P = MMC_CLK period

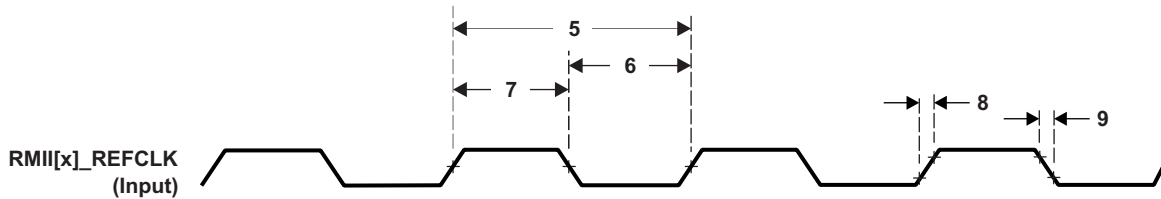


Figure 7-93. MMC[x]_CLK Timing

Table 7-89. Switching Characteristics for MMC[x]_CMD and MMC[x]_DAT[7:0]—Standard Mode

(see Figure 7-94)

| NO. | PARAMETER | | OPP100 | | | OPP50 | | | UNIT |
|-----|-------------------|---|--------|-----|-----|-------|-----|------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 10 | $t_{d}(CLKL-CMD)$ | Delay time, MMC_CLK falling clock edge to MMC_CMD transition | -4 | | 14 | -4 | | 17.5 | ns |
| 11 | $t_{d}(CLKL-DAT)$ | Delay time, MMC_CLK falling clock edge to MMC_DATx transition | -4 | | 14 | -4 | | 17.5 | ns |

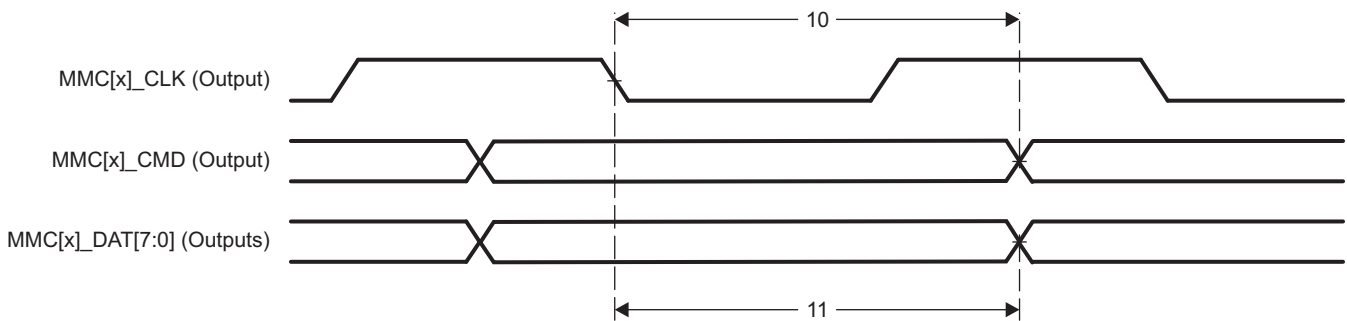


Figure 7-94. MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—Standard Mode

Table 7-90. Switching Characteristics for MMC[x]_CMD and MMC[x]_DAT[7:0]—High-Speed Mode

(see [Figure 7-95](#))

| NO. | PARAMETER | | OPP100 | | | OPP50 | | | UNIT |
|-----|--------------------------|--|--------|-----|-----|-------|-----|------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 12 | $t_{d(\text{CLKL-CMD})}$ | Delay time, MMC_CLK rising clock edge to MMC_CMD transition | 3 | | 14 | 3 | | 17.5 | ns |
| 13 | $t_{d(\text{CLKL-DAT})}$ | Delay time, MMC_CLK rising clock edge to MMC_DATx transition | 3 | | 14 | 3 | | 17.5 | ns |

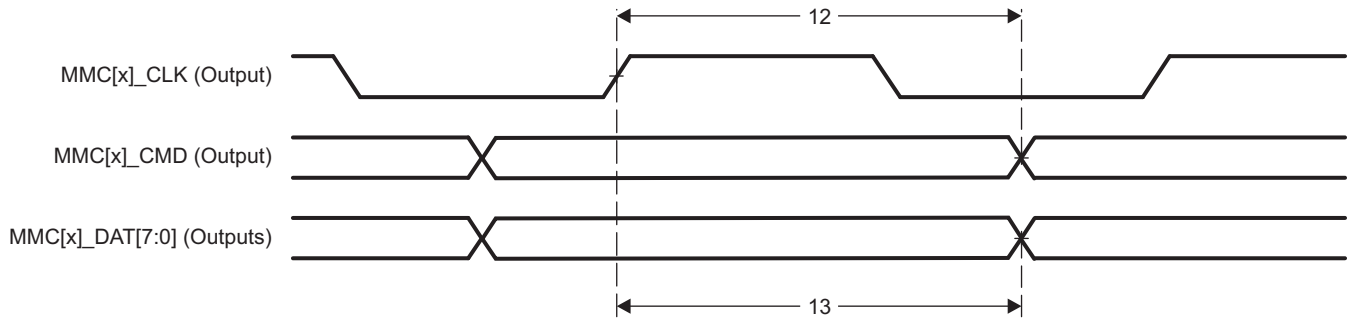


Figure 7-95. MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—High-Speed Mode

7.14 Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)

For more information, see the Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem Interface (PRU-ICSS) section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

7.14.1 Programmable Real-Time Unit (PRU-ICSS PRU)

Table 7-91. PRU-ICSS PRU Timing Conditions

| PARAMETER | | MIN | MAX | UNIT |
|-------------------------|-----------------------------------|-----|-----|------|
| Output Condition | | | | |
| C _{load} | Capacitive load for each bus line | | 30 | pF |

7.14.1.1 PRU-ICSS PRU Direct Input/Output Mode Electrical Data and Timing

Table 7-92. PRU-ICSS PRU Timing Requirements - Direct Input Mode

(see [Figure 7-96](#))

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|----------------------|---|----------------------|------|------|
| 1 | t _{w(GPI)} | Pulse width, GPI | 2 × P ⁽¹⁾ | | ns |
| 2 | t _{r(GPI)} | Rise time, GPI | 1.00 | 3.00 | ns |
| | t _{f(GPI)} | Fall time, GPI | 1.00 | 3.00 | ns |
| 3 | t _{sk(GPI)} | Internal skew between GPI[n:0] signals ⁽²⁾ | PRU0 | 1.00 | ns |
| | | | PRU1 | 3.00 | |

(1) P = L3_CLK (PRU-ICSS ocp clock) period.

(2) n = 16

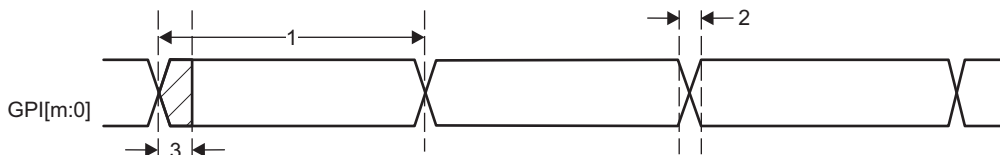


Figure 7-96. PRU-ICSS PRU Direct Input Timing

Table 7-93. PRU-ICSS PRU Switching Requirements – Direct Output Mode

(see [Figure 7-69](#))

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|----------------------|---|----------------------|------|------|
| 1 | t _{w(GPO)} | Pulse width, GPO | 2 × P ⁽¹⁾ | | ns |
| 2 | t _{r(GPO)} | Rise time, GPO | 1.00 | 3.00 | ns |
| | t _{f(GPO)} | Fall time, GPO | 1.00 | 3.00 | ns |
| 3 | t _{sk(GPO)} | Internal skew between GPO[n:0] signals ⁽²⁾ | PRU0 | 1.00 | ns |
| | | | PRU1 | 5.00 | |

(1) P = L3_CLK (PRU-ICSS ocp clock) period

(2) n = 15

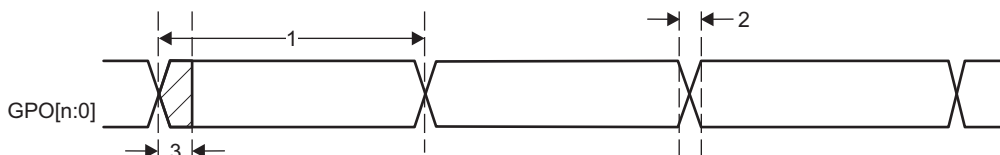


Figure 7-97. PRU-ICSS PRU Direct Output Timing

7.14.1.2 PRU-ICSS PRU Parallel Capture Mode Electrical Data and Timing

Table 7-94. PRU-ICSS PRU Timing Requirements - Parallel Capture Mode

(see Figure 7-98 and Figure 7-99)

| NO. | | | MIN | MAX | UNIT |
|-----|--------------------------|---|-------|------|------|
| 1 | $t_{c(CLOCKIN)}$ | Cycle time, CLOCKIN | 20.00 | | ns |
| 2 | $t_{w(CLOCKIN_L)}$ | Pulse duration, CLOCKIN low | 10.00 | | ns |
| 3 | $t_{w(CLOCKIN_H)}$ | Pulse duration, CLOCKIN high | 10.00 | | ns |
| 4 | $t_{r(CLOCKIN)}$ | Rising time, CLOCKIN | 1.00 | 3.00 | ns |
| 5 | $t_{f(CLOCKIN)}$ | Falling time, CLOCKIN | 1.00 | 3.00 | ns |
| 6 | $t_{su(DATAIN-CLOCKIN)}$ | Setup time, DATAIN valid before CLOCKIN | 5.00 | | ns |
| 7 | $t_{h(CLOCKIN-DATAIN)}$ | Hold time, DATAIN valid after CLOCKIN | 0.00 | | ns |
| 8 | $t_{r(DATAIN)}$ | Rising time, DATAIN | 1.00 | 3.00 | ns |
| | $t_{f(DATAIN)}$ | Falling time, DATAIN | 1.00 | 3.00 | ns |

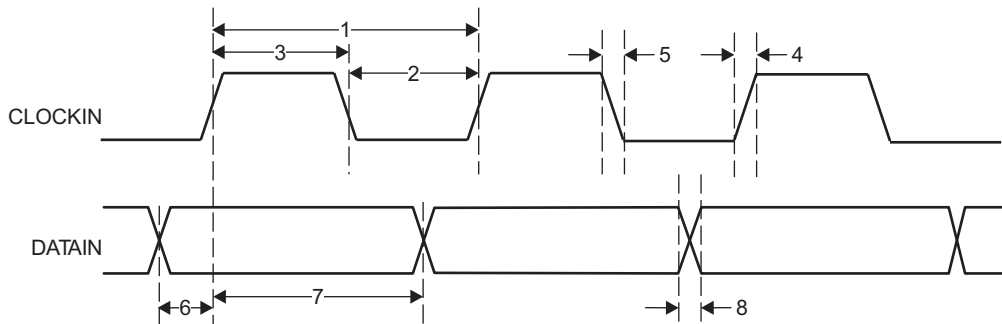


Figure 7-98. PRU-ICSS PRU Parallel Capture Timing - Rising Edge Mode

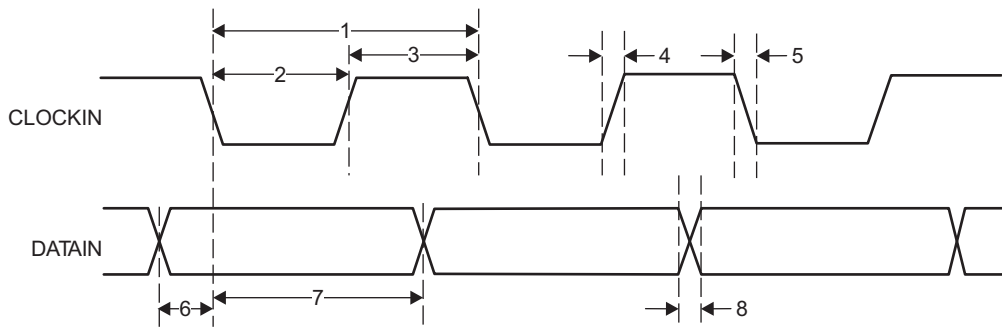


Figure 7-99. PRU-ICSS PRU Parallel Capture Timing - Falling Edge Mode

7.14.1.3 PRU-ICSS PRU Shift Mode Electrical Data and Timing

Table 7-95. PRU-ICSS PRU Timing Requirements – Shift In Mode

(see Figure 7-100)

| NO. | | | MIN | MAX | UNIT |
|-----|-----------------|----------------------|-----------------------|-----------------------|------|
| 1 | $t_{c(DATAIN)}$ | Cycle time, DATAIN | 10.00 | | ns |
| 2 | $t_{w(DATAIN)}$ | Pulse width, DATAIN | $0.45 \times P^{(1)}$ | $0.55 \times P^{(1)}$ | ns |
| 3 | $t_{r(DATAIN)}$ | Rising time, DATAIN | 1.00 | 3.00 | ns |
| 4 | $t_{f(DATAIN)}$ | Falling time, DATAIN | 1.00 | 3.00 | ns |

(1) P = L3_CLK (PRU-ICSS ocp clock) period.

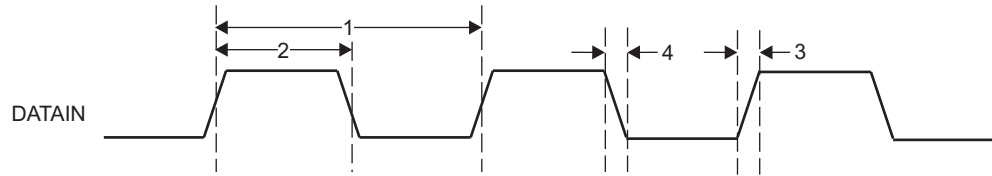


Figure 7-100. PRU-ICSS PRU Shift In Timing

Table 7-96. PRU-ICSS PRU Switching Requirements - Shift Out Mode

(see Figure 7-101)

| NO. | | | MIN | MAX | UNIT |
|-----|--------------------------------|---------------------------------------|-----------------------|-----------------------|------|
| 1 | $t_c(\text{CLOCKOUT})$ | Cycle time, CLOCKOUT | 10.00 | | ns |
| 2 | $t_w(\text{CLOCKOUT})$ | Pulse width, CLOCKOUT | $0.45 \times P^{(1)}$ | $0.55 \times P^{(1)}$ | ns |
| 3 | $t_r(\text{CLOCKOUT})$ | Rising time, CLOCKOUT | 1.00 | 3.00 | ns |
| 4 | $t_f(\text{CLOCKOUT})$ | Falling time, CLOCKOUT | 1.00 | 3.00 | ns |
| 5 | $t_d(\text{CLOCKOUT-DATAOUT})$ | Delay time, CLOCKOUT to DATAOUT valid | 0.00 | 3.00 | ns |
| 6 | $t_r(\text{DATAOUT})$ | Rising time, DATAOUT | 1.00 | 3.00 | ns |
| | $t_f(\text{DATAOUT})$ | Falling time, DATAOUT | 1.00 | 3.00 | ns |

(1) P = L3_CLK (PRU-ICSS ocp clock) period.

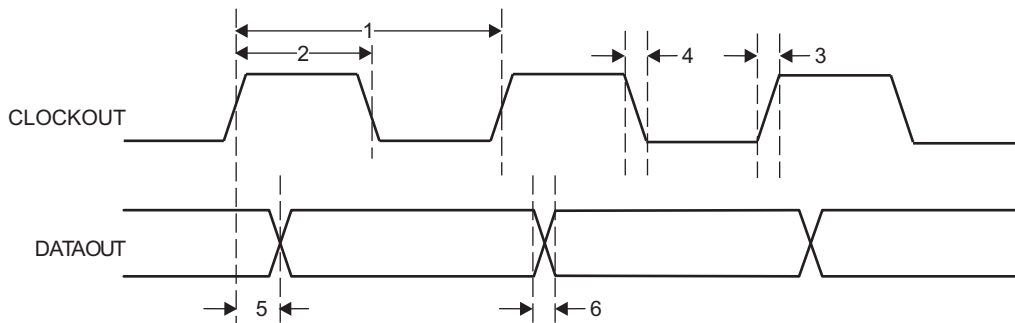


Figure 7-101. PRU-ICSS PRU Shift Out Timing

7.14.2 PRU-ICSS EtherCAT (PRU-ICSS ECAT)

Table 7-97. PRU-ICSS ECAT Timing Conditions

| PARAMETER | | MIN | MAX | UNIT |
|-------------------------|-----------------------------------|-----|-----|------|
| Output Condition | | | | |
| C_{load} | Capacitive load for each bus line | | 30 | pF |

7.14.2.1 PRU-ICSS ECAT Electrical Data and Timing

Table 7-98. PRU-ICSS ECAT Timing Requirements – Input Validated With LATCH_IN

(see Figure 7-102)

| NO. | | | MIN | MAX | UNIT |
|-----|---|---|--------|------|------|
| 1 | $t_w(\text{EDIO_LATCH_IN})$ | Pulse width, EDIO_LATCH_IN | 100.00 | | ns |
| 2 | $t_r(\text{EDIO_LATCH_IN})$ | Rising time, EDIO_LATCH_IN | 1.00 | 3.00 | ns |
| 3 | $t_f(\text{EDIO_LATCH_IN})$ | Falling time, EDIO_LATCH_IN | 1.00 | 3.00 | ns |
| 4 | $t_{su}(\text{EDIO_DATA_IN-EDIO_LATCH_IN})$ | Setup time, EDIO_DATA_IN valid before EDIO_LATCH_IN active edge | 20.00 | | ns |
| 5 | $t_h(\text{EDIO_LATCH_IN-EDIO_DATA_IN})$ | Hold time, EDIO_DATA_IN valid after EDIO_LATCH_IN active edge | 20.00 | | ns |

Table 7-98. PRU-ICSS ECAT Timing Requirements – Input Validated With LATCH_IN (continued)

(see Figure 7-102)

| NO. | | | MIN | MAX | UNIT |
|-----|-------------------------|----------------------------|------|------|------|
| 6 | $t_{r}(EDIO_DATA_IN)$ | Rising time, EDIO_DATA_IN | 1.00 | 3.00 | ns |
| | $t_{f}(EDIO_DATA_IN)$ | Falling time, EDIO_DATA_IN | 1.00 | 3.00 | ns |

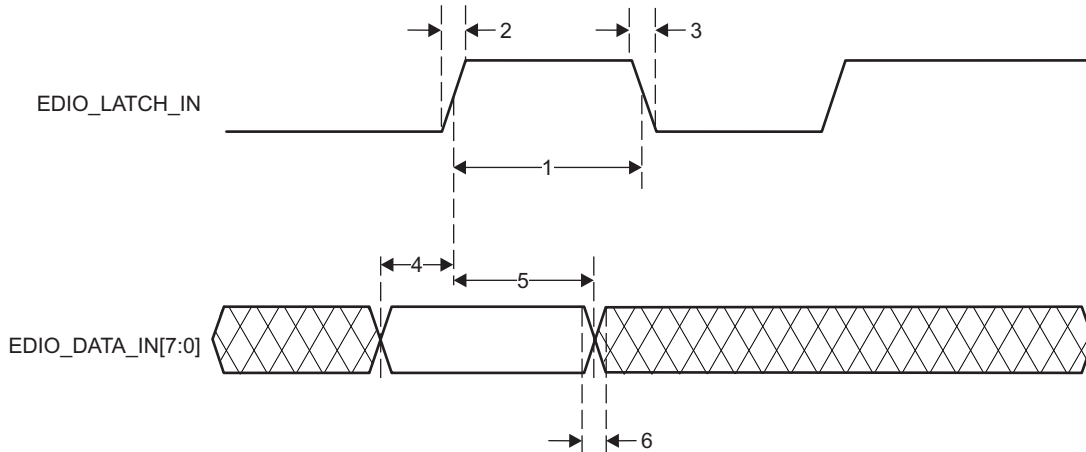


Figure 7-102. PRU-ICSS ECAT Input Validated With LATCH_IN Timing

Table 7-99. PRU-ICSS ECAT Timing Requirements – Input Validated With SYNCx

(see Figure 7-103)

| NO. | | | MIN | MAX | UNIT |
|-----|--|---|--------|------|------|
| 1 | $t_w(EDC_SYNCx_OUT)$ | Pulse width, EDC_SYNCx_OUT | 100.00 | | ns |
| 2 | $t_r(EDC_SYNCx_OUT)$ | Rising time, EDC_SYNCx_OUT | 1.00 | 3.00 | ns |
| 3 | $t_f(EDC_SYNCx_OUT)$ | Falling time, EDC_SYNCx_OUT | 1.00 | 3.00 | ns |
| 4 | $t_{su}(EDIO_DATA_IN-EDC_SYNCx_OUT)$ | Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT active edge | 20.00 | | ns |
| 5 | $t_h(EDC_SYNCx_OUT-EDIO_DATA_IN)$ | Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT active edge | 20.00 | | ns |
| 6 | $t_r(EDIO_DATA_IN)$ | Rising time, EDIO_DATA_IN | 1.00 | 3.00 | ns |
| | $t_f(EDIO_DATA_IN)$ | Falling time, EDIO_DATA_IN | 1.00 | 3.00 | ns |

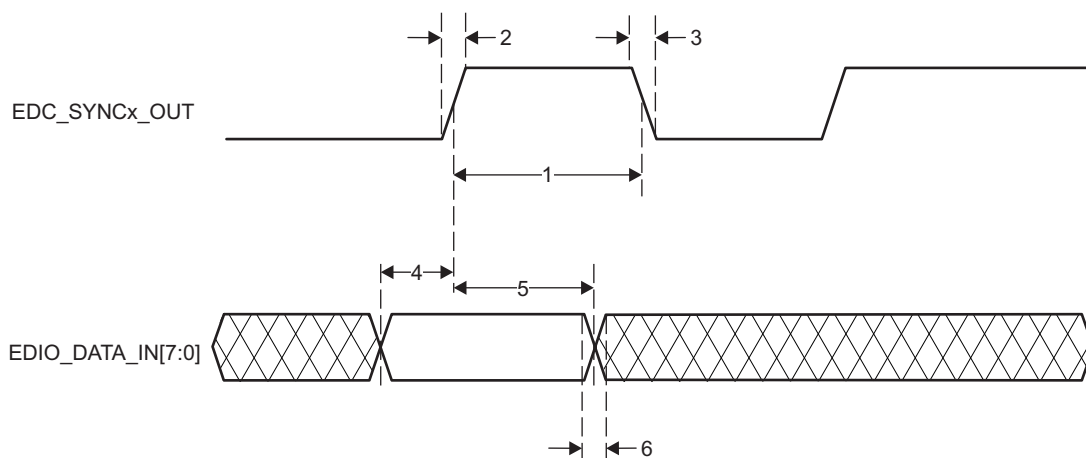


Figure 7-103. PRU-ICSS ECAT Input Validated With SYNCx Timing

Table 7-100. PRU-ICSS ECAT Timing Requirements – Input Validated With Start of Frame (SOF)

(see Figure 7-104)

| NO. | | | MIN | MAX | UNIT |
|-----|---|--|--------------------|--------------------|------|
| 1 | $t_w(\text{EDIO_SOF})$ | Pulse duration, EDIO_SOF | $4 \times P^{(1)}$ | $5 \times P^{(1)}$ | ns |
| 2 | $t_r(\text{EDIO_SOF})$ | Rising time, EDIO_SOF | 1.00 | 3.00 | ns |
| 3 | $t_f(\text{EDIO_SOF})$ | Falling time, EDIO_SOF | 1.00 | 3.00 | ns |
| 4 | $t_{su}(\text{EDIO_DATA_IN-EDIO_SOF})$ | Setup time, EDIO_DATA_IN valid before EDIO_SOF active edge | 20.00 | | ns |
| 5 | $t_h(\text{EDIO_SOF-EDIO_DATA_IN})$ | Hold time, EDIO_DATA_IN valid after EDIO_SOF active edge | 20.00 | | ns |
| 6 | $t_r(\text{EDIO_DATA_IN})$ | Rising time, EDIO_DATA_IN | 1.00 | 3.00 | ns |
| | $t_f(\text{EDIO_DATA_IN})$ | Falling time, EDIO_DATA_IN | 1.00 | 3.00 | ns |

(1) P = PRU-ICSS IEP clock source period.

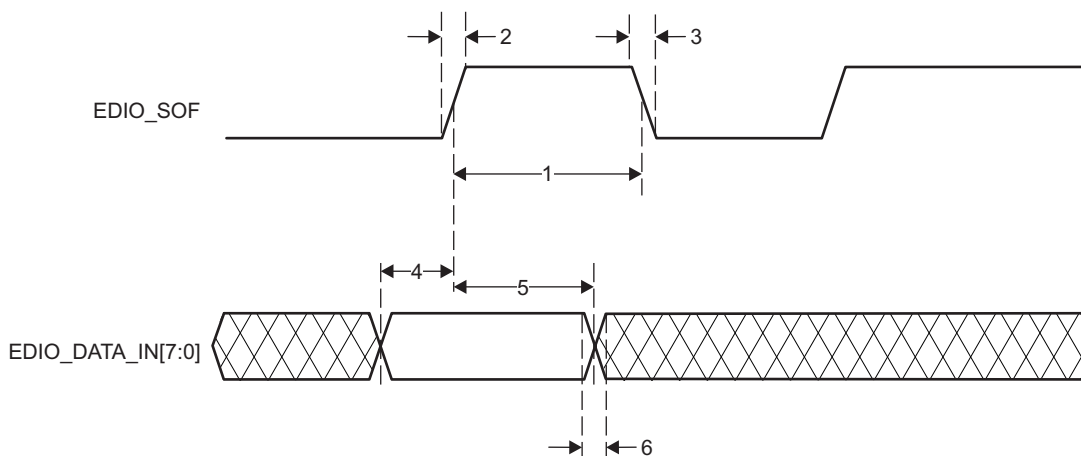


Figure 7-104. PRU-ICSS ECAT Input Validated With SOF

Table 7-101. PRU-ICSS ECAT Timing Requirements - LATCHx_IN

(see Figure 7-105)

| NO. | | | MIN | MAX | UNIT |
|-----|-------------------------------|-------------------------------|--------------------|------|------|
| 1 | $t_w(\text{EDC_LATCHx_IN})$ | Pulse duration, EDC_LATCHx_IN | $3 \times P^{(1)}$ | | ns |
| 2 | $t_r(\text{EDC_LATCHx_IN})$ | Rising time, EDC_LATCHx_IN | 1.00 | 3.00 | ns |
| 3 | $t_f(\text{EDC_LATCHx_IN})$ | Falling time, EDC_LATCHx_IN | 1.00 | 3.00 | ns |

(1) P = PRU-ICSS IEP clock source period.

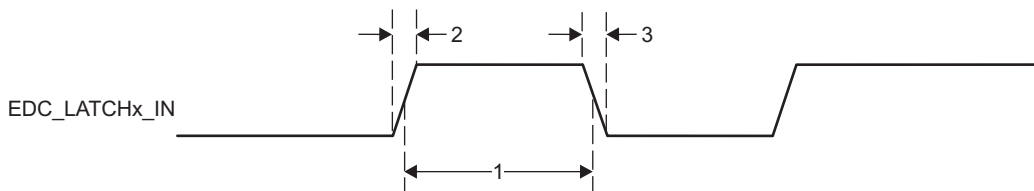


Figure 7-105. PRU-ICSS ECAT LATCHx_IN Timing

Table 7-102. PRU-ICSS ECAT Switching Requirements - Digital I/Os

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|--|--|---------------------|---------------------|------|
| 1 | $t_w(\text{EDIO_OUTVALID})$ | Pulse duration, EDIO_OUTVALID | $14 \times P^{(1)}$ | $32 \times P^{(1)}$ | ns |
| 2 | $t_r(\text{EDIO_OUTVALID})$ | Rising time, EDIO_OUTVALID | 1.00 | 3.00 | ns |
| 3 | $t_f(\text{EDIO_OUTVALID})$ | Falling time, EDIO_OUTVALID | 1.00 | 3.00 | ns |
| 4 | $t_d(\text{EDIO_OUTVALID-EDIO_DATA_OUT})$ | Delay time, EDIO_OUTVALID to EDIO_DATA_OUT | 0.00 | $18 \times P^{(1)}$ | ns |
| 5 | $t_r(\text{EDIO_DATA_OUT})$ | Rising time, EDIO_DATA_OUT | 1.00 | 3.00 | ns |
| 6 | $t_f(\text{EDIO_DATA_OUT})$ | Falling time, EDIO_DATA_OUT | 1.00 | 3.00 | ns |
| 7 | $t_{sk}(\text{EDIO_DATA_OUT})$ | EDIO_DATA_OUT skew | | 8.00 | ns |

(1) P = PRU-ICSS IEP clock source period.

7.14.3 PRU-ICSS MII_RT and Switch

Table 7-103. PRU-ICSS MII_RT Switch Timing Conditions

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|-----------|-----|-----------|------|
| Input Conditions | | | | | |
| t_R | Input signal rise time | $1^{(1)}$ | | $3^{(1)}$ | ns |
| t_F | Input signal fall time | $1^{(1)}$ | | $3^{(1)}$ | ns |
| Output Condition | | | | | |
| C_{LOAD} | Output load capacitance | 3 | | 20 | pF |

(1) Except when specified otherwise.

7.14.3.1 PRU-ICSS MDIO Electrical Data and Timing

Table 7-104. PRU-ICSS MDIO Timing Requirements – MDIO_DATA

(see [Figure 7-106](#))

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|---------------------------|--|-----|-----|-----|------|
| 1 | $t_{su}(\text{MDIO-MDC})$ | Setup time, MDIO valid before MDC high | 90 | | | ns |
| 2 | $t_h(\text{MDIO-MDC})$ | Hold time, MDIO valid from MDC high | 0 | | | ns |

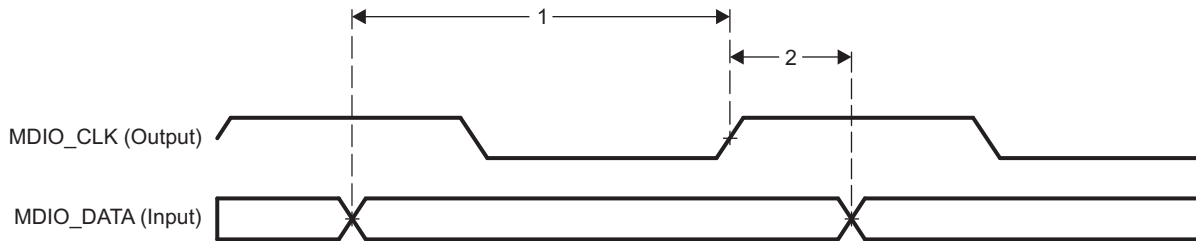


Figure 7-106. PRU-ICSS MDIO_DATA Timing - Input Mode

Table 7-105. PRU-ICSS MDIO Switching Characteristics - MDIO_CLK

(see [Figure 7-107](#))

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|--------------------|--------------------------|-----|-----|-----|------|
| 1 | $t_c(\text{MDC})$ | Cycle time, MDC | 400 | | | ns |
| 2 | $t_w(\text{MDCH})$ | Pulse duration, MDC high | 160 | | | ns |
| 3 | $t_w(\text{MDCL})$ | Pulse duration, MDC low | 160 | | | ns |
| 4 | $t_t(\text{MDC})$ | Transition time, MDC | | | 5 | ns |

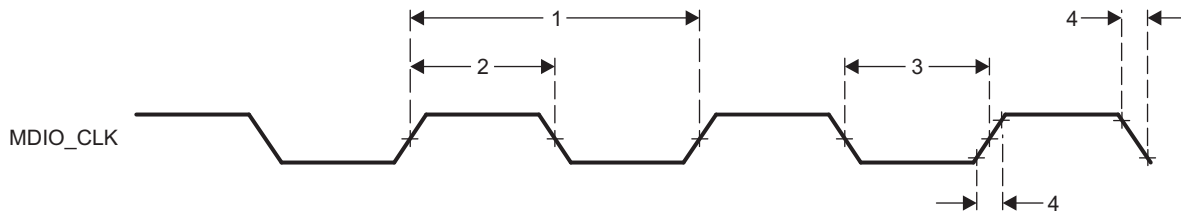


Figure 7-107. PRU-ICSS MDIO_CLK Timing

Table 7-106. PRU-ICSS MDIO Switching Characteristics – MDIO_DATA

(see Figure 7-108)

| NO. | | MIN | TYP | MAX | UNIT |
|-----|--|-----|-----|-----|------|
| 1 | $t_{d(MDC-MDIO)}$ Delay time, MDC high to MDIO valid | 10 | | 390 | ns |

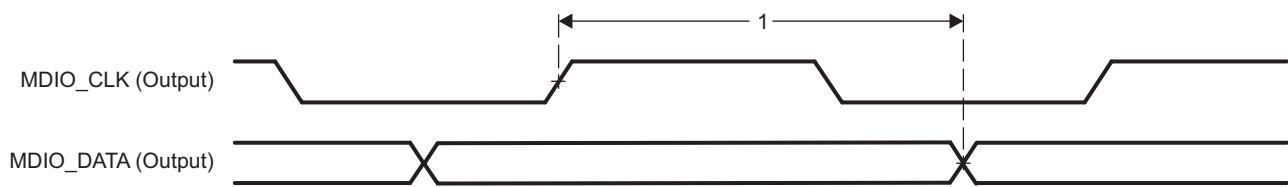


Figure 7-108. PRU-ICSS MDIO_DATA Timing – Output Mode

7.14.3.2 PRU-ICSS MII_RT Electrical Data and Timing

NOTE

In order to guarantee the MII_RT I/O timing values published in the device data manual, the PRU ocp_clk clock must be configured for 200 MHz (default value) and the TX_CLK_DELAY bit field in the PRUSS_MII_RT_TXCFG0/1 register must be set to 6 h (non-default value).

Table 7-107. PRU-ICSS MII_RT Timing Requirements – MII_RXCLK

(see Figure 7-109)

| NO. | | 10 Mbps | | | 100 Mbps | | | UNIT |
|-----|---|---------|-----|--------|----------|-----|--------|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_c(RX_CLK)$ Cycle time, RX_CLK | 399.96 | | 400.04 | 39.996 | | 40.004 | ns |
| 2 | $t_w(RX_CLKH)$ Pulse duration, RX_CLK high | 140 | | 260 | 14 | | 26 | ns |
| 3 | $t_w(RX_CLKL)$ Pulse duration, RX_CLK low | 140 | | 260 | 14 | | 26 | ns |
| 4 | $t_t(RX_CLK)$ Transition time, RX_CLK | | | 3 | | | 3 | ns |

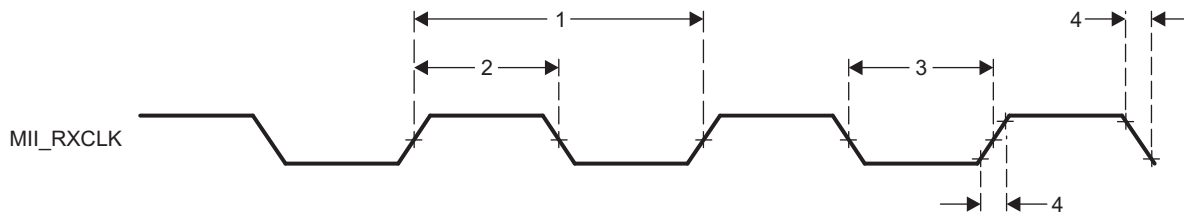


Figure 7-109. PRU-ICSS MII_RXCLK Timing

Table 7-108. PRU-ICSS MII_RT Timing Requirements - MII[x]_TXCLK

(see Figure 7-110)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|-----|-----------------|-----------------------------|---------|-----|--------|----------|-----|--------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_c(TX_CLK)$ | Cycle time, TX_CLK | 399.96 | | 400.04 | 39.996 | | 40.004 | ns |
| 2 | $t_w(TX_CLKH)$ | Pulse duration, TX_CLK high | 140 | | 260 | 14 | | 26 | ns |
| 3 | $t_w(TX_CLKL)$ | Pulse duration, TX_CLK low | 140 | | 260 | 14 | | 26 | ns |
| 4 | $t_t(TX_CLK)$ | Transition time, TX_CLK | | | 3 | | | 3 | ns |

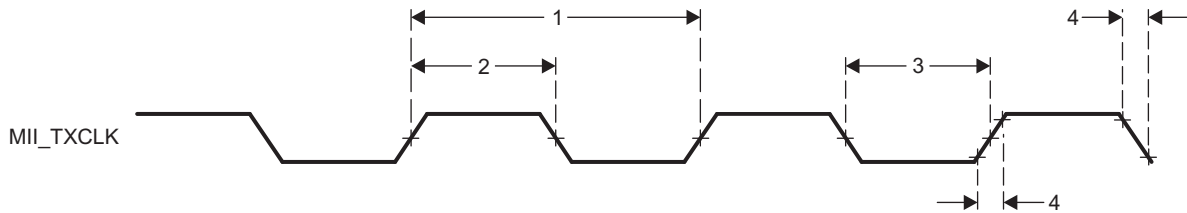


Figure 7-110. PRU-ICSS MII_TXCLK Timing

Table 7-109. PRU-ICSS MII_RT Timing Requirements - MII_RXD[3:0], MII_RXDV, and MII_RXER

(see Figure 7-111)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|-----|--------------------------|--|---------|-----|-----|----------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su}(RXD-RX_CLK)$ | Setup time, RXD[3:0] valid before RX_CLK | 8 | | 8 | 8 | | ns | |
| | $t_{su}(RX_DV-RX_CLK)$ | Setup time, RX_DV valid before RX_CLK | | | | | | | |
| | $t_{su}(RX_ER-RX_CLK)$ | Setup time, RX_ER valid before RX_CLK | | | | | | | |
| 2 | $t_h(RX_CLK-RXD)$ | Hold time RXD[3:0] valid after RX_CLK | 8 | | 8 | 8 | | ns | |
| | $t_h(RX_CLK-RX_DV)$ | Hold time RX_DV valid after RX_CLK | | | | | | | |
| | $t_h(RX_CLK-RX_ER)$ | Hold time RX_ER valid after RX_CLK | | | | | | | |

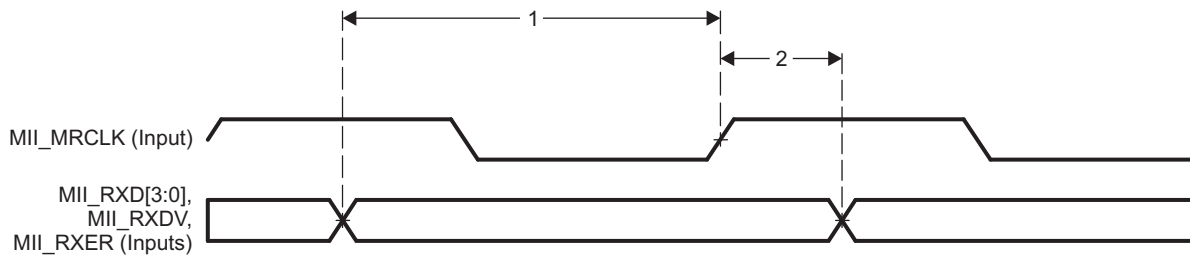


Figure 7-111. PRU-ICSS MII_RXD[3:0], MII_RXDV, and MII_RXER Timing

Table 7-110. PRU-ICSS MII_RT Switching Characteristics - MII_TXD[3:0] and MII_TXEN

(see [Figure 7-112](#))

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|-----|-----------------------|---|---------|-----|-----|----------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_d(TX_CLK-TXD)$ | Delay time, TX_CLK high to TXD[3:0] valid | 5 | | 25 | 5 | | 25 | ns |
| | $t_d(TX_CLK-TX_EN)$ | Delay time, TX_CLK to TX_EN valid | | | | | | | |

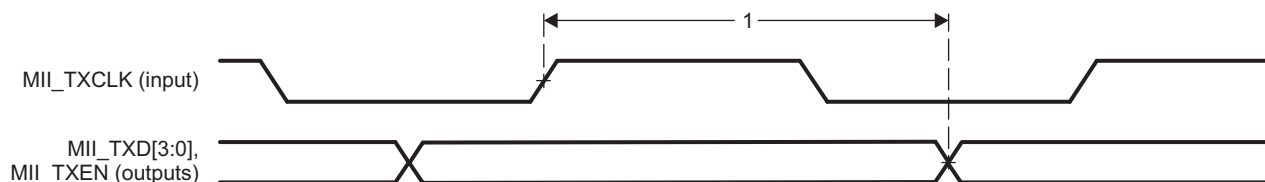


Figure 7-112. PRU-ICSS MII_TXD[3:0], MII_TXEN Timing

7.14.4 PRU-ICSS Universal Asynchronous Receiver Transmitter (PRU-ICSS UART)

Table 7-111. Timing Requirements for PRU-ICSS UART Receive

(see [Figure 7-113](#))

| NO. | | | MIN | MAX | UNIT |
|-----|-----------|---|---------------|---------------|------|
| 3 | $t_w(RX)$ | Pulse duration, receive start, stop, data bit | $0.96U^{(1)}$ | $1.05U^{(1)}$ | ns |

(1) $U = \text{UART baud time} = 1/\text{programmed baud rate}$.

Table 7-112. Switching Characteristics Over Recommended Operating Conditions for PRU-ICSS UART Transmit

(see [Figure 7-113](#))

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|--------------------------------|--|---------------|---------------|------|
| 1 | $f_{\text{baud}}(\text{baud})$ | Maximum programmable baud rate | 0 | 12 | MHz |
| 2 | $t_w(TX)$ | Pulse duration, transmit start, stop, data bit | $U - 2^{(1)}$ | $U + 2^{(1)}$ | ns |

(1) $U = \text{UART baud time} = 1/\text{programmed baud rate}$.

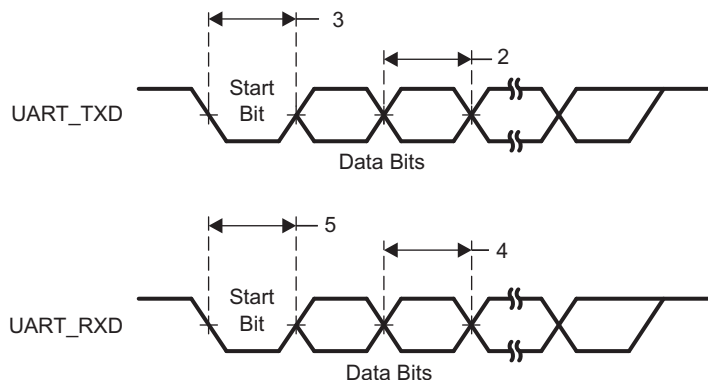


Figure 7-113. PRU-ICSS UART Timing

7.15 Universal Asynchronous Receiver Transmitter (UART)

For more information, see the Universal Asynchronous Receiver Transmitter (UART) section of the [AM335x and AMIC110 Sitara Processors Technical Reference Manual](#).

7.15.1 UART Electrical Data and Timing

Table 7-113. Timing Requirements for UARTx Receive

(see [Figure 7-114](#))

| NO. | | MIN | MAX | UNIT |
|-----|---|---------------|---------------|------|
| 3 | $t_{w(RX)}$ Pulse duration, receive start, stop, data bit | $0.96U^{(1)}$ | $1.05U^{(1)}$ | ns |

(1) U = UART baud time = $1/\text{programmed baud rate}$.

Table 7-114. Switching Characteristics for UARTx Transmit

(see [Figure 7-114](#))

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|---------------|---------------|------|
| 1 | $f_{\text{baud(baud)}}$ Maximum programmable baud rate | | 3.6864 | MHz |
| 2 | $t_{w(TX)}$ Pulse duration, transmit start, stop, data bit | $U - 2^{(1)}$ | $U + 2^{(1)}$ | ns |

(1) U = UART baud time = $1 / \text{programmed baud rate}$

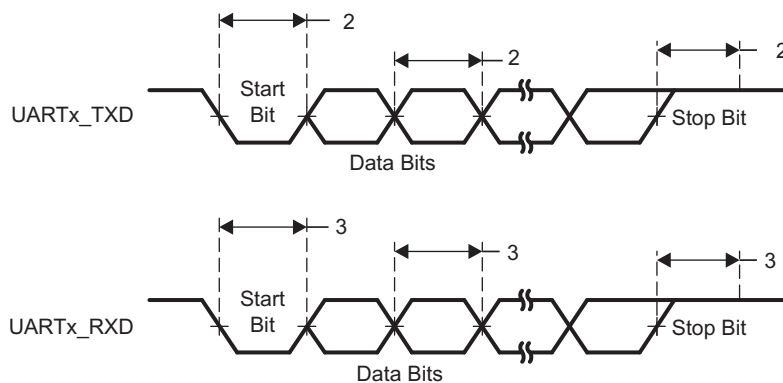


Figure 7-114. UART Timings

7.15.2 UART IrDA Interface

The IrDA module operates in three different modes:

- Slow infrared (SIR) (≤ 115.2 kbps)
- Medium infrared (MIR) (0.576 Mbps and 1.152 Mbps)
- Fast infrared (FIR) (4 Mbps).

Figure 7-115 shows the UART IrDA pulse parameters. Table 7-115 and Table 7-116 list the signaling rates and pulse durations for UART IrDA receive and transmit modes.

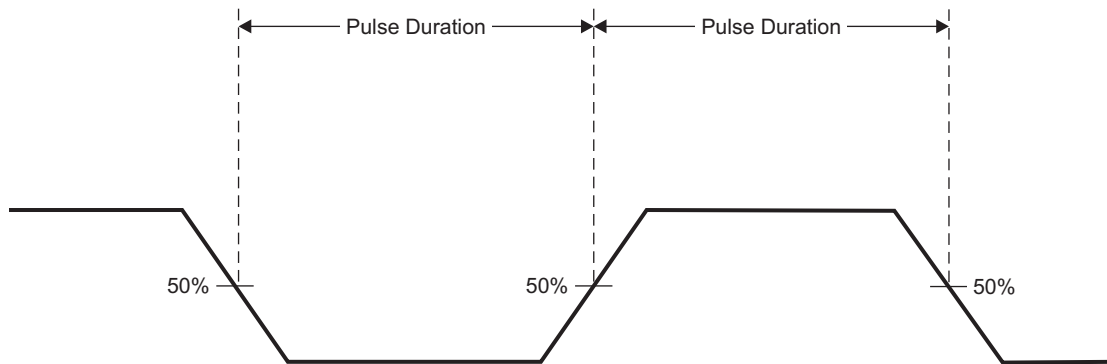


Figure 7-115. UART IrDA Pulse Parameters

Table 7-115. UART IrDA—Signaling Rate and Pulse Duration—Receive Mode

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | UNIT |
|-----------------------|---------------------------|-------|---------|
| | MIN | MAX | |
| SIR | | | |
| 2.4 kbps | 1.41 | 88.55 | μ s |
| 9.6 kbps | 1.41 | 22.13 | μ s |
| 19.2 kbps | 1.41 | 11.07 | μ s |
| 38.4 kbps | 1.41 | 5.96 | μ s |
| 57.6 kbps | 1.41 | 4.34 | μ s |
| 115.2 kbps | 1.41 | 2.23 | μ s |
| MIR | | | |
| 0.576 Mbps | 297.2 | 518.8 | ns |
| 1.152 Mbps | 149.6 | 258.4 | ns |
| FIR | | | |
| 4 Mbps (single pulse) | 67 | 164 | ns |
| 4 Mbps (double pulse) | 190 | 289 | ns |

Table 7-116. UART IrDA—Signaling Rate and Pulse Duration—Transmit Mode

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | UNIT |
|-----------------------|---------------------------|------|------|
| | MIN | MAX | |
| SIR | | | |
| 2.4 kbps | 78.1 | 78.1 | μs |
| 9.6 kbps | 19.5 | 19.5 | μs |
| 19.2 kbps | 9.75 | 9.75 | μs |
| 38.4 kbps | 4.87 | 4.87 | μs |
| 57.6 kbps | 3.25 | 3.25 | μs |
| 115.2 kbps | 1.62 | 1.62 | μs |
| MIR | | | |
| 0.576 Mbps | 414 | 419 | ns |
| 1.152 Mbps | 206 | 211 | ns |
| FIR | | | |
| 4 Mbps (single pulse) | 123 | 128 | ns |
| 4 Mbps (double pulse) | 248 | 253 | ns |

8 Device and Documentation Support

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, XAM3358AZCE). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

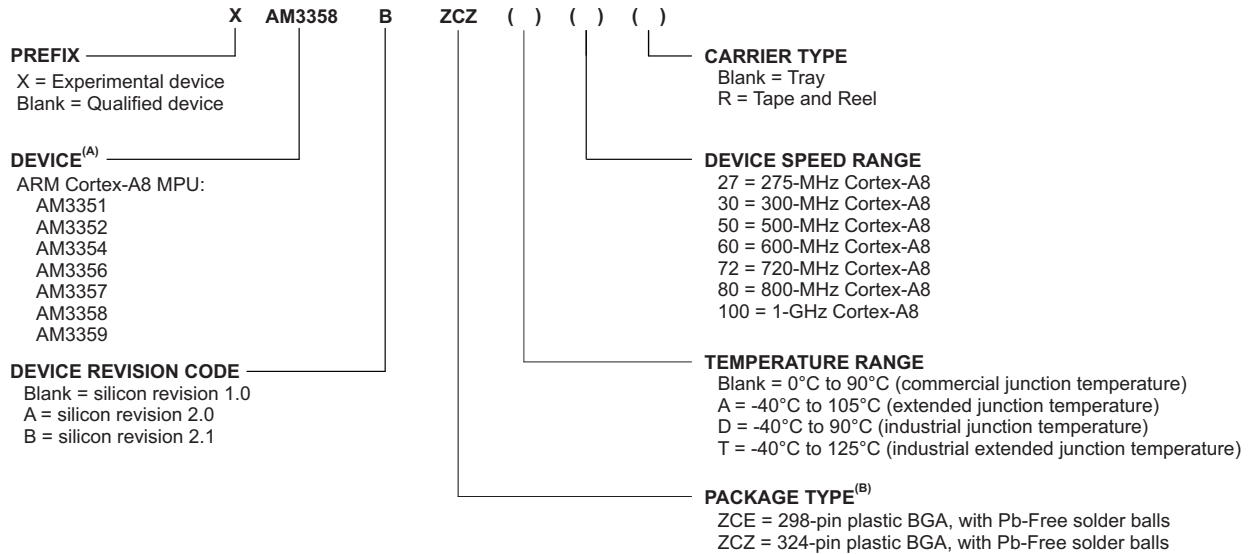
Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZCE), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, 27 is 275 MHz). [Figure 8-1](#) provides a legend for reading the complete device name for any AM335x device.

For orderable part numbers of AM335x devices in the ZCE and ZCZ package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [AM335x Sitara Processors Silicon Errata](#).



- A. The AM3358 device shown in this device nomenclature example is one of several valid part numbers for the AM335x family of devices. For orderable device part numbers, see the Package Option Addendum of this document.
- B. BGA = Ball grid array

Figure 8-1. AM335x Device Nomenclature

8.2 Tools and Software

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

Design Kits and Evaluation Modules

AM335x Evaluation Module Enables developers to immediately start evaluating the AM335x processor family (AM3351, AM3352, AM3354, AM3356, AM3358) and begin building applications such as portable navigation, portable gaming, home/building automation and others.

AM335x Starter Kit Provides a stable and affordable platform to quickly start evaluation of Sitara ARM Cortex-A8 AM335x Processors (AM3351, AM3352, AM3354, AM3356, AM3358) and accelerate development for smart appliance, industrial and networking applications. It is a low-cost development platform based on the ARM Cortex-A8 processor that is integrated with options such as Dual Gigabit Ethernet, DDR3 and LCD touch screen.

BeagleBone Black Development Board Low-cost, open source, community-supported development platform for ARM Cortex-A8 processor developers and hobbyists. Boot Linux in under 10-seconds and get started on Sitara AM335x ARM Cortex-A8 processor development in less than 5 minutes with just a single USB cable.

BeagleBone Development Board Low-cost, community-supported development platform for ARM Cortex-A8 processor developers. Boot Linux in under 10-seconds and get started on Sitara AM335x ARM Cortex-A8 processor development in less than 5 minutes with just a single USB cable. For TI-supported hardware platforms, consider the Sitara ARM AM335x Starter Kit or AM335x Evaluation Module.

Data Concentrator Evaluation Module Based on AM3359 as the main processor and has Power Line Communication (PLC) Module to support various OFDM PLC communication standards. TMDSDC3359 also has capability to support multiple interfaces, sub-1GHz and 2.4GHz RF, Ethernet, RS-232, and RS-485. This evaluation module is ideal development platform for smart grid infrastructure applications including data concentrator, convergent node of grid sensor network, and control equipment of power automation.

WiLink™ 8 Dual Band 2.4 & 5 GHz Wi-Fi® + Bluetooth® COM8 Evaluation Module Enables customers to add both Wi-Fi and Bluetooth to home and building automation, smart energy, gateways, wireless audio, enterprise, wearables and many more industrial and Internet of Things (IoT) applications. TI's WiLink 8 modules are certified and offer high throughput and extended range along with Wi-Fi and Bluetooth coexistence in a power-optimized design. Drivers for the Linux and Android high-level operating systems (HLOSs) are available free of charge

from TI for the Sitara AM335x microprocessor (Linux and Android version restrictions apply).

WiLink 8 Module 2.4 GHz WiFi + Bluetooth COM8 Evaluation Module Enables customers to add Wi-Fi and Bluetooth (WL183x module only) to embedded applications based on TI's Sitara microprocessors. TI's WiLink 8 Wi-Fi + Bluetooth modules are pre-certified and offer high throughput and extended range along with Wi-Fi and Bluetooth coexistence (WL183x modules only) in a power-optimized design. Drivers for the Linux and Android high-level operating systems (HLOSs) are available free of charge from TI for the Sitara AM335x microprocessor (Linux and Android version restrictions apply).

TI Designs

EtherCAT Communications Development Platform Allows designers to implement real-time EtherCAT communications standards in a broad range of industrial automation equipment. It enables low foot print designs in applications such as industrial automation, factory automation or industrial communication with minimal external components and with best in class low power performance.

PROFIBUS Communications Development Platform Allows designers to implement PROFIBUS communications standards in a broad range of industrial automation equipment. It enables low foot print designs in applications such as industrial automation, factory automation or industrial communication with minimal external components and with best in class low power performance.

Ethernet/IP Communications Development Platform Allows designers to implement Ethernet/IP communications standards in a broad range of industrial automation equipment. It enables low foot print designs in applications such as industrial automation, factory automation or industrial communication with minimal external components and with best in class low power performance.

Acontis EtherCAT Master Stack Reference Design Highly portable software stack that can be used on various embedded platforms. The EC-Master supports the high performance TI Sitara MPUs, it provides a sophisticated EtherCAT Master solution which customers can use to implement EtherCAT communication interface boards, EtherCAT based PLC or motion control applications. The EC-Master architectural design does not require additional tasks to be scheduled, thus the full stack functionality is available even on an OS less platform such as TI Starterware supported on AM335x. Due to this architecture combined with the high speed Ethernet driver it is possible to implement EtherCAT master based applications on the Sitara platform with short cycle times of 100 microseconds or even below.

Solar Inverter Gateway Development Platform Reference Design Adds communication functions to solar energy generation systems to enable system monitoring, real-time feedback, system updates, and more. The TIDEP0044 reference design describes the implementation of a solar inverter gateway using display, Ethernet, USB, and CAN on the TMDXEVM3358 featuring TI's AM335x processor.

G3 Power Line Communications Data Concentrator on BeagleBone Black Platform Offers a simplified approach for evaluating G3-PLC utilizing Beagle Bone Black powered by the Sitara AM335x processor. Users can establish a G3-PLC network with one service node. Single phase coupling is supported.

IEC 61850 Demonstration of Substation Bay Controller on Beaglebone Cape and Starter Kit Low-cost, simplified implementation of an IEC 61850 Substation Bay Controller is demonstrated by running the Triangle MicroWorks IEC 61850 stack efficiently on the TI AM335X platform with a Linux target layer definition. Many different substation automation applications can be built on top of the AM335X platform and 61850 stack demonstration.

PRU Real-Time I/O Evaluation Reference Design BeagleBone Black add-on board that allows users get to know TI's powerful Programmable Real-Time Unit (PRU) core and basic functionality. The PRU is a low-latency microcontroller subsystem integrated in the Sitara AM335x and AM437x family of devices. The PRU core is optimized for deterministic, real-time processing, direct access to I/Os and ultra-low-latency requirements. With LEDs and push buttons for GPIO, audio, a temp sensor, optional character display and more, this add-on board includes schematics, bill of materials (BOM), design files, and design guide to teach the basics of the PRU.

Smart Home and Energy Gateway Reference Design Provides example implementation for measurement, management and communication of energy systems for smart homes and buildings. This example design is a bridge between different communication interfaces, such as WiFi, Ethernet, ZigBee or Bluetooth, that are commonly found in residential and commercial buildings. Since objects in the house and buildings are becoming more and more connected, the gateway design needs to be flexible to accommodate different RF standard, since no single RF standard is dominating the market. This example gateway addresses this problem by supporting existing legacy RF standards (WiFi, Bluetooth) and newer RF standards (ZigBee, BLE).

Streaming Audio Reference Design Minimizes design time for customers by offering small form factor hardware and major software components, including streaming protocols and internet radio services. With this reference design, TI offers a quick and easy transition path to the AM335x and WiLink8 platform solution. This proven combo solution provides key advantages in this market category that helps bring your products to the next level.

Software

Processor SDK for AM335X Sitara Processors - Linux and TI-RTOS Support Unified software platform for TI embedded processors providing easy setup and fast out-of-the-box access to benchmarks and demos. All releases of Processor SDK are consistent across TI's broad portfolio, allowing developers to seamlessly reuse and migrate software across devices. Developing scalable platform solutions has never been easier than with the Processor SDK and TI's embedded processor solutions.

G3 Data Concentrator Power-Line Communication Modem G3-PLC standard for narrowband OFDM Power Line Communications. The data concentrator solution is designed for the head-end systems which communicate with the end meters ("service node") in the neighborhood area network.

PRIME Data Concentrator Power-Line Communication Modem PRIME standard for narrowband OFDM Power Line Communications. The data concentrator solution is designed for the head-end systems which communicate with the end meters ("service node") in the neighborhood area network.

TI Dual-Mode Bluetooth Stack Comprised of Single-Mode and Dual-Mode offerings implementing the Bluetooth 4.0 specification. The Bluetooth stack is fully Bluetooth Special Interest Group (SIG) qualified, certified and royalty-free, provides simple command line sample applications to speed development, and upon request has MFI capability.

Cryptography for TI Devices Enables encryption, crypto for TI devices. These files contain only cryptographic modules that were part of a TI software release. For the complete software release please search ti.com for your device part number, and download the Software Development Kit (SDK).

Development Tools

Clock Tree Tool for Sitara ARM Processors Interactive clock tree configuration software that provides information about the clocks and modules in Sitara devices.

Code Composer Studio (CCS) Integrated Development Environment (IDE) for Sitara ARM Processors

Integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

Pin Mux Tool Provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDK) or used to configure customer's custom software. Version 3 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

Power Estimation Tool (PET) Provides users the ability to gain insight in to the power consumption of select TI processors. The tool includes the ability for the user to choose multiple application scenarios and understand the power consumption as well as how advanced power saving techniques can be applied to further reduce overall power consumption.

Uniflash Standalone Flash Tool for TI Microcontrollers (MCU), Sitara Processors and SimpleLink devices

Programs on-chip flash memory on TI MCUs and onboard flash memory for Sitara processors. Uniflash has a GUI, command line, and scripting interface. CCS Uniflash is available free of charge.

XDS200 USB Debug Probe Connects to the target board via a TI 20-pin connector (with multiple adapters for TI 14-pin, ARM 10-pin and ARM 20-pin) and to the host PC via USB2.0 High Speed (480Mbps). It also requires a license of Code Composer Studio IDE running on the host PC.

XDS560v2 System Trace USB and Ethernet Debug Probe Adds system pin trace in its large external memory buffer. Available for selected TI devices, this external memory buffer captures device-level information that allows obtaining accurate bus performance activity and throughput, as well as power management of core and peripherals. Also, all XDS debug probes support Core and System Trace in all ARM and DSP processors that feature an Embedded Trace Buffer (ETB).

XDS560v2 System Trace USB Debug Probe Adds system pin trace in its large external memory buffer. Available for selected TI devices, this external memory buffer captures device-level information that allows obtaining accurate bus performance activity and throughput, as well as power management of core and peripherals. Also, all XDS debug probes support Core and System Trace in all ARM and DSP processors that feature an Embedded Trace Buffer (ETB).

Models

AM335x ZCE IBIS Model ZCE package IBIS model

AM335x ZCZ IBIS Model ZCZ package IBIS model

AM335x ZCE Rev. 2.1 BSDL Model ZCE package BSDL model for the revision 2.1 TI F781962A Fixed- and Floating-Point DSP with Boundary Scan

AM335x ZCZ Rev. 2.1 BSDL Model ZCZ package BSDL model for the revision 2.1 TI F781962A Fixed- and Floating-Point DSP with Boundary Scan

8.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

Errata

AM335x Sitara Processors Silicon Errata

Describes the known exceptions to the functional specifications for the AM335x Sitara Processors.

Application Reports

Processor SDK RTOS Customization: Modifying Board Library to Change UART Instance on AM335x

Describes the procedure to modify the default UART0 example in the AM335x Processor SDK RTOS package to enable UART1. On the BeagleBone Black (BBB) P9 header, pins 24(TX) and 26(RX) are connected to UART1. This procedure shows a test to verify that UART1 is enabled on the BBB.

High-Speed Layout Guidelines As modern bus interface frequencies scale higher, care must be taken in the printed circuit board (PCB) layout phase of a design to ensure a robust solution.

AM335x Reliability Considerations in PLC Applications Programmable Logic Controllers (PLC) are used as the main control in an automation system with high- reliability expectations and long life in harsh environments. Processors used in these applications require an assessment of performance verses expected power on hours to achieve the optimal performance for the application.

AM335x Thermal Considerations Discusses the thermal considerations of the AM335x devices. It offers guidance on analysis of the processor's thermal performance, suggests improvements for an end system to aid in overcoming some of the existing challenges of producing a good thermal design, and provides real power/thermal data measured with AM335x EVMs for user evaluation.

User's Guides

TPS65910Ax User's Guide for AM335x Processors User's Guide A reference for connectivity between the TPS65910Ax power-management integrated circuit (PMIC) and the AM335x processor.

AM335x and AMIC110 Sitara Processors Technical Reference Manual

Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

G3 Power Line Communications Data Concentrator on BeagleBone Black Platform Design Guide

Provide the foundation that you need including methodology, testing, and design files to quickly evaluate and customize the system. TI Designs help you accelerate your time to market.

Powering the AM335x with the TPS65217x A reference for connectivity between the TPS65217 power management IC and the AM335x processor.

Powering the AM335x With the TPS650250 Details a power solution for the AM335x application processor with a TPS650250 Power Management Unit (PMU) or Power Management IC (PMIC).

Selection and Solution Guides

Connected Sensors Building Automation Systems Guide The use of connected sensors has a wide range of uses in building automation applications, from monitoring human safety and security, controlling the environment and ambience specified by the comfort preferences of the end user, or either periodic or continuous data logging of environmental and system data to detect irregular system conditions.

White Papers

Building Automation for Enhanced Energy And Operational Efficiency Discusses building automation solutions, focusing on aspects of the Building Control System. TI's Sitara processors facilitate intelligent automation of the control systems. The scalable Sitara processor portfolio offers an opportunity to build a platform solution that also spans beyond Building Control Systems.

POWERLINK on TI Sitara Processors Supports Ethernet standard features such as cross-traffic, hot-plugging and different types of network configurations such as star, ring and mixed topologies.

EtherNet/IP on TI's Sitara AM335x Processors EtherNet/IP™ (EtherNet/Industrial Protocol) is an industrial automation networking protocol based on the IEEE 802.3 Ethernet standard that has dominated the world of IT networking for the past three decades.

PROFINET on TI's Sitara AM335x Processors To integrate PROFINET into the Sitara AM335x processor, TI has built upon its programmable realtime unit (PRU) technology to create an industrial communication sub-system (ICSS).

Profibus on AM335x and AM1810 Sitara ARM Microprocessor PROFIBUS, one of the most used communication technologies, is installed in more than 35 million industrial nodes worldwide and is growing at a rate of approximately 10 percent each year.

EtherCAT on Sitara AM335x ARM Cortex-A8 Microprocessors Emerging real-time industrial Ethernet standard for industrial automation applications, such as input/output (I/O) devices, sensors and programmable logic controllers (PLCs).

Mainline Linux Ensures Stability and Innovation Enabling and empowering the rapid development of new functionality starts at the foundational level of the system's software environment – that is, at the level of the Linux kernel – and builds upward from there.

Complete Solutions for Next-Generation Wireless Connected Audio Robust, feature-rich and high-performance connectivity technology for Wi-Fi and Bluetooth.

Data Concentrators: The Core of Energy and Data Management With a large install base, it is essential to establish an automated metering infrastructure (AMI). With automated meter reading (AMR) measurement, the communication of meter data to the central billing station will be seamless.

Linaro Speeds Development in TI Linux SDKs Linaro's software is not a Linux distribution; in fact, it is distribution neutral. The focus of the organization's 120 engineers is on optimizing base-level open-source software in areas that interact directly with the silicon such as multimedia, graphics, power management, the Linux kernel and booting processes.

Getting Started on TI ARM Embedded Processor Development Beginning with an overview of ARM technology and available processor platforms, this paper will then explore the fundamentals of embedded design that influence a system's architecture and, consequently, impact processor selection.

Power Optimization Techniques for Energy-Efficient Systems The TI Sitara processor solutions offer the flexibility to design application-specific systems. The latest Sitara AM335x processors provide a scalable architecture with speed ranging from 300 MHz to 1 GHz.

The Yocto Project: Changing the Way Embedded Linux Software Solutions are Developed Enabling complex silicon devices such as SoC with operating firmware and application software can be a challenge for equipment manufacturers who often are more comfortable with hardware than software issues.

Smart Thermostats are a Cool Addition to the Connected Home Because of the pervasiveness of residential broadband connectivity and the explosion in options, the key to the connected home is – connectivity.

BeagleBone Low-Cost Development Board Provides a Clear Path to Open-source Resources

Ready-to-use open-source hardware platform for rapid prototyping and firmware and software development.

Enable Security and Amp Up Chip Performance With Hardware-Accelerated Cryptography

Cryptography is one of several techniques or methodologies that are typically implemented in contemporary electronic systems to construct a secure perimeter around a device where information or digital content is being protected.

Gesture Recognition: Enabling Natural Interactions With Electronics Enabling humans and machines to interface more easily in the home, the automobile, and at work.

Developing Android Applications for ARM Cortex-A8 Cores The flexibility, power, versatility and ubiquity of the Android operating system (OS) and associated ecosystem have been a boon to developers of applications for ARM processor cores.

Other Documents

Industrial Communication with Sitara AM335x ARM Cortex-A8 Microprocessors The industry's first low- power ARM Cortex-A8 devices to incorporate multiple industrial communication protocols on a single chip. The six pin-to-pin and software-compatible devices in this generation of processors, along with industrial hardware development tools, software and analog complements, provide a total industrial system solution.

Sitara Processors Using the ARM Cortex-A series of cores, are optimized system solutions that go beyond the core, delivering products that support rich graphics capabilities, LCD displays and multiple industrial protocols.

Industrial Communication with Sitara AM335x ARM Cortex-A8 Microprocessors Describes the key features and benefits of multiple, on-chip, production-ready industrial Ethernet and field bus communication protocols with master and slave functionality.

8.4 Related Links

[Table 8-1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|--------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| AM3359 | Click here | Click here | Click here | Click here | Click here |
| AM3358 | Click here | Click here | Click here | Click here | Click here |
| AM3357 | Click here | Click here | Click here | Click here | Click here |
| AM3356 | Click here | Click here | Click here | Click here | Click here |
| AM3354 | Click here | Click here | Click here | Click here | Click here |
| AM3352 | Click here | Click here | Click here | Click here | Click here |
| AM3351 | Click here | Click here | Click here | Click here | Click here |

8.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.6 Trademarks

Sitara, SmartReflex, WiLink, E2E are trademarks of Texas Instruments.
NEON is a trademark of ARM Ltd or its subsidiaries.
ARM, Cortex are registered trademarks of ARM Ltd or its subsidiaries.
Bluetooth is a registered trademark of Bluetooth SIG.
EtherCAT is a registered trademark of EtherCAT Technology Group.
Android is a trademark of Google Inc.
PowerVR SGX is a trademark of Imagination Technologies Limited.
Linux is a registered trademark of Linus Torvalds.
Wi-Fi is a registered trademark of Wi-Fi Alliance.
All other trademarks are the property of their respective owners.

8.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Via Channel

The ZCE package has been specially engineered with Via Channel technology. This allows larger than normal PCB via and trace sizes and reduced PCB signal layers to be used in a PCB design with the 0.65-mm pitch package, and substantially reduces PCB costs. It allows PCB routing in only two signal layers (four layers total) due to the increased layer efficiency of the Via Channel BGA technology.

Via Channel technology implemented on the ZCE package makes it possible to build an AM335x-based product with a 4-layer PCB, but a 4-layer PCB may not meet system performance goals. Therefore, system performance using a 4-layer PCB design must be evaluated during product design.

9.2 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| AM3351BZCE30 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3351BZCE30 | Samples |
| AM3351BZCE30R | ACTIVE | NFBGA | ZCE | 298 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3351BZCE30 | Samples |
| AM3351BZCE60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3351BZCE60 | Samples |
| AM3351BZCE60R | ACTIVE | NFBGA | ZCE | 298 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3351BZCE60 | Samples |
| AM3351BZCEA30 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3351BZCEA30 | Samples |
| AM3351BZCEA30R | ACTIVE | NFBGA | ZCE | 298 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3351BZCEA30 | Samples |
| AM3351BZCEA60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3351BZCEA60 | Samples |
| AM3352BZCE30 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3352BZCE30 | Samples |
| AM3352BZCE30R | ACTIVE | NFBGA | ZCE | 298 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | | AM3352BZCE30 | Samples |
| AM3352BZCE60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3352BZCE60 | Samples |
| AM3352BZCEA30 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3352BZCEA30 | Samples |
| AM3352BZCEA30R | ACTIVE | NFBGA | ZCE | 298 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3352BZCEA30 | Samples |
| AM3352BZCEA60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3352BZCEA60 | Samples |
| AM3352BZCEA60R | ACTIVE | NFBGA | ZCE | 298 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3352BZCEA60 | Samples |
| AM3352BZCED30 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3352BZCED30 | Samples |
| AM3352BZCED60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3352BZCED60 | Samples |
| AM3352BZCZ100 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3352BZCZ100 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| AM3352BZCZ30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3352BZCZ30 | Samples |
| AM3352BZCZ60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3352BZCZ60 | Samples |
| AM3352BZCZ80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3352BZCZ80 | Samples |
| AM3352BZCZA100 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3352BZCZA100 | Samples |
| AM3352BZCZA30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3352BZCZA30 | Samples |
| AM3352BZCZA60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3352BZCZA60 | Samples |
| AM3352BZCZA80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3352BZCZA80 | Samples |
| AM3352BZCZD30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3352BZCZD30 | Samples |
| AM3352BZCZD60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3352BZCZD60 | Samples |
| AM3352BZCZD80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3352BZCZD80 | Samples |
| AM3352BZCZT60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 125 | AM3352BZCZT60 | Samples |
| AM3352BZCZT60R | ACTIVE | NFBGA | ZCZ | 324 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 125 | AM3352BZCZT60 | Samples |
| AM3354BZCE60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3354BZCE60 | Samples |
| AM3354BZCEA60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3354BZCEA60 | Samples |
| AM3354BZCED60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3354BZCED60 | Samples |
| AM3354BZCZ100 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3354BZCZ100 | Samples |
| AM3354BZCZ30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3354BZCZ30 | Samples |
| AM3354BZCZ60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3354BZCZ60 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| AM3354BZCZ80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3354BZCZ80 | Samples |
| AM3354BZCZA100 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3354BZCZA100 | Samples |
| AM3354BZCZA60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3354BZCZA60 | Samples |
| AM3354BZCZA80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3354BZCZA80 | Samples |
| AM3354BZCZA80R | ACTIVE | NFBGA | ZCZ | 324 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | | AM3354BZCZA80 | Samples |
| AM3354BZCZD60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3354BZCZD60 | Samples |
| AM3354BZCZD80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3354BZCZD80 | Samples |
| AM3356BZCEA60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | | AM3356BZCEA60 | Samples |
| AM3356BZCZ30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3356BZCZ30 | Samples |
| AM3356BZCZ60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3356BZCZ60 | Samples |
| AM3356BZCZ80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3356BZCZ80 | Samples |
| AM3356BZCZA30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3356BZCZA30 | Samples |
| AM3356BZCZA60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3356BZCZA60 | Samples |
| AM3356BZCZA80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3356BZCZA80 | Samples |
| AM3356BZCZD30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3356BZCZD30 | Samples |
| AM3356BZCZD60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3356BZCZD60 | Samples |
| AM3357BZCZA30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3357BZCZA30 | Samples |
| AM3357BZCZA60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3357BZCZA60 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| AM3357BZCZA80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3357BZCZA80 | Samples |
| AM3357BZCZD30 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3357BZCZD30 | Samples |
| AM3357BZCZD60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 90 | AM3357BZCZD60 | Samples |
| AM3358BZCE60 | ACTIVE | NFBGA | ZCE | 298 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3358BZCE60 | Samples |
| AM3358BZCZ100 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3358BZCZ100 | Samples |
| AM3358BZCZ60 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3358BZCZ60 | Samples |
| AM3358BZCZ80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 90 | AM3358BZCZ80 | Samples |
| AM3358BZCZA100 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3358BZCZA100 | Samples |
| AM3358BZCZA80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3358BZCZA80 | Samples |
| AM3359BZCZA80 | ACTIVE | NFBGA | ZCZ | 324 | 126 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | AM3359BZCZA80 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM3358 :

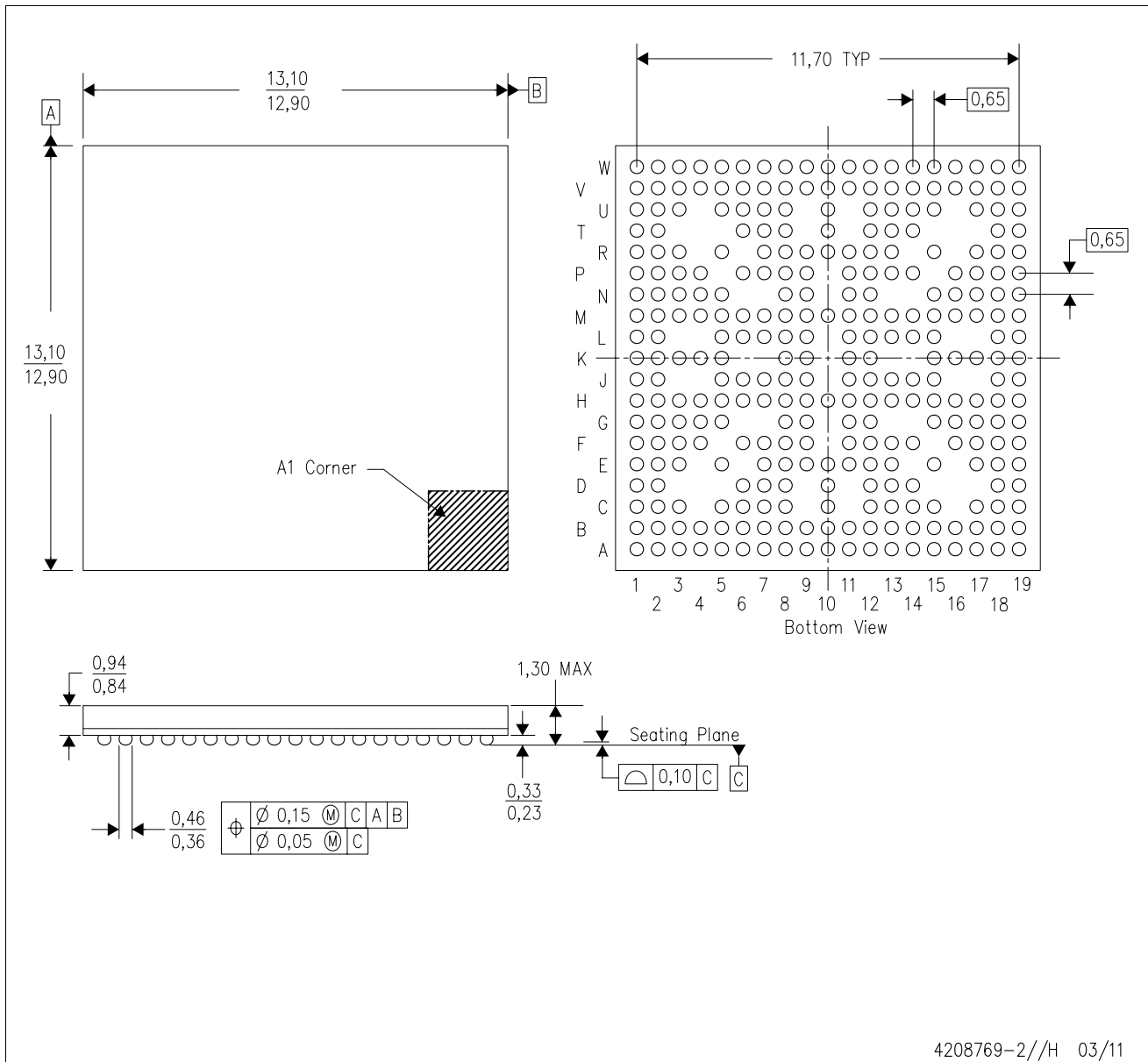
- Enhanced Product: [AM3358-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

ZCE (S-PBGA-N298)

PLASTIC BALL GRID ARRAY

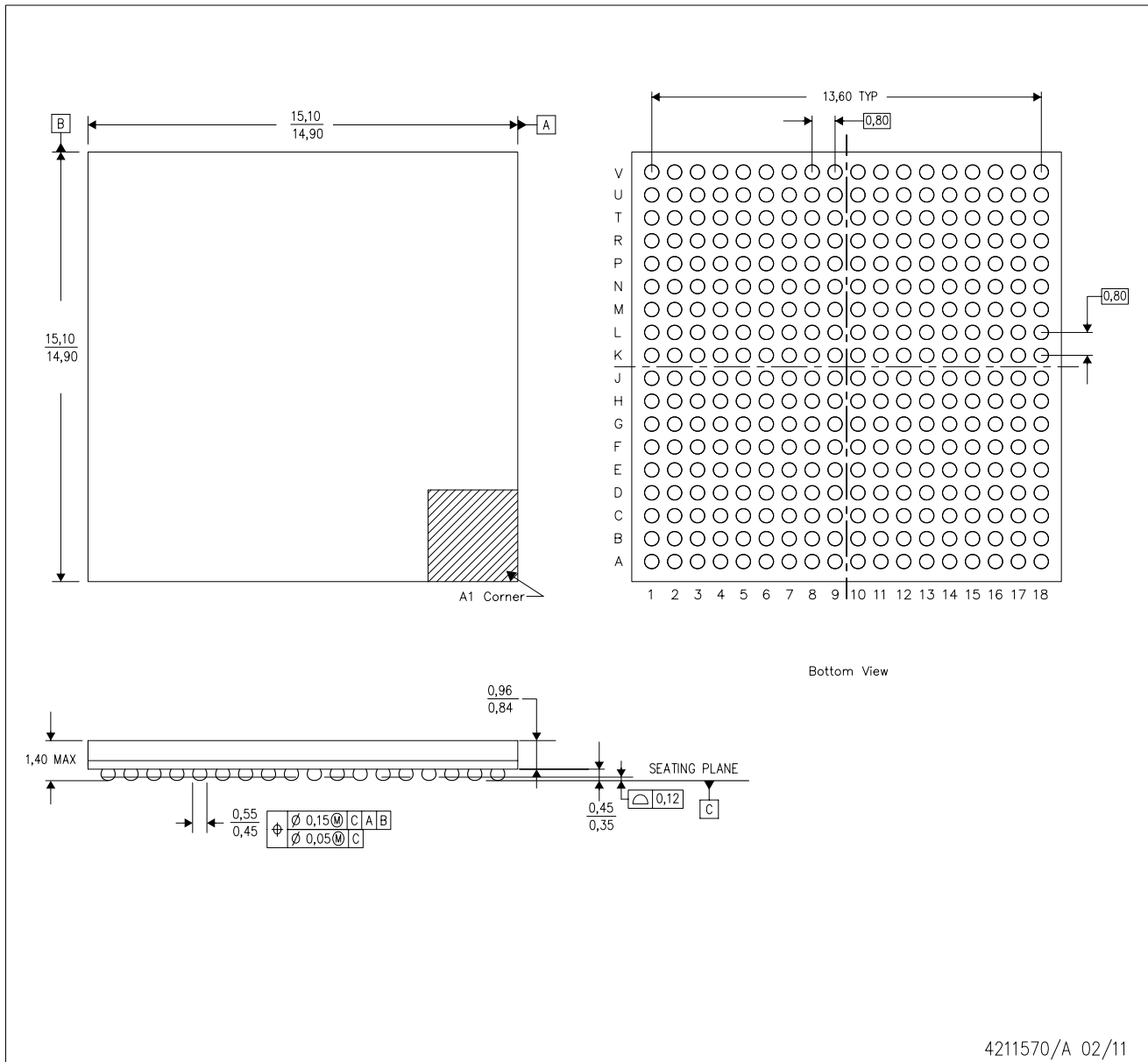


4208769-2//H 03/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. This is a Pb-free solder ball design.

ZCZ (S-PBGA-N324)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. This is a Pb-free solder ball design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.