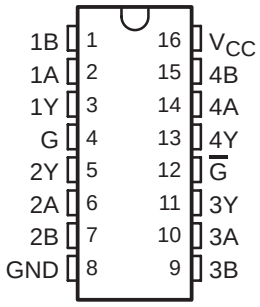
- **Switching Rates up to 32 MHz**
- **Operates From Single 3.3-V Supply**
- **Ultra-Low Power Dissipation . . . 27 mW Typ**
- **Open-Circuit, Short-Circuit, and Terminated Fail-Safe**
- **−0.3-V to 5.5-V Common-Mode Range With ±200-mV Sensitivity**
- **Accepts 5-V Logic Inputs With 3.3-V $V_{CC}$**
- **Input Hysteresis . . . 50 mV Typ**
- **235 mW With Four Receivers at 32 MHz**
- **Pin-to-Pin Compatible With AM26C32, AM26LS32, and MB570**

**D OR NS† PACKAGE**
**(TOP VIEW)**




## description/ordering information

The AM26LV32, BiCMOS, quadruple, differential line receiver with 3-state outputs is designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 receivers with reduced common-mode voltage range due to reduced supply voltage.

The device is optimized for balanced bus transmission at switching rates up to 32 MHz. The enable function is common to all four receivers and offers a choice of active-high or active-low inputs. The 3-state outputs permit connection directly to a bus-organized system. Each device features receiver high input impedance and input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range from −0.3 V to 5.5 V. When the inputs are open circuited, the outputs are in the high logic state. This device is designed using the Texas Instruments (TI™) proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed.

This device offers optimum performance when used with the AM26LV31 quadruple line drivers.

The AM26LV32C is characterized for operation from 0°C to 70°C. The AM26LV32I is characterized for operation from −45°C to 85°C.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | D | Tape and reel | AM26LV32CDG4 | AM26LV32C |
| | | | AM26LV32CDR | |
| | | | AM26LV32CDRG4 | |
| | NS | Tube | AM26LV32CNS | 26LV32 |
| | | Tape and reel | AM26LV32CNSR | |
| −40°C to 85°C | SOP – D | Tube | AM26LV32ID | AM26LV32I |
| | | | AM26LV32IDR | |
| | SOP – NS | Tube | AM26LV32INS | 26LV32I |
| | | Tape and reel | AM26LV32INSR | |

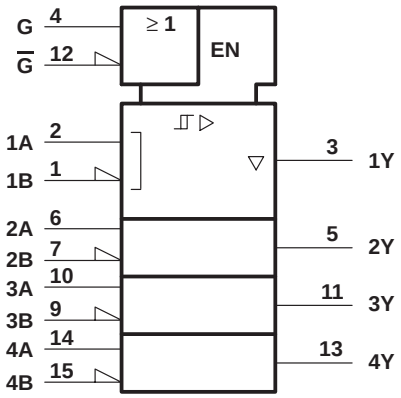
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each receiver)**

| DIFFERENTIAL INPUT | ENABLES | | OUTPUT |
|---|---|---|---|
| | G | $\overline{G}$ | |
| $V_{ID} \geq 0.2$ V | H<br>X | X<br>L | H<br>H |
| $-0.2$ V $< V_{ID} < 0.2$ V | H<br>X | X<br>L | ?<br>? |
| $V_{ID} \leq -0.2$ V | H<br>X | X<br>L | L<br>L |
| Open, shorted, or terminated† | H<br>X | X<br>L | H<br>H |
| X | L | H | Z |

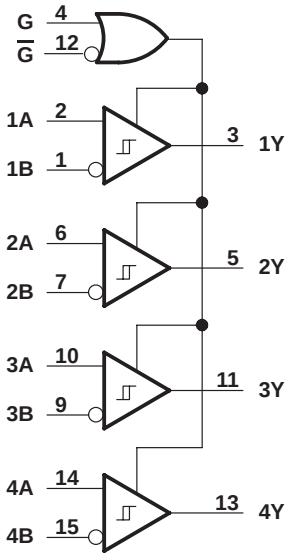
H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate
† See application information attached.

## logic symbol‡

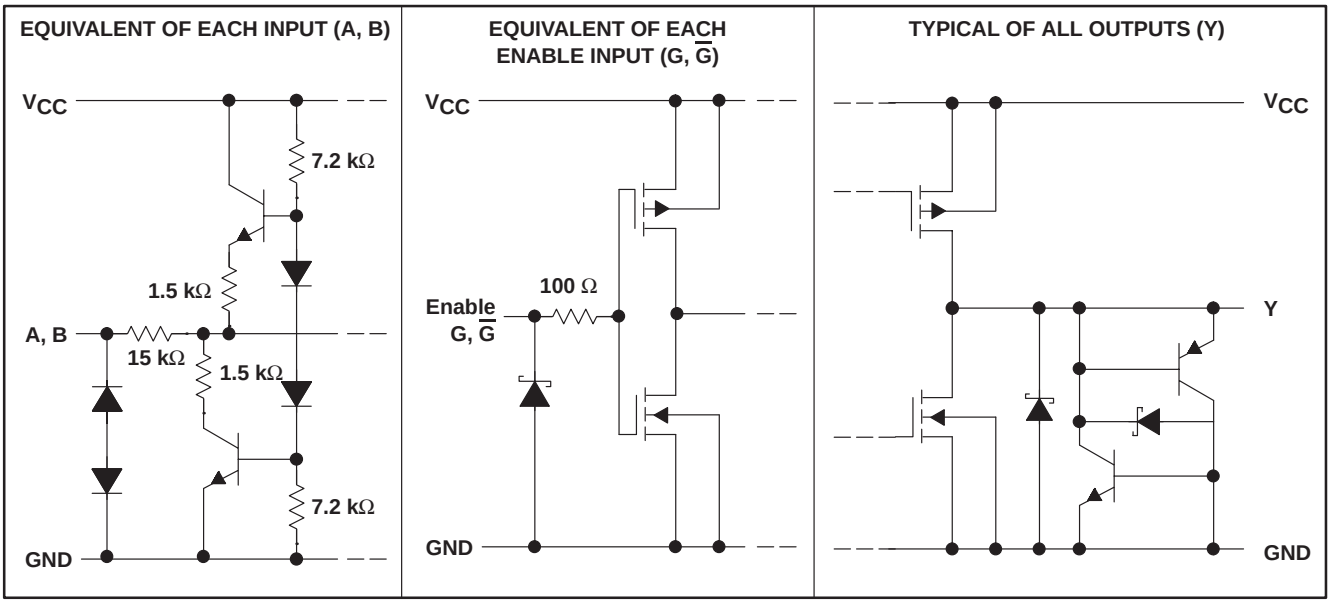



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## schematics of equivalent inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . −0.3 V to 6 V
Input voltage range, $V_I$ (A or B inputs) . . . . . −4 V to 8 V
Differential input voltage, $V_{ID}$ (see Note 2) . . . . . ±12 V
Enable input voltage range . . . . . −0.3 V to 6 V
Output voltage range, $V_O$ . . . . . −0.3 V to 6 V
Maximum output current, $I_O$ . . . . . ±25 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . 73°C/W
NS package . . . . . 64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 3 | 3.3 | 3.6 | V |
| High-level input voltage, $V_{IH(EN)}$ | | 2 | | | V |
| Low-level input voltage, $V_{IL(EN)}$ | | | | 0.8 | V |
| Common-mode input voltage, $V_{IC}$ | | −0.3 | | 5.5 | V |
| Differential input voltage, $V_{ID}$ | | | | ±5.8 | |
| High-level output current, $I_{OH}$ | | | | −5 | mA |
| Low-level output current, $I_{OL}$ | | | | 5 | mA |
| Operating free-air temperature, $T_A$ | AM26LV32C | 0 | | 70 | °C |
| | AM26LV32I | −40 | | 85 | |

## electrical characteristics over recommended supply-voltage and operating free-air temperature ranges (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Differential input high-threshold voltage | | | | | 0.2 | V |
| $V_{IT-}$ | Differential input low-threshold voltage | | | −0.2 | | | V |
| $V_{IK}$ | Enable input clamp voltage | $I_I$ = −18 mA | | | −0.8 | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 200 mV, | $I_{OH}$ = −5 mA | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = −200 mV, | $I_{OL}$ = 5 mA | | 0.17 | 0.5 | V |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = 0 to $V_{CC}$ | | | | ±50 | μA |
| $I_{IH(E)}$ | High-level enable input current | $V_{CC}$ = 0 or 3 V, | $V_I$ = 5.5 V | | | 10 | μA |
| $I_{IL(E)}$ | Low-level enable input current | $V_{CC}$ = 3.6 V, | $V_I$ = 0 V | | | −10 | |
| $r_I$ | Input resistance | | | 7 | 12 | | kΩ |
| $I_I$ | Input current | $V_I$ = 5.5 V or −0.3 V, | All other inputs GND | | | ±700 | μA |
| $I_{CC}$ | Supply current | $V_{I(E)}$ = $V_{CC}$ or GND, | No load, line inputs open | | 8 | 17 | mA |
| $C_{pd}$ | Power dissipation capacitance‡ | One channel | | | 150 | | pF |

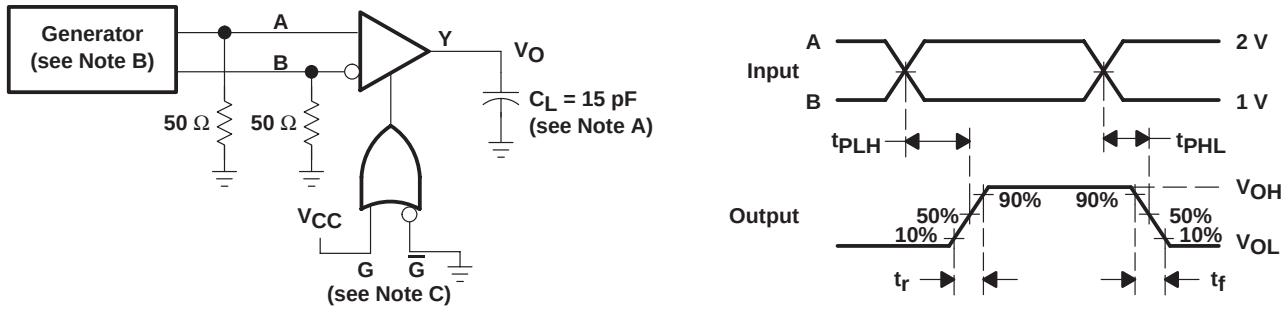
† All typical values are at $V_{CC}$ = 3.3 V and $T_A$ = 25°C.
‡ $C_{pd}$ determines the no-load dynamic current: $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$.

## switching characteristics, $V_{CC}$ = 3.3 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | See Figure 1 | 8 | 16 | 20 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | 8 | 16 | 20 | |
| $t_t$ | Transistion time ($t_r$ or $t_f$) | See Figure 1 | | 5 | | ns |
| $t_{PZH}$ | Output-enable time to high level | See Figure 2 | | 17 | 40 | ns |
| $t_{PZL}$ | Output-enable time to low level | See Figure 3 | | 10 | 40 | ns |
| $t_{PHZ}$ | Output-disable time from high level | See Figure 2 | | 20 | 40 | ns |
| $t_{PLZ}$ | Output-disable time from low level | See Figure 3 | | 16 | 40 | ns |
| $t_{sk(p)}$§ | Pulse skew | | | 4 | 6 | ns |
| $t_{sk(o)}$¶ | Pulse skew | | | 4 | 6 | ns |
| $t_{sk(pp)}$# | Pulse skew (device to device) | | | 6 | 9 | ns |

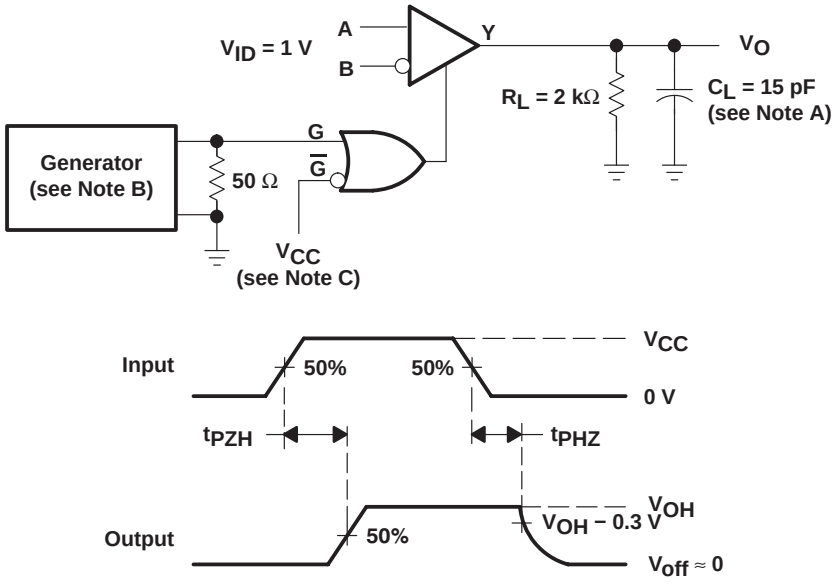
§ $t_{sk(p)}$ is $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
¶ $t_{sk(o)}$ is the maximum difference in propagation delay times between any two channels of the same device switching in the same direction.
# $t_{sk(pp)}$ is the maximum difference in propagation delay times between any two channels of any two devices switching in the same direction.

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $Z_O$ = 50 Ω, PRR = 10 MHz, $t_r$ and $t_f$ (10% to 90%) ≤ 2 ns, 50% duty cycle.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

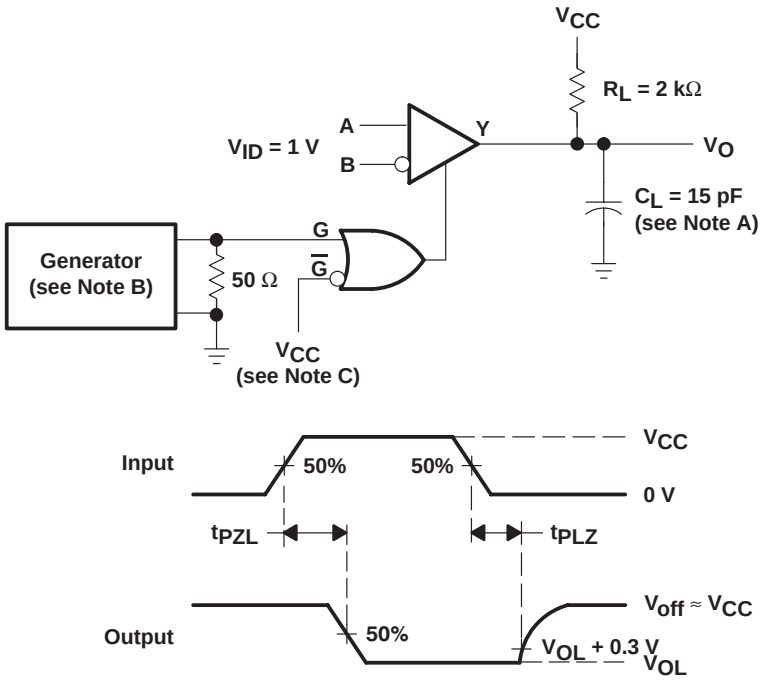
**Figure 1. $t_{PLH}$ and $t_{PHL}$ Test Circuit and Voltage Waveforms**




NOTES: A. $C_L$ includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $Z_O$ = 50 Ω, PRR = 10 MHz, $t_r$ and $t_f$ (10% to 90%) ≤ 2 ns, 50% duty cycle.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

**Figure 2. $t_{PZH}$ and $t_{PHZ}$ Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $Z_O$ = 50 Ω, PRR = 10 MHz, $t_r$ and $t_f$ (10% to 90%) ≤ 2 ns, 50% duty cycle.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

**Figure 3. $t_{PZL}$ and $t_{PLZ}$ Test Circuit and Voltage Waveforms**

## APPLICATION INFORMATION

### fail-safe conditions

The AM26LV32 quadruple differential line receiver is designed to function properly when appropriately connected to active drivers. Applications do not always have ideal situations where all bits are being used, the receiver inputs are never left floating, and fault conditions don't exist. In actuality, most applications have the capability to either place the drivers in a high-impedance mode or power down the drivers altogether, and cables may be purposely (or inadvertently) disconnected, both of which lead to floating receiver inputs. Furthermore, even though measures are taken to avoid fault conditions like a short between the differential signals, this does occur. The AM26LV32 has an internal fail-safe circuitry which prevents the device from putting an unknown voltage signal at the receiver outputs. In the following three cases, a high-state is produced at the respective output:

1. Open fail-safe − Unused input pins are left open. Do not tie unused pins to ground or any other voltage. Internal circuitry places the output in the high state.
2. 100-ohm terminated fail-safe − Disconnected cables, drivers in high-impedance state, or powered-down drivers will not cause the AM26LV32 to malfunction. The outputs will remain in a high state under these conditions. When the drivers are either turned-off or placed into the high-impedance state, the receiver input may still be able to pick up noise due to the cable acting as an antenna. To avoid having a large differential voltage being generated, the use of twisted-pair cable will induce the noise as a common-mode signal and will be rejected.
3. Shorted fail-safe − Fault conditions that short the differential input pairs together will not cause incorrect data at the outputs. A differential voltage ($V_{ID}$) of 0 V will force a high state at the outputs. Shorted fail-safe, however, is not supported across the recommended common-mode input voltage ($V_{IC}$) range. An unwanted state can be induced to all outputs when an input is shorted and is biased with a voltage between −0.3 V and 5.5 V. The shorted fail-safe circuitry will function properly when an input is shorted, but with no external common-mode voltage applied.

### fail-safe precautions

The internal fail-safe circuitry was designed such that the input common-mode ($V_{IC}$) and differential ($V_{ID}$)voltages must be observed. In order to ensure the outputs of unused or inactive receivers remain in a high state when the inputs are open-circuited, shorted, or terminated, extra precaution must be taken on the active signal. In applications where the drivers are placed in a high-impedance mode or are powered-down, it is recommended that for 1, 2, or 3 active receiver inputs, the low-level input voltage ($V_{IL}$) should be greater than 0.4 V. As in all data transmission applications, it is necessary to provide a return ground path between the two remote grounds (driver and receiver ground references) to avoid ground differences. Table 1 and Figures 4 through 7 are examples of active input voltages with their respective waveforms and the effect each have on unused or inactive outputs. Note that the active receivers behave as expected, regardless of the input levels.

## APPLICATION INFORMATION

**Table 1. Active Receiver Inputs vs Outputs**

| 1, 2, OR 3 ACTIVE INPUTS | | | SEE FIGURE | 1, 2, OR 3 ACTIVE OUTPUTS | 3, 2, OR 1 UNUSED OR INACTIVE OUTPUTS |
|---|---|---|---|---|---|
| $V_{IL}$† | $V_{ID}$ | $V_{IC}$† | | | |
| 900 mV | 200 mV | 1 V | 4 | Known state | High state |
| −100 mV | 200 mV | 0 V | 5 | Known state | ? |
| 600 mV | 800 mV | 1 V | 6 | Known state | High state |
| 0 | 800 mV | 400 mV | 7 | Known state | ? |

† Measured with respect to ground.

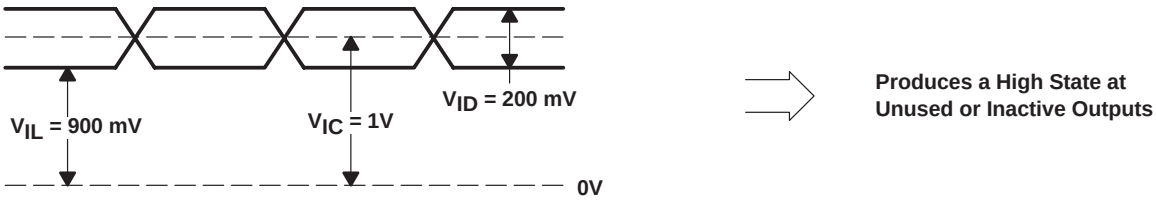



**Figure 4. Waveform One**

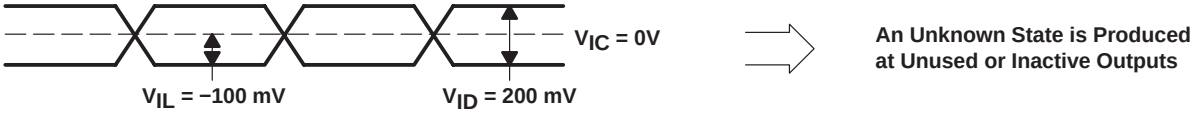



**Figure 5. Waveform Two**

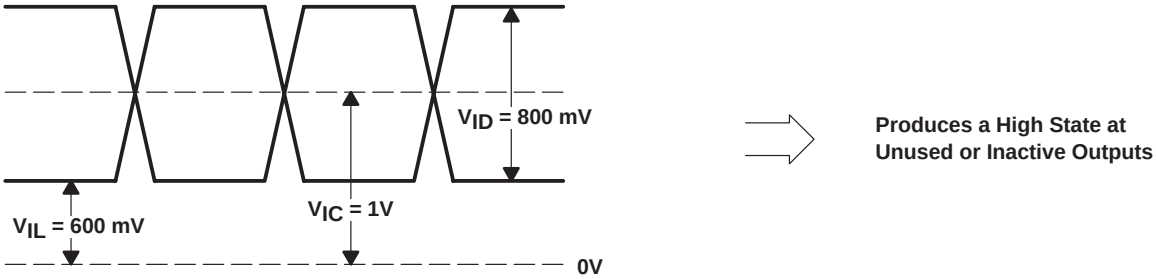



**Figure 6. Waveform Three**

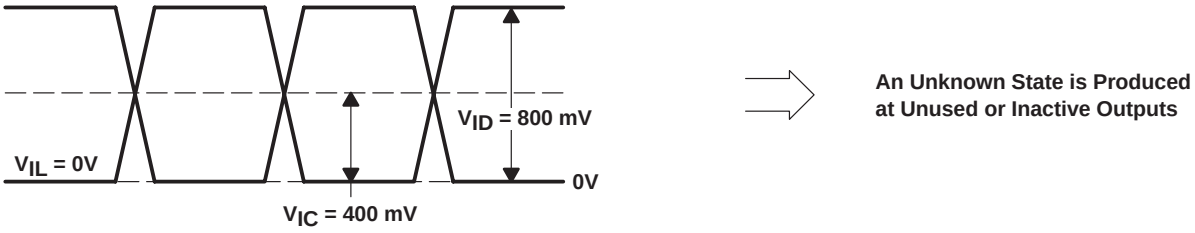



**Figure 7. Waveform Four**

## APPLICATION INFORMATION

In most applications, it is not customary to have a common-mode input close to ground and to have a differential voltage larger than 2 V. Since the common-mode input voltage is typically around 1.5 V, a 2-V $V_{ID}$ would result in a $V_{IL}$ of 0.5 V, thus satisfying the recommended $V_{IL}$ level of greater than 0.4 V.

Figure 8 plots seven different input threshold curves from a variety of production lots and shows how the fail-safe circuitry behaves with the input common-mode voltage levels. These input threshold curves are representative samples of production devices. The curves specifically illustrate a typical range of input threshold variation. The AM26LV32 is specified with ±200 mV of input sensitivity to account for the variance in input threshold. Each data point represents the input's ability to produce a known state at the output for a given $V_{IC}$ and $V_{ID}$. Applying a differential voltage at or above a certain point on a curve would produce a known state at the output. Applying a differential voltage less than a certain point on a curve would activate the fail-safe circuit and the output would be in a high state. For example, inspecting the top input threshold curve reveals that for a $V_{IC}$ = 1.6 V, $V_{ID}$ yields around 87 mV. Applying 90 mV of differential voltage to this particular production lot generates a known receiver output voltage. Applying a $V_{ID}$ of 80 mV activates the input fail-safe circuitry and the receiver output is placed in the high state. Texas Instruments specifies the input threshold at ±200 mV, since normal process variations affect this parameter. Note that at common-mode input voltages around 0.2 V, the input differential voltages are low compared to their respective data points. This phenomenon points to the fact that the inputs are very sensitive to small differential voltages around 0.2 V $V_{IC}$. It is recommended that $V_{IC}$ levels be kept greater than 0.5 V to avoid this increased sensitivity at $V_{IC} \approx 0.2$ V. In most applications, since $V_{IC}$ typically is 1.5 V, the fail-safe circuitry functions properly to provide a high state at the receiver output.

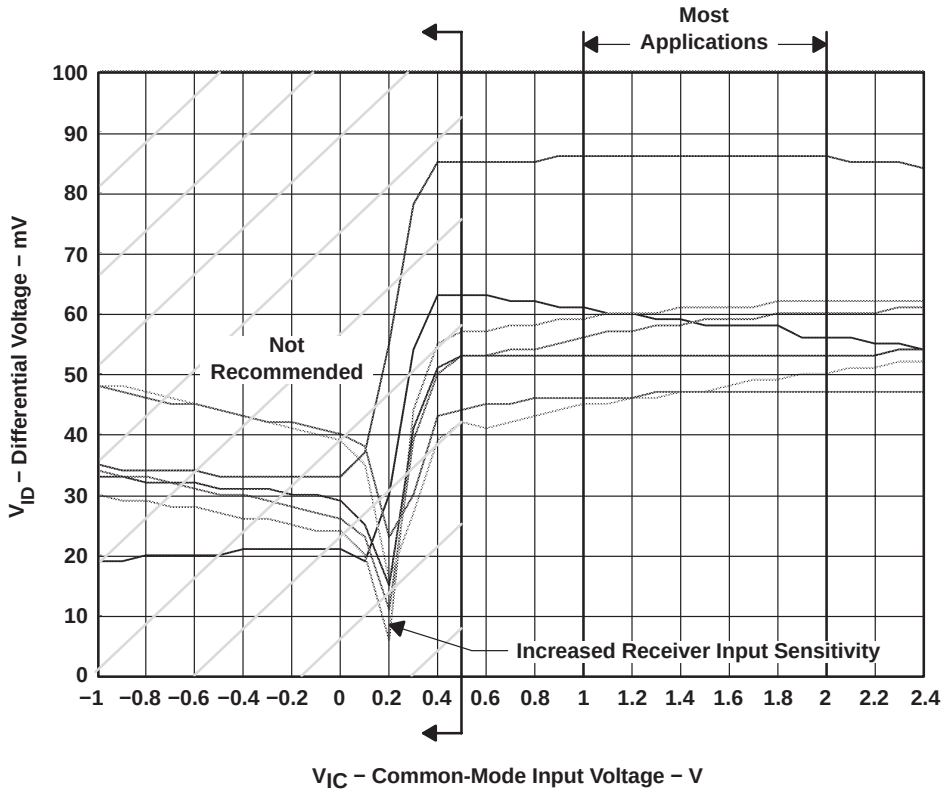



**Figure 8. $V_{IC}$ Versus $V_{ID}$ Receiver Sensitivity Levels**

## APPLICATION INFORMATION

Figure 9 represents a typical application where two receivers are not used. In this case, there is no need to worry about the output voltages of the unused receivers since they are not connected in the system architecture.

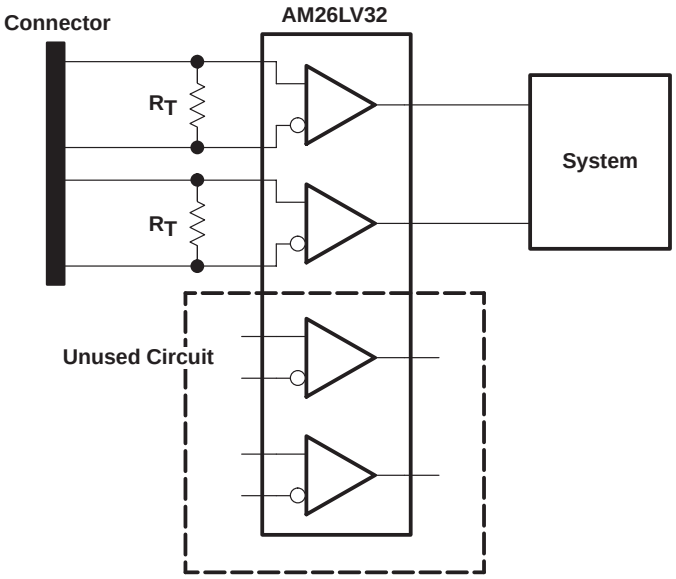



**Figure 9. Typical Application with Unused Receivers**

Figure 10 shows a common application where one or more drivers are either disabled or powered down. To ensure the inactive receiver outputs are in a high state, the active receiver inputs must have $V_{IL}$ > 0.4 V and $V_{IC}$ > 0.5 V.

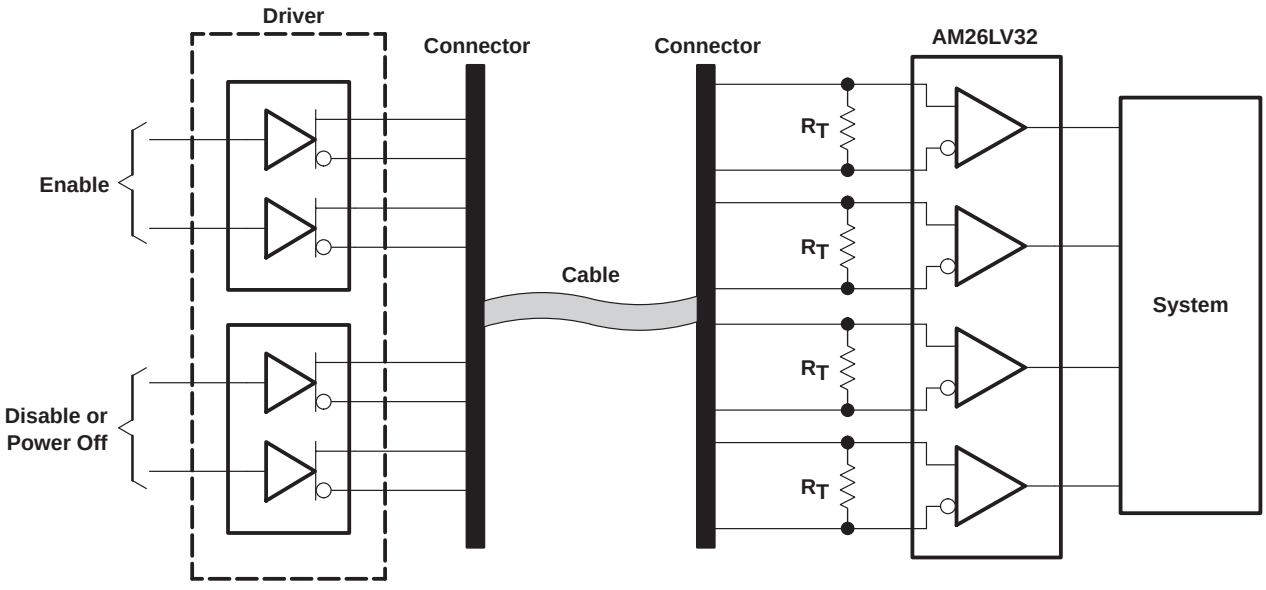



**Figure 10. Typical Application Where Two or More Drivers are Disabled**

## APPLICATION INFORMATION

Figure 11 is an alternative application design to replace the application in Figure 10. This design uses two AM26LV32 devices, instead of one. However, this design does not require the input levels be monitored to ensure the outputs are in the correct state, only that they comply to the RS-232 standard.

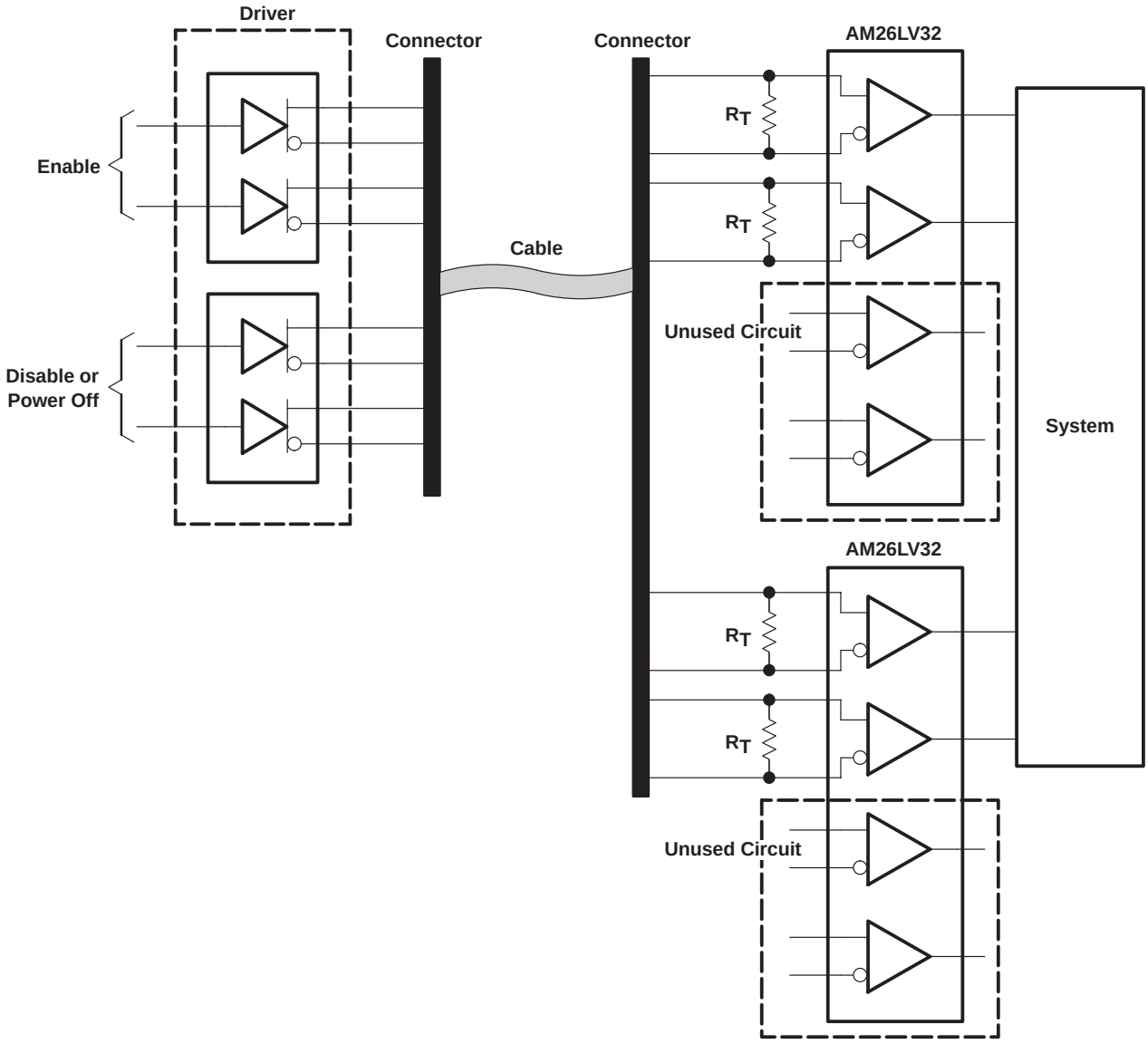



**Figure 11. Alternative Solution for Figure 10**

## APPLICATION INFORMATION

Figures 12 and 13 show typical applications where a disconnected cable occurs. Figure 12 illustrates a typical application where a cable is disconnected. Similar to Figure 10, the active input levels must be monitored to make sure the inactive receiver outputs are in a high state. An alternative solution is shown in Figure 13.

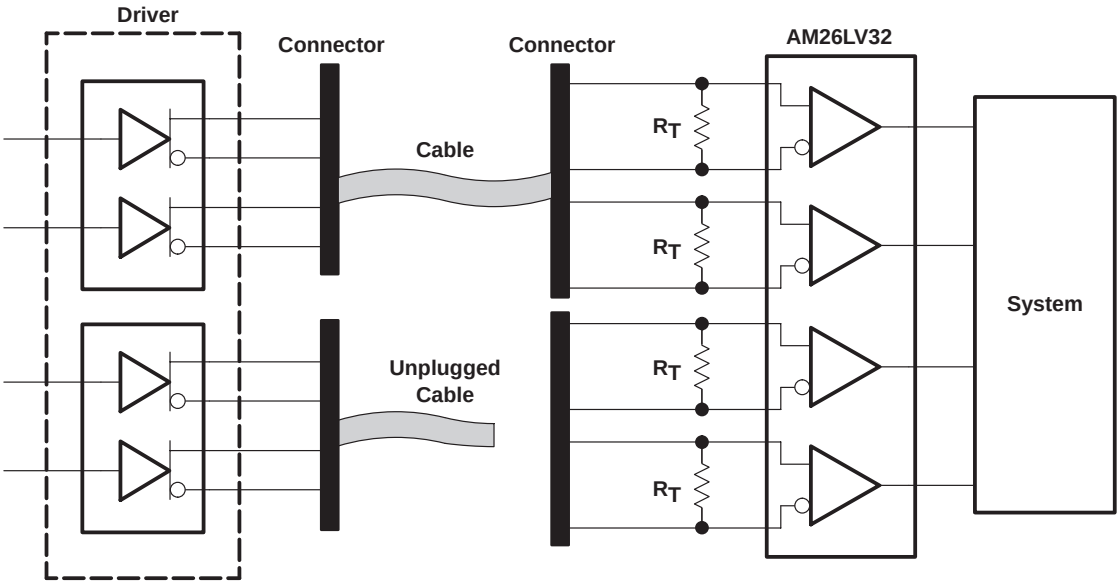



**Figure 12. Typical Application Where Two or More Drivers are Disconnected**

## APPLICATION INFORMATION

Figure 13 is an alternative solution so the receiver inputs do not have to be monitored. This solution also requires the use of two AM26LV32 devices, instead of one.

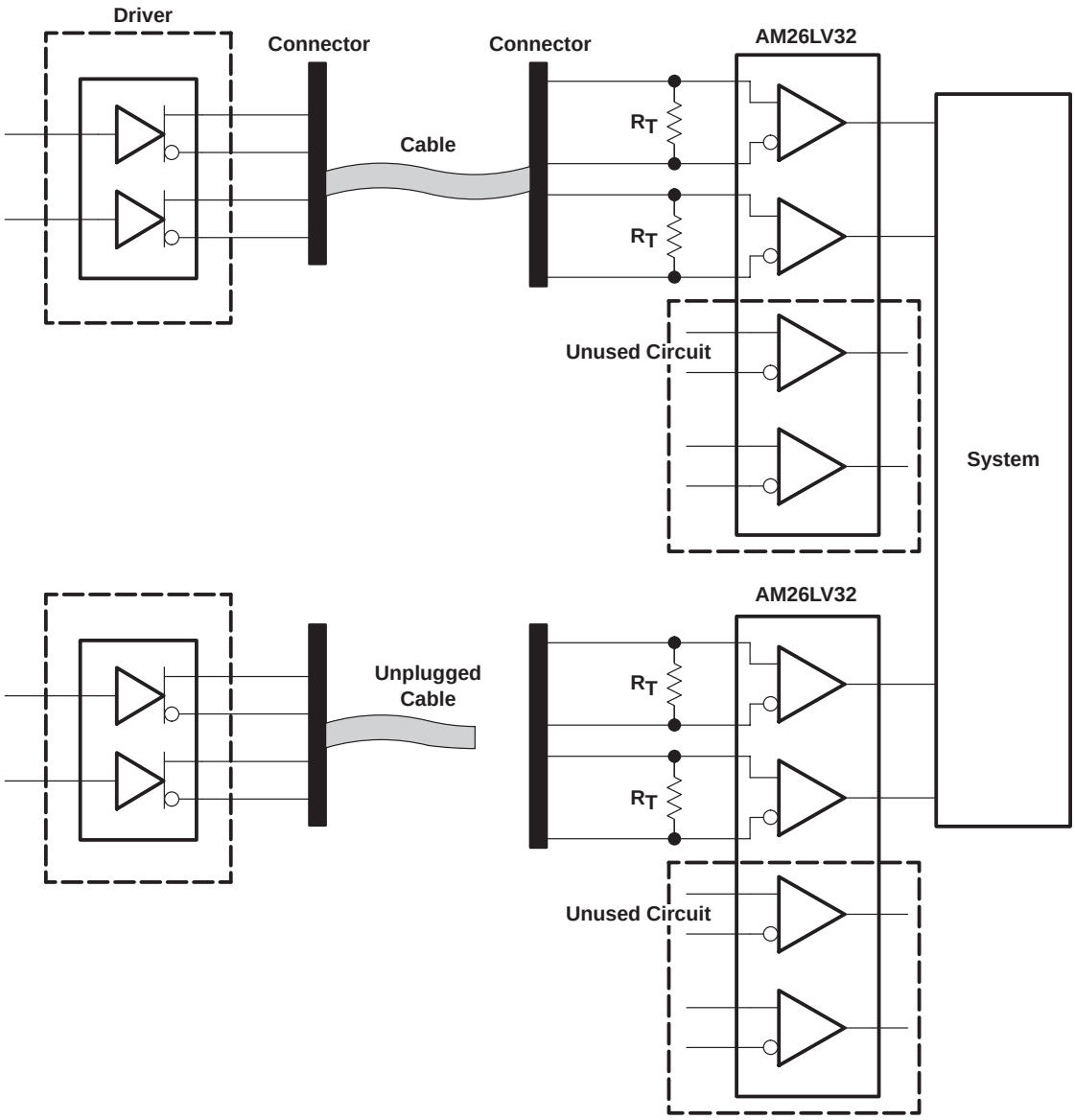



**Figure 13. Alternative Solution to Figure 12**

## APPLICATION INFORMATION

When designing a system using the AM26LV32, the device provides a robust solution where fail-safe and fault conditions are of concern. The RS-422-like inputs accept common-mode input levels from −0.3 V to 5.5 V with a specified sensitivity of ±200mV. As previously shown, care must be taken with active input levels since they can affect the outputs of unused or inactive bits. However, most applications meet or exceed the requirements to allow the device to perform properly.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| AM26LV32CD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32CDE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32CDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32CDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32CDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32CDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32CNSLE | OBSOLETE | SO | NS | 16 | | TBD | Call TI | Call TI |
| AM26LV32CNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32CNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32CNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32ID | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32IDE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32IDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32IDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32IDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32IDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32INS | ACTIVE | SO | NS | 16 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32INSE4 | ACTIVE | SO | NS | 16 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32INSG4 | ACTIVE | SO | NS | 16 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32INSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32INSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| AM26LV32INSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

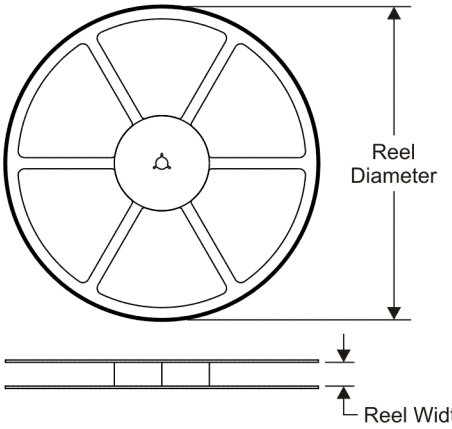
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

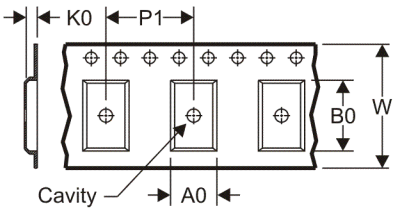
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

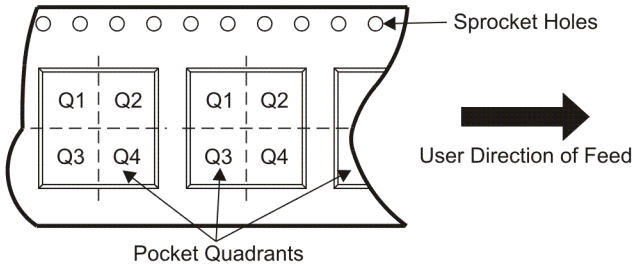



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

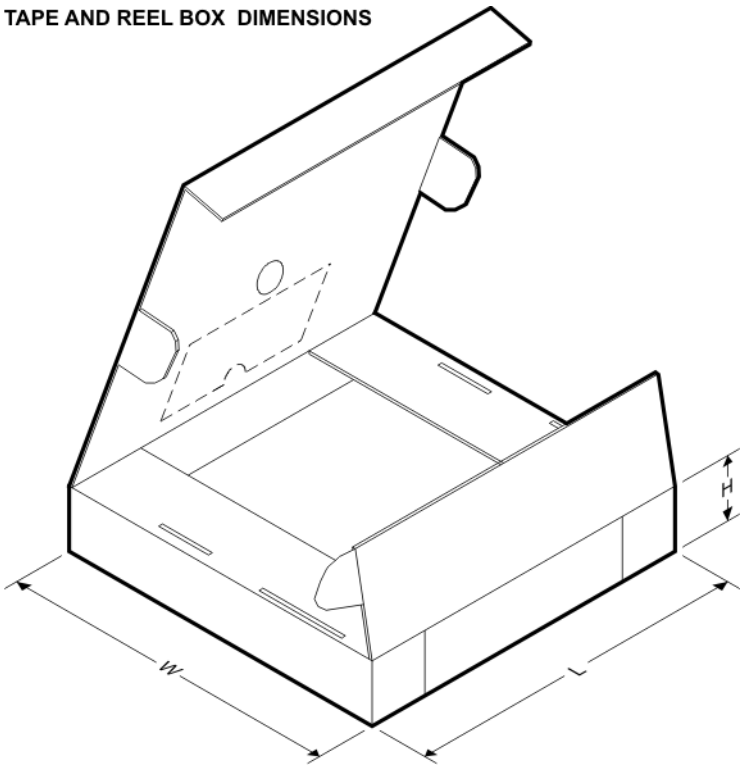
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AM26LV32CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LV32CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LV32CNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| AM26LV32IDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| AM26LV32INSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



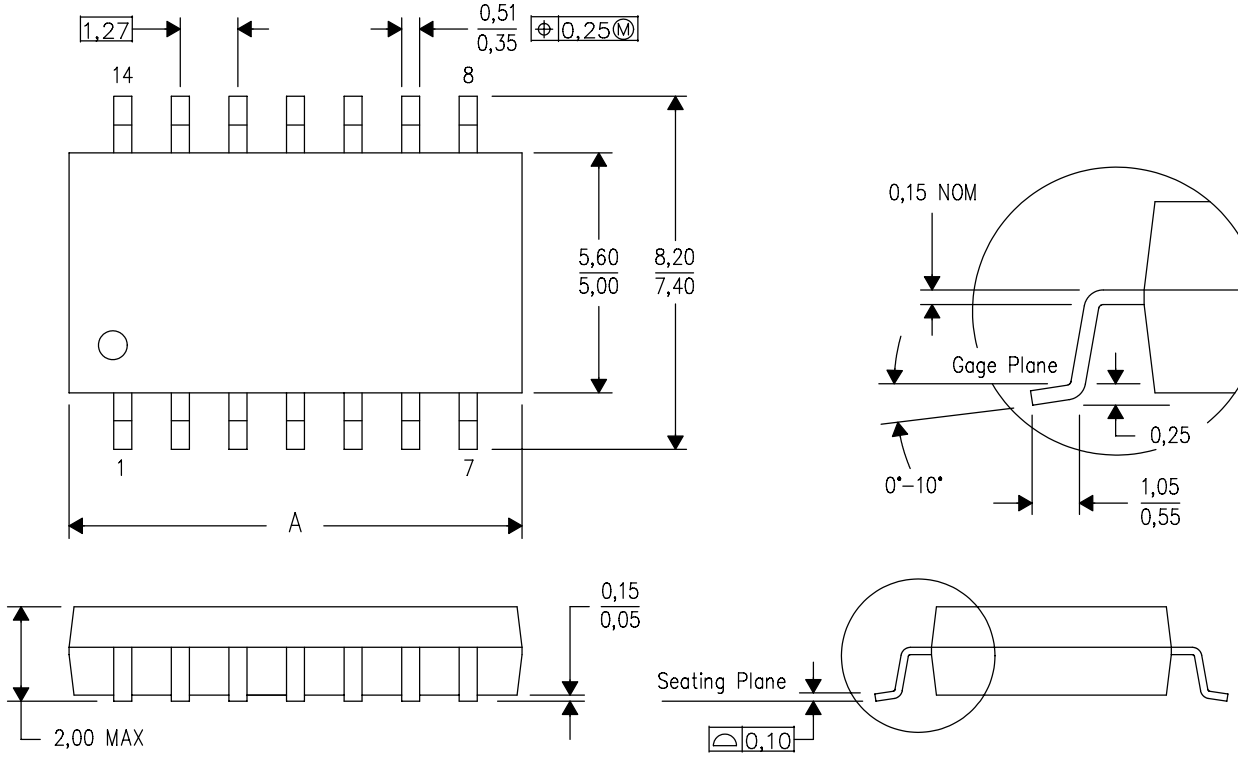

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| AM26LV32CDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| AM26LV32CDR | SOIC | D | 16 | 2500 | 346.0 | 346.0 | 33.0 |
| AM26LV32CNSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| AM26LV32IDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| AM26LV32INSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

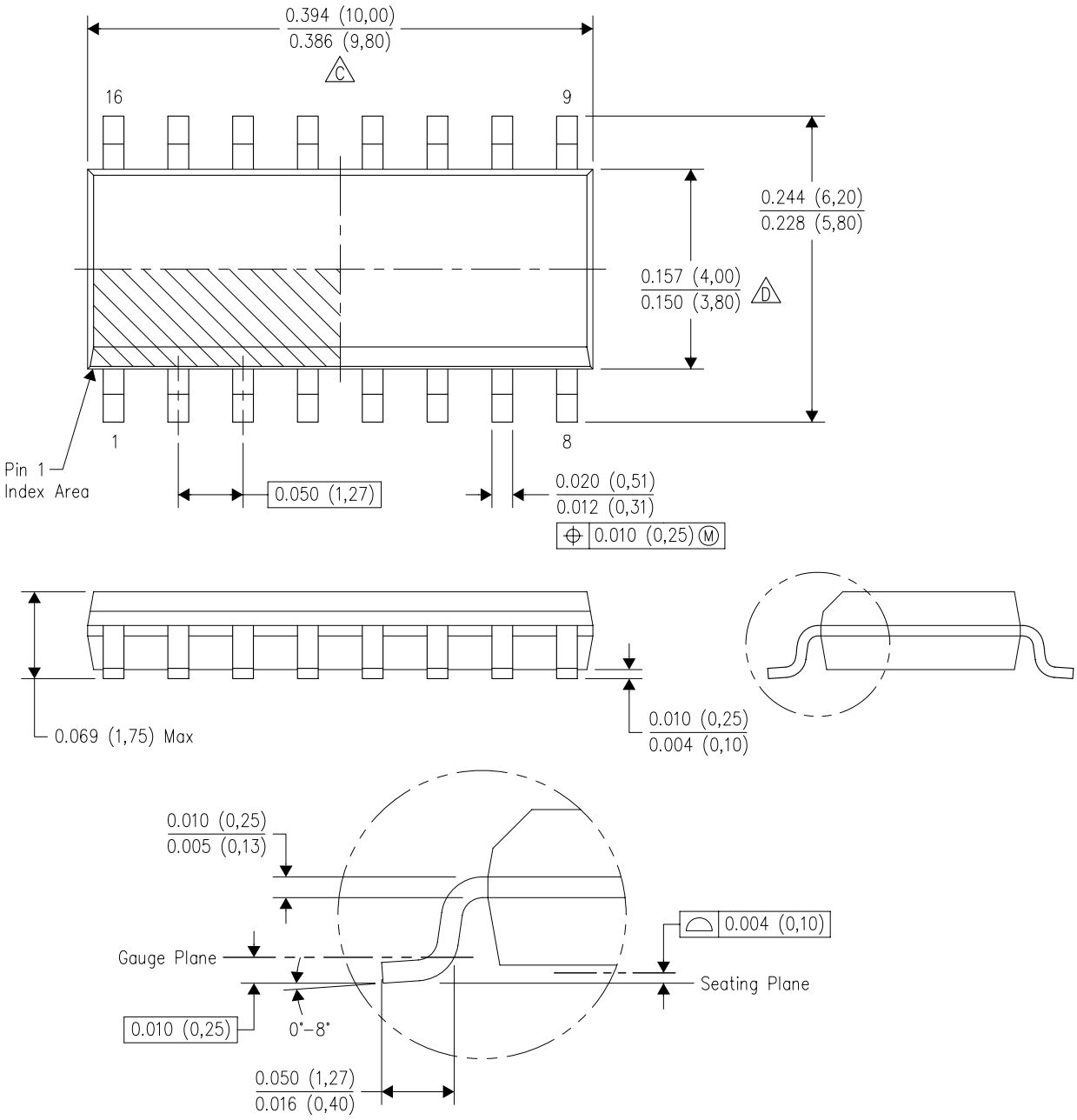



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

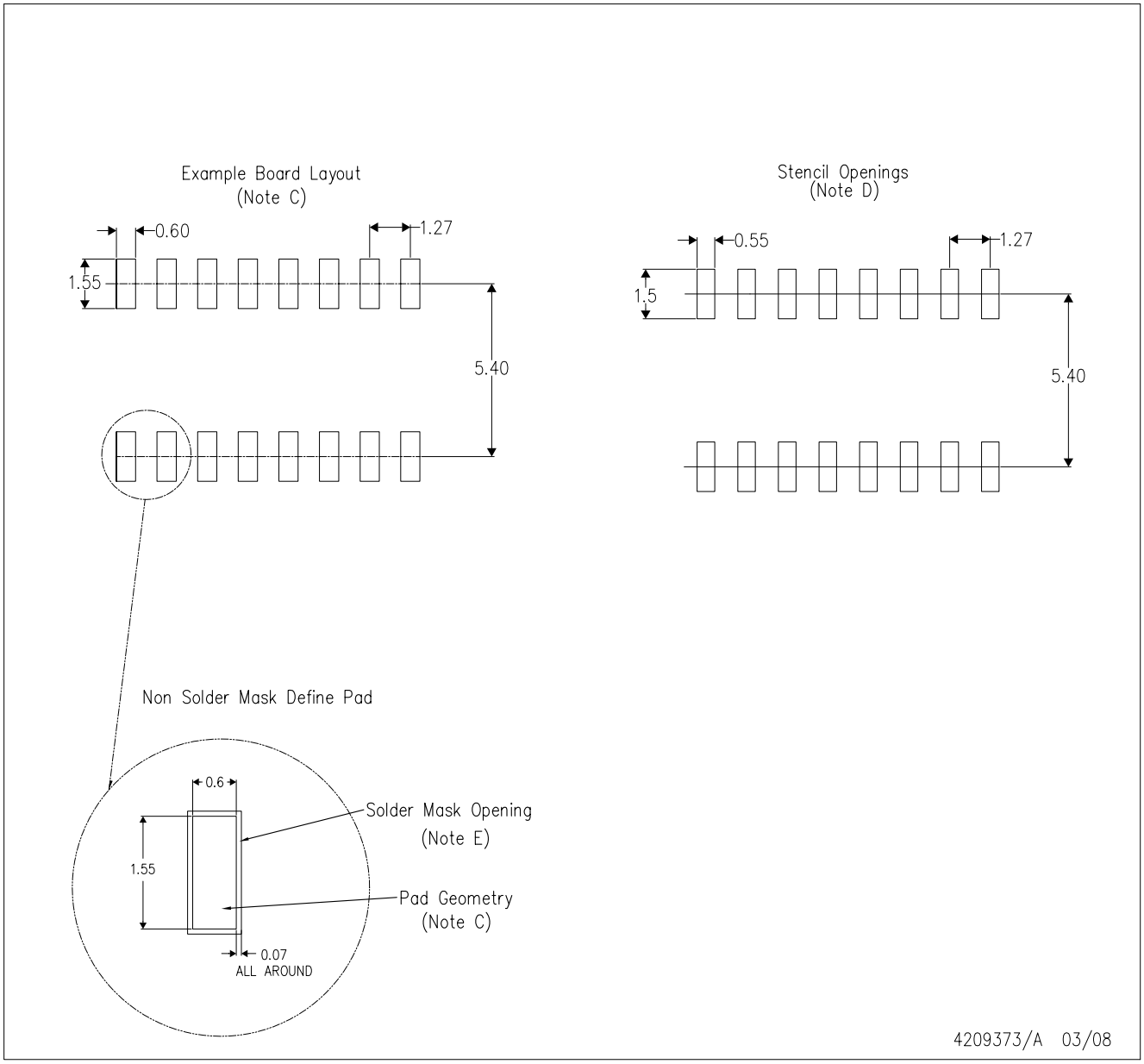
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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