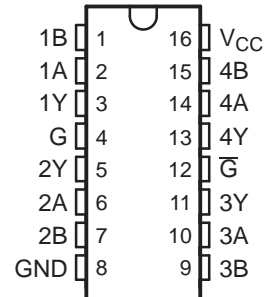


## LOW-VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH $\pm 15$ -kV IEC ESD PROTECTION

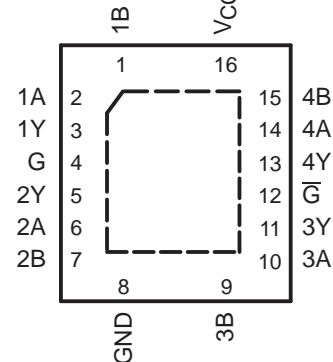
### FEATURES

- Meets or Exceeds Standard TIA/EIA-422-B and ITU Recommendation V.11
- Operates From a Single 3.3-V Power Supply
- ESD Protection for RS422 Bus Pins
  - $\pm 15$ -kV Human-Body Model (HBM)
  - $\pm 8$ -kV IEC61000-4-2, Contact Discharge
  - $\pm 15$ -kV IEC61000-4-2, Air-Gap Discharge
- Switching Rates up to 32 MHz
- Low Power Dissipation: 27 mW Typ
- Open-Circuit, Short-Circuit, and Terminated Fail-Safe
- $\pm 7$ -V Common-Mode Input Voltage Range With  $\pm 200$ -mV Sensitivity
- Accepts 5-V Logic Inputs With 3.3-V Supply (Enable Inputs)
- Input Hysteresis: 35 mV Typ
- Pin-to-Pin Compatible With AM26C32, AM26LS32
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Package Options: SOP, SOIC, TSSOP, QFN

D, NS, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



### DESCRIPTION/ORDERING INFORMATION

The AM26LV32E consists of quadruple differential line receivers with 3-state outputs. These differential receivers have  $\pm 15$ -kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and  $\pm 8$ -kV ESD (IEC61000-4-2, Contact Discharge) protection for RS422 bus pins.

This device is designed to meet TIA/EIA-422-B and ITU recommendation V.11 drivers with reduced supply voltage. The device is optimized for balanced bus transmission at switching rates up to 32 MHz. The 3-state outputs permit connection directly to a bus-organized system.

The AM26LV32E has an internal fail-safe circuitry that prevents the device from putting an unknown voltage signal at the receiver outputs. In the open fail-safe, shorted fail-safe, and terminated fail-safe, a high state is produced at the respective output.

This device is supported for partial-power-down applications using  $I_{off}$ .  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The AM26LV32EI is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION**

| T <sub>A</sub> | PACKAGE <sup>(1)(2)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | SOIC – D                  | Tape and reel | AM26LV32EIDR          | AM26LV32EI       |
|                | SOP – NS                  | Tape and reel | AM26LV32EINSR         | 26LV32EI         |
|                | TSSOP – PW                | Tape and reel | AM26LV32EIPWR         | SB32             |
|                | QFN – RGY                 | Tape and reel | AM26LV32EIRGYR        | SB32             |

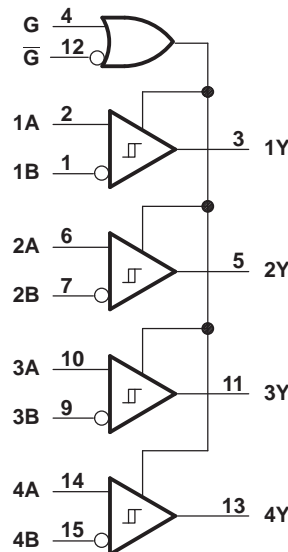
- (1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

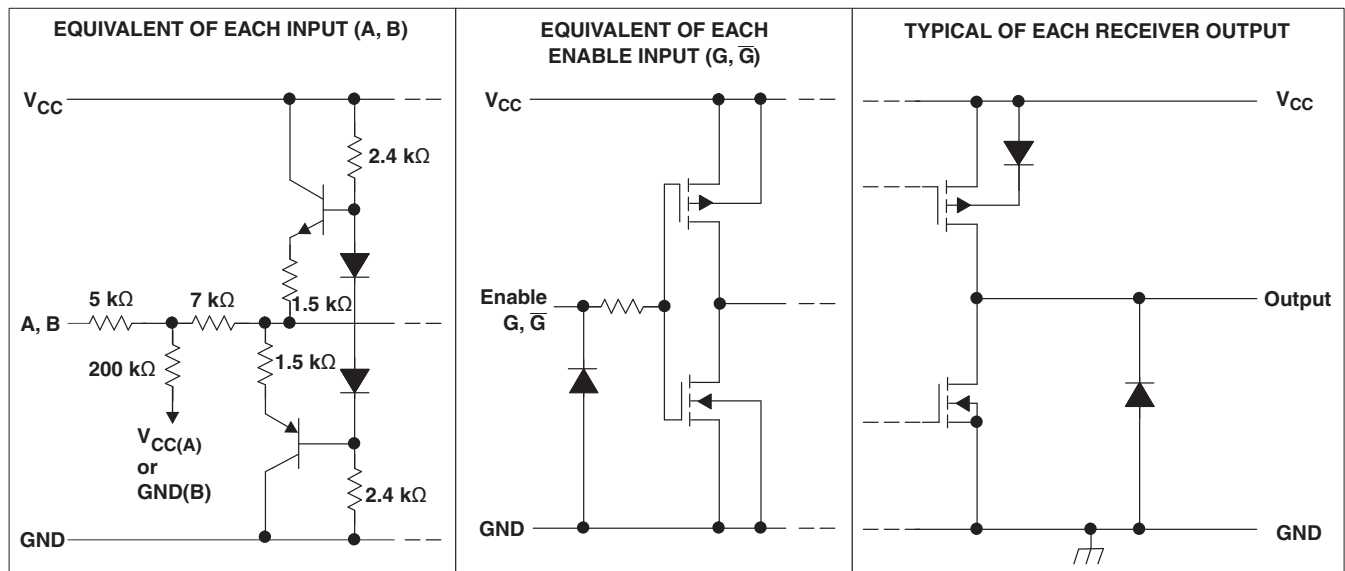
**FUNCTION TABLE<sup>(1)</sup>  
(each receiver)**

| DIFFERENTIAL INPUT           | ENABLES |           | OUTPUT |
|------------------------------|---------|-----------|--------|
|                              | G       | $\bar{G}$ |        |
| $V_{ID} \geq 0.2 V$          | H       | X         | H      |
|                              | X       | L         | H      |
| $-0.2 V < V_{ID} < 0.2 V$    | H       | X         | ?      |
|                              | X       | L         | ?      |
| $V_{ID} \leq -0.2 V$         | H       | X         | L      |
|                              | X       | L         | L      |
| Open, shorted, or terminated | H       | X         | H      |
|                              | X       | L         | H      |
| X                            | L       | H         | Z      |

- (1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**SCHEMATIC**


All resistor values are nominal.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

over operating free-air temperature range (unless otherwise noted)

|               |   | MIN         | MAX | UNIT |
|---------------|---|-------------|-----|------|
| $V_{CC}$      | Supply voltage range <sup>(3)</sup>         | -0.5        | 6   | V    |
| $V_I$         | Input voltage range                         | -14         | 14  | V    |
|               | A or B inputs                               |             |     |      |
| $V_{ID}$      | Differential input voltage <sup>(4)</sup>   | -14         | 14  | V    |
|               | Enable Inputs                               |             |     |      |
| $V_O$         | Output voltage range                        | -0.5        | 6   | V    |
| $I_{IK}$      | Input clamp current range                   |             | -20 | mA   |
| $I_{OK}$      | Output clamp current range                  |             | -20 | mA   |
| $I_O$         | Maximum output current                      |             | ±20 | mA   |
| $T_J$         | Operating virtual junction temperature      |             | 150 | °C   |
| $\theta_{JA}$ | Package thermal impedance <sup>(5)(6)</sup> | D package   | 73  | °C/W |
|               |   | NS package  | 64  |      |
|               |   | PW package  | 108 |      |
|               |   | RGY package | 39  |      |
| $T_A$         | Operating free-air temperature range        | -40         | 85  | °C   |
| $T_{stg}$     | Storage temperature range                   | -65         | 150 | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This device is designed to meet TIA/EIA-422-B and ITU.
- (3) All voltage values except differential input voltage are with respect to the network GND.
- (4) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
- (5) Maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} - T_A)/\theta_{JA}$ . Selecting the maximum of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

|          |                                 | MIN | NOM | MAX | UNIT |
|----------|---------------------------------|-----|-----|-----|------|
| $V_{CC}$ | Supply voltage                  | 3   | 3.3 | 3.6 | V    |
| $V_{IH}$ | Enable high-level input voltage | 2   |     | 5.5 | V    |
| $V_{IL}$ | Enable low-level input voltage  | 0   |     | 0.8 | V    |
| $V_{IC}$ | Common-mode input voltage       | -7  |     | 7   | mA   |
| $V_{ID}$ | Differential input voltage      | -7  |     | 7   | mA   |
| $I_{OH}$ | High-level output current       |     |     | -5  | mA   |
| $I_{OL}$ | Low-level output current        |     |     | 5   | mA   |
| $T_A$    | Operating free-air temperature  | -40 |     | 85  | °C   |

## ELECTRICAL CHARACTERISTICS

over recommended ranges of common-mode input, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS  | MIN   | TYP <sup>(1)</sup> | MAX       | UNIT       |    |
|-----------|--|---|--------------------|-----------|------------|----|
| $V_{IT+}$ | Positive-going input threshold voltage, differential input |   |                    | 0.2       | V          |    |
| $V_{IT-}$ | Negative-going input threshold voltage, differential input | -0.2  |                    |           | V          |    |
| $V_{hys}$ | Input hysteresis ( $V_{IT+} - V_{IT-}$ )                   |   | 35                 |           | mV         |    |
| $V_{IK}$  | Input clamp voltage, G and $\bar{G}$                       | $I_I = -18$ mA  |                    | -1.5      | V          |    |
| $V_{OH}$  | High-level output voltage                                  | $V_{ID} = 200$ mV, $I_{OH} = -5$ mA                     | 2.4                | 3.2       | V          |    |
|           |  | $V_{ID} = 200$ mV, $I_{OH} = -100$ $\mu$ A              | $V_{CC} - 0.1$     |           |            |    |
| $V_{OL}$  | Low-level output voltage                                   | $V_{ID} = -200$ mV, $I_{OL} = 5$ mA                     | 0.17               | 0.5       | V          |    |
|           |  | $V_{ID} = -200$ mV, $I_{OL} = 100$ $\mu$ A              |                    | 0.1       |            |    |
| $I_{OZ}$  | High-impedance state output current                        | $V_O = V_{CC}$ or GND                                   |                    | $\pm 50$  | $\mu$ A    |    |
| $I_{off}$ | Output current with power off                              | $V_{CC} = 0$ V, $V_O = 0$ or 5.5 V                      |                    | $\pm 100$ | $\mu$ A    |    |
| $I_I$     | Line input current   | Other input at 0 V                                      | $V_I = 10$ V       |           | 1.5        | mA |
|           |  |   | $V_I = -10$ V      |           | -2.5       |    |
| $I_I$     | Enable input current, G and $\bar{G}$                      | $V_I = V_{CC}$ or GND                                   |                    | $\pm 1$   | $\mu$ A    |    |
| $r_i$     | Input resistance   | $V_{IC} = -7$ V to 7 V, Other input at 0 V              | 4                  | 17        | k $\Omega$ |    |
| $I_{CC}$  | Supply current (total package)                             | G, $\bar{G} = V_{CC}$ or GND, No load, Line inputs open |                    | 8         | 17         | mA |
| $C_{pd}$  | Power dissipation capacitance <sup>(2)</sup>               | One channel   |                    | 150       | pF         |    |

(1) All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ$ C.

(2)  $C_{pd}$  determines the no-load dynamic current consumption:  $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER    |   | TEST CONDITIONS                             | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|--------------|---|---|-----|--------------------|-----|------|
| $t_{PLH}$    | Propagation delay time, low- to high-level output | See <a href="#">Figure 1</a>                | 8   | 16                 | 26  | ns   |
| $t_{PHL}$    | Propagation delay time, high- to low-level output |   | 8   | 16                 | 26  | ns   |
| $t_t$        | Transition time                                   | See <a href="#">Figure 1</a>                |     | 5                  |     | ns   |
| $t_{PZH}$    | Output-enable time to high level                  | See <a href="#">Figure 2</a>                |     | 17                 | 40  | ns   |
| $t_{PZL}$    | Output-enable time to low level                   | See <a href="#">Figure 3</a>                |     | 10                 | 40  | ns   |
| $t_{PHZ}$    | Output-disable time from high level               | See <a href="#">Figure 2</a>                |     | 20                 | 40  | ns   |
| $t_{PLZ}$    | Output-disable time from low level                | See <a href="#">Figure 3</a>                |     | 16                 | 40  | ns   |
| $t_{sk(p)}$  | Pulse skew  | See <a href="#">Figure 1</a> <sup>(2)</sup> |     | 4                  | 6   | ns   |
| $t_{sk(o)}$  | Pulse skew  | See <a href="#">Figure 1</a> <sup>(3)</sup> |     | 4                  | 6   | ns   |
| $t_{sk(pp)}$ | Pulse skew (device to device)                     | See <a href="#">Figure 1</a> <sup>(4)</sup> |     | 6                  | 9   | ns   |
| $f_{(max)}$  | Maximum operating frequency                       | See <a href="#">Figure 1</a>                |     | 32                 |     | MHz  |

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2)  $t_{sk(p)}$  is  $|t_{pLH} - t_{pHL}|$  of each channel of same device.

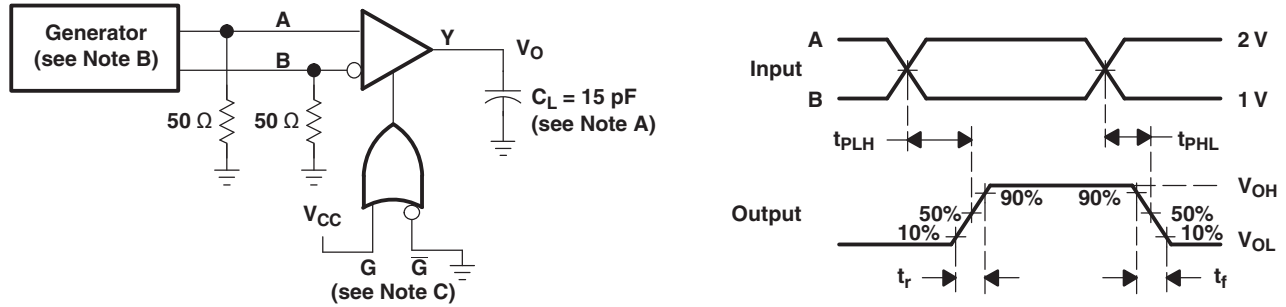
(3)  $t_{sk(o)}$  is the maximum difference in propagation delay times between any two channels of same device switching in the same direction.

(4)  $t_{sk(pp)}$  is the maximum difference in propagation delay times between any two channels of any two devices switching in the same direction.

## ESD PROTECTION

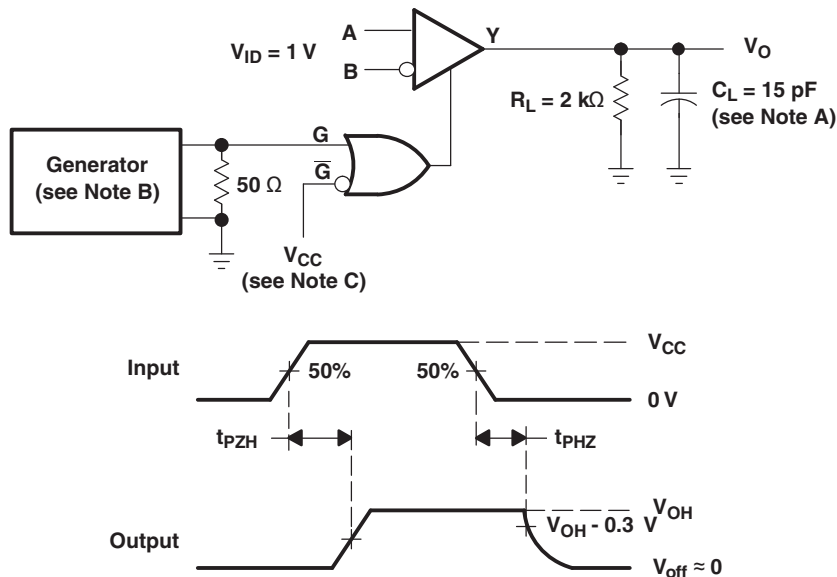
| PARAMETER      | TEST CONDITIONS                 | TYP | UNIT |
|----------------|---------------------------------|-----|------|
| Receiver input | HBM                             | ±15 | kV   |
|                | IEC61000-4-2, Air-Gap Discharge | ±15 |      |
|                | IEC61000-4-2, Contact Discharge | ±8  |      |

PARAMETER MEASUREMENT INFORMATION



- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%,  $t_r = t_f \leq 2\text{ns}$ .
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform  $\overline{G}$ .

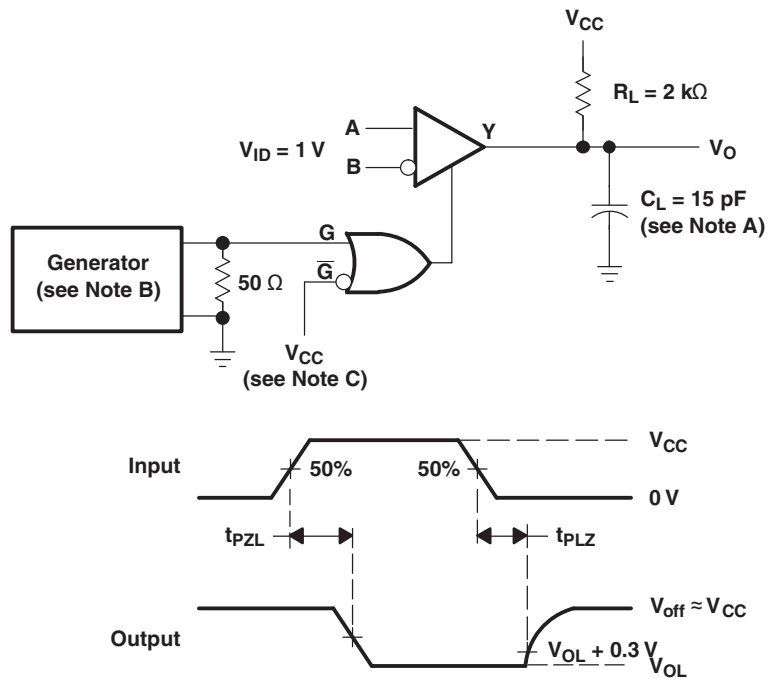
Figure 1. Test Circuit and Voltage Waveforms,  $t_{PLH}$  and  $t_{PHL}$



- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%,  $t_r = t_f \leq 2\text{ns}$ .
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform  $\overline{G}$ .

Figure 2. Test Circuit and Voltage Waveforms,  $t_{PZH}$  and  $t_{PHZ}$

PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%,  $t_r = t_f \leq 2\text{ns}$ .
- C. To test the active-low enable  $\bar{G}$ , ground G and apply an inverted waveform  $\bar{G}$ .

Figure 3. Test Circuit and Voltage Waveforms,  $t_{PZL}$  and  $t_{PLZ}$

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| AM26LV32EIDR     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| AM26LV32EIDRG4   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| AM26LV32EINSR    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| AM26LV32EINSRG4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| AM26LV32EIPWR    | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| AM26LV32EIPWRG4  | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| AM26LV32EIRGYR   | ACTIVE                | VQFN         | RGY             | 16   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| AM26LV32EIRGYRG4 | ACTIVE                | VQFN         | RGY             | 16   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF AM26LV32E :**

- Enhanced Product: [AM26LV32E-EP](#)

NOTE: Qualified Version Definitions:



- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AM26LV32EIDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| AM26LV32EINSR  | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| AM26LV32EIPWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| AM26LV32EIRGYR | VQFN         | RGY             | 16   | 3000 | 330.0              | 12.4               | 3.8     | 4.3     | 1.5     | 8.0     | 12.0   | Q1            |

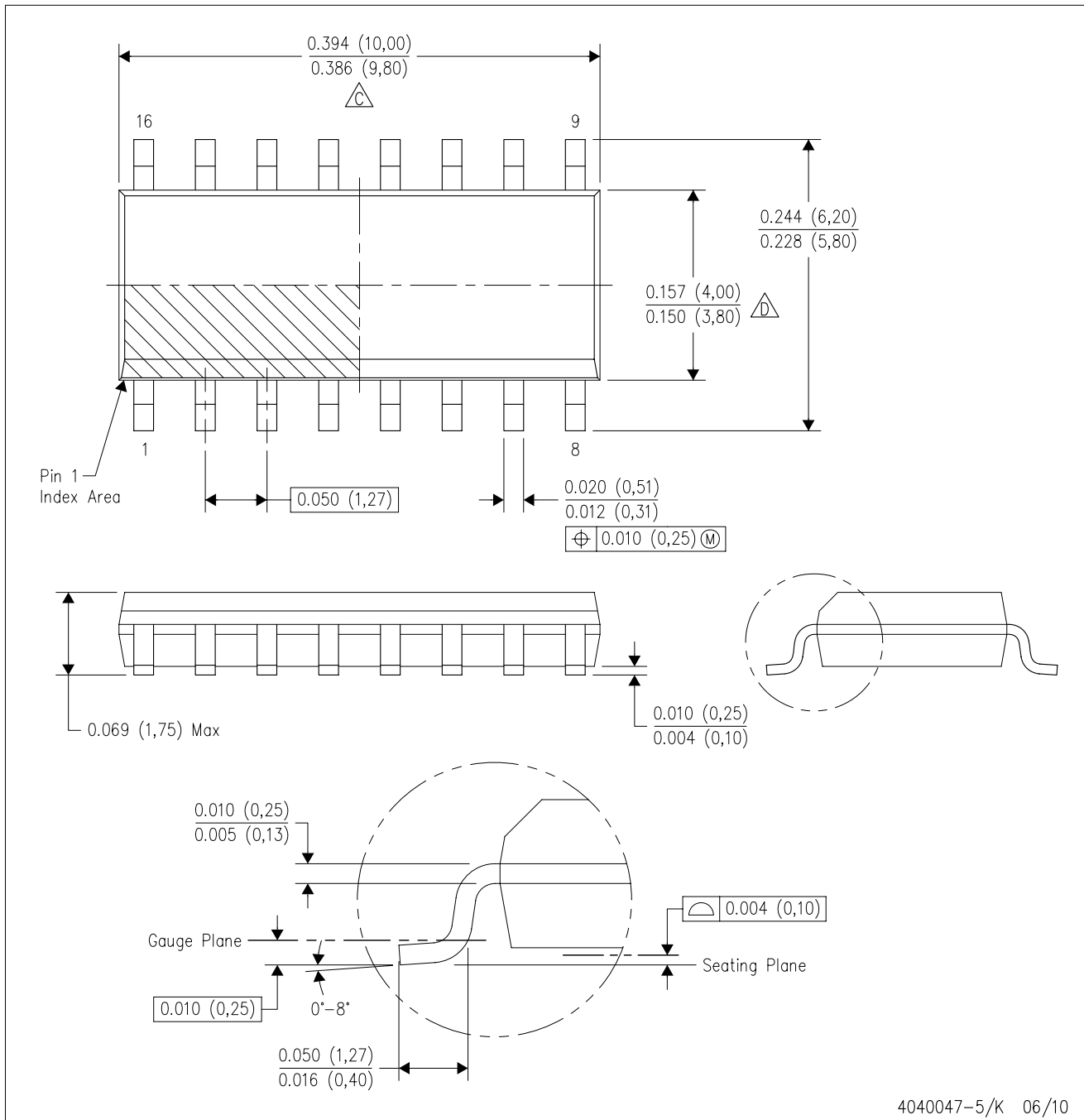
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal



| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AM26LV32EIDR   | SOIC         | D               | 16   | 2500 | 346.0       | 346.0      | 33.0        |
| AM26LV32EINSR  | SO           | NS              | 16   | 2000 | 346.0       | 346.0      | 33.0        |
| AM26LV32EIPWR  | TSSOP        | PW              | 16   | 2000 | 346.0       | 346.0      | 29.0        |
| AM26LV32EIRGYR | VQFN         | RGY             | 16   | 3000 | 346.0       | 346.0      | 29.0        |

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

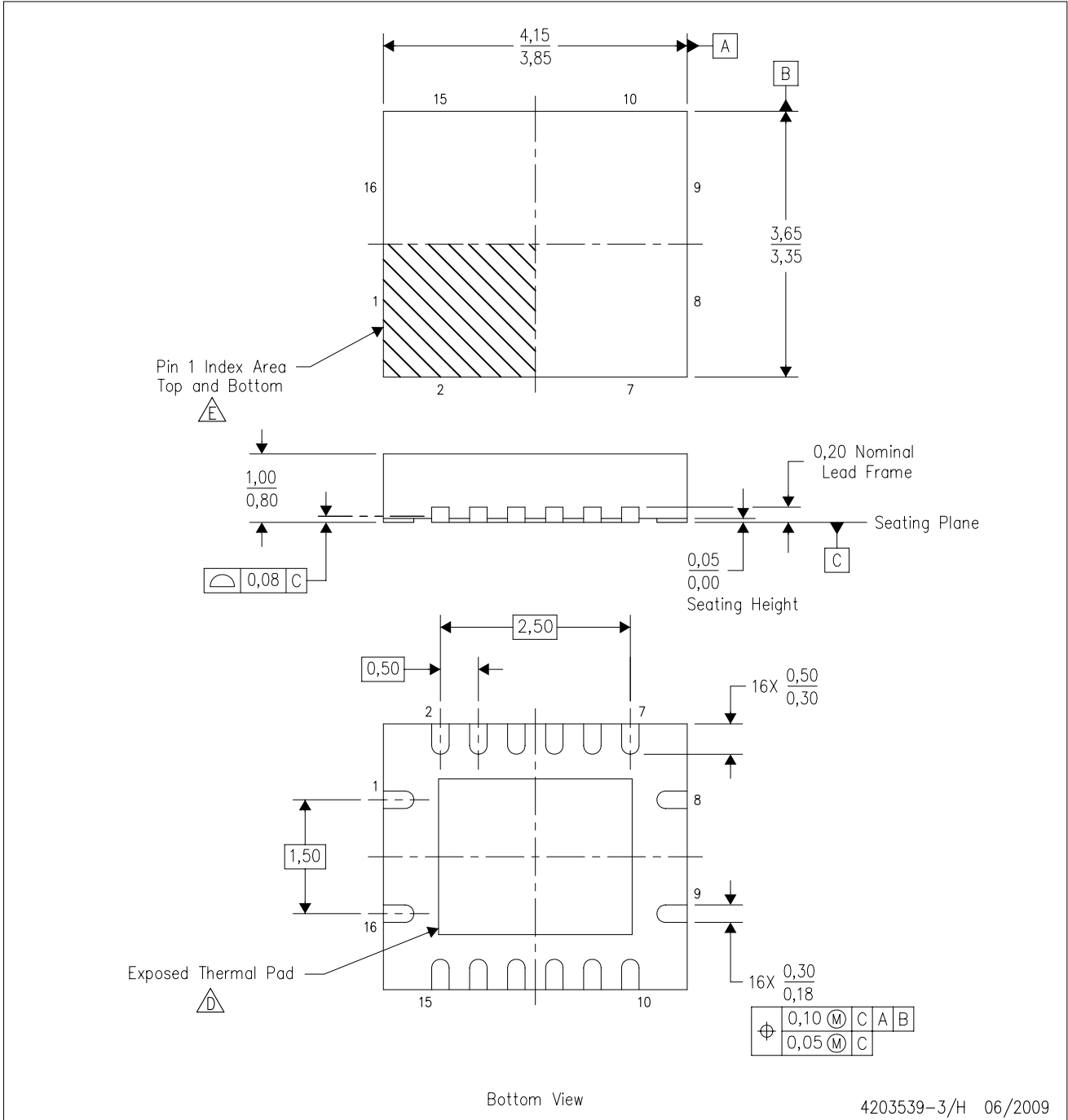


4040047-5/K 06/10

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-3/H 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BB.

## THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N16)

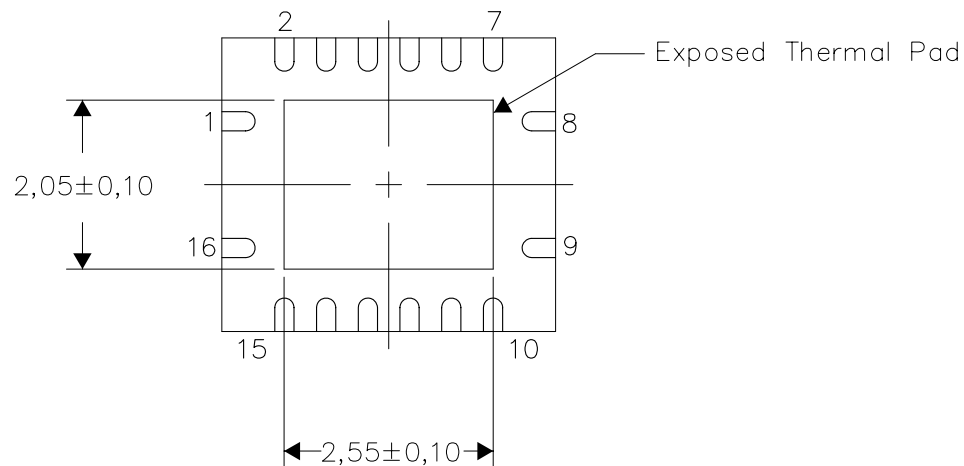
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

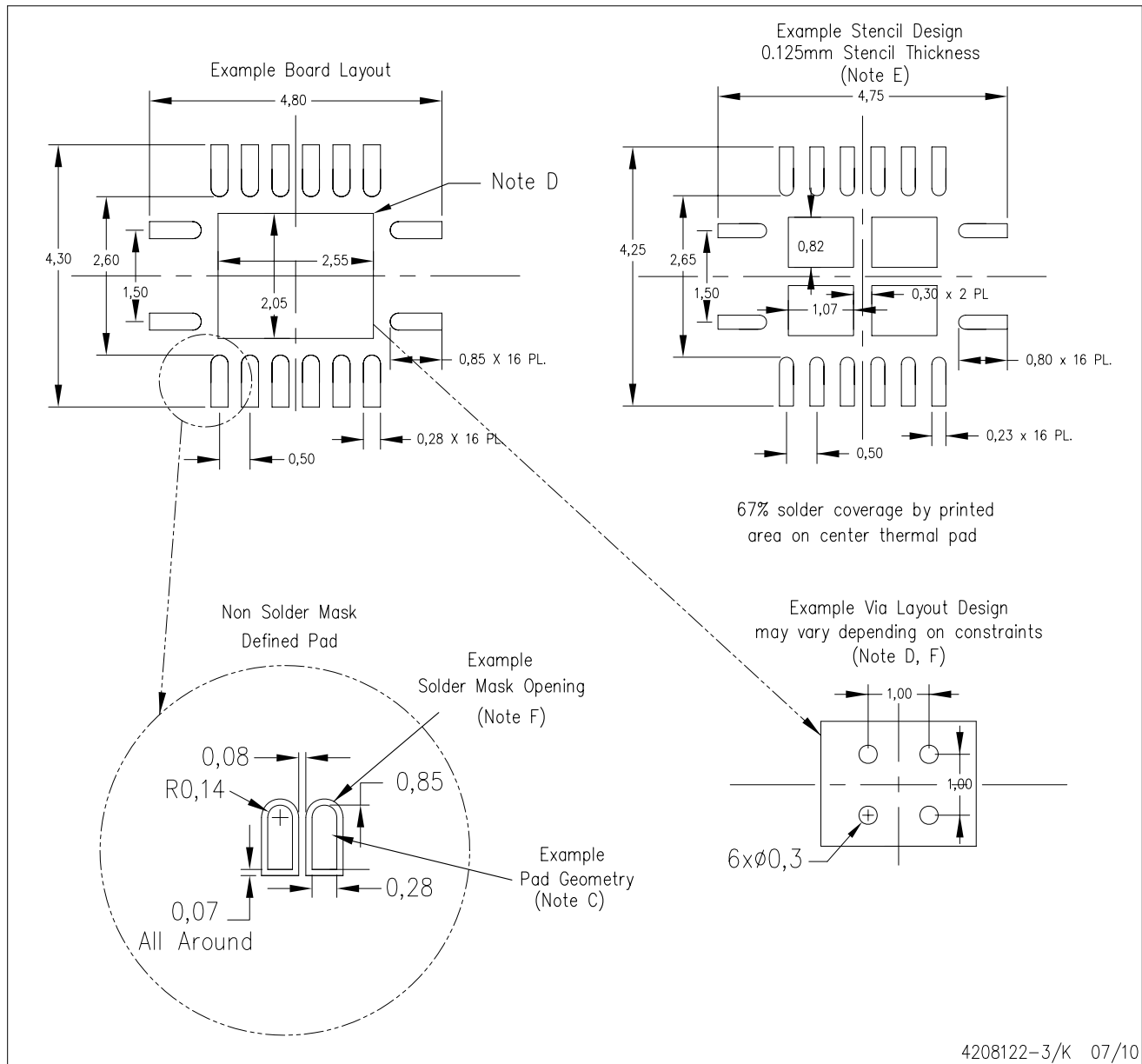
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206353-3/K 07/10

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



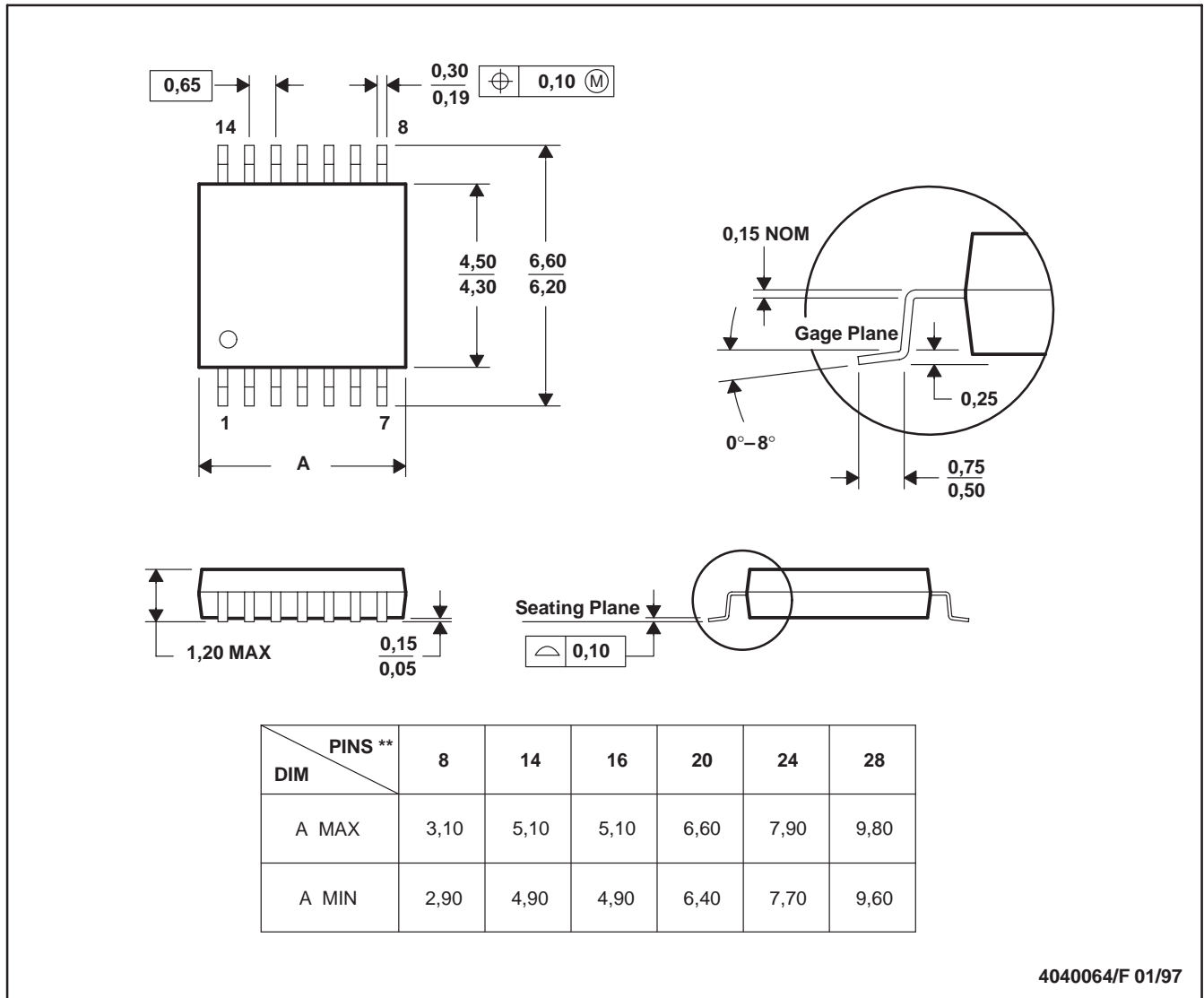
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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| Logic                       | <a href="http://logic.ti.com">logic.ti.com</a>                     | Industrial                 | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
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