

## ADuM3400/ADuM3401/ADuM3402

### FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x

Low power operation

5 V operation

1.4 mA per channel maximum @ 0 Mbps to 2 Mbps

4.3 mA per channel maximum @ 10 Mbps

34 mA per channel maximum @ 90 Mbps

3 V operation

0.9 mA per channel maximum @ 0 Mbps to 2 Mbps

2.4 mA per channel maximum @ 10 Mbps

20 mA per channel maximum @ 90 Mbps

Bidirectional communication

3 V/5 V level translation

High temperature operation: 105°C

High data rate: dc to 90 Mbps (NRZ)

Precise timing characteristics

2 ns maximum pulse-width distortion

2 ns maximum channel-to-channel matching

High common-mode transient immunity: >25 kV/μs

Output enable function

16-lead SOIC wide body, Pb-free package

Safety and regulatory approvals

UL recognition: 2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice #5A

VDE Certificate of Conformity

DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01

DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000

V<sub>IORM</sub> = 560 V peak

### APPLICATIONS

General-purpose multichannel isolation

SPI® interface/data converter isolation

RS-232/RS-422/RS-485 transceivers

Industrial field bus isolation

### GENERAL DESCRIPTION

The ADuM340x<sup>1</sup> are 4-channel digital isolators based on Analog Devices' *iCoupler*® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

*iCoupler* devices remove the design difficulties commonly associated with optocouplers. Typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM340x isolators provide three independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. The ADuM340x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

In comparison to the ADuM140x isolators, the ADuM340x isolators contain various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD/burst/surge). The precise capability in these tests for either the ADuM140x or ADuM340x products is strongly determined by the design and layout of the user's board or module. For more information, see [Application Note AN-793, ESD/Latch-Up Considerations with \*iCoupler\* Isolation Products](#).

<sup>1</sup> Protected by U.S. Patents 5,952,849 and 6,873,065. Other patents pending.

### FUNCTIONAL BLOCK DIAGRAMS

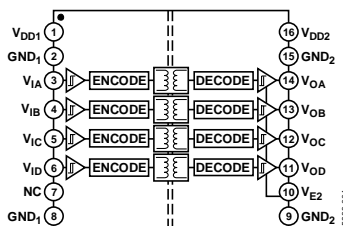


Figure 1. ADuM3400 Functional Block Diagram

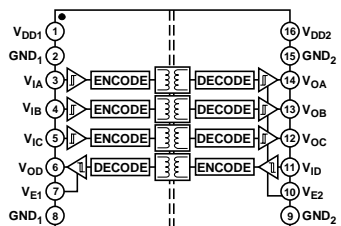


Figure 2. ADuM3401 Functional Block Diagram

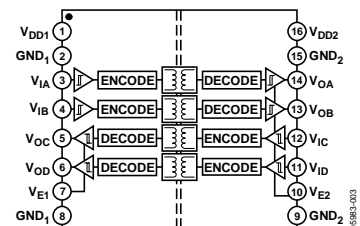


Figure 3. ADuM3402 Functional Block Diagram

#### Rev. 0

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## REVISION HISTORY

3/06—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 V OPERATION<sup>1</sup>

4.5 V ≤ V<sub>DD1</sub> ≤ 5.5 V, 4.5 V ≤ V<sub>DD2</sub> ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T<sub>A</sub> = 25°C, V<sub>DD1</sub> = V<sub>DD2</sub> = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current per Channel, Quiescent	I <sub>DD1(Q)</sub>		0.57	0.83	mA	
Output Supply Current per Channel, Quiescent	I <sub>DDO(Q)</sub>		0.29	0.35	mA	
ADuM3400, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1(Q)</sub>		2.9	3.5	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(Q)</sub>		1.2	1.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1(10)</sub>		9.0	11.6	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(10)</sub>		3.0	5.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1(90)</sub>		72	100	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(90)</sub>		19	36	mA	45 MHz logic signal freq.
ADuM3401, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1(Q)</sub>		2.5	3.2	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(Q)</sub>		1.6	2.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1(10)</sub>		7.4	10.6	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(10)</sub>		4.4	6.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1(90)</sub>		59	82	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(90)</sub>		32	46	mA	45 MHz logic signal freq.
ADuM3402, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	I <sub>DD1(Q), I<sub>DD2(Q)</sub></sub>		2.0	2.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	I <sub>DD1(10), I<sub>DD2(10)</sub></sub>		6.0	7.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	I <sub>DD1(90), I<sub>DD2(90)</sub></sub>		51	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I <sub>IA</sub> , I <sub>IB</sub> , I <sub>IC</sub> , I <sub>ID</sub> , I <sub>E1</sub> , I <sub>E2</sub>	-10	+0.01	+10	μA	0 ≤ V <sub>IA</sub> , V <sub>IB</sub> , V <sub>IC</sub> , V <sub>ID</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub> , 0 ≤ V <sub>E1</sub> , V <sub>E2</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub>
Logic High Input Threshold	V <sub>IH</sub> , V <sub>EH</sub>	2.0			V	
Logic Low Input Threshold	V <sub>IL</sub> , V <sub>EL</sub>			0.8	V	
Logic High Output Voltages	V <sub>OAH</sub> , V <sub>OBH</sub> , V <sub>OCH</sub> , V <sub>ODH</sub>	V <sub>DD1</sub> , V <sub>DD2</sub> - 0.1	5.0		V	I <sub>OX</sub> = -20 μA, V <sub>IX</sub> = V <sub>IXH</sub>
		V <sub>DD1</sub> , V <sub>DD2</sub> - 0.4	4.8		V	I <sub>OX</sub> = -4 mA, V <sub>IX</sub> = V <sub>IXH</sub>
Logic Low Output Voltages	V <sub>OAL</sub> , V <sub>OBL</sub> , V <sub>OCL</sub> , V <sub>ODL</sub>		0.0	0.1	V	I <sub>OX</sub> = 20 μA, V <sub>IX</sub> = V <sub>IXL</sub>
			0.04	0.1	V	I <sub>OX</sub> = 400 μA, V <sub>IX</sub> = V <sub>IXL</sub>
			0.2	0.4	V	I <sub>OX</sub> = 4 mA, V <sub>IX</sub> = V <sub>IXL</sub>

# ADuM3400/ADuM3401/ADuM3402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>SWITCHING SPECIFICATIONS</b>						
<b>ADuM340xARW</b>						
Minimum Pulse Width <sup>3</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		1			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	50	65	100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching <sup>7</sup>	t <sub>PSKCD/OD</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>ADuM340xBRW</b>						
Minimum Pulse Width <sup>3</sup>	PW			100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		10			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	32	50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			15	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	t <sub>PSKCD</sub>			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>ADuM340xCRW</b>						
Minimum Pulse Width <sup>3</sup>	PW		8.3	11.1	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		90	120		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	18	27	32	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			10	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	t <sub>PSKCD</sub>			2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			5	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>For All Models</b>						
Output Disable Propagation Delay (High/Low-to-High Impedance)	t <sub>PHZ</sub> , t <sub>PLH</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance-to-High/Low)	t <sub>PZH</sub> , t <sub>PZL</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>		2.5		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output <sup>8</sup>	CM <sub>H</sub>	25	35		kV/μs	V <sub>ix</sub> = V <sub>DD1</sub> /V <sub>DD2</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>8</sup>	CM <sub>L</sub>	25	35		kV/μs	V <sub>ix</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Refresh Rate	f <sub>r</sub>		1.2		Mbps	
Input Dynamic Supply Current per Channel <sup>9</sup>	I <sub>DDI (D)</sub>		0.20		mA/Mbps	
Output Dynamic Supply Current per Channel <sup>9</sup>	I <sub>DDO (D)</sub>		0.05		mA/Mbps	

- <sup>1</sup> All voltages are relative to their respective ground.
- <sup>2</sup> The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total  $V_{DD1}$  and  $V_{DD2}$  supply currents as a function of data rate for ADuM3400/ADuM3401/ADuM3402 channel configurations.
- <sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
- <sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
- <sup>5</sup>  $t_{PHL}$  propagation delay is measured from the 50% level of the falling edge of the  $V_{ix}$  signal to the 50% level of the falling edge of the  $V_{ox}$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level of the rising edge of the  $V_{ix}$  signal to the 50% level of the rising edge of the  $V_{ox}$  signal.
- <sup>6</sup>  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  or  $t_{PLH}$  that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
- <sup>7</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
- <sup>8</sup>  $CM_H$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O < 0.8 V$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
- <sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

# ADuM3400/ADuM3401/ADuM3402

## ELECTRICAL CHARACTERISTICS—3 V OPERATION<sup>1</sup>

2.7 V ≤ V<sub>DD1</sub> ≤ 3.6 V, 2.7 V ≤ V<sub>DD2</sub> ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T<sub>A</sub> = 25°C, V<sub>DD1</sub> = V<sub>DD2</sub> = 3.0 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current per Channel, Quiescent	I <sub>DD1(Q)</sub>		0.31	0.49	mA	
Output Supply Current per Channel, Quiescent	I <sub>DD0(Q)</sub>		0.19	0.27	mA	
<b>ADuM3400, Total Supply Current, Four Channels<sup>2</sup></b>						
<b>DC to 2 Mbps</b>						
V <sub>DD1</sub> Supply Current	I <sub>DD1(Q)</sub>		1.6	2.1	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(Q)</sub>		0.7	1.2	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
V <sub>DD1</sub> Supply Current	I <sub>DD1(10)</sub>		4.8	7.1	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(10)</sub>		1.8	2.3	mA	5 MHz logic signal freq.
<b>90 Mbps (CRW Grade Only)</b>						
V <sub>DD1</sub> Supply Current	I <sub>DD1(90)</sub>		37	54	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(90)</sub>		11	15	mA	45 MHz logic signal freq.
<b>ADuM3401, Total Supply Current, Four Channels<sup>2</sup></b>						
<b>DC to 2 Mbps</b>						
V <sub>DD1</sub> Supply Current	I <sub>DD1(Q)</sub>		1.4	1.9	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(Q)</sub>		0.9	1.5	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
V <sub>DD1</sub> Supply Current	I <sub>DD1(10)</sub>		4.1	5.6	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(10)</sub>		2.5	3.3	mA	5 MHz logic signal freq.
<b>90 Mbps (CRW Grade Only)</b>						
V <sub>DD1</sub> Supply Current	I <sub>DD1(90)</sub>		31	44	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2(90)</sub>		17	24	mA	45 MHz logic signal freq.
<b>ADuM3402, Total Supply Current, Four Channels<sup>2</sup></b>						
<b>DC to 2 Mbps</b>						
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	I <sub>DD1(Q), I<sub>DD2(Q)</sub></sub>		1.2	1.7	mA	DC to 1 MHz logic signal freq.
<b>10 Mbps (BRW and CRW Grades Only)</b>						
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	I <sub>DD1(10), I<sub>DD2(10)</sub></sub>		3.3	4.4	mA	5 MHz logic signal freq.
<b>90 Mbps (CRW Grade Only)</b>						
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	I <sub>DD1(90), I<sub>DD2(90)</sub></sub>		24	39	mA	45 MHz logic signal freq.
<b>For All Models</b>						
Input Currents	I <sub>IA</sub> , I <sub>IB</sub> , I <sub>IC</sub> , I <sub>ID</sub> , I <sub>E1</sub> , I <sub>E2</sub>	-10	+0.01	+10	μA	0 ≤ V <sub>IA</sub> , V <sub>IB</sub> , V <sub>IC</sub> , V <sub>ID</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub> , 0 ≤ V <sub>E1</sub> , V <sub>E2</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub>
Logic High Input Threshold	V <sub>IH</sub> , V <sub>EH</sub>	1.6			V	
Logic Low Input Threshold	V <sub>IL</sub> , V <sub>EL</sub>			0.4	V	
Logic High Output Voltages	V <sub>OAH</sub> , V <sub>OBH</sub> , V <sub>OCH</sub> , V <sub>ODH</sub>	V <sub>DD1</sub> , V <sub>DD2</sub> - 0.1	3.0		V	I <sub>Ox</sub> = -20 μA, V <sub>Ix</sub> = V <sub>IxH</sub>
		V <sub>DD1</sub> , V <sub>DD2</sub> - 0.4	2.8		V	I <sub>Ox</sub> = -4 mA, V <sub>Ix</sub> = V <sub>IxH</sub>
Logic Low Output Voltages	V <sub>OAL</sub> , V <sub>OBL</sub> , V <sub>OCL</sub> , V <sub>ODL</sub>		0.0	0.1	V	I <sub>Ox</sub> = 20 μA, V <sub>Ix</sub> = V <sub>IxL</sub>
			0.04	0.1	V	I <sub>Ox</sub> = 400 μA, V <sub>Ix</sub> = V <sub>IxL</sub>
			0.2	0.4	V	I <sub>Ox</sub> = 4 mA, V <sub>Ix</sub> = V <sub>IxL</sub>
<b>SWITCHING SPECIFICATIONS</b>						
<b>ADuM340xARW</b>						
Minimum Pulse Width <sup>3</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		1			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	50	75	100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching <sup>7</sup>	t <sub>PSKCD/OD</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels

# ADuM3400/ADuM3401/ADuM3402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>ADuM340xBRW</b>						
Minimum Pulse Width <sup>3</sup>	PW			100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		10			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	38	50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>    <sup>5</sup>	PWD			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			22	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	t <sub>PSKCD</sub>			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>ADuM340xCRW</b>						
Minimum Pulse Width <sup>3</sup>	PW		8.3	11.1	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		90	120		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	34	45	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>    <sup>5</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			16	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	t <sub>PSKCD</sub>			2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			5	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>For All Models</b>						
Output Disable Propagation Delay (High/Low-to-High Impedance)	t <sub>PHZ</sub> , t <sub>PLH</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance-to-High/Low)	t <sub>PZH</sub> , t <sub>PZL</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>		3		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output <sup>8</sup>	CM <sub>H</sub>	25	35		kV/μs	V <sub>ix</sub> = V <sub>DD1</sub> /V <sub>DD2</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>8</sup>	CM <sub>L</sub>	25	35		kV/μs	V <sub>ix</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Refresh Rate	f <sub>r</sub>		1.1		Mbps	
Input Dynamic Supply Current per Channel <sup>9</sup>	I <sub>DDI(D)</sub>		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel <sup>9</sup>	I <sub>DDO(D)</sub>		0.03		mA/Mbps	

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V<sub>DD1</sub> and V<sub>DD2</sub> supply currents as a function of data rate for ADuM3400/ADuM3401/ADuM3402 channel configurations.

<sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.

<sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.

<sup>5</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>ix</sub> signal to the 50% level of the falling edge of the V<sub>ox</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>ix</sub> signal to the 50% level of the rising edge of the V<sub>ox</sub> signal.

<sup>6</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> or t<sub>PLH</sub> that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>7</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>8</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

# ADuM3400/ADuM3401/ADuM3402

## ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION<sup>1</sup>

5 V/3 V operation:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ ; 3 V/5 V operation:  $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ ; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at  $T_A = 25^\circ\text{C}$ ;  $V_{DD1} = 3.0\text{ V}$ ,  $V_{DD2} = 5\text{ V}$  or  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$ .

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DD1(Q)}$					
5 V/3 V Operation			0.57	0.83	mA	
3 V/5 V Operation			0.31	0.49	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$					
5 V/3 V Operation			0.29	0.27	mA	
3 V/5 V Operation			0.19	0.35	mA	
ADuM3400, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
$V_{DD1}$ Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			2.9	3.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.6	2.1	mA	DC to 1 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.7	1.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
$V_{DD1}$ Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			9.0	11.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.8	7.1	mA	5 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			1.8	2.3	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.0	5.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
$V_{DD1}$ Supply Current	$I_{DD1(90)}$					
5 V/3 V Operation			72	100	mA	45 MHz logic signal freq.
3 V/5 V Operation			37	54	mA	45 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(90)}$					
5 V/3 V Operation			11	15	mA	45 MHz logic signal freq.
3 V/5 V Operation			19	36	mA	45 MHz logic signal freq.
ADuM3401, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
$V_{DD1}$ Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			2.5	3.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.4	1.9	mA	DC to 1 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.6	2.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
$V_{DD1}$ Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			7.4	10.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.1	5.6	mA	5 MHz logic signal freq.
$V_{DD2}$ Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			2.5	3.3	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.4	6.5	mA	5 MHz logic signal freq.



# ADuM3400/ADuM3401/ADuM3402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (90)</sub>		59	82	mA	45 MHz logic signal freq.
5 V/3 V Operation			31	44	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (90)</sub>		17	24	mA	45 MHz logic signal freq.
5 V/3 V Operation			32	46	mA	45 MHz logic signal freq.
3 V/5 V Operation						45 MHz logic signal freq.
ADuM3402, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (Q)</sub>		2.0	2.8	mA	DC to 1 MHz logic signal freq.
5 V/3 V Operation			1.2	1.7	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (Q)</sub>		1.2	1.7	mA	DC to 1 MHz logic signal freq.
5 V/3 V Operation			2.0	2.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation						DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (10)</sub>		6.0	7.5	mA	5 MHz logic signal freq.
5 V/3 V Operation			3.3	4.4	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (10)</sub>		3.3	4.4	mA	5 MHz logic signal freq.
5 V/3 V Operation			6.0	7.5	mA	5 MHz logic signal freq.
3 V/5 V Operation						5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (90)</sub>		46	62	mA	45 MHz logic signal freq.
5 V/3 V Operation			24	39	mA	45 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (90)</sub>		24	39	mA	45 MHz logic signal freq.
5 V/3 V Operation			46	62	mA	45 MHz logic signal freq.
3 V/5 V Operation						45 MHz logic signal freq.
For All Models						
Input Currents	I <sub>IA</sub> , I <sub>IB</sub> , I <sub>IC</sub> , I <sub>ID</sub> , I <sub>E1</sub> , I <sub>E2</sub>	-10	+0.01	+10	μA	0 ≤ V <sub>IA</sub> , V <sub>IB</sub> , V <sub>IC</sub> , V <sub>ID</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub> , 0 ≤ V <sub>E1</sub> , V <sub>E2</sub> ≤ V <sub>DD1</sub> or V <sub>DD2</sub>
Logic High Input Threshold	V <sub>IH</sub> , V <sub>EH</sub>					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V <sub>IL</sub> , V <sub>EL</sub>					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V <sub>OA</sub> H, V <sub>OB</sub> H, V <sub>OC</sub> H, V <sub>OD</sub> H	V <sub>DD1</sub> , V <sub>DD2</sub> - 0.1	V <sub>DD1</sub> , V <sub>DD2</sub>		V	I <sub>OX</sub> = -20 μA, V <sub>Ix</sub> = V <sub>IxH</sub>
		V <sub>DD1</sub> , V <sub>DD2</sub> - 0.4	V <sub>DD1</sub> , V <sub>DD2</sub> - 0.2		V	I <sub>OX</sub> = -4 mA, V <sub>Ix</sub> = V <sub>IxH</sub>
Logic Low Output Voltages	V <sub>OAL</sub> , V <sub>OBL</sub> , V <sub>OCL</sub> , V <sub>ODL</sub>		0.0	0.1	V	I <sub>OX</sub> = 20 μA, V <sub>Ix</sub> = V <sub>IxL</sub>
			0.04	0.1	V	I <sub>OX</sub> = 400 μA, V <sub>Ix</sub> = V <sub>IxL</sub>
			0.2	0.4	V	I <sub>OX</sub> = 4 mA, V <sub>Ix</sub> = V <sub>IxL</sub>
SWITCHING SPECIFICATIONS						
ADuM340xARW						
Minimum Pulse Width <sup>3</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		1			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	50	70	100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching <sup>7</sup>	t <sub>PSKCD/OD</sub>			50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels

# ADuM3400/ADuM3401/ADuM3402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>ADuM340xBRW</b>						
Minimum Pulse Width <sup>3</sup>	PW			100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		10			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	15	35	50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			22	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	t <sub>PSKCD</sub>			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>ADuM340xCRW</b>						
Minimum Pulse Width <sup>3</sup>	PW		8.3	11.1	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		90	120		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	t <sub>PHL</sub> , t <sub>PLH</sub>	20	30	40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion,  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>5</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			14	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels <sup>7</sup>	t <sub>PSKCD</sub>			2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			5	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
<b>For All Models</b>						
Output Disable Propagation Delay (High/Low-to-High Impedance)	t <sub>PHZ</sub> , t <sub>PLH</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance-to-High/Low)	t <sub>PZH</sub> , t <sub>PZL</sub>		6	8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>					C <sub>L</sub> = 15 pF, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output <sup>8</sup>	CM <sub>H</sub>	25	35		kV/μs	V <sub>ix</sub> = V <sub>DD1</sub> /V <sub>DD2</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>8</sup>	CM <sub>L</sub>	25	35		kV/μs	V <sub>ix</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Refresh Rate	f <sub>r</sub>					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel <sup>9</sup>	I <sub>DDI (D)</sub>					
5 V/3 V Operation			0.20		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current per Channel <sup>9</sup>	I <sub>DDO (D)</sub>					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

- <sup>1</sup> All voltages are relative to their respective ground.
- <sup>2</sup> The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total  $V_{DD1}$  and  $V_{DD2}$  supply currents as a function of data rate for ADuM3400/ADuM3401/ADuM3402 channel configurations.
- <sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
- <sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
- <sup>5</sup>  $t_{PHL}$  propagation delay is measured from the 50% level of the falling edge of the  $V_{ix}$  signal to the 50% level of the falling edge of the  $V_{ox}$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level of the rising edge of the  $V_{ix}$  signal to the 50% level of the rising edge of the  $V_{ox}$  signal.
- <sup>6</sup>  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  or  $t_{PLH}$  that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
- <sup>7</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
- <sup>8</sup>  $CM_H$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O < 0.8 V$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
- <sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

# ADuM3400/ADuM3401/ADuM3402

## PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input to Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	
Capacitance (Input to Output) <sup>1</sup>	C <sub>I-O</sub>		2.2		pF	f = 1 MHz
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ <sub>JCI</sub>		33		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ <sub>JCO</sub>		28		°C/W	

<sup>1</sup> Device considered a 2-terminal device; Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 shorted together and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

## REGULATORY INFORMATION

The ADuM340x is approved by the organizations listed in Table 5.

Table 5.

UL <sup>1</sup>	CSA	VDE <sup>2</sup>
Recognized under 1577 component recognition program <sup>1</sup> Double/reinforced insulation, 2500 V rms isolation voltage  File E214100	Approved under CSA Component Acceptance Notice #5A Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms maximum working voltage  File 205078	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01 <sup>2</sup> Basic insulation, 560 V peak  Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000 Reinforced insulation, 560 V peak File 2471900-4880-0001

<sup>1</sup> In accordance with UL1577, each ADuM340x is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).

<sup>2</sup> In accordance with DIN EN 60747-5-2, each ADuM340x is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN EN 60747-5-2 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS

Table 7.

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage $\leq 150$ V rms For Rated Mains Voltage $\leq 300$ V rms For Rated Mains Voltage $\leq 400$ V rms		I-IV I-III I-II	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	560	V peak
Input-to-Output Test Voltage, Method b1 $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test, $t_m = 1$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	1050	V peak
Input-to-Output Test Voltage, Method a After Environmental Tests Subgroup 1 $V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	896	V peak
After Input and/or Safety Test Subgroup 2/3 $V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge $< 5$ pC		672	V peak
Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR} = 10$ sec)	$V_{TR}$	4000	V peak
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure; also see Figure 4)			
Case Temperature	$T_S$	150	$^{\circ}C$
Side 1 Current	$I_{S1}$	265	mA
Side 2 Current	$I_{S2}$	335	mA
Insulation Resistance at $T_S, V_{IO} = 500$ V	$R_S$	$>10^9$	$\Omega$

These isolators are suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The \* marking on packages denotes DIN EN 60747-5-2 approval.

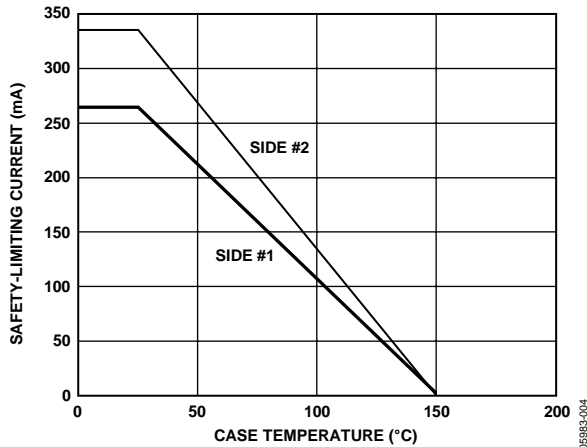


Figure 4. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	$T_A$	-40	+105	$^{\circ}C$
Supply Voltages <sup>1</sup>	$V_{DD1}, V_{DD2}$	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

<sup>1</sup> All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

# ADuM3400/ADuM3401/ADuM3402

## ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	$T_{ST}$	-65	+150	°C
Ambient Operating Temperature	$T_A$	-40	+105	°C
Supply Voltages <sup>1</sup>	$V_{DD1}, V_{DD2}$	-0.5	+7.0	V
Input Voltage <sup>1, 2</sup>	$V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}$	-0.5	$V_{DD1} + 0.5$	V
Output Voltage <sup>1, 2</sup>	$V_{OA}, V_{OB}, V_{OC}, V_{OD}$	-0.5	$V_{DD0} + 0.5$	V
Average Output Current per Pin <sup>3</sup>				
Side 1	$I_{O1}$	-18	+18	mA
Side 2	$I_{O2}$	-22	+22	mA
Common-Mode Transients <sup>4</sup>	$CM_H, CM_L$	-100	+100	kV/ $\mu$ s

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup>  $V_{DD1}$  and  $V_{DD0}$  refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.

<sup>3</sup> See Figure 4 for maximum rated current values for various temperatures.

<sup>4</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 10. Truth Table (Positive Logic)

$V_{IX}$ Input <sup>1</sup>	$V_{EX}$ Input <sup>2</sup>	$V_{DD1}$ State <sup>1</sup>	$V_{DD0}$ State <sup>1</sup>	$V_{OX}$ Output <sup>1</sup>	Notes
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs return to the input state within 1 $\mu$ s of $V_{DD1}$ power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs return to the input state within 1 $\mu$ s of $V_{DD0}$ power restoration if $V_{EX}$ state is H or NC. Outputs return to high impedance state within 8 ns of $V_{DD0}$ power restoration if $V_{EX}$ state is L.

<sup>1</sup>  $V_{IX}$  and  $V_{OX}$  refer to the input and output signals of a given channel (A, B, C, or D).  $V_{EX}$  refers to the output enable signal on the same side as the  $V_{OX}$  outputs.  $V_{DD1}$  and  $V_{DD0}$  refer to the supply voltages on the input and output sides of the given channel, respectively.

<sup>2</sup> In noisy environments, connecting  $V_{EX}$  to an external logic high or low is recommended.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

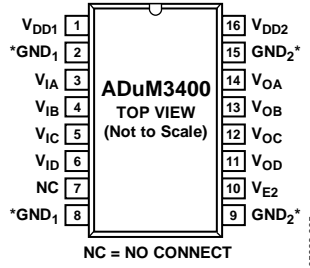


Figure 5. ADuM3400 Pin Configuration

\*Pin 2 and Pin 8 are internally connected and connecting both to GND<sub>1</sub> is recommended. Pin 9 and Pin 15 are internally connected and connecting both to GND<sub>2</sub> is recommended. In noisy environments, connecting output enables (Pin 7 for ADuM3401/ADuM3402 and Pin 10 for all models) to an external logic high or low is recommended.

Table 11. ADuM3400 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2, 8	GND <sub>1</sub>	Ground 1. Ground Reference for Isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>IC</sub>	Logic Input C.
6	V <sub>ID</sub>	Logic Input D.
7	NC	No Connect.
9, 15	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. V <sub>OA</sub> , V <sub>OB</sub> , V <sub>OC</sub> , and V <sub>OD</sub> outputs are enabled when V <sub>E2</sub> is high or disconnected. V <sub>OA</sub> , V <sub>OB</sub> , V <sub>OC</sub> , and V <sub>OD</sub> outputs are disabled when V <sub>E2</sub> is low. In noisy environments, connecting V <sub>E2</sub> to an external logic high or low is recommended.
11	V <sub>OD</sub>	Logic Output D.
12	V <sub>OC</sub>	Logic Output C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

# ADuM3400/ADuM3401/ADuM3402

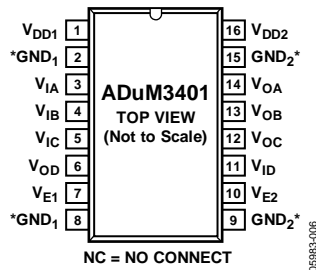


Figure 6. ADuM3401 Pin Configuration

\*Pin 2 and Pin 8 are internally connected and connecting both to GND<sub>1</sub> is recommended. Pin 9 and Pin 15 are internally connected and connecting both to GND<sub>2</sub> is recommended. In noisy environments, connecting output enables (Pin 7 for ADuM3401/ADuM3402 and Pin 10 for all models) to an external logic high or low is recommended.

Table 12. ADuM3401 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2, 8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>IC</sub>	Logic Input C.
6	V <sub>OD</sub>	Logic Output D.
7	V <sub>E1</sub>	Output Enable 1. Active high logic input. V <sub>OD</sub> output is enabled when V <sub>E1</sub> is high or disconnected. V <sub>OD</sub> is disabled when V <sub>E1</sub> is low. In noisy environments, connecting V <sub>E1</sub> to an external logic high or low is recommended.
9, 15	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. V <sub>OA</sub> , V <sub>OB</sub> , and V <sub>OC</sub> outputs are enabled when V <sub>E2</sub> is high or disconnected. V <sub>OA</sub> , V <sub>OB</sub> , and V <sub>OC</sub> outputs are disabled when V <sub>E2</sub> is low. In noisy environments, connecting V <sub>E2</sub> to an external logic high or low is recommended.
11	V <sub>ID</sub>	Logic Input D.
12	V <sub>OC</sub>	Logic Output C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.



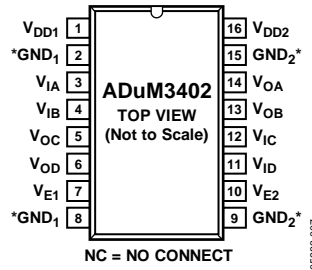


Figure 7. ADuM3402 Pin Configuration

\*Pin 2 and Pin 8 are internally connected and connecting both to GND<sub>1</sub> is recommended. Pin 9 and Pin 15 are internally connected and connecting both to GND<sub>2</sub> is recommended. In noisy environments, connecting output enables (Pin 7 for ADuM3401/ADuM3402 and Pin 10 for all models) to an external logic high or low is recommended.

**Table 13. ADuM3402 Pin Function Descriptions**

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2, 8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
3	V <sub>IA</sub>	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	V <sub>OC</sub>	Logic Output C.
6	V <sub>OD</sub>	Logic Output D.
7	V <sub>E1</sub>	Output Enable 1. Active high logic input. V <sub>OC</sub> and V <sub>OD</sub> outputs are enabled when V <sub>E1</sub> is high or disconnected. V <sub>OC</sub> and V <sub>OD</sub> outputs are disabled when V <sub>E1</sub> is low. In noisy environments, connecting V <sub>E1</sub> to an external logic high or low is recommended.
9, 15	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. V <sub>OA</sub> and V <sub>OB</sub> outputs are enabled when V <sub>E2</sub> is high or disconnected. V <sub>OA</sub> and V <sub>OB</sub> outputs are disabled when V <sub>E2</sub> is low. In noisy environments, connecting V <sub>E2</sub> to an external logic high or low is recommended.
11	V <sub>ID</sub>	Logic Input D.
12	V <sub>IC</sub>	Logic Input C.
13	V <sub>OB</sub>	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

## TYPICAL PERFORMANCE CHARACTERISTICS

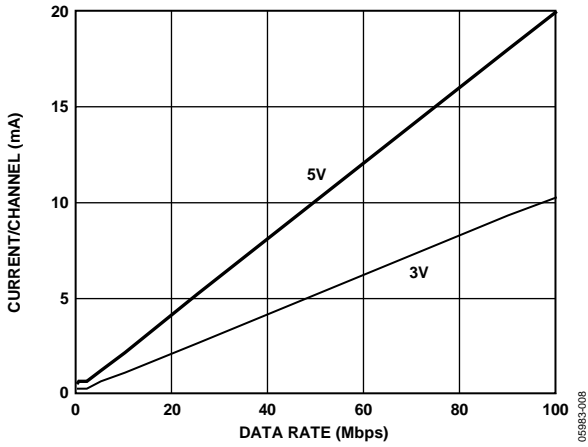


Figure 8. Typical Input Supply Current per Channel vs. Data Rate (No Load)

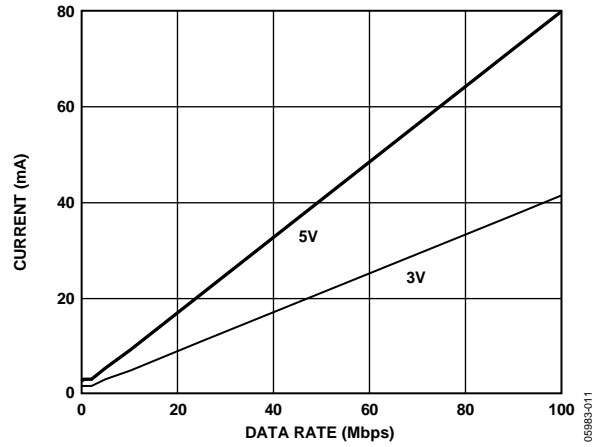


Figure 11. Typical ADuM3400  $V_{DD1}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

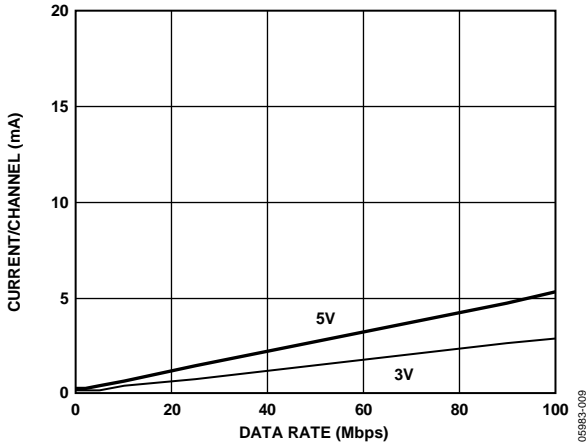


Figure 9. Typical Output Supply Current per Channel vs. Data Rate (No Load)

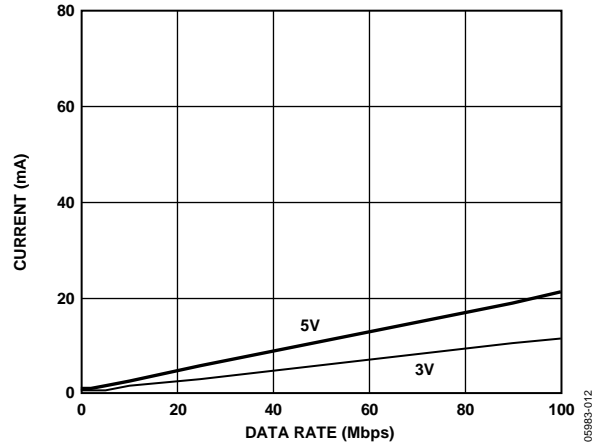


Figure 12. Typical ADuM3400  $V_{DD2}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

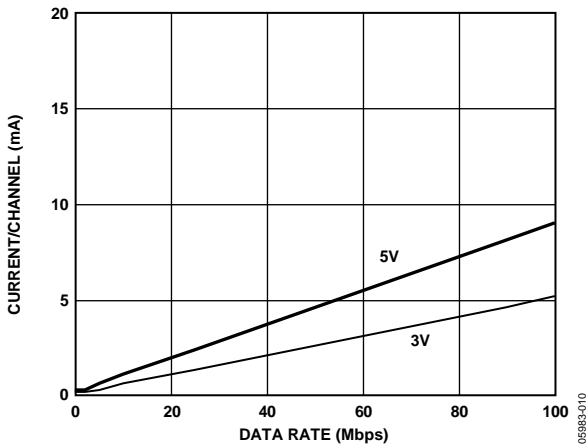


Figure 10. Typical Output Supply Current per Channel vs. Data Rate (15 pF Output Load)

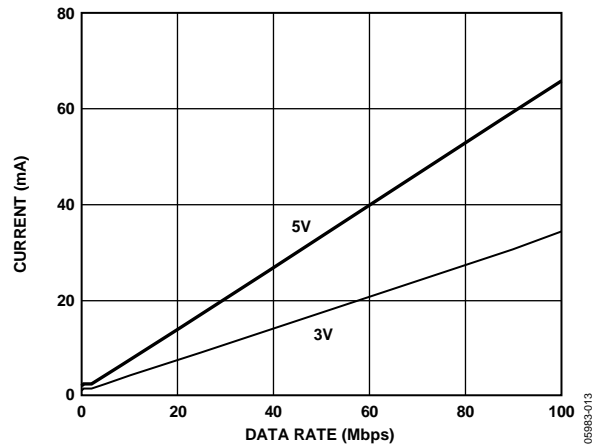


Figure 13. Typical ADuM3401  $V_{DD1}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

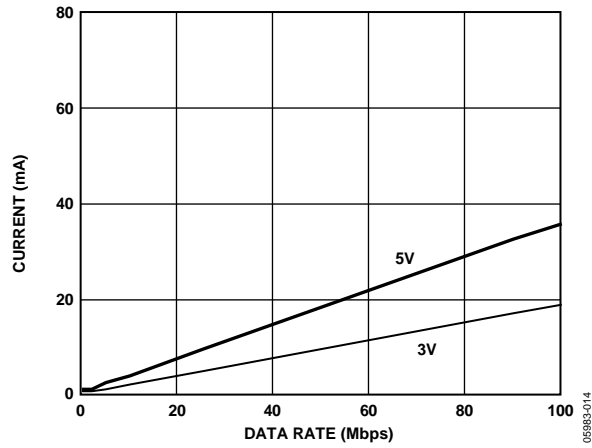


Figure 14. Typical ADuM3401  $V_{DD2}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

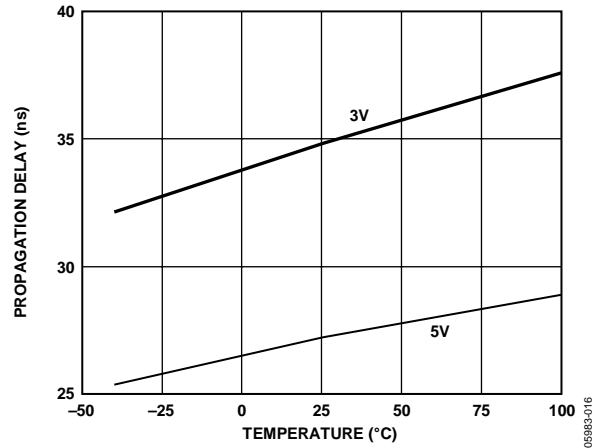


Figure 16. Propagation Delay vs. Temperature, C Grade

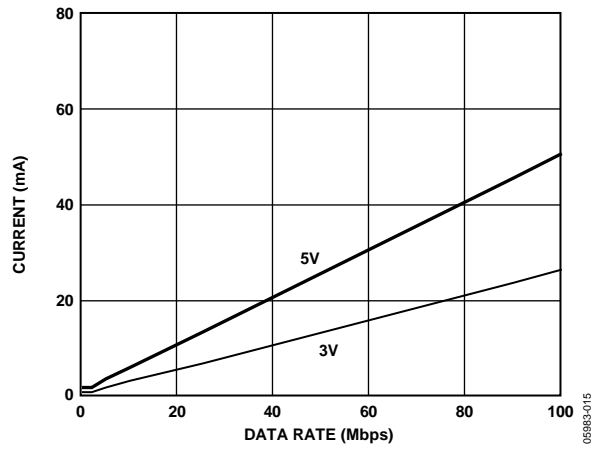


Figure 15. Typical ADuM3402  $V_{DD1}$  or  $V_{DD2}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

## APPLICATION INFORMATION

### PC BOARD LAYOUT

The ADuM340x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for  $V_{DD1}$  and between Pin 15 and Pin 16 for  $V_{DD2}$ . The capacitor value should be between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ . The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

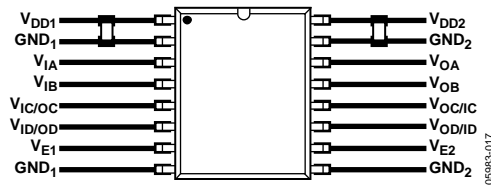


Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, thereby leading to latch-up or permanent damage.

### SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design which varies widely by application. The ADuM340x incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation technique between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM340x improve system-level ESD reliability, they are no substitute for a robust system-level design. See [Application Note AN-793 ESD/Latch-Up Considerations with iCoupler Isolation Products](#) for detailed recommendations on board layout and system-level design.

### PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high.

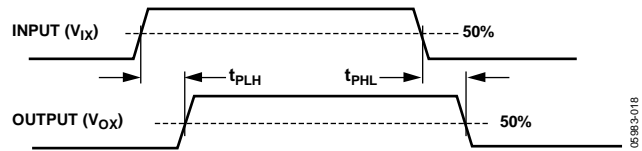


Figure 18. Propagation Delay Parameters

Pulse-width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM340x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM340x components operating under the same conditions.

### DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 2  $\mu\text{s}$ , a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5  $\mu\text{s}$ , the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 10) by the watchdog timer circuit.

The limitation on the ADuM340x's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM340x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \Pi r_n^2; n = 1, 2, \dots, N$$

where:

$\beta$  is magnetic flux density (gauss).

$N$  is the number of turns in the receiving coil.

$r_n$  is the radius of the  $n^{\text{th}}$  turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM340x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.

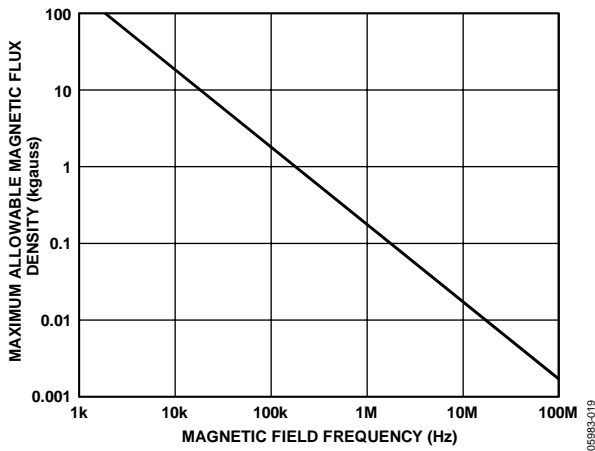


Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM340x transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM340x is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM340x to affect the component's operation.

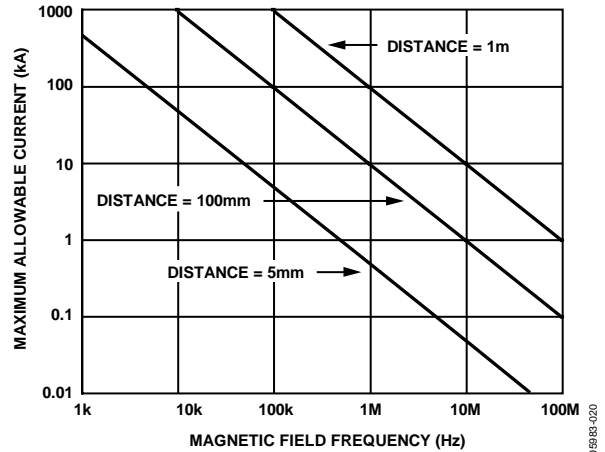


Figure 20. Maximum Allowable Current for Various Current-to-ADuM340x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

# ADuM3400/ADuM3401/ADuM3402

## POWER CONSUMPTION

The supply current at a given channel of the ADuM340x isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5 f_r$$
$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5 f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5 f_r$$
$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5 f_r$$

where:

$I_{DDI(D)}$ ,  $I_{DDO(D)}$  are the input and output dynamic supply currents per channel (mA/Mbps).

$C_L$  is the output load capacitance (pF).

$V_{DDO}$  is the output supply voltage (V).

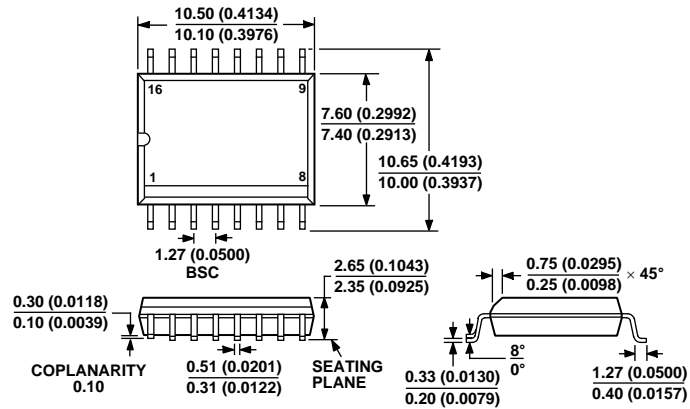
$f$  is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.

$f_r$  is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$ ,  $I_{DDO(Q)}$  are the specified input and output quiescent supply currents (mA).

To calculate the total  $I_{DD1}$  and  $I_{DD2}$  supply current, the supply currents for each input and output channel corresponding to  $V_{DD1}$  and  $V_{DD2}$  are calculated and totaled. Figure 8 provides per-channel input supply current as a function of data rate. Figure 9 and Figure 10 provide per-channel supply output current as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 11 through Figure 15 provide total  $V_{DD1}$  and  $V_{DD2}$  supply current as a function of data rate for ADuM3400/ADuM3401/ADuM3402 channel configurations.

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 21. 16-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body (RW-16)

Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model	Temperature Range (°C)	Number of Inputs, V <sub>DD1</sub> Side	Number of Inputs, V <sub>DD2</sub> Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse-Width Distortion (ns)	Package Option <sup>1</sup>
ADuM3400ARWZ <sup>2,3</sup>	-40 to +105	4	0	1	100	40	RW-16
ADuM3400BRWZ <sup>2,3</sup>	-40 to +105	4	0	10	50	3	RW-16
ADuM3400CRWZ <sup>2,3</sup>	-40 to +105	4	0	90	32	2	RW-16
ADuM3401ARWZ <sup>2,3</sup>	-40 to +105	3	1	1	100	40	RW-16
ADuM3401BRWZ <sup>2,3</sup>	-40 to +105	3	1	10	50	3	RW-16
ADuM3401CRWZ <sup>2,3</sup>	-40 to +105	3	1	90	32	2	RW-16
ADuM3402ARWZ <sup>2,3</sup>	-40 to +105	2	2	1	100	40	RW-16
ADuM3402BRWZ <sup>2,3</sup>	-40 to +105	2	2	10	50	3	RW-16
ADuM3402CRWZ <sup>2,3</sup>	-40 to +105	2	2	90	32	2	RW-16

<sup>1</sup> RW-16 = 16-lead wide body SOIC.

<sup>2</sup> Tape and reel are available. The addition of an "RL" suffix designates a 13" (1,000 units) tape and reel option.

<sup>3</sup> Z = Pb-free part.

**NOTES**