Data Sheet

LTC4296-1

5-Port SPoE PSE Controller

FEATURES

- IEEE 802.3cg-compliant SPoE PSE
- Five independent PSE ports
- Wide input-supply operating range: 6 V to 60 V
- Adjustable source and return electronic circuit breakers
- 52 µA (typical) and 51 µA (typical) input supply current in sleep and disabled states, respectively
- Charge pump enhances the external, high-side, N-channel MOSFETs
- Supports SCCP with external microcontroller
- SPI bus interface with PEC
- Voltage, current, and temperature telemetry
- Per port power-good comparators
- PD sleep, wake-up, and wake-up forwarding support
- Available in 48-lead, 7 mm × 7 mm, QFN package

APPLICATIONS

- Operational technology (OT) systems
- Building and factory automation systems
- Field instruments and switches
- Security systems
- Traffic control systems

GENERAL DESCRIPTION

The LTC4296-1 is an IEEE 802.3cg-compliant, five port, single-pair power over Ethernet (SPoE), power sourcing equipment (PSE) controller. SPoE simplifies system design and installation with standardized power and Ethernet data over a single-pair cable. The LTC4296-1 is designed for interoperability with 802.3cg powered devices (PDs) in 24 V or 54 V systems. The LTC4296-1 delivers power using external, low drain-to-source on resistance ($R_{DS(ON)}$), N-channel metal-oxide semiconductor field-effect transistors (MOSFETs), which minimize voltage drop and ensure application ruggedness.

High-side circuit breakers with foldback, analog current limit (ACL) provide controlled inrush and short-circuit protection. An optional low-side circuit breaker protects the negative output against backfeed faults, and ground faults in nonisolated applications. PD classification via the serial communication classification protocol (SCCP) and maintain full voltage signature (MFVS) ensure that the full operating voltage is only applied to the cable when a PD is present. The SWx pins disconnect port power snubbers during detection and classification. PD initiated sleep and wake-up are supported. The WAKEUP pin supports wake-up forwarding. Telemetry, status, and software control features are accessed via a serial peripheral interface (SPI) bus interface with packet error code (PEC) protection.

The LTC4296-1 provides a versatile SPoE, PSE solution for 10BASE-T1L controllers and switches and can easily be integrated with the Analog Devices, Inc., 10BASE-T1L transceiver portfolio, such as the ADIN1100 (physical layer, PHY), ADIN1110 (MAC-PHY), and ADIN2111 (2-port switch).

TYPICAL APPLICATION

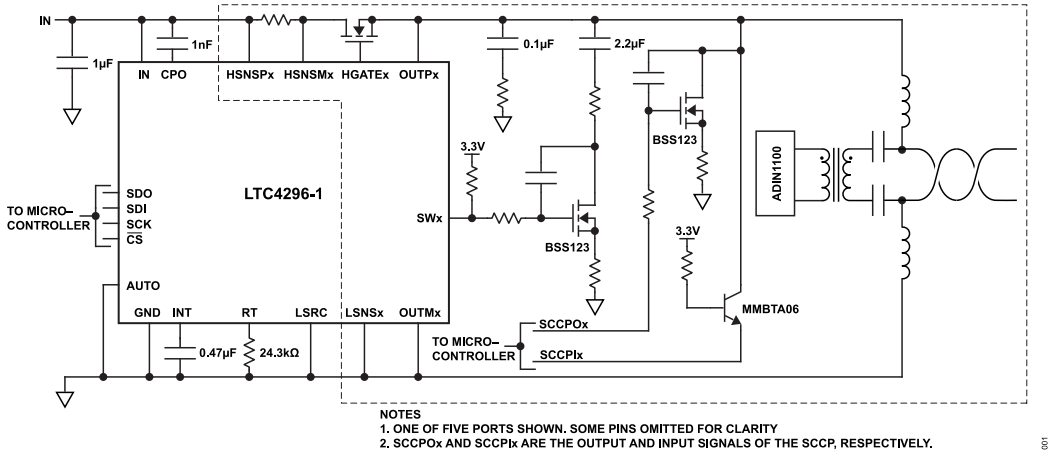

Figure 1. IEEE 802.3cg-Compliant, SPoE PSE

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REVISION HISTORY

1/2023—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

Specifications apply over the full operating temperature range, and the input supply voltage (V_{IN}) = 6 V and 60 V, unless otherwise noted. Pin voltages are referred to as V_{PIN}, and pin currents are referred to as I_{PIN}, where PIN is the name of pin. All currents into the device pins are positive, and all currents out of the device pins are negative. All voltages are referenced to GND, unless otherwise specified.

Table 1. Electrical Characteristics

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IN					
Input Supply Operating Range, V_{IN}		6		60	V
Input Supply Current, I_{IN}	All ports in power-on state		6.5	10	mA
	All ports in sleep state, serial bus idle		52	140	µA
	All ports in disabled state, serial bus idle		51	135	µA
	All ports in detection state		80	90	mA
INT					
INT Voltage, V_{INT}	I_{INT} = 0 µA or −100 µA	4.1	4.3	4.5	V
HSNSPx and HSNSMx					
Analog Foldback Current-Limit Threshold, V_{ILIMx}	$V_{ILIMx} = V_{HSNSPx} - V_{HSNSMx}$, $V_{IN} - V_{OUTPx} < 12$ V, V_{HSNSPx} = 6 V or 60 V	177	186	193	mV
	$V_{IN} - V_{OUTPx}$ = 60 V, V_{HSNSPx} = 60 V	37	41	46	mV
HSNSPx Input Current, I_{IN_HSNSPx}	$V_{IN} = V_{HSNSPx} = V_{HSNSMx}$ = 60 V		95	190	µA
HSNSMx Input Current, I_{IN_HSNSMx}	$V_{IN} = V_{HSNSPx} = V_{HSNSMx}$ = 60 V		66	128	µA
LSNS0					
Port 0 Forward Circuit Breaker Threshold, $\Delta V_{LSNS0(FCB)}$	$\Delta V_{LSNS0(FCB)} = V_{OUTM0} - V_{LSNS0}$	60	76	90	mV
Port 0 Reverse Circuit Breaker Threshold, $\Delta V_{LSNS0(RCB)}$	$\Delta V_{LSNS0(RCB)} = V_{LSNS0} - V_{OUTM0}$	60	76	90	mV
Deep Sleep Return Path Reverse Fault Threshold, $V_{SLP(RCB)}$	All ports in sleep and disabled state, serial bus idle, $V_{SLP(RCB)} = V_{LSNS0}$	–1.2	–0.87	–0.25	V
Deep Sleep Return Path Forward Fault Threshold, $I_{SLP(FCB)}$	All ports in sleep and disabled state, serial bus idle	15	34	45	mA
Deep Sleep Return Path Short Circuit Current, I_{SLP_LSNS0}	All ports in sleep and disabled state, serial bus idle, V_{LSNS0} = 2.5 V	40	79	110	mA
Deep Sleep Return Path Impedance, R_{SLP_LSNS0}	All ports in sleep and disabled state, serial bus idle, I_{LSNS0} = 10 mA	17	22	45	Ω
LSNS1/SNS2 and LSNS3/LSNS4					
Forward Circuit Breaker Threshold, $\Delta V_{LSNSx(FCB)}$	$\Delta V_{LSNSx(FCB)} = V_{OUTMx} - V_{LSNSx}$	60	76	90	mV
Reverse Circuit Breaker Threshold, $\Delta V_{LSNSx(RCB)}$	$\Delta V_{LSNSx(RCB)} = V_{LSNSx} - V_{OUTMx}$	60	76	90	mV
Input Current, I_{LSNSx}	V_{LSNSx} = –0.1 V or +0.1 V, T_A = 25°C		–2.5		µA
HGATEx					
External Port Source Path N-Channel MOSFET Gate Drive, ΔV_{HGATEx}	AUTO high, $\Delta V_{HGATEx} = V_{HGATEx} - V_{OUTPx}$, I_{HGATEx} = 0 µA or –1 µA	9.3	10.2	10.6	V
HGATEx Pull-Up Current, I_{HGATEx_UP}	Power-on state, ΔV_{HGATEx} = 3 V	–45	–34	–28	µA
HGATEx Fast Pull-Down Current, I_{HGATEx_FAST}	Power-on state, $V_{HSNSPx} - V_{HSNSMx}$ = 0.3 V, ΔV_{HGATEx} = 3 V	40	72	150	mA
HGATEx Slow Pull-Down Current, I_{HGATEx_SLOW}	Disabled state, ΔV_{HGATEx} = 1.5 V, V_{OUTPx} = 0 V	8	16	24	mA
	Disabled state, ΔV_{HGATEx} = 1.5 V, V_{OUTPx} = –2 V	40	110	185	µA
HGATEx Fast Pull-Down Dropout Voltage, $V_{PULLDOWN\_FASTx}$	Power-on state, V_{OUTPx} = 0 V, I_{HGATEx} = 1 mA, $V_{HSNSPx} - V_{HSNSMx}$ = 0.3 V		1.1	1.4	V
HGATEx Slow Pull-Down Dropout Voltage, $V_{PULLDOWN\_SLOWx}$	Disabled state, V_{OUTPx} = 0 V, I_{HGATEx} = 10 µA		0.14	0.3	V
HGATEx Inrush Slew Rate, dV_{HGATEx}/dt	Power-on state, $V_{HSNSPx} - V_{HSNSMx} < 30$ mV	14	16.5	19	V/ms
LGATE					
External Return Path N-Channel Gate Drive, ΔV_{LGATE}	Power-on state, 6 V < V_{IN} < 8.6 V, I_{LGATE} = 0 µA or –1 µA	V_{IN} – 0.2		V_{IN}	V
	Power-on state, $V_{IN} \geq 8.6$ V, I_{LGATE} = 0 mA or –1mA	8.25	9.5	9.8	V
LGATE Pull-Up Current, $I_{LGATE(UP)}$	AUTO high, $V_{LGATE} - V_{LSRC}$ = 3 V	–3.3	–2.2	–0.6	mA
LGATE Pull-Down Current, $I_{LGATE(DWN)}$	LGATE disabled, V_{LGATE} = 3 V, V_{LSRC} = 0 V	70	180	270	mA

ELECTRICAL CHARACTERISTICS

Table 1. Electrical Characteristics (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LGATE Pull-Down Voltage, $V_{LGATE(OFF)}$	LGATE disabled, I_{LGATE} = 10 µA, V_{LSRC} = 0 V		0.6	1	V
AUTO					
Input Threshold Voltage, V_{AUTO}	V_{AUTO} rising	1.15	1.205	1.25	V
Input Hysteresis	V_{AUTO} falling, T_A = 25°C		11		mV
Input Current, I_{AUTO}	V_{AUTO} = 5.5 V	–100		+100	nA
Pulse Width of Spike Suppressed, t_{SP_AUTO}	Positive going spike, T_A = 25°C		28		µs
	Negative going spike, T_A = 25°C		7		µs
PORT SOURCE CURRENT READBACK ANALOG-TO-DIGITAL CONVERTER (ADC)					
Resolution[1]	T_A = 25°C		11		Bits
Full-Scale	T_A = 25°C		204.8		mV
Gain Error[2]	$V_{HSNSPx} – V_{HSNSMx}$ < 200 mV			±2.5	%
Offset[2]	Code 2048 center	–250	–50	150	µV
Integral Nonlinearity (INL)[2]				±1	LSB
Conversion Time[3]		3.3	3.6	4	ms
V_{IN}, PORT OUTPUT VOLTAGE, AND PORT RETURN CURRENT READBACK ADC (GLOBAL ADC)					
Resolution[1]	T_A = 25°C		11		Bits
Voltage Readback Full-Scale	$V_{OUTPx} – V_{OUTMx}$, V_{IN}, low gain, T_A = 25°C		72.09		V
	$V_{OUTPx} – V_{OUTMx}$, V_{IN}, high gain, T_A = 25°C		36.04		V
Current Readback Full-Scale	$V_{OUTMx} – V_{LSNSx}$, T_A = 25°C		204.8		mV
Full-Scale Gain Error	T_A = 25°C		±2.5		%
Offset	Code 2048 center, T_A = 25°C		±1		LSB
INL	T_A = 25°C		±1		LSB
Conversion Time[3]		3.3	3.6	4	ms
INTERNAL CHECK VOLTAGE REFERENCE (ACCESSIBLE THROUGH THE GLOBAL ADC)					
Code	T_A = 25°C		3548		LSB
Tolerance				±3.5	%
Conversion Time[3]		3.3	3.6	4	ms
INTERNAL TEMPERATURE SENSOR (ACCESSIBLE THROUGH THE GLOBAL ADC)					
Weight	T_A = 25°C		0.25		°C/LSB
Error	T_A = 25°C		±5		°C
Conversion Time[3]		3.3	3.6	4	ms
SDI, SCK, and $\overline{CS}$					
Digital Input Low Voltage, V_{ILD}				0.8	V
Digital Input High Voltage, V_{IHD}		2			V
Input Current, I_{SPI}	V_{SDI}, V_{SCK}, and $V_{\overline{CS}}$ = 5.5 V	–1		+1	µA
SDO and SWx					
Output Low Voltage, V_{OL}	I_{SDO}, I_{SWx} = 3 mA			0.4	V
Output Leakage Current, I_{LEAK}	V_{PIN} = 5.5 V, where PIN denotes SDO or SWx	–1		+1	µA
THERMAL SHUTDOWN INTERNAL TEMPERATURE	T_A = 25°C				
Junction, $T_{SHUTDOWN}$			175		°C
Junction Hysteresis, $T_{SHUTDOWN(HYST)}$			30		°C
OUTPx and OUTMx					
Open-Circuit Detection Voltage, V_{OC}[2]	Detection state, I_{OUTPx} = 0 µA	5.05	5.2	5.5	V
Invalid PD Signature Voltage High Range, $V_{BAD\_HI\_PSE}$[2]	Detection state, invalid signature high threshold	4.7		5	V
Invalid PD Signature Voltage Low Range, $V_{BAD\_LO\_PSE}$[2]	Detection state, invalid signature low threshold	3.7		4.05	V

ELECTRICAL CHARACTERISTICS

Table 1. Electrical Characteristics (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Sleep State Output Voltage, V_{SLEEP}[2]	Sleep state, I_{OUTPx} = 0 mA, –1.85 mA, or 100 µA	3.15	3.4	3.575	V
Port Disabled Voltage at OUTPx, $V_{DISABLE}$[2]	Port disabled, I_{OUTPx} = 50 µA			1	V
OUTPx Discharge Current During Settle-Sleep State, $I_{DISCHARGE}$[2]	Settle-sleep state, I_{OUTPx}, V_{OUTPx} − V_{OUTMx} = 6 V	1.2	2.1	3.6	mA
Short-Circuit Current, I_{SC}[2]	Sleep state, I_{OUTPx}, V_{OUTPx} − V_{OUTMx} = 0 V	–6.8	–5.5	–4.25	mA
Valid Wake-Up Current Input Range, I_{WAKEUP}[2]	Sleep state, I_{OUTPx}	–1.85		–1.25	mA
Detection Probe Current Range, I_{VALID}[2]	Detection state, V_{OUTPx} − V_{OUTMx} = 0 V	–16	–14	–12	mA
	Detection state, V_{OUTPx} − V_{OUTMx} = 4.7 V	–16	–13	–11	mA
High-Side Power-Good Threshold Voltage, ΔV_{OUTPx_PWRGD}	Port enabled, ΔV_{OUTPx_PWRGD} = V_{OUTPx} − V_{IN}, V_{OUTMx} = 0 V, V_{OUTPx} rising	390	440	510	mV
High-Side Power-Good Threshold Voltage Hysteresis, $\Delta V_{OUTPx\_PWRGD(HYST)}$	Port enabled, V_{OUTPx} falling, T_A = 25°C		22		mV
Low-Side Power-Good Threshold Voltage, ΔV_{OUTMx_PWRGD}	Port enabled, ΔV_{OUTMx_PWRGD} = V_{OUTMx}, ΔV_{OUTPx_PWRGD} = 0 V	150	200	250	mV
WAKEUP					
Internal Pull-Up Current, I_{PU}	V_{WAKEUP} = 1.2 V	–125	–100	–75	µA
Internal Pull-Down Resistance, R_{PD}	V_{WAKEUP} = 5.5 V	0.4	1.2	2.25	MΩ
Internal Pull-Up Voltage, V_{OH}	I_{WAKEUP} = 0 µA or 50 µA	3.25	3.8	4.5	V
Input Threshold Voltage, V_{ITH}	V_{WAKEUP} rising	1.15	1.205	1.25	V
Input Threshold Voltage Hysteresis, $V_{ITH(HYST)}$	V_{WAKEUP} falling, T_A = 25°C		10		mV
Pulse Width of Spike Suppressed, t_{SP_WAKEUP}	Positive going spike, T_A = 25°C		30		µs
	Negative going spike, T_A = 25°C		6		µs
PORT TIMING CHARACTERISTICS					
Detection State Timeout, t_{DET}	Detection state, invalid signature	2.55		3.11	ms
Detection Signature Hold Time, t_{SIG_HOLD}	Detection state, valid signature	1		1.22	ms
Power-Up State Timeout Tolerance, t_{INRUSH_TOL}	Power-up state, short-circuit, programmable			±7	%
Port Source Circuit Breaker Overload Fault Delay Time Tolerance, t_{LIM_TOL}	Programmable, V_{HSNSPx} − V_{HSNSMx} > V_{ILIMx}			±7	%
Port Return Circuit Breaker Delay Time, t_{LSNS_FAULT}	V_{LSNSx} = 1.2 V	1.3	1.8	2.4	µs
	V_{LSNSx} = –0.1 V	2	4	6.3	µs
Overload Delay Tolerance, t_{OD_TOL}	Overload state, programmable			±7	%
Port MFVS Valid Hold Time, t_{MFVS}	V_{HSNSPx} − V_{HSNSMx} > V_{MFVS}, V_{MFVS} programmable	4	5	6	ms
Port MFVS Dropout Time, t_{MFVDO}	V_{HSNSPx} − V_{HSNSMx} < V_{MFVS}	300	350	400	ms
OUTPx Sleep Regulator Overload Fault Delay Time Tolerance, $t_{LIM\_SLEEP\_TOL}$	Idle or sleep states, programmable			±20	%
Restart Delay Tolerance, $t_{RESTART\_TOL}$	Restart state, programmable			±7	%
Wake-Up Deglitch Time, t_{WAKEUP}		0.05		0.1	ms
Turn Off Time, t_{OFF}	Settle-sleep to overload, V_{OUTPx} = 5 V	409		500	ms
SPI BUS TIMING					
SCK Frequency, $1/t_{CLK}$				1	MHz
SDI Setup Time Before SCK Rising Edge, t_1		26			ns
SDI Hold Time After SCK Rising Edge, t_2		25			ns
SCK Low, t_3		200			ns
SCK High, t_4		200			ns
$\overline{CS}$ Rising Edge to $\overline{CS}$ Falling Edge, t_5		650			ns
SCK Rising Edge to $\overline{CS}$ Rising Edge, t_6		800			ns
$\overline{CS}$ Falling Edge to SCK Rising, t_7		1			µs
SCK Falling Edge to SDO Valid, t_8[4]				100	ns
$\overline{CS}$ Rising Edge to SDO Rising, t_9[4]				250	ns

ELECTRICAL CHARACTERISTICS

1 Both port and global ADCs have a bipolar input range that is spanned by 11 bits plus a sign bit.

2 This specification is tested at V_{IN} = 6 V. The operation at V_{IN} = 60 V is guaranteed by design.

3 This specification is guaranteed by design.

4 This specification does not include the rise or fall time of the SDO. While the fall time (typically 5 ns due to the internal pull-down transistor) is not a concern, the rising-edge transition time, t_{RISE}, is dependent on the pull-up resistance and load capacitance on the SDO pin.

TIMING DIAGRAM

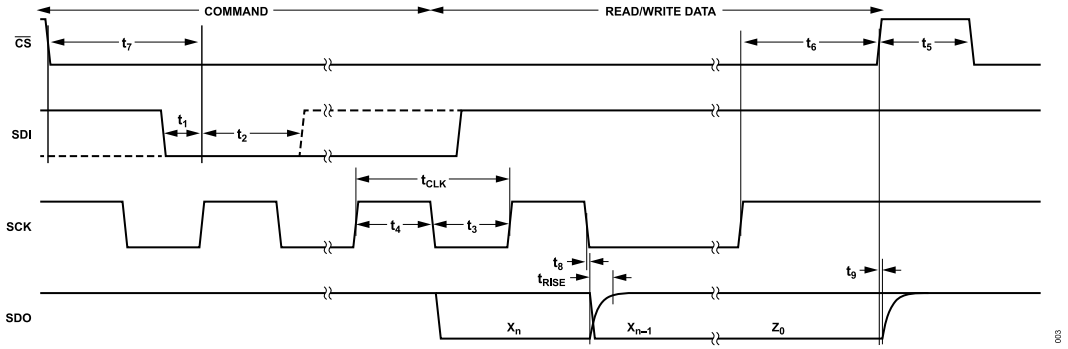

Figure 2. SPI Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature is exceeded when this protection is active. Continuous operation more than the specified absolute maximum operating junction temperature can impair device reliability or permanently damage the device.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
IN	–0.3 V to +80 V
INT	–0.3 V to +6 V
Input Voltages	
SDI, SCK, $\overline{CS}$, AUTO, and RT	–0.3 V to +6 V
HSNSPx and HSNSMx	–0.3 V to +80 V
HSNSPx to HSNSMx	–5 V to +10 V
OUTMx	–5.5 V to +80 V
LSNSx	–5.5 V to +80 V
OUTPx	–5.5 V to +80 V
Output Voltages	
SDO, WAKEUP, and SWx	–0.3 V to +6 V
LGATE to LSRC[1]	–0.3 V to +15 V
LSRC	–5.5 V to +4 V
CPO to IN[1]	–0.3 V to +15 V
HGATEx to OUTPx[1]	–0.3 V to +15 V
Output Currents	
SDO and SWx	±5 mA
RT	–10 mA to +1 mA
Temperature	
Operating Junction Range[2]	–40 to +125°C
Storage Range	–65°C to +150°C
Lead (Soldering, 10 sec)	300°C

[1] Externally forced voltage absolute maximums. The LTC4296-1 can exceed these during normal operation.

[2] The LTC4296-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4296-1 is guaranteed over the –40°C to 125°C operating junction temperature range.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
05-08-7073	18	2.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

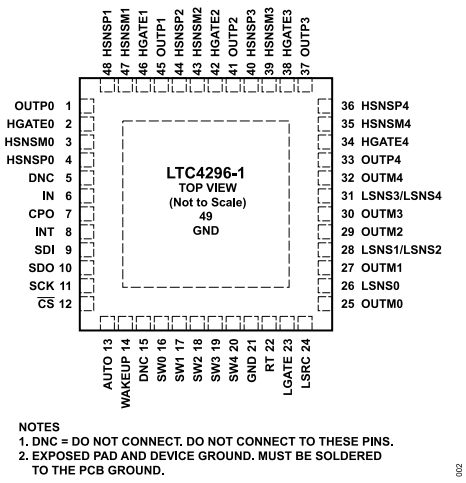

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic[1]	Description
1, 33, 37, 41, 45	OUTPx	Port x Positive Output. Connect the OUTPx pin to the source of the Port x, top-side, external N-channel MOSFET. Do not connect the OUTPx pin if Port x is unused.
2, 34, 38, 42, 46	HGATEx	Port x High-Side Gate Drive. Connect the HGATEx pin to the gate of the Port x, top-side, external N-channel MOSFET. Do not connect the HGATEx pin if Port x is unused.
3, 35, 39, 43, 47	HSNSMx	Port x High-Side Kelvin Sense Negative Input. Connect the HSNSMx pin directly to the negative terminal of the Port x, top-side, current-sense resistor. Connect the sense-resistor negative terminal to the drain of the Port x, top-side, external N-channel MOSFET. If Port x is unused, connect the HSNSMx pin to the HSNSPx pin.
4, 36, 40, 44, 48	HSNSPx	Port x High-Side Kelvin Sense Positive Input. Connect the HSNSPx pins directly to the positive terminal of the Port x, top-side, current-sense resistor. If Port x is unused, connect to IN.
5, 15	DNC	Do Not Connect. Do not connect to these pins.
6	IN	Supply Voltage Input.
7	CPO	Charge-Pump Output. Connect a 1 nF, 16 V capacitor from CPO to IN.
8	INT	Internal 4.3 V Regulator Bypass. Connect a 470 nF bypass capacitor from INT to GND.
9	SDI	SPI Serial Data Input.
10	SDO	SPI Serial Data Open-Drain Output. Connect SDO to logic high through a pull-up resistor.
11	SCK	SPI Serial Clock Input.
12	$\overline{CS}$	SPI Chip Select Input, Active Low.
13	AUTO	Auto Mode Enable for All Ports, Active High. Tie AUTO low to configure the LTC4296-1 in manual mode for performing microcontroller assisted PD classification. Tie AUTO high for applications that support physical detection. See the Autonomous Mode section for additional uses for the AUTO pin.
14	WAKEUP	Bidirectional Wake-Up. During a PD initiated wake-up event on a port, the WAKEUP pin is pulled high to 3.75 V with an internal 100 µA pull-up current. The WAKEUP pin is pulled down to GND by an internal 1.2 MΩ resistor. The WAKEUP pin can also be pulled to logic high externally to wake up one or more ports. Do not connect the WAKEUP Pin if unused.
16 to 20	SWx	Open-Drain Snubber Switch Output for Port x, Active High. SWx drives an external N-channel MOSFET to disconnect the power snubber during classification. See the Classification State section for additional information. Do not connect SWx if unused.
21	GND	Device Ground.
22	RT	Internal Oscillator Frequency Program Pin. Connect a 24.3 kΩ resistor between the RT pin and GND to set the internal oscillator frequency.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

Table 4. Pin Function Descriptions (Continued)

Pin No.	Mnemonic[1]	Description
23	LGATE	Low-Side Gate Drive. If a low-side, external N-channel MOSFET is present, connect LGATE to the MOSFET gate. Do not connect LGATE if a low-side, external MOSFET is not present.
24	LSRC	Low-Side External MOSFET Source Connection. Connect LSRC to GND.
25	OUTM0	Port 0, Negative Output, and Low-Side Kelvin Sense Positive Input. Connect OUTM0 directly to the positive terminal of the Port 0, low-side, current-sense resistor. Connect to LSNS0 if Port 0 is unused.
26	LSNS0	Port 0, Low-Side, Kelvin Sense Negative Input. Connect LSNS0 directly to the negative terminal of the Port 0, low-side, current-sense resistor. If a low-side, external N-channel MOSFET is present, connect LSNS0 to the MOSFET drain. If a low-side external MOSFET is not present, connect LSNS0 to GND.
27	OUTM1	Port 1, Negative Output, and Low-Side Kelvin Sense Positive Input. Connect OUTM1 directly to the positive terminal of the Port 1, low-side, current-sense resistor. Connect to LSNS1/LSNS2 if Port 1 is unused.
28	LSNS1/LSNS2	Port 1 and Port 2, Low-Side, Kelvin Sense Negative Input. Connect LSNS1/LSNS2 directly to the negative terminals of the Port 0 and Port 1, low-side, current-sense resistors. If a low-side, external N-channel MOSFET is present, connect LSNS1/LSNS2 to the MOSFET drain. If a low-side external MOSFET is not present, connect LSNS1/LSNS2 to GND.
29	OUTM2	Port 2, Negative Output, and Low-Side Kelvin Sense Positive Input. Connect OUTM2 directly to the positive terminal of the Port 2, low-side, current-sense resistor. Connect OUTM2 to LSNS1/LSNS2 if Port 2 is unused.
30	OUTM3	Port 3, Negative Output, and Low-Side Kelvin Sense Positive Input. Connect OUTM3 directly to the positive terminal of the Port 3, low-side, current-sense resistor. Connect OUTM3 to LSNS3/LSNS4 if Port 3 is unused.
31	LSNS3/LSNS4	Port 3 and Port 4, Low-Side, Kelvin Sense Negative Input. Connect LSNS3/LSNS4 directly to the negative terminals of the Port 3 and Port 4, low-side current-sense resistors. If a low-side, external N-channel MOSFET is present, connect LSNS3/LSNS4 to the MOSFET drain. If a low-side external MOSFET is not present, connect LSNS3/LSNS4 to GND.
32	OUTM4	Port 4, Negative Output, and Low-Side Kelvin Sense Positive Input. Connect OUTM4 directly to the positive terminal of the Port 4, low-side, current-sense resistor. Connect OUTM4 to LSNS3/LSNS4 if Port 4 is unused.
49	GND	Exposed Pad and Device Ground. Must be soldered to the printed circuit board (PCB) ground.

[1] Where x is to 0 through 4.

TYPICAL PERFORMANCE CHARACTERISTICS

All tests were performed with V_{IN} = V_{HSNSPx} = V_{HSNSMx} = 60 V at room temperature, unless otherwise noted.

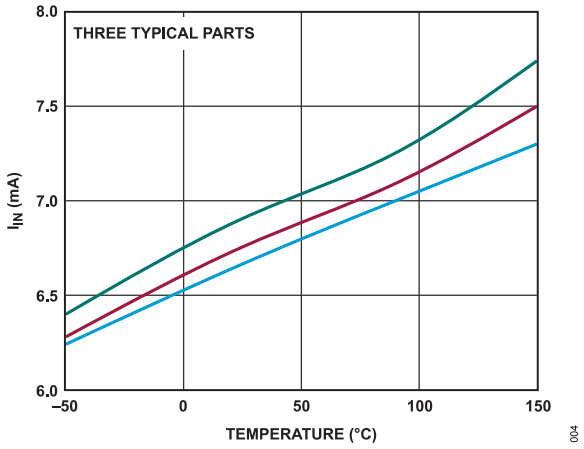

Figure 4. I_{IN} vs. Temperature, All Ports in Power-On State

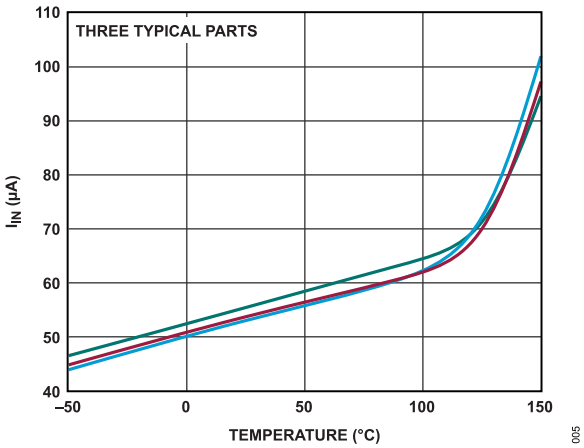

Figure 5. I_{IN} vs. Temperature, All Ports in Sleep State

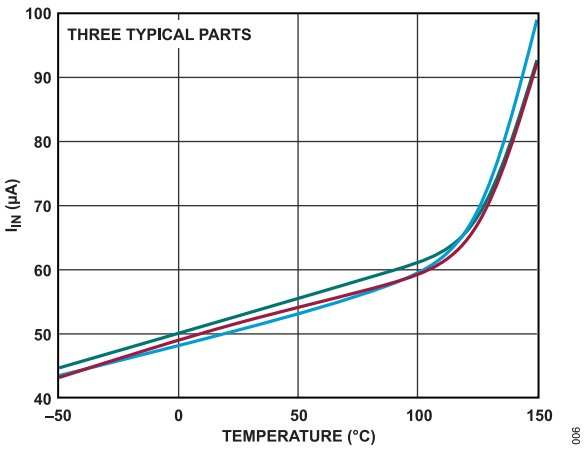

Figure 6. I_{IN} vs. Temperature, All Ports in Disabled State

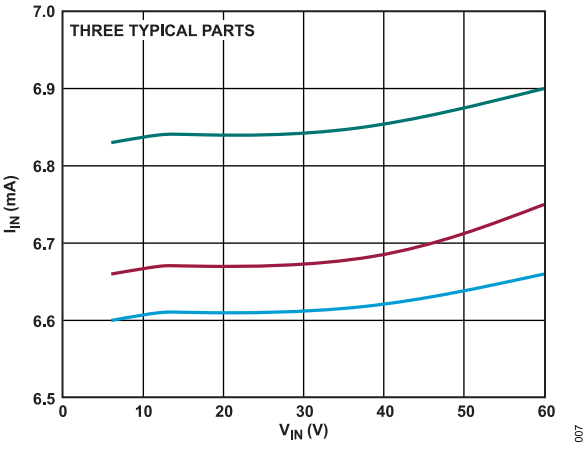

Figure 7. I_{IN} vs. V_{IN}, All Ports in Power-On State

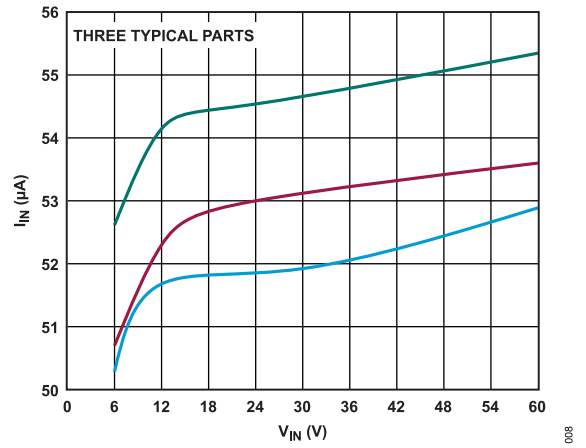

Figure 8. I_{IN} vs. V_{IN}, All Ports in Sleep State

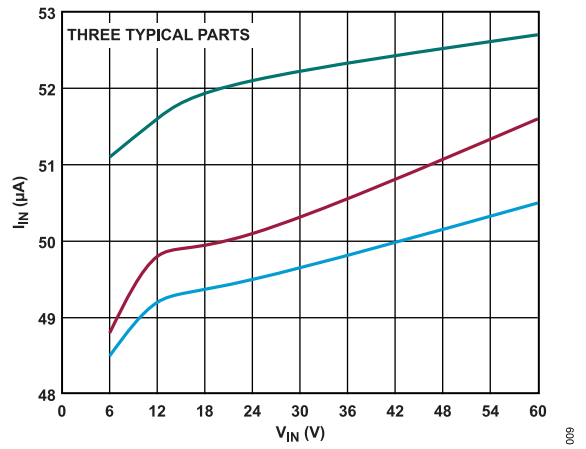

Figure 9. I_{IN} vs. V_{IN}, All Ports in Disabled State

TYPICAL PERFORMANCE CHARACTERISTICS

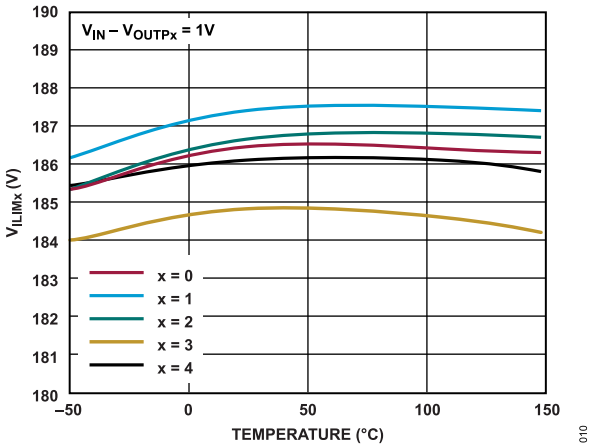

Figure 10. V_{ILIMx} vs. Temperature, $V_{IN} - V_{OUTPx}$ = 1 V

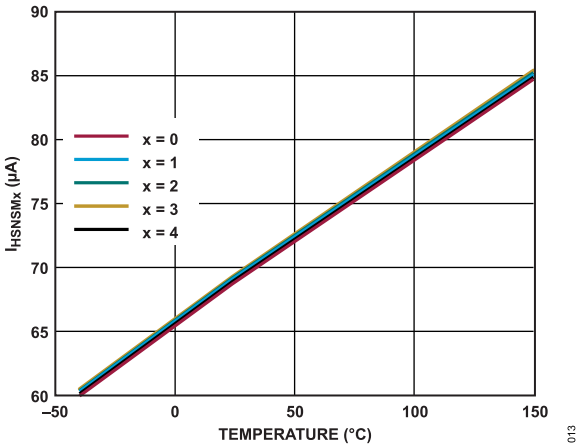

Figure 13. I_{HSNSMx} vs. Temperature, Port in Power-On State

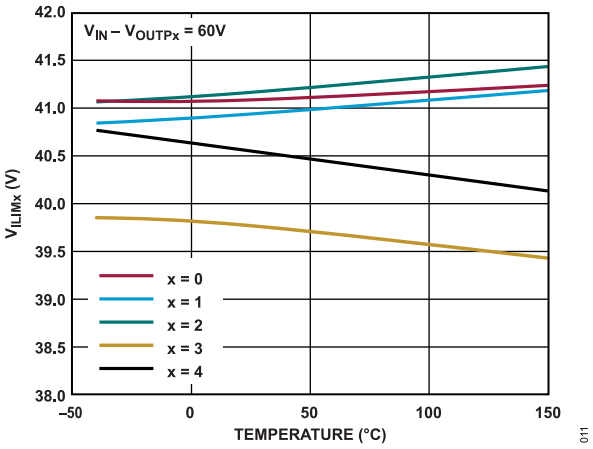

Figure 11. V_{ILIMx} vs. Temperature, $V_{IN} - V_{OUTPx}$ = 60 V

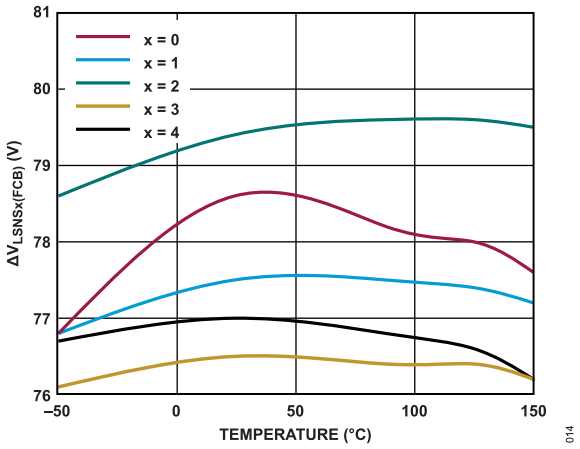

Figure 14. $\Delta V_{LSNSx(FCB)}$ vs. Temperature

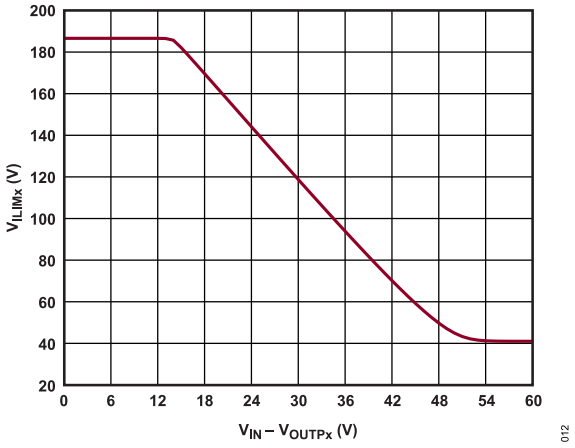

Figure 12. V_{ILIMx} vs. $V_{IN} - V_{OUTPx}$

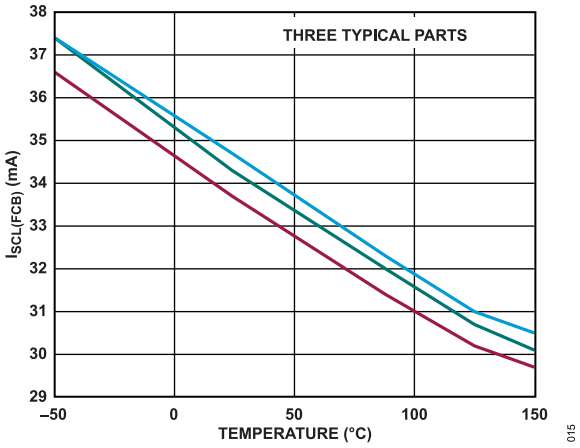

Figure 15. $I_{SLP(FCB)}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

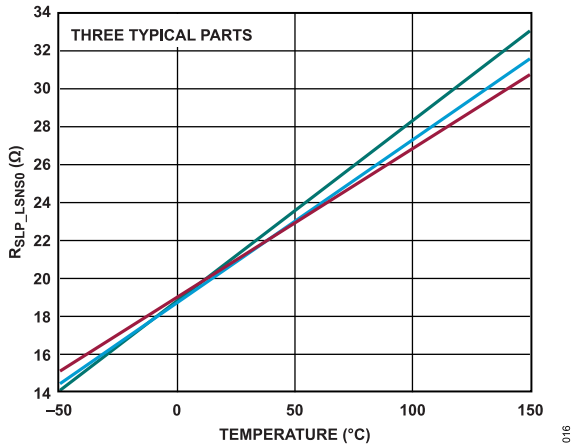

Figure 16. R_{SLP_LSNS0} vs. Temperature

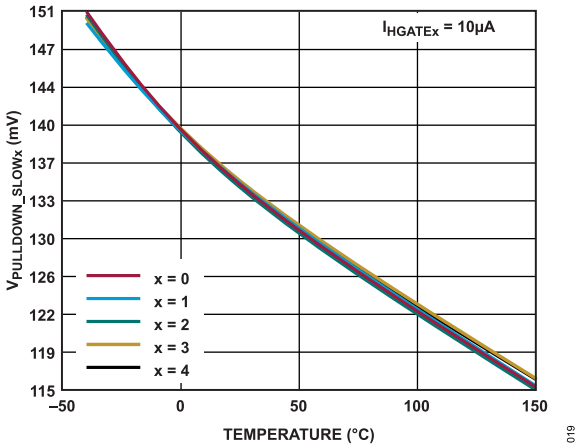

Figure 19. $V_{PULLDOWN\_SLOWx}$ vs. Temperature

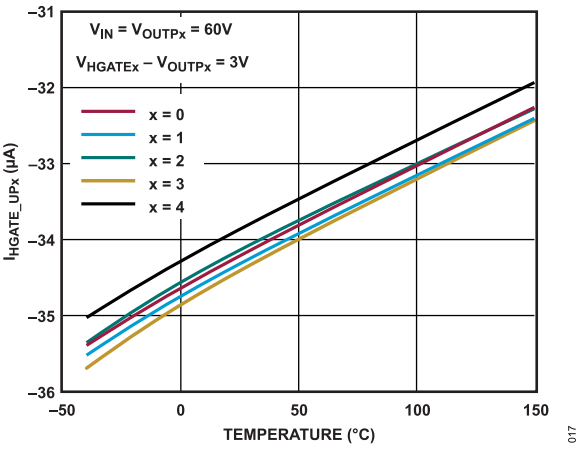

Figure 17. I_{HGATE_UPx} vs. Temperature

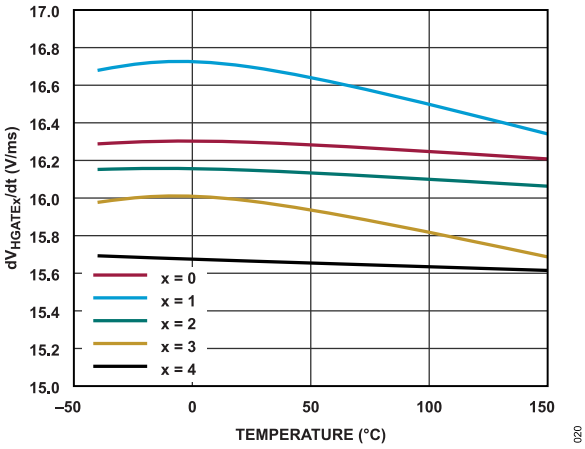

Figure 20. dV_{HGATEx}/dt vs. Temperature

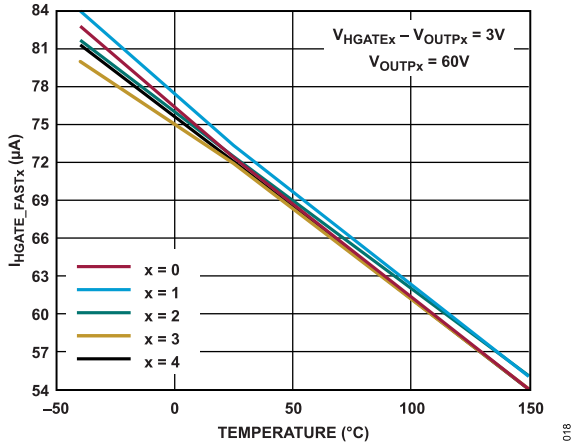

Figure 18. I_{HGATE_FASTx} vs. Temperature

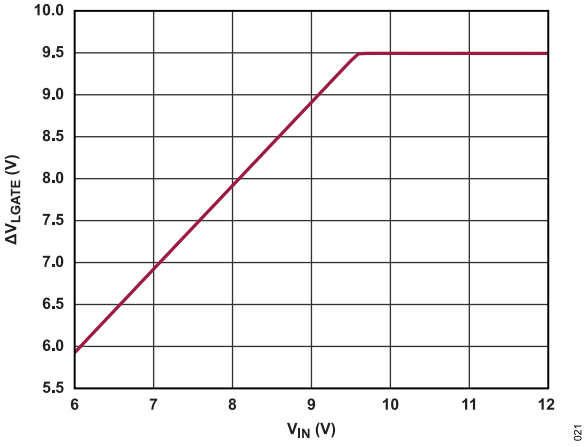

Figure 21. ΔV_{LGATE} vs. V_{IN}

TYPICAL PERFORMANCE CHARACTERISTICS

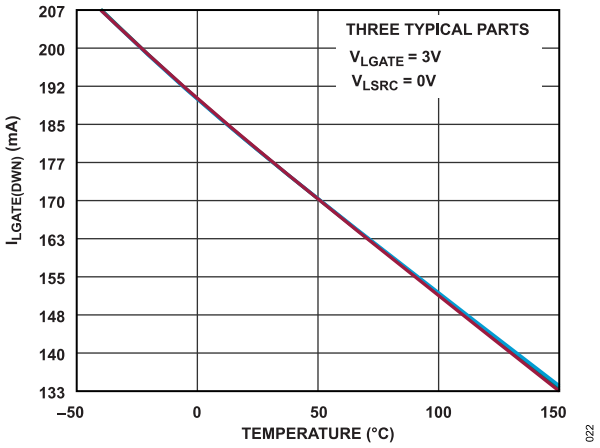

Figure 22. $I_{LGATE(DWN)}$ vs. Temperature, LGATE Disabled

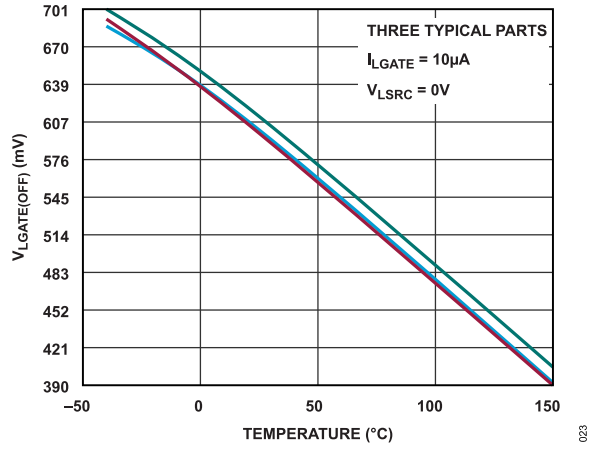

Figure 23. $V_{LGATE(OFF)}$ vs. Temperature

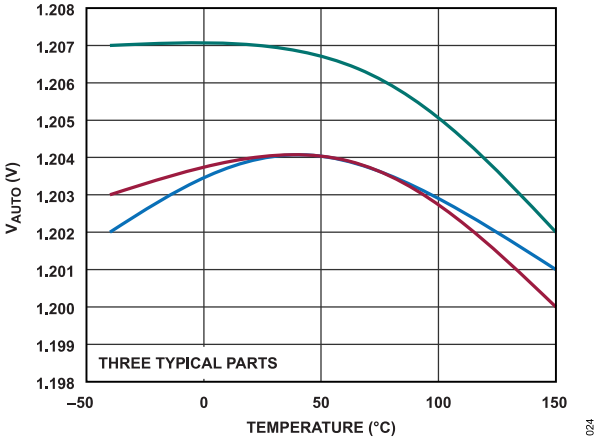

Figure 24. V_{AUTO} vs. Temperature, Rising Edge

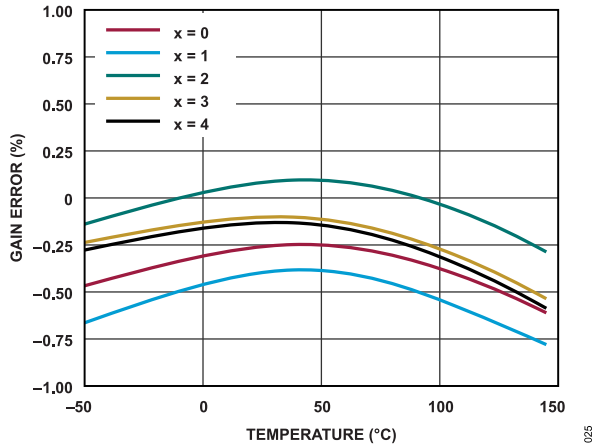

Figure 25. Port Source Current Readback ADC Gain Error vs. Temperature

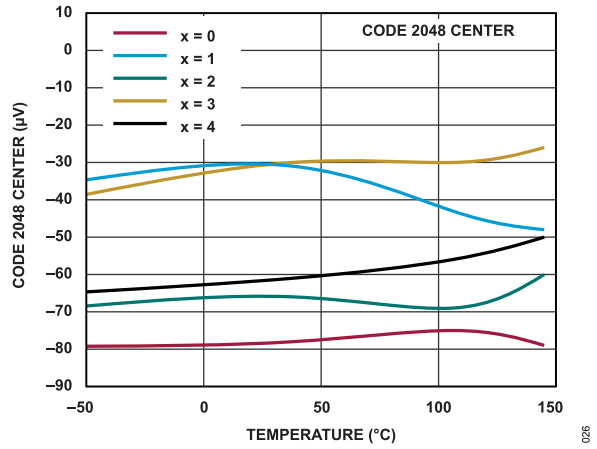

Figure 26. Port Source Current Readback ADC Offset vs. Temperature

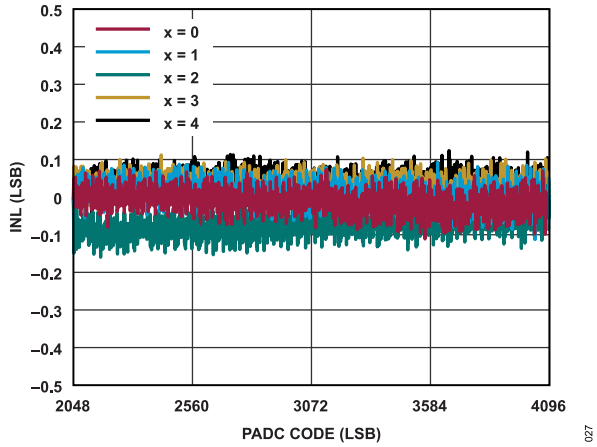

Figure 27. Port Source Current Readback ADC INL

TYPICAL PERFORMANCE CHARACTERISTICS

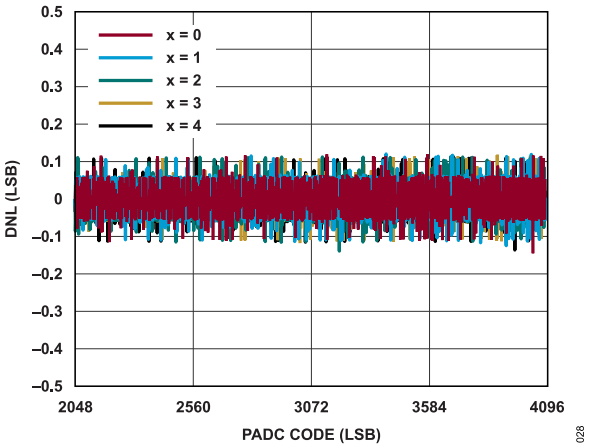

Figure 28. Port Source Current Readback ADC Differential Nonlinearity (DNL)

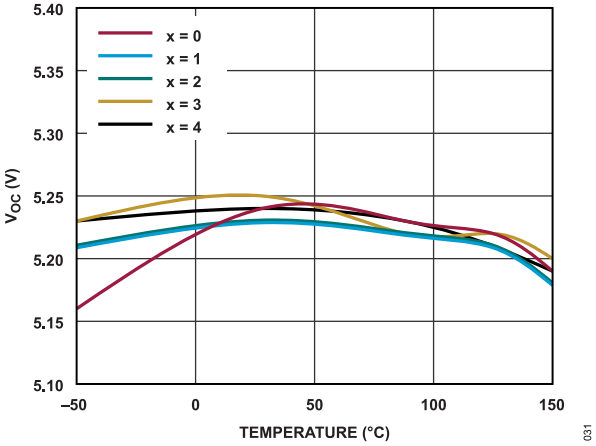

Figure 31. V_{OC} vs. Temperature

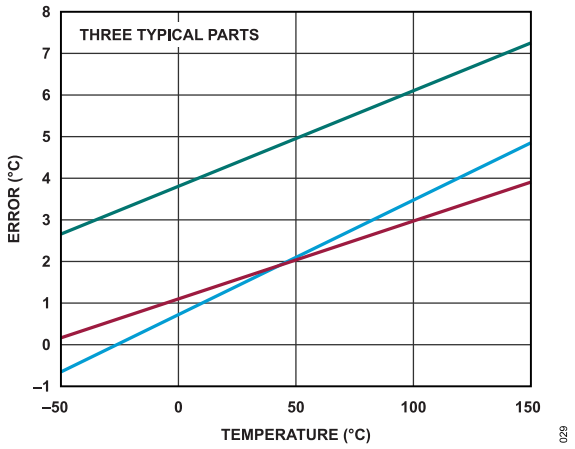

Figure 29. Internal Temperature Sensor Error vs. Temperature

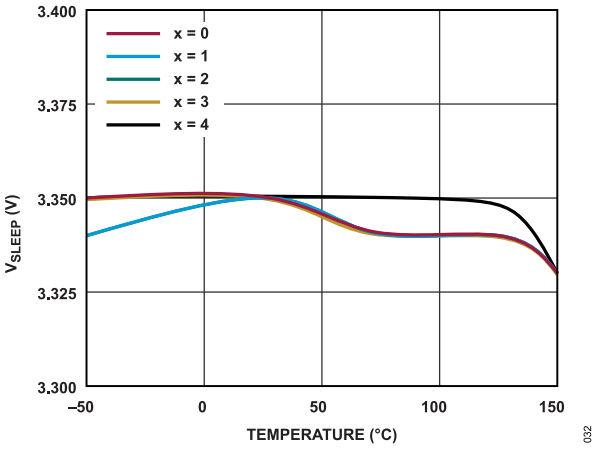

Figure 32. V_{SLEEP} vs. Temperature

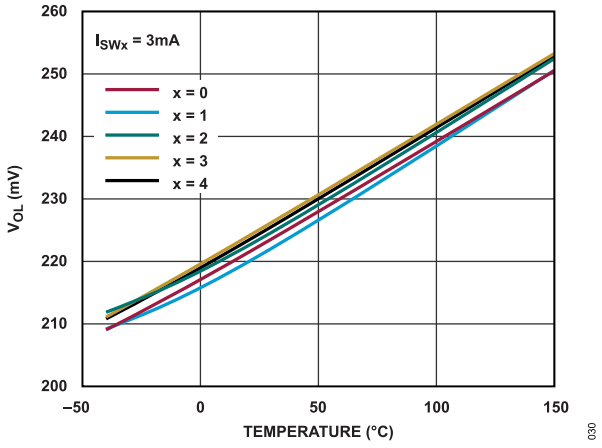

Figure 30. SWx V_{OL} vs. Temperature

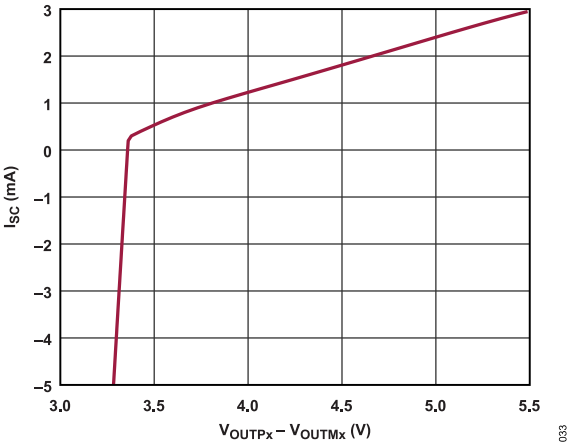

Figure 33. I_{SC} vs. $V_{OUTPx} - V_{OUTMx}$, Sleep State

TYPICAL PERFORMANCE CHARACTERISTICS

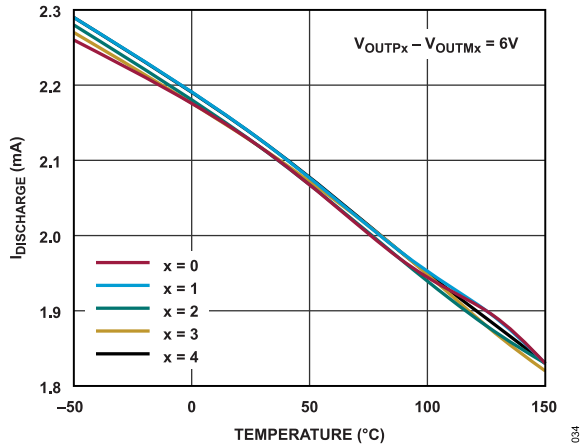

Figure 34. $I_{DISCHARGE}$ vs. Temperature, Settle-Sleep State

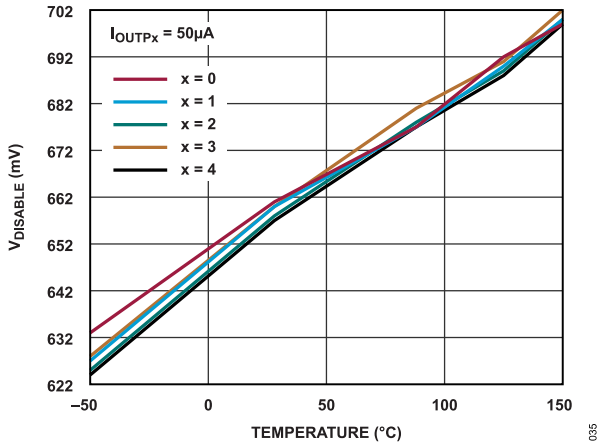

Figure 35. $V_{DISABLE}$ vs. Temperature

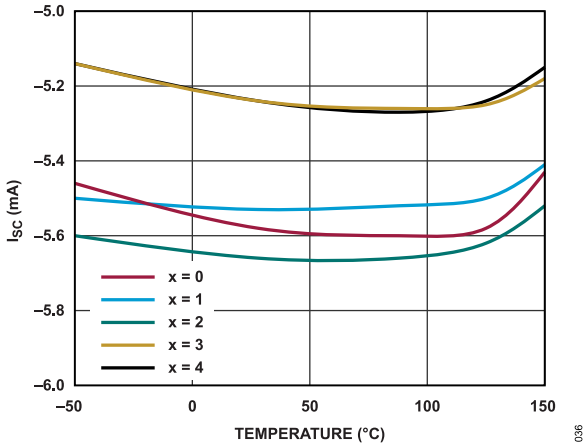

Figure 36. I_{SC} vs. Temperature, Sleep State

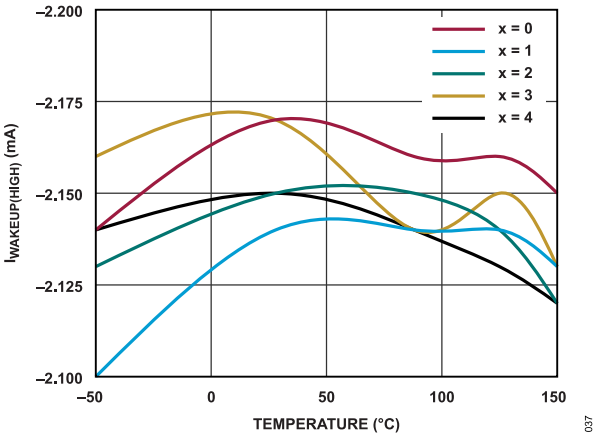

Figure 37. $I_{WAKEUP(HIGH)}$ vs. Temperature

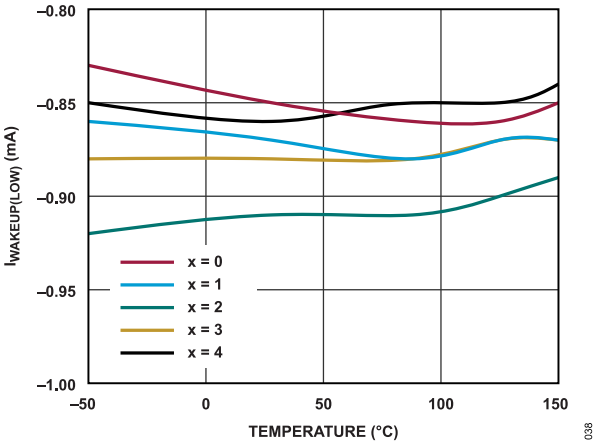

Figure 38. $I_{WAKEUP(LOW)}$ vs. Temperature

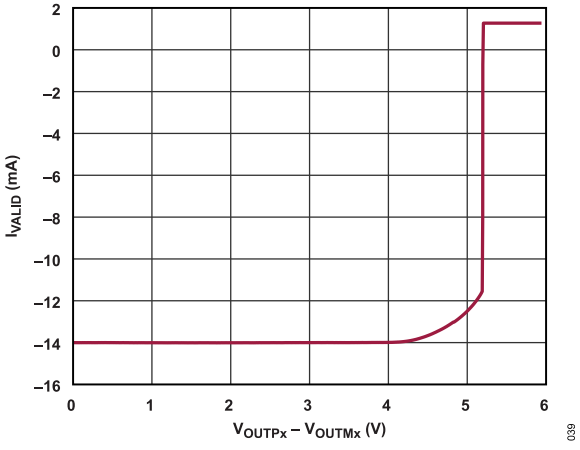

Figure 39. I_{VALID} vs. $V_{OUTPx} - V_{OUTMx}$

TYPICAL PERFORMANCE CHARACTERISTICS

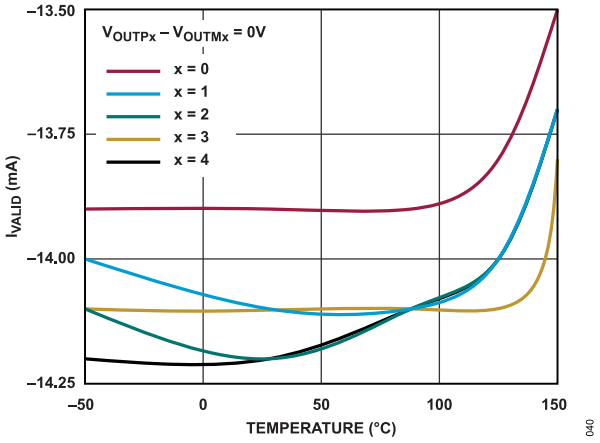

Figure 40. I_{VALID} vs. Temperature, V_{OUTPx} – V_{OUTMx} = 0 V

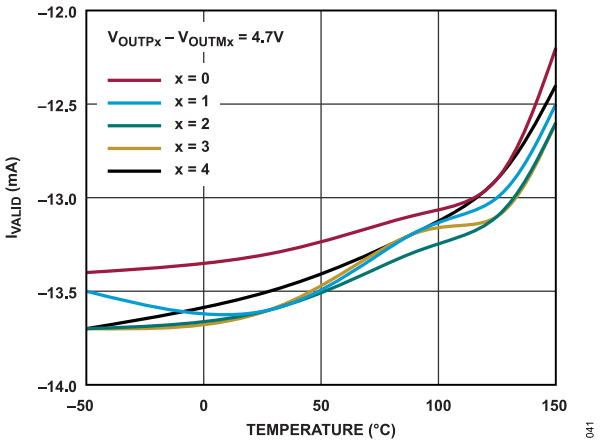

Figure 41. I_{VALID} vs. Temperature, V_{OUTPx} – V_{OUTMx} = 4.7 V

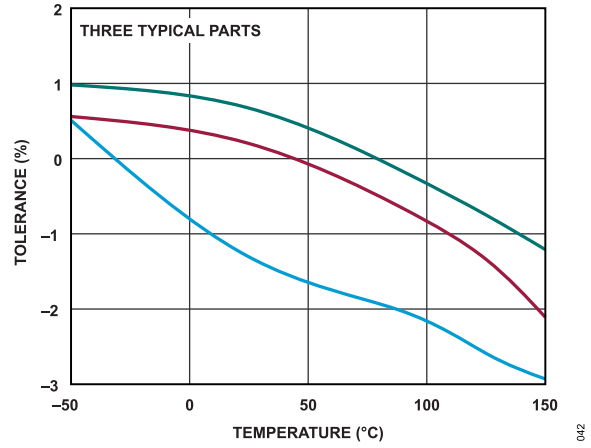

Figure 42. Timer Tolerance vs. Temperature (t_{INRUSH_TOL}, t_{LIM_TOL}, t_{OD_TOL}, and $t_{RESTART\_TOL}$)

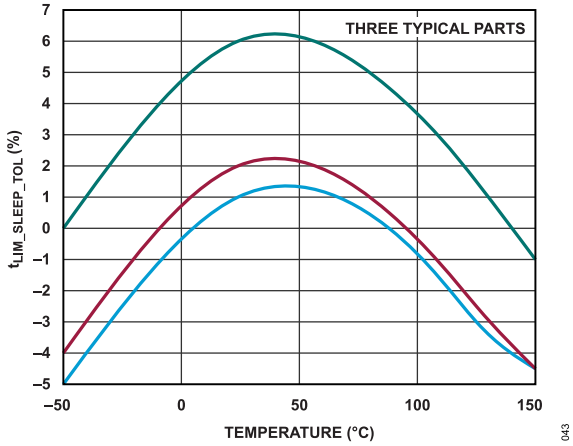

Figure 43. $t_{LIM\_SLEEP\_TOL}$ vs. Temperature

THEORY OF OPERATION

OVERVIEW

The LTC4296-1 is an IEEE 802.3cg-compliant, SPoE, PSE controller that controls and monitors power delivery for up to five PDs. The complementary data protocol for SPoE is 10BASE-T1L.

With a host microcontroller, the LTC4296-1 provides the circuitry required to implement an IEEE 802.3cg-compliant PSE design. Additional required components include a per port external, N-channel MOSFET and a sense resistor to implement high-side electronic circuit breakers with foldback ACL. An optional low-side, N-channel MOSFET, combined with per port, low-side sense resistors can be used to implement a low-side electronic circuit breaker. The LTC4296-1 application circuit provides the fault tolerance mandated by IEEE 802.3cg, increases system reliability, and minimizes power losses compared to designs with on-board MOSFETs.

The source and return circuit breakers offer protection against the following output faults at the connector:

- A short between the two conductors
- A short on one conductor or both conductors to an external positive voltage
- A short on the positive conductor to ground

The host microcontroller is used to configure the LTC4296-1 for PD classification by writing to the configuration registers using the SPI. The host microcontroller can also communicate with the LTC4296-1 via the SPI to read telemetry, such as port status, port voltages, and currents. The data integrity of the SPI is verified with the PEC feature.

SPoE

SPoE is a standard protocol for sending power over 2-wire Ethernet data cables. SPoE is similar in concept to traditional power over Ethernet (PoE) but differs significantly in definition and implementation. The differences stem mainly from the unique power coupling techniques used in a 2-wire circuit, as opposed to 4-wire and 8-wire, pair-oriented powering techniques of PoE. SPoE enables the simultaneous transmission of power and data over a single conductor pair, for example, balanced twisted pair or coaxial cable (Figure 44).

Single pair Ethernet (SPE) data connections consist of a single pair of wires, AC-coupled at each end to avoid ground loops. Unlike PoE systems that transmit power common mode to the data, SPoE systems, diplex power and data over a single pair of conductors.

IEEE 802.3cg (SPoE) is an extension of 802.3bu power over data lines (PoDL). The IEEE Standards Association ratified PoDL in 2016. Multiple complementary data standards are already ratified or in development, ranging from 10 Mbps to 10 Gbps and higher. PoDL defines protocols for detecting, classifying, powering, disconnecting, and standby power operation. IEEE 802.3cg was ratified in 2019 to add features targeting long reach protocols, such as 10BASE-T1L, with cable lengths of up to 1 km.

SPoE was tailored to meet building and factory automation market requirements. SPoE also defines the classification-based power delivery protocol for the PSE and PD. Classification ensures PSE and PD compatibility and avoids applying power into a short-circuit or an open-circuit. The PSE performs detection, followed by classification, of the PD before applying the full operating voltage. During classification, the PSE requests information such as class, type, and cable resistance measurement (CRM) support from the PD.

If the PSE determines that the PD is compatible, it applies the full operating voltage to the PD at the medium dependent interface/power interface (MDI/PI). If CRM is supported, the PSE and PD can negotiate allocation of surplus power to the PD. The PSE can skip classification and power up a PD that provides a valid detection signature. A PD providing an invalid detection signature, however, must undergo classification before being powered. A PD is required to present a valid MFVS to remain fully powered. If the PD is disconnected or goes to sleep, the PSE detects the absence of the MFVS and removes the full operating voltage. The PSE removes the output voltage entirely in the event of a fault or short-circuit.

After removing the full operating voltage in the absence of the MFVS, the PSE enters a low power sleep state and provides V_{SLEEP} (3.4 V typical) at the port.

Wake-up functions from sleep are flexible and can flow either upstream (PD initiated) or downstream (PSE initiated). The PD can request restoration of the full operating voltage by presenting a wake-up current signature to the PSE. The PSE can also initiate a wake-up of the PD by providing the full operating voltage after successful classification.

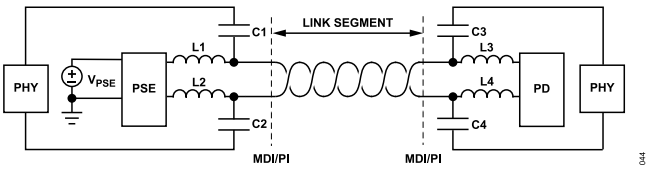

Figure 44. Basic SPoE Architecture

THEORY OF OPERATION

10BASE-T1L Field Switch PSE

The LTC4296-1 provides a solution for 10BASE-T1L field switches that require a PSE at each port.

Classification of the PD connected to each link segment ensures that the overall power provided to the switch is appropriately distributed across the subsystems.

An example of a 10BASE-T1L field switch is shown in Figure 45. The field switch host processor manages the 5× port Ethernet switch (integrated MAC) and the LTC4296-1 over a SPI.

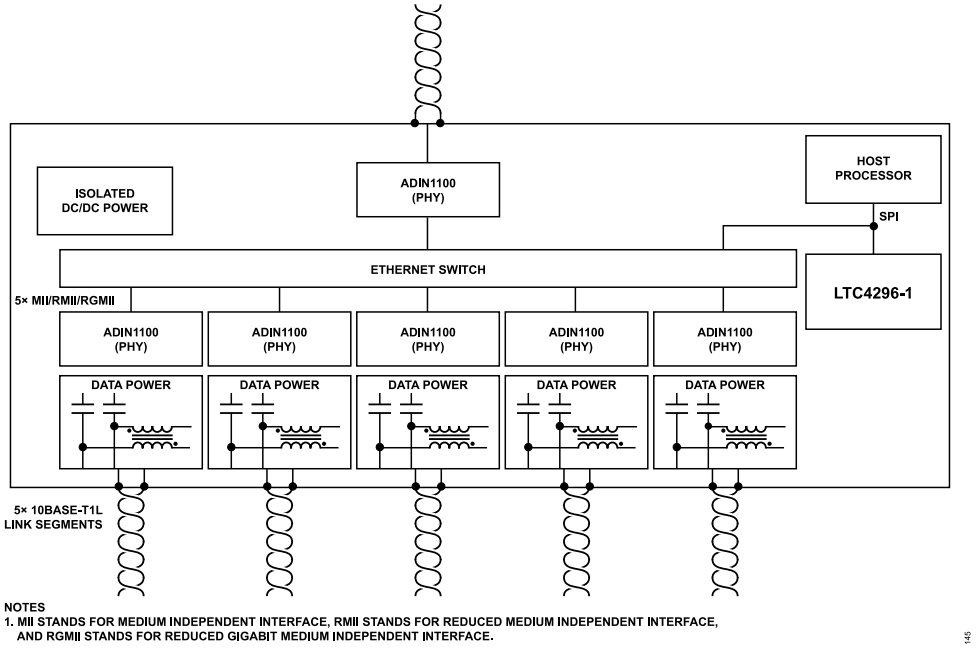

Figure 45. 10BASE-T1L Field Switch PSE

THEORY OF OPERATION

Classification for Discoverable Systems

The SPoE class defines the PSE output voltage range and maximum power sourced or consumed in the system. PoDL comprises Class 0 through Class 15. Class 10 through Class 15 are defined by IEEE 802.3cg for discoverable systems as shown in Table 5 and Table 6. Class 10 through Class 12 provide a 24 V nominal PSE output voltage, as required by many industrial, factory automation, legacy building automation, and wet locations. Each of the three 24 V classes represents a different cabling definition and accompanying maximum power transfer. Class 13 through Class 15 provide a 54 V nominal PSE output voltage, to maximize power transfer without exceeding the safety extra low voltage (SELV). Compatible SPoE, PSE and PD class pairs are shown in Table 7.

PoDL defines the SCCP for classifying a PD. The SCCP uses three basic symbols: initialization, read-slot, and write-slot. Classification is performed in the detection state by the host microcontroller using the SCCP. Refer to the EVAL-SPoE-KIT-AZ Evaluation Kit User Guide (the LTC4296-1 demonstration board) for additional information on how to implement the SCCP with the host microcontroller.

IEEE 802.3cg also supports an optional CRM feature as part of the SCCP. CRM allows a PSE to allocate additional power otherwise allocated for cable loss to a PD when connected through less than the maximum allowed cable resistance.

Table 5. IEEE 802.3cg Class Power Requirements Matrix for PSE and PDs

Class Symbol and Unit	Class Description	Class 10	Class 11	Class 12	Class 13	Class 14	Class 15
V_{PSE} (V)	PSE output voltage	20 to 30			50 to 58		
$I_{PI(MAX)}$ (mA)	Cable current	92	240	632	231	600	1579
$P_{CLASS(MIN)}$ (W)	PSE output power	1.85	4.8	12.63	11.54	30	79
$V_{PD(MIN)}$ (V)	PD input voltage	14			35		
$P_{PD(MAX)}$ (W)	PD power	1.23	3.2	8.4	7.7	20	52
$R_{LINK\_SEG\_LOOP}$ (Ω)	Cable resistance	65	25	9.5	65	25	9.5

Table 6. IEEE 802.3cg Class Power Requirements Matrix Example Link Segment Maximum Distances

	Maximum Lengths (m)					
Example Cable	Class 10	Class 11	Class 12	Class 13	Class 14	Class 15
14AWG, 14 Gauge Cable	1000[1]	1000	400	1000[1]	1000	400
18AWG, 18 Gauge Cable	1000	400	158	1000	400	158
24AWG, 24 Gauge Cable	300	100	40	300	100	40

[1] IEEE 802.3cg limits cable length to 1000 m.

Table 7. PSE and PD Class Compatibility Matrix

	PSE Class					
PD Class	10	11	12	13	14	15
10	Yes	Yes	Yes	No	No	No
11	No	Yes	Yes	No	No	No
12	No	No	Yes	No	No	No
13	No	No	No	Yes	Yes	Yes
14	No	No	No	No	Yes	Yes
15	No	No	No	No	No	Yes

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USAGE CASES

802.3cg-Compliant PSE

The primary usage case for the LTC4296-1 is an 802.3cg-compliant PSE. With this case, the LTC4296-1 AUTO pin is pulled low and a host operates the LTC4296-1 ports semimanually through the states shown in Figure 46. In each state, the LTC4296-1 controls the port output voltage accordingly.

From a system power-up or device reset, the LTC4296-1 starts in the disabled state. An LTC4296-1 port is enabled by the host and moves on to the idle state. The LTC4296-1 then awaits a command from the host to move on to the next state.

When ready, the host configures the LTC4296-1 port to enter the detection state. Note that the LTC4296-1 checks the port current status before moving on to detection.

When the port is in the detection state, the host sets the LTC4296-1 to the classification state and performs the SCCP with a valid PD. Once the host microcontroller determines that the class of the PD is compatible, it can then command the port to enter the power-up state.

During the power-up state, the LTC4296-1 controls inrush and monitors the port output voltage to determine when inrush is complete.

After a successful power-up, the port enters the power-on state and remains there until the LTC4296-1 detects a current overload fault or an MFVS timeout, or the device is instructed by the host to exit power-on when power is no longer available.

If the LTC4296-1 removes power to the port due to an invalid MFVS, it monitors the port voltage discharge in the settle-sleep state.

The LTC4296-1 enters the low power, sleep state after a successful port discharge. In this state, the LTC4296-1 waits for the user, host, or PD to initiate a wake-up before returning to the detection state.

While in the idle, power-on, settle-sleep, or sleep states, the LTC4296-1 monitors the port for current overload fault conditions. If a fault occurs, the LTC4296-1 turns off the port and waits a set time in the overload state before entering the idle state.

A port that fails to exit either the detection or power-up states successfully before the maximum allotted time enters the restart state. The port then waits a set time before re-entering the idle state.

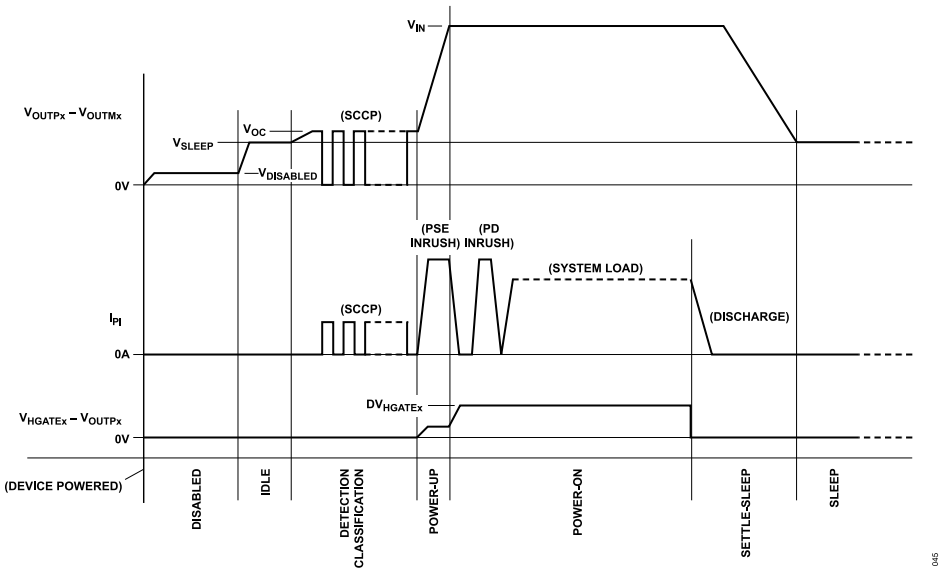

Figure 46. Simplified 802.3cg-Compliant PSE State Sequence (Not to Scale)

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Autonomous Mode

For applications that do not require classification, the LTC4296-1 can operate in an autonomous mode without a host controller when the AUTO pin is pulled high. In autonomous mode, the LTC4296-1 powers up any port when a PD presents a valid detection signature. This mode is ideal for applications that only require a basic detection. Power-up can be forced, regardless of the detection signature, by setting the signature override good bit (Register PxCFG1, Bit 0, SIG_OVERRIDE_GOOD).

PORT STATE DESCRIPTIONS

Overview

Every port in the LTC4296-1 implements the PSE state described in the usage cases (see the 802.3cg-Compliant PSE section and the Autonomous Mode section). A detailed description of each state is provided in the subsequent sections.

Disabled State

A port starts in the disabled state after a power-on or software reset event. In this state, the high-side MOSFET is turned off, and the port voltage is discharged to less than $V_{DISABLED}$ with an internal pull-down. The port remains in this state until it is enabled by the software enable bit (Register PxCFG0, Bit 0, SW_EN) or if the AUTO pin is high and not masked (Register PxCFG0, Bit 1, HW_EN_MASK). Once enabled, the port enters the idle state.

Idle State

In the Idle state, the port output is biased by the LTC4296-1 to V_{SLEEP}. If the output voltage is in the V_{SLEEP} range, the output current is less than the I_{WAKEUP} maximum, and the AUTO pin is high or the software PSE ready is asserted (Register PxCFG0, Bit 6, SW_PSE_READY), the port proceeds to the detection state. If the port current exceeds I_{WAKEUP} for t_{LIM_SLEEP}, the port enters the overload state.

Detection State

PD detection is performed in the detection state. During detection, a probing current, I_{VALID}, is sourced and the port searches for a PD. A PD not requiring classification presents a valid detection signature voltage in the range of 4.05 V to 4.55 V when the PSE sources I_{VALID}. Figure 47 shows a typical valid PD detection sequence.

The PSE must accept a PD detection signature as valid when a valid detection signature voltage is present for at least t_{SIG_HOLD} and must reject voltages less than $V_{BAD\_LO\_PSE}$ (3.7 V) or greater than $V_{BAD\_HI\_PSE}$ (5 V), dark shaded regions in Figure 48. The PSE can accept or reject voltages in the undefined ranges between the must-reject and must-accept limits (light shaded regions).

A port exits the detection state after t_{DET} unless the detection timer is disabled (PxCFG0, Bit 11, TDET_DISABLE). If the t_{DET} timer expires without detecting a valid PD signature, the port enters the restart state and then returns to the idle state.

For use cases not requiring classification, the following conditions must be met to proceed to the power-up state:

- A valid detection signature is found (or Register PxCFG1, Bit 0, SIG_OVERRIDE_GOOD, is set).
- The global software power-good bit is set (Register GCFG, Bit 0, SW_VIN_PGOOD).
- The port software power available bit is set (Register PxCFG0, Bit 5, SW_POWER_AVAILABLE). If the port software power available bit is not set, the port goes to the restart state after exiting the detection state.

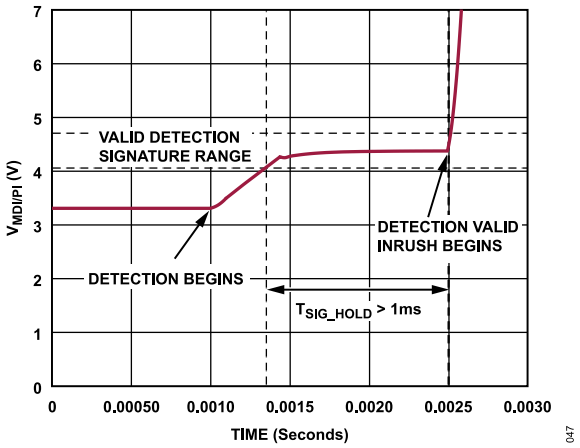

Figure 47. Typical Valid Detection Sequence Waveform

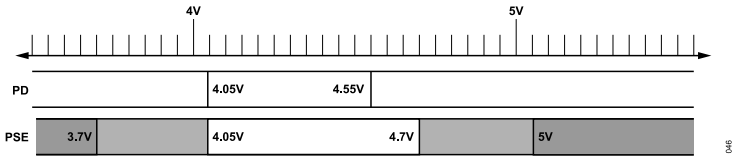

Figure 48. IEEE 802.3bu Signature Voltage Range

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Classification State

Classification is performed in the detection state by the host microcontroller using the SCCP. Refer to the EVAL-SPoE-KIT-AZ Evaluation Kit User Guide (the LTC4296-1 demonstration board) for additional information on how to implement the SCCP with the host microcontroller.

Classification is configured by setting the software PSE ready bit (PxCFG0, Bit6, SW_PSE_READY) and setting the classification mode bit (PXCFG0, Bit 13, SET_CLASSIFICATION_MODE) before entering the detection state. When the classification mode bit is asserted while in the detection state, the port SWx pin pulls low to disable the external, snubber switch MOSFET (M2) of the port.

If the microcontroller determines that a valid PD with a compatible class is present, the port can proceed to the power-up state by setting the port software power available bit (Register PxCFG0, Bit 5, SW_POWER_AVAILABLE) and the end classification bit (Register PxCFG0, Bit 14, END_CLASSIFICATION).

If a PD with a valid signature or a PD with a compatible class is not present, the port can be returned to the idle state via the restart state by clearing the port software power available bit and setting Register PxCFG0, Bit 14, END_CLASSIFICATION.

Power-Up State

In the power-up state, the port ramps up the HGATEx voltage in a controlled manner to limit inrush current. Under normal power-up circumstances, the HGATEx voltage increases until the port reaches V_{ILIMx}, or until the maximum HGATEx inrush slew rate, dV_{HGATEx}/dt, is reached. The inrush time (t_{INRUSH}) timer is initiated upon entry of the power-up state.

When the port output voltage has ramped up, the port current decreases, and the HGATEx pin voltage continues rising to fully enhance the external MOSFET. The final gate-to-source voltage for the MOSFET is ΔV_{HGATEx}. Power-up is complete when the voltage between the IN pin and the port OUTPx pin drops to less than the high-side, power-good threshold voltage, ΔV_{OUTPx_PWRGD}.

If inrush is not complete within t_{INRUSH}, the port enters the restart state, and the t_{INRUSH} timer done bit of the port is set (Register PxEV, Bit 3, TINRUSH_TIMER_DONE). The t_{INRUSH} timer limit is programmable (PxCFG1, Bits[3:2], TINRUSH_TIMER). If the inrush completes within t_{INRUSH}, the port proceeds to the power-on state.

Power-On State

During operation in the power-on state, the high-side output current is continuously monitored and limited by the port current sense ADC and an electronic circuit breaker with foldback ACL, respectively. If the PD does not present a valid MFVS for more than t_{MFVDO}, the port goes to the settle-sleep state and starts discharging the port output voltage to the V_{SLEEP} range. If the host decides power is not available, it can deassert the port software power available bit (Register PxCFG0, Bit 5, SW_POWER_AVAILABLE), and the port goes into the restart state.

Settle-Sleep State

In the settle-sleep state, the port output is discharged to V_{SLEEP} by the pull-down current $I_{DISCHARGE}$. If the output voltage discharges to V_{SLEEP} within t_{OFF}, the port goes to the sleep state. A port enters the overload state from the settle-sleep state if it is unable to discharge the port output to V_{SLEEP} within t_{OFF}.

Sleep State

In the sleep state, the port output is maintained at V_{SLEEP} and monitored for a wake-up signature current, I_{WAKEUP}, from the PD. The PSE enters the detection state after a valid wake-up signature is detected for at least t_{WAKEUP}. A wake-up event can also be initiated by the PSE application host microcontroller via the SPI or the WAKEUP pin.

In the sleep state, an internal low dropout (LDO) regulator continues to bias the port output voltage to V_{SLEEP}. A PD in the sleep state consumes less than 100 µA. A PD can request the PSE to reapply the full operating voltage by presenting the wake-up signature current (I_{WAKEUP_PD}) from 1.3 mA to 1.8 mA for at least the WAKEUP_PD time (t_{WAKEUP_PD}) of 0.2 ms minimum. If the PSE output current is in the range of I_{WAKEUP} for at least t_{WAKEUP}, the PSE is required to wake up and go to the detection state. A PSE may or may not wake up in response to currents in the 0.5 mA to 1.25 mA range or the 1.85 mA to 2.5 mA range. A PSE does not wake up in response to currents less than 0.5 mA or greater than 2.5 mA (see Figure 49). A port can force a valid PD wake-up signature condition by setting the prebias override good bit (Register PxCFG1, Bit 8, PREBIAS_OVERRIDE_GOOD).

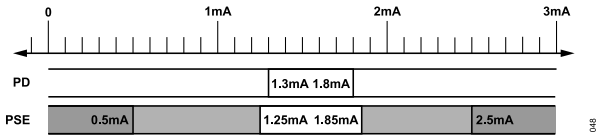

Figure 49. IEEE 802.3bu Wake-Up Current Ranges

A port can disable the PD initiated wake-up by setting the upstream wake-up disable bit in the Port Configuration 0 register (Register PxCFG0, Bit 4, UPSTREAM_WAKEUP_DISABLE).

A port can also be forced to exit the sleep state by setting the software wake-up bit (Register PxCFG0, Bit 2, SW_PSE_WAKEUP). Alternatively, if the downstream wake-up disable bit (Register PxCFG0, Bit 3, DOWNSTREAM_WAKEUP_DISABLE) is not set, the port can be forced to exit the sleep state by raising the WAKEUP pin.

Restart State

In the restart state, the port output is biased to V_{SLEEP}. A port waits for at least the restart time ($t_{RESTART}$) before reentering the

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idle state. The $t_{RESTART}$ timer limits are programmable (Register PxCFG1, Bits[5:4], TOD_TRESTART_TIMER).

Overload State

A current overload fault can occur during any state except the disabled state or detection state. This fault causes the port to enter the overload state.

In the overload state, the port high-side MOSFET is turned off, and the port output voltage is discharged to the $V_{DISABLE}$ range. The port waits the overload delay time (t_{OD}) before going to the idle state. The t_{OD} timer limits are programmable (PxCFG1, Bits[5:4], TOD_TRESTART_TIMER).

Maintain Full Voltage Signature (MFVS)

MFVS detection guarantees that the full operating voltage is applied only when a PD is connected and requires full power. A PD must draw more than 11 mA to ensure it continues to receive the full operating voltage. In the power-on state, a port must consider the MFVS present when the port current exceeds the maximum hold current ($I_{HOLD(MAX)}$) of 10 mA for at least t_{MFVS}. The port MFVS is absent when the port current drops to less than the minimum hold current ($I_{HOLD(MIN)}$) of 2.5 mA for at least t_{MFVDO}. A port can consider the MFVS present or absent when the port current is in the I_{HOLD} range (Figure 50). If the MFVS is absent, the port enters the settle-sleep state and discharges the port output voltage to the V_{SLEEP} range.

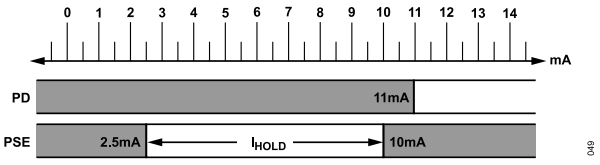

Figure 50. IEEE 802.3bu MFVS Current Ranges

The LTC4296-1 offers a number of advanced power management features. The WAKEUP pin can be used as a hardware interrupt to indicate a PD initiated wake-up or to forward a wake-up request, both of which can be disabled through the SPI. The LTC4296-1 also has a low current deep sleep mode that is useful in battery-powered applications when all the ports are either in the disabled or sleep state.

A port can be forced to stay in the power-on state if the MFVS is absent by disabling the t_{MFVDO} timer (Register PxCFG0, Bit 7, TMFVDO_TIMER_DISABLE).

The MFVS threshold of a port is programmable (Register PxADCCFG, Bits[7:0], MFVS_THRESHOLD). The following equation gives the optimum code as a function of the high-side sense resistor, R1, and the value is rounded to the nearest integer:

$$MFVS\ Threshold\ Code = 62.5 \times R1 \quad (1)$$

HOST SERIAL INTERFACE

The LTC4296-1 communicates with the system host using the SPI. The $\overline{CS}$ input allows the host to select the end device at a time for serial communication when multiple end devices share a common SPI bus.

SPI Clock Phase and Polarity

The LTC4296-1 operates in SPI Mode 3 (SCK polarity (CPOL) = 1, clock phrase (CPHA) = 0, and idle CLK = 1). Consequently, data on the SDI must be stable during the rising edge of SCK as shown in Figure 51 and Figure 52 (write and read, respectively).

Data Transfers

Every command (read or write) is 1 byte long consisting of 7 bits of address and 1 read and/or write bit. Every register value is 2 bytes long. The command and data are transferred with the MSB first.

On a write, the data value on the SDI is latched into the device on the rising edge of the SCK (Figure 51). Similarly, on a read, the data value output on the SDO is valid during the rising edge of the SCK and transitions on the falling edge of the SCK (Figure 52). $\overline{CS}$ must remain low for the entire duration of a command sequence, including between a command byte and subsequent data.

PEC Byte

The PEC byte is a cyclic redundancy check (CRC) value calculated for all the bits in a register group in the order the bits are passed, using the initial PEC value of 0x41, and this characteristic polynomial, $x^8 + x^2 + x + 1$.

To calculate the 8-bit PEC value, take the following steps:

1. Initialize the PEC to 0x41.
2. For each data bit (DIN) coming into the register group, set IN0 = DIN XOR PEC, Bit 7, and then IN1 = PEC0 XOR IN0, and IN2 = PEC1 XOR IN0.
3. Update the 8-bit PEC as PEC7 = PEC6, PEC6 = PEC5 … PEC3 = PEC2, PEC2 = IN2, PEC1 = IN1, and PEC0 = IN0.
4. Go back to Step 2 until all data is shifted. The 8-bit result is the final PEC byte.

For a given SPI transaction, the PEC byte is calculated over the entire command byte, which includes the address and a read and/or write bit, using the previous steps. The PEC byte is then reinitialized to 0x41 for subsequent data-word reads or writes. The PEC byte is calculated for each data-word separately.

The LTC4296-1 calculates a PEC byte for any command or data received and compares it with the PEC byte received following the command or data. The command or data is regarded as valid only if the PEC bytes match. For a SPI read operation, the LTC4296-1 attaches the calculated PEC byte at the end of the data it shifts out on the SDO pin.

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Serial data transactions with an invalid command byte sequence or PEC byte result in the command fault bit (Register GFLTEV, Bit 3, COMMAND_FAULT) or the PEC fault bit (Register GFLTEV, Bit 2, PEC_FAULT), respectively, being set in the global fault event register. The global command register can also be used to protect the registers from unintended writes by writing a code to disable the write access to the register map. To enable write access after a reset event, the host must first unlock the LTC4296-1 by writing the unlock key to the global command register (Register GCMD, Bits[7:0], WRITE_PROTECT). See the register descriptions found in Table 8 through Table 13.

Sample Code provides a pseudo code implementation of the SPI write and read operations with PEC.

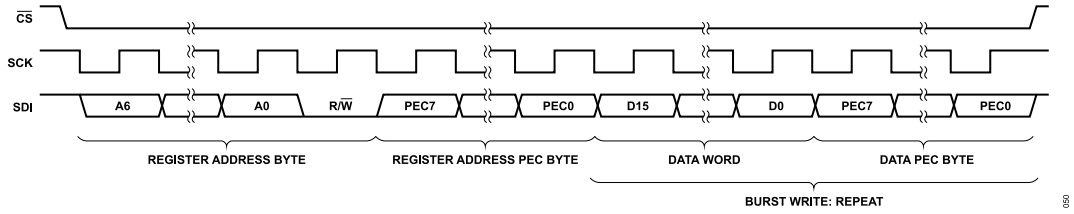


Figure 51. SPI Write

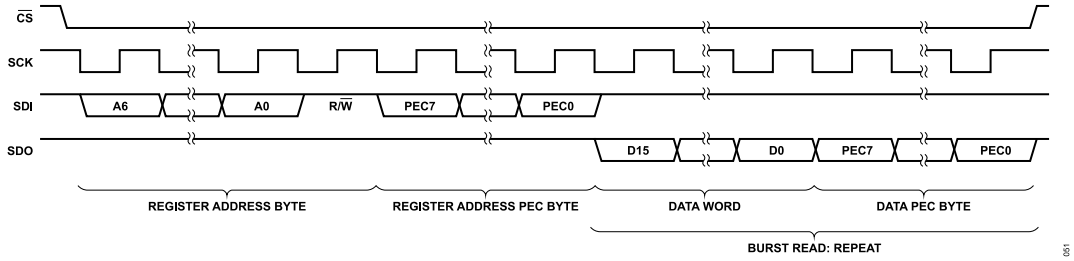


Figure 52. SPI Read

SAMPLE CODE

Pseudo Code Implementation of SPI Write and Read Operations with PEC

```
//**************************************************************************
// Copyright 2022 Analog Devices, Inc.
// All rights reserved.
//
// EXAMPLE: LTC4296-1 SPI PEC Calculation and Read/Write Transactions in C
//**************************************************************************/
uint8_t get_pec_byte(uint8_t data, uint8_t seed)
{
  uint8_t pec = seed;
  uint8_t din, in0, in1, in2;
  int bit;
  for(bit=7; bit>=0; bit--)
  {
    din = (data>>bit) & 0x01;
    in0 = din ^ ( (pec>>7) & 0x01 );
    in1 = in0 ^ ( pec & 0x01);
    in2 = in0 ^ ( (pec>>1) & 0x01 );
    pec = (pec << 1);
    pec &= ~(0x07);
    pec = pec | in0 | (in1<<1) | (in2<<2);
  }
  return pec;
}

void example_write(uint8_t register_address, uint16_t value)
{
  uint8_t tx_buf[5];
  // command byte: register address with r/w bit
  tx_buf[0] = (register_address << 1) & ~(0x01); // r/w bit = 0 for write

  // pec byte from command byte
  tx_buf[1] = get_pec_byte(tx_buf[0], 0x41);

  // data word: 2 bytes, MSB first
  tx_buf[2] = value >> 8; // MSB
  tx_buf[3] = value & 0xFF; // LSB

  // pec byte from data word by using pec calculation twice
  uint8_t intermediate = get_pec_byte(tx_buf[2], 0x41);
  tx_buf[4] = get_pec_byte(tx_buf[3], intermediate);

  // transmit 5 bytes on spi bus
  spi_tx(tx_buf, 5);
}

uint16_t example_read(uint8_t register_address)
{
  uint8_t tx_buf[2];
  uint8_t rx_buf[3];

  // command byte: register address with r/w bit
  tx_buf[0] = (register_address << 1) | 0x01;

  // pec byte from command byte
```

SAMPLE CODE

```
  tx_buf[1] = get_pec_byte(tx_buf[0], 0x41);

  // transmit command byte and pec byte
  spi_tx(tx_buf,2);

  // receive data word and pec byte into rx_buf
  spi_rx(rx_buf,3);

  // construct register value from received data word
  uint16_t register_value = ((uint16_t)rx_buf[0] << 8) | (uint16_t)rx_buf[1];
  return register_value;
}
//*************************************************************************/
```

REGISTER MAP

In the access column of Table 8, R means read only. No effect on the write operation, no effect on the read operation, and reads back the current value. R/W means read and write. Write changes the value to the written value, and read has no effect and reads back the current value. Write 1 to clear means if the bit in the written value is 1, that bit is set to 0, or the bit is not affected. Write 1 to clear has no effect on the read operation and reads back the current value. W means write only. Write changes the value to the written value, and read has no effect, and the read back value is undefined and/or a don't care.

Note that register addresses not listed in Table 8 are reserved and must not be written to.

Table 8. Register Map

Register Address	Register Name	Description	Reset	Access
0x02	GFLTEV	Global Fault Event Register, Read/Write 1 to Clear. Indicates presence of global level faults.	0x0010	R/W
0x03	GFLTMSK	Global Fault Event Mask Register, Read/Write. Provides mask for the global level fault events.	0x000F	R/W
0x06	GCAP	Global Capability Register, Read Only. Presents supported features of PoDL standard.	0x0025	R
0x07	GIOST	Global Status Register, Read Only. Presents status of the inputs and outputs.	0x0000	R
0x08	GCMD	Global Command Register, Read/Write. Entry point for the host to configure the chip.	0x00A0	R/W
0x09	GCFG	Global Configuration Register, Read/Write. Enables the host to configure global functions.	0x0009	R/W
0x0A	GADCCFG	Global ADC Configuration Register, Read/Write. Allows the host to configure the global ADC.	0x0000	R/W
0x0B	GADCDAT	Global ADC Data Register, Read Only. Allows the host to read the latest global ADC measurement.	0x0000	R
0x10	P0EV	Port 0 Event Register, Read/Write 1 to Clear. Indicates presence of Port 0 events.	0x0000	R/W
0x12	P0ST	Port 0 Status Register, Read Only. Provides status of Port 0 events.	0x0000	R
0x13	P0CFG0	Port 0 Configuration Register 0, Read/Write. Provides Port 0 configuration.	0x0002	R/W
0x14	P0CFG1	Port 0 Configuration Register 1, Read/Write. Provides Port 0 configuration.	0x0008	R/W
0x15	P0ADCCFG	Port 0 ADC Configuration Register, Read/Write. Provides Port 0 ADC configuration.	0x0006	R/W
0x16	P0ADCDAT	Port 0 ADC Data Register, Read Only. Allows the host to read the latest Port 0 ADC measurement.	0x0000	R
0x17	P0SELFTEST	Port 0 Self Test Register, Read/Write. Enables the host to perform diagnosis on Port 0.	0x0000	R/W
0x20	P1EV	Port 1 Event Register, Read/Write 1 to Clear. Indicates presence of Port 1 events.	0x0000	R/W
0x22	P1ST	Port 1 Status Register, Read Only. Provides status of Port 1 events.	0x0000	R
0x23	P1CFG0	Port 1 Configuration Register 0, Read/Write. Provides Port 1 configuration.	0x0002	R/W
0x24	P1CFG1	Port 1 Configuration Register 1, Read/Write. Provides Port 1 configuration.	0x0008	R/W
0x25	P1ADCCFG	Port 1 ADC Configuration Register, Read/Write. Provides Port 1 ADC configuration.	0x0006	R/W
0x26	P1ADCDAT	Port 1 ADC Data Register, Read Only. Allows the host to read the latest Port 1 ADC measurement.	0x0000	R
0x27	P1SELFTEST	Port 1 Self Test Register, Read/Write. Enables the host to perform diagnosis on Port 1.	0x0000	R/W

REGISTER MAP

Table 8. Register Map (Continued)

Register Address	Register Name	Description	Reset	Access
0x30	P2EV	Port 2 Event Register, Read/Write 1 to Clear. Indicates presence of Port 2 events.	0x0000	R/W
0x32	P2ST	Port 2 Status Register, Read Only. Provides status of Port 2 events.	0x0000	R
0x33	P2CFG0	Port 2 Configuration Register 0, Read/Write, Provides Port 2 configuration.	0x0002	R/W
0x34	P2CFG1	Port 2 Configuration Register 1, Read/Write. Provides Port 2 configuration.	0x0000	R/W
0x35	P2ADCCFG	Port 2 ADC Configuration Register, Read/Write. Provides Port 2 ADC configuration.	0x0006	R/W
0x36	P2ADCDAT	Port 2 ADC Data Register, Read Only. Allows the host to Read the Latest Port 2 ADC measurement.	0x0000	R
0x37	P2SELFTEST	Port 2 Self Test Register, Read/Write. Enable the host to perform diagnosis on Port 2.	0x0000	R/W
0x40	P3EV	Port 3 Event Register, Read/Write 1 to Clear. Indicates presence of Port 3 events.	0x0000	R/W
0x42	P3ST	Port 3 Status Register, Read Only. Provides status of Port 3 events.	0x0000	R
0x43	P3CFG0	Port 3 Configuration Register 0, Read/Write. Provides Port 3 Configuration.	0x0002	R/W
0x44	P3CFG1	Port 3 Configuration Register 1, Read/Write. Provides Port 3 Configuration.	0x0008	R/W
0x45	P3ADCCFG	Port 3 ADC Configuration Register, Read/Write. Provides Port 3 ADC configuration.	0x0006	R/W
0x46	P3ADCDAT	Port 3 ADC Data Register, Read Only. Allows the host to read the latest Port 3 ADC measurement.	0x0000	R
0x47	P3SELFTEST	Port 3 Self Test Register, Read/Write. Enables the host to perform diagnosis on Port 3.	0x0000	R/W
0x50	P4EV	Port 4 Event Register, Read/Write 1 to Clear. Indicates presence of Port4 Events.	0x0000	R/W
0x52	P4ST	Port 4 Status Register, Read Only. Provides status of Port 4 events.	0x0000	R
0x53	P4CFG0	Port 4 Configuration Register 0, Read/Write. Provides Port 4 configuration.	0x0002	R/W
0x54	P4CFG1	Port 4 Configuration Register 1, Read/Write. Provides Port 4 Configuration.	0x0008	R/W
0x55	P4ADCCFG	Port 4 ADC Configuration Register, Read/Write. Provides Port 4 ADC configuration.	0x0006	R/W
0x56	P4ADCDAT	Port 4 ADC Data Register, Read Only. Allows the host to read the latest Port 4 ADC measurement.	0x0000	R
0x57	P4SELFTEST	Port 4 Self Test Register, Read/Write. Enables the host to perform diagnosis on Port 4.	0x0000	R/W

GLOBAL EVENTS

Table 9. GFLTEV (Register Address 0x02): Global Fault Event Register, Read/Write 1 to Clear, and Indicates Presence of Global Level Faults

Bit(s)	Name	Description
[15:5]	Reserved	Reserved for future use.
4	UVLO_DIGITAL	Set this bit if the digital core was in undervoltage lockout (UVLO). This bit is an unmaskable interrupt.
3	COMMAND_FAULT	Set if an invalid or disallowed command was sent by the host. (for example, accessing an invalid register address).
2	PEC_FAULT	Set if a PEC fault has occurred during the SPI transaction.
1	MEMORY_FAULT	Set if a fault has or faults have occurred in the memory.

REGISTER MAP

Table 9. GFLTEV (Register Address 0x02): Global Fault Event Register, Read/Write 1 to Clear, and Indicates Presence of Global Level Faults (Continued)

Bit(s)	Name	Description
0	LOW_CKT_BRK_FAULT	Set if one or more circuit breakers are tripped in the return path or if there is a fault in the deep sleep return path.

Table 10. GFLTMSK (Register Address 0x03): Global Fault Event Mask Register, Read/Write, Provides Mask for the Global Level Fault Events

Bit(s)	Name	Description
[15:4]	Reserved	Reserved for future use.
3	COMMAND_FAULT	If this bit is cleared, the command interrupt is cleared.
2	PEC_FAULT	If this bit is cleared, the PEC interrupt is cleared.
1	MEMORY_FAULT	If this bit is cleared, the memory interrupt is cleared.
0	LOW_CKT_BRK_FAULT	If this bit is cleared, the return path interrupt is cleared.

GLOBAL STATUS

Table 11. GCAP (Register Address 0x06): Global Capability Register, Read Only, Presents Supported Features of the PoDL Standard

Bit(s)	Name	Description
[15:7]	Reserved	Reserved for future use.
6	SCCP_SUPPORT	Set to 1 if the SCCP is supported. Note that the SCCP is not supported by the LTC4296-1 without external microcontroller support.
5	WAKE_FWD_SUPPORT	Set to 1 if wake-up forwarding is supported (wake-up forwarding is supported by the LTC4296-1).
[4:0]	NUMPORTS	Number of PSE ports.

Table 12. GIOST (Register Address 0x07): Global Status Register, Read Only, Presents Status of the Inputs and Outputs

Bit(s)	Name	Description
[15:9]	Reserved	Reserved for future use.
8	PG_OUT4	Status of Port 4 power good.
7	PG_OUT3	Status of Port 3 power good.
6	PG_OUT2	Status of Port 2 power good.
5	PG_OUT1	Status of Port 1 power good.
4	PG_OUT0	Status of Port 0 power good.
3	PAD_AUTO	Status of AUTO pin.
2	PAD_WAKEUP	Status of WAKEUP pin as driven by the host.
1	PAD_WAKEUP_DRIVE	Status of WAKEUP pin as driven by the IC.
0	Reserved	Reserved for future use.

GLOBAL COMMAND

Table 13. GCMD (Register Address 0x08): Global Command Register, Read/Write, Entry Point for the Host to Configure the Chip

Bit(s)	Name	Description
[15:8]	SW_RESET	After writing the reset code (0x73) in this field, the digital logic is reset (software reset).
[7:0]	WRITE_PROTECT	After writing the write unlock key (0x05), write access to all writeable registers is enabled. After writing the write lock key (0xA0), write access to all writeable registers is disabled. Write access to this field is always enabled.

CONFIGURATION

Table 14. GCFG (Register Address 0x09): Global Configuration Register, Read/Write, Enables the Host to Configure Global Functions

Bit(s)	Name	Description
[15:6]	Reserved	Reserved for future use.
5	MASK_LOWFAULT	Write 1 to prevent ports from entering overload due to low-side faults.
4	TLIM_DISABLE	Write 1 to disable current-limit timers (t_{LIM}) of all ports.

REGISTER MAP

Table 14. GCFG (Register Address 0x09): Global Configuration Register, Read/Write, Enables the Host to Configure Global Functions (Continued)

Bit(s)	Name	Description
[3:2]	TLIM_TIMER_SLEEP	Configures the sleep regulator fault timer for all the ports and the deep sleep return path fault timer as follows: 00b = 15.6 ms. 01b = 31.2 ms. 10b = 62.5 ms (default). 11b = disables sleep fault timers.
1	REFRESH	Write 1 to copy contents from nonvolatile memory into the volatile memory. Auto cleared after completion.
0	SW_VIN_PGOOD	Write 1 to indicate that the system is ready to source the required power to connected PDs.

GLOBAL ADC

Table 15. GADCCFG (Register Address 0x0A): Global ADC Configuration Register, Read/Write, Allows the Host to Configure the Global ADC

Bit(s)	Name	Description
[15:7]	Reserved	Reserved for future use.
[6:5]	GADC_SAMPLE_MODE	Configures global ADC in following modes as follows: 00b = disabled. 01b = single-shot mode (autocleared after one measurement). 10b = continuous mode with low gain. 11b = continuous mode with high gain.
[4:0]	GADC_SEL	Configures global ADC inputs as follows: 00000b = GND. 00001b = V_{IN}. 00010b = temperature. 00100b = Port 0 output voltage. 00101b = Port 0 return sense voltage. 00110b = Port 1 output voltage. 00111b = Port 1 return sense voltage. 01000b = Port 2 output voltage. 01001b = Port 2 return sense voltage. 01010b = Port 3 output voltage. 01011b = Port 3 return sense voltage. 01100b = Port 4 output voltage. 01101b = Port 4 return sense voltage. 1XXXXb = Internal check voltage reference.

Table 16. GADCDAT (Register Address 0x0B): Global ADC Data Register, Read Only, Allows the Host to Read the Latest Global ADC Measurement

Bit(s)	Name	Description
[15:14]	Reserved	Reserved for future use.
13	GADC_MISSED	Set when the host has missed reading one or more of the results stored by the global ADC in Register Address GADCDAT, Bits[11:0], GADC.
12	GADC_NEW	Set when a new result is stored by the global ADC in Register Address GADCDAT, Bits[11:0], GADC.
[11:0]	GADC	Global ADC Accumulation Result.

REGISTER MAP

PORT X EVENTS

Table 17. PxEV (Register Address 0xx0): Port x Event Register, Read/Write 1 to Clear, Indicates Presence of Port x Events

Bit(s)	Name	Description
[15:10]	Reserved	Reserved for future use.
9	VALID_SIGNATURE	Set when a valid signature was detected on the port.
8	INVALID_SIGNATURE	Set when an invalid signature was detected on the port.
7	TOFF_TIMER_DONE	Set when the t_{OFF} timer expired when the port was discharging toward V_{SLEEP}.
6	OVERLOAD_DETECTED_ISLEEP	Set when the overload timer t_{LIM} expired due to overcurrent while the port was attempting to apply V_{SLEEP} at the power interface.
5	OVERLOAD_DETECTED_IPOWERED	Set when the overload timer t_{LIM} expired due to overcurrent while the port was in the power-up or power-on state.
4	MFVS_TIMEOUT	Set when power was removed due to t_{MFVDO} timer expiration.
3	TINRUSH_TIMER_DONE	Set when t_{INRUSH} timer expired when the port was in the power-up state.
2	PD_WAKEUP	Set when an upstream (PD initiated) wake-up is detected, that is, the port current was in the valid wake-up current range for at least t_{WAKEUP} when the port was in the sleep state.
1	LSNS_FORWARD_FAULT	Set when low-side forward circuit breaker fault event has occurred on the port.
0	LSNS_REVERSE_FAULT	Set when low-side reverse circuit breaker fault event has occurred on the port.

PORT X STATUS

Table 18. PxST (Register Address 0xx2): Port x Status Register, Read Only, Provides Status of Port x Events

Bit(s)	Name	Description
[15:14]	Reserved	Reserved for future use.
13	DET_VHIGH	Set when port voltage is greater than $V_{BAD\_HI\_PSE}$ during detection.
12	DET_VLOW	Set when port voltage is less than $V_{BAD\_LO\_PSE}$ during detection.
11	POWER_STABLE_HI	Set when following inrush port is sourcing the full operating voltage and $V_{IN} - V_{OUTPx}$ is less than ΔV_{OUTPx_PWRGD}.
10	POWER_STABLE_LO	Set when following inrush port is sourcing the full operating voltage and V_{OUTMx} less than delta ΔV_{OUTMx_PWRGD}.
9	POWER_STABLE	Set when the port is delivering the full operating voltage to the output.
8	OVERLOAD_HELD	Set when the port is in the overload state.
7	PI_SLEEPING	Set when the port is in the settle-sleep or sleep state.
6	PI_PREBIASED	Set when the port is in the idle state.
5	PI_DETECTING	Set when the port is in the detection state.
4	PI_POWERED	Set when the port is in the power-up or power-on state.
3	PI_DISCHARGE_EN	Set when the port is in the settle-sleep state.
[2:0]	PSE_STATUS	PSE status decoded as follows: 000b = port is disabled. 001b = port is in sleeping. 010b = port is delivering power. 011b = port is searching. 100b = port is in error. 101b = port is idle. 110b = port is preparing for detection. 111b = port is in an unknown state.

PORT X CONFIGURATION

Table 19. PxCFG0 (Register Address 0xx3): Port x Configuration Register 0, Read/Write, Provides Port x Configuration

Bit(s)	Name	Description
15	SW_INRUSH	Write 1 to skip prebias and detection and directly power up the PD.
14	END_CLASSIFICATION	Write 1 to end classification. Autocleared by the IC.
13	SET_CLASSIFICATION_MODE	Write 1 to set the port in classification mode.

REGISTER MAP

Table 19. PxCFG0 (Register Address 0xx3): Port x Configuration Register 0, Read/Write, Provides Port x Configuration (Continued)

Bit(s)	Name	Description
12	DISABLE_DETECTION_PULLUP	Write 1 to disable the detection pull-up current.
11	TDET_DISABLE	Write 1 to disable the detection timer.
10	FOLDBACK_DISABLE	Write 1 to disable foldback during port inrush in the power-up state.
9	SOFT_START_DISABLE	Write 1 to disable soft-start during port inrush in the power-up state.
8	TOFF_TIMER_DISABLE	Write 1 to disable the t_{OFF} timer to allow the port arbitrarily long time for discharging in the settle-sleep state.
7	TMFVDO_TIMER_DISABLE	Write 1 to disable the t_{MFVDO} timer to prevent the port from shutting off in absence of a valid MFVS.
6	SW_PSE_READY	Write 1 to indicate that the port is ready for detection.
5	SW_POWER_AVAILABLE	Write 1 to indicate that the port is able to source power to the connected PD.
4	UPSTREAM_WAKEUP_DISABLE	Write 1 to disable the upstream (PD initiated) wake-up of the port.
3	DOWNSTREAM_WAKEUP_DISABLE	Write 1 to disable the downstream (PSE initiated) wake-up of the port.
2	SW_PSE_WAKEUP	Write 1 to wake up the port.
1	HW_EN_MASK	Write 0 to mask the AUTO pin.
0	SW_EN	Write 1 to enable the port.

Table 20. PxCFG1 (Address 0xx4): Port x Configuration Register 1, Read/Write, Provides Port x Configuration

Bit(s)	Name	Description
[15:9]	Reserved	Reserved for future use.
8	PREBIAS_OVERRIDE_GOOD	Write 1 to simulate a valid wake-up signature.
[7:6]	TLIM_TIMER_TOP	Write as follows to configure the top-side fault timer (t_{LIM}): 00b = 59.9 ms (default). 01b = 29.9 ms. 10b = 15 ms. 11b = 0.46 ms. Note that the t_{LIM} timer decrements towards zero in the presence of the fault event and increment towards the configured value in absence of the fault event. The decrement rate is 8x the increment rate
[5:4]	TOD_TRESTART_TIMER	Write as follows to configure the overload delay timer and restart timer: 00b = default (t_{OD} = 1.1 sec and $t_{RESTART}$ = 551 ms). 01b = 2x of default. 10b = 4x of default. 11b = forever.
[3:2]	TINRUSH_TIMER	Write as follows to configure the t_{INRUSH} timer: 00b = 3.5 ms. 01b = 14 ms. 10b = 56.2 ms (default). 11b = forever.
1	SIG_OVERRIDE_BAD	Write 1 to simulate an invalid detection voltage signature.
0	SIG_OVERRIDE_GOOD	Write 1 to simulate a valid detection voltage signature.

Table 21. PxADCCFG (Register Address 0xx5): Port x ADC Configuration Register, Read/Write, Provides Port x ADC Configuration

Bit(s)	Name	Description
[15:8]	Reserved	Reserved for future use.
[7:0]	MFVS_THRESHOLD	MFVS threshold to be set based on the MFVS Threshold Code = 62.5 x R1 equation. See the Maintain Full Voltage Signature (MFVS) section for additional information.

REGISTER MAP

Table 22. PxADCDAT (Register Address 0xx6): Port x ADC Data Register, Read Only, Allows the Host to Read the Latest Port x ADC Measurement

Bit(s)	Name	Description
[15:14]	Reserved	Reserved for future use.
13	Missed	Set when the host has missed one or more measurements of source current stored in Register PxADCDAT, Bits[11:0], SOURCE_CURRENT.
12	New	Set when a new measurement result of source current is stored by the port ADC in Register PxADCDAT, Bits[11:0], SOURCE_CURRENT.
[11:0]	SOURCE_CURRENT	Source current measurement

PORT X DIAGNOSIS

Table 23. PxSELFTEST (Register Address 0xx7): Port x Self Test Register, Read/Write, Enable the Host to Perform Diagnosis on Port x

Bit(s)	Name	Description
[15:2]	Reserved	Reserved for future use.
1	FORCE_BAD_OUTM	Write 1 to simulate a power bad on OUTMx pin of the port.
0	FORCE_BAD_OUTP	Write 1 to simulate a power bad on OUTPx pin of the port.

APPLICATIONS INFORMATION

OVERVIEW

Figure 53 shows a typical LTC4296-1 circuit for one of five ports. The high-side, electronic circuit breaker with foldback ACL of each port controls inrush current during power-up and protects against output faults. The circuit breaker controls the gate-to-source voltage of the N-channel, M1 MOSFET with the HGATEx and OUTPx pins while monitoring the voltage of the R1 current-sense resistor with the HSNSPx and HSNSMx pins. The port power snubber (R3 + R4, and C4) stabilizes the ACL, and it is disconnected by the M2 MOSFET during classification. The auxiliary snubber (R5 and C5) provides a well-defined AC impedance when the M2 switch is disabled. The M3 MOSFET is driven by the host microcontroller to assert a logic low during the SCCP write operation. The Q1 NPN transistor limits the voltage sensed by the microcontroller during the SCCP.

Power controlled by the LTC4296-1 and data from a PHY, such as the ADIN1100, are coupled to the port through a power-coupling network circuit. A common-mode choke (CMC) and diplexer inductors comprise the power-coupling network, which is further discussed in the Power-Coupling Network Selection section.

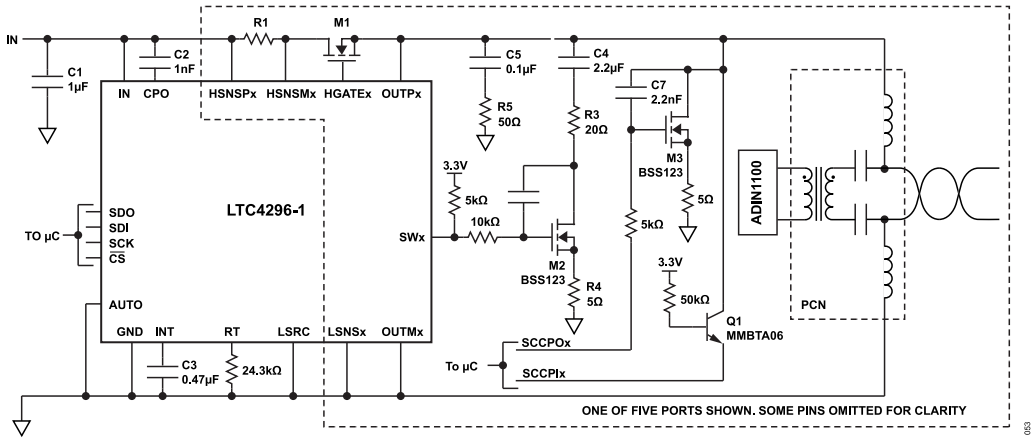


Figure 53. Typical LTC4296-1 Circuit (One of the Five Ports Is Shown)

APPLICATIONS INFORMATION

POWER SUPPLY

When selecting a power supply, the tolerance of the supply and the voltage drops across the power path components at the highest PD load must fall within the V_{PSE} range specified in Table 5 for the desired Class. The LTC4296-1 is designed to service up to five ports that share the same voltage class (20 V to 30 V or 50 V to 58 V).

To ensure data integrity, the PSE power supply at the LTC4296-1 input must meet ripple specifications as required by IEEE 802.3cg. Ripple must be measured at the medium dependent interface (MDI) connector with a digital storage oscilloscope (DSO) using the AC-coupled 100 Ω resistor and scope probe shown in Figure 54. The observed ripple must be less than 0.1 V p-p within a bandwidth of 1 kHz to 10 MHz. The observed ripple is then post processed with a transfer function H(f) given by the following equation and must be less than 0.01 V p-p within a bandwidth of 1 kHz to 10 MHz:

$$H(f) = \frac{f}{\sqrt{f^2 + {f_0}^2}} \quad (2)$$

where f_0 = 100 kHz.

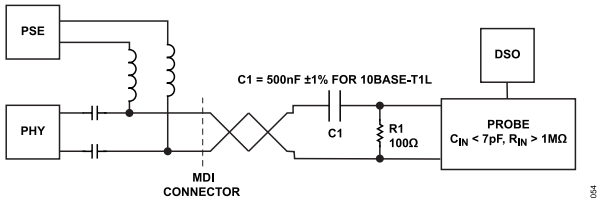


Figure 54. Power Supply Ripple Measurement Setup (C_{IN} Is the Input Capacitance, and R_{IN} Is the Input Resistance.)

EXTERNAL COMPONENT SELECTION

Typical application components for Class 10 to Class 14 are shown in the Figure 55. Typical application components for Class 15 are shown in Figure 56. Additional guidance on selecting components is provided in the following sections.

Capacitor Selection

The LTC4296-1 IN pin operates from an input voltage from 6 V to 60 V. Place a low equivalent series resistance (ESR) decoupling capacitance (C1) of at least 1 µF from IN to GND. Common ceramic capacitors have significant voltage coefficients; the capacitance is reduced as the applied voltage increases. To minimize this problem, the IN pin bypass capacitor must be rated X7R and twice the maximum operating voltage.

The LTC4296-1 generates its own internal supplies at the INT and CPO pins. Place a 470 nF, 6.3 V decoupling capacitor (C3) from INT to GND and place a 1 nF, 16 V decoupling capacitor (C2) from CPO to IN. The C4, C5, C6, C7, C8, and C9 capacitors must have proper supply voltage ratings for the class applications.

Input Transient Voltage Suppressor (TVS) Selection

A TVS (D1) connected between IN and GND helps protect the LTC4296-1 (and any other device on this rail) from overvoltage due to a supply spike during a cable surge or forced backfeed voltages. The TVS clamp voltage and power rating must meet the surge current requirements and maximum voltage ratings of the devices on the rail.

High-Side MOSFET Selection

The LTC4296-1 foldback ACL feature reduces the port current-limit threshold voltage when the drain-to-source voltage (V_{DS}) of the MOSFET exceeds 12 V. Foldback can be disabled by setting the port foldback disable bit (Register PxCFG0, Bit 9, FOLDBACK_DISABLE). A port high-side N-channel MOSFET (M1) with an adequate safe operating area (SOA) consistent with the foldback ACL profile shown in Figure 12 must be used to ensure reliability during inrush and short-circuit conditions. Divide the foldback ACL profile sense-resistor voltage with the R1 sense-resistor value of the port for comparison against the MOSFET SOA curve current. The MOSFET SOA curve current must be less than the scaled foldback ACL curve current for t_{INRUSH} and t_{LIM} and the maximum operating ambient temperature of the system.

Additional considerations when selecting a MOSFET are $R_{DS(ON)}$ and V_{DS}. Low $R_{DS(ON)}$ minimizes heat losses for port DC currents. The maximum rated V_{DS} of the MOSFET must exceed the peak power-supply voltage.

Figure 55 and Figure 56 provide a high-side, N-channel MOSFET recommendation that meets the SOA requirements for each respective class.

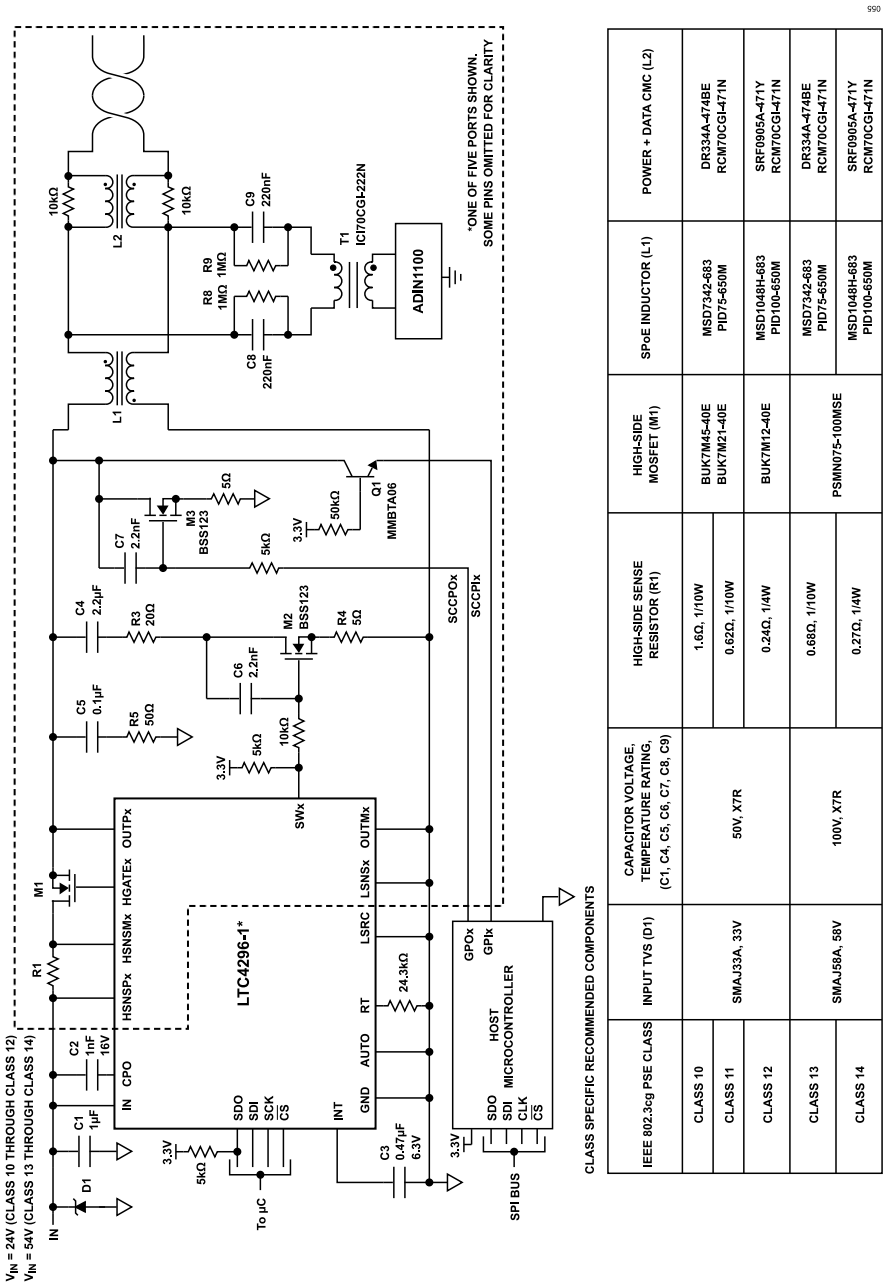
High-Side Sense-Resistor Selection

The LTC4296-1 is designed to work with a range of sense resistors that are required to meet the power class requirements of the IEEE 802.3cg. A sense resistor for each port sets the respective high-side ACL current threshold (I_{LIM}) of the port per the following equation:

$$R1 < V_{ILIMx}/I_{LIM}\ (\Omega) \quad (3)$$

The ACL threshold must be in the $I_{PI(MAX)} < I_{LIM} < 1.41 \times I_{PI(MAX)}$ range.

APPLICATIONS INFORMATION



CLASS SPECIFIC RECOMMENDED COMPONENTS

IEEE 802.3cg PSE CLASS	INPUT TVS (D1)	CAPACITOR VOLTAGE, TEMPERATURE RATING, (C1, C4, C5, C6, C7, C8, C9)	HIGH-SIDE SENSE RESISTOR (R1)	HIGH-SIDE MOSFET (M1)	SPoE INDUCTOR (L1)	POWER + DATA CMC (L2)
CLASS 10	SMAJ33A, 33V	50V, X7R	1.6Ω, 1/10W	BUK7M45-40E BUK7M21-40E	MSD7342-683 PID75-650M	DR334A-474BE RCM70CGI-471N
CLASS 11			0.62Ω, 1/10W			
CLASS 12			0.24Ω, 1/4W	BUK7M12-40E	MSD1048H-683 PID100-650M	SRF0905A-471Y RCM70CGI-471N
CLASS 13	SMAJ58A, 58V	100V, X7R	0.68Ω, 1/10W	PSMN075-100MSE	MSD7342-683 PID75-650M	DR334A-474BE RCM70CGI-471N
CLASS 14			0.27Ω, 1/4W		MSD1048H-683 PID100-650M	SRF0905A-471Y RCM70CGI-471N

Figure 55. LTC4296-1 802.3cg Class 10 Through Class 14 Application

APPLICATIONS INFORMATION

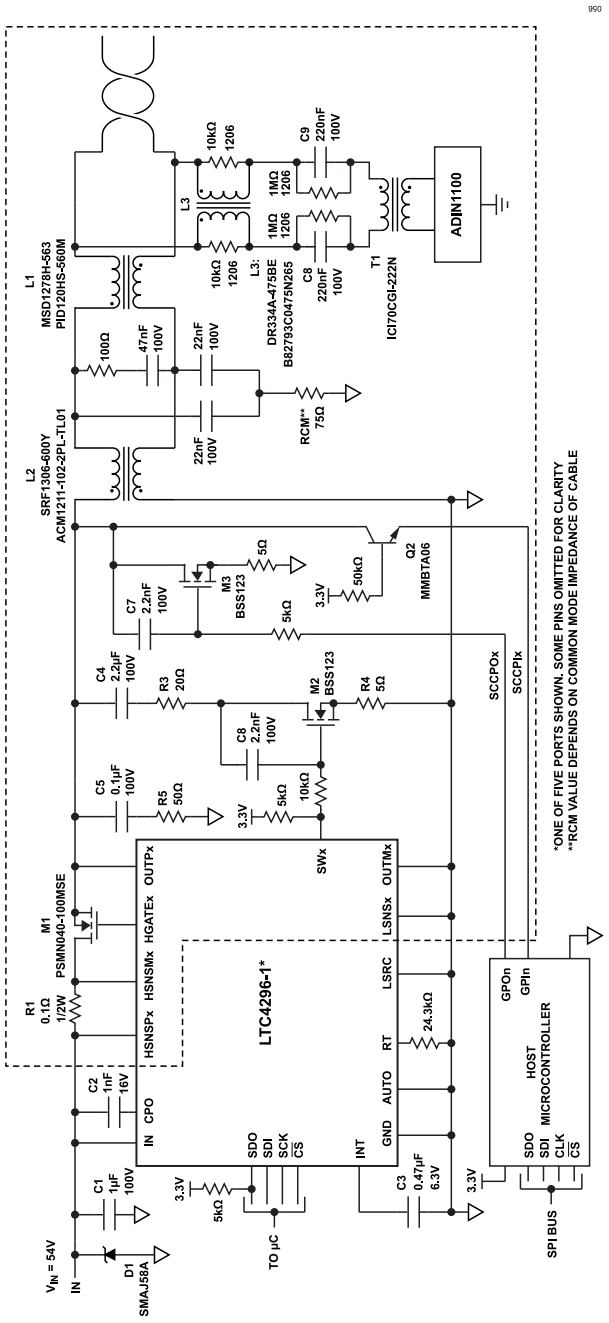


Figure 56. LTC4296-1 802.3cg Class 15 Application

The sense resistors must have ±1% tolerance or better and no more than a ±200 ppm/°C temperature coefficient. Appropriate wattage must be selected for the sense resistors per the following equation:

$$P_{R1} > 2 \times (V_{ILIMx})^2/R1 \text{ (W)} \quad (4)$$

It is good practice to select a power rating for at least double the resistor application power.

Figure 55 and Figure 56 provide a high-side sense-resistor value and power rating for each 802.3cg power class.

Refer to the Layout Guidelines section for proper Kelvin sensing with the sense resistor.

Power-Coupling Network Selection

Power and data are coupled together at the MDI through a power coupling network (PCN). The PHY is AC-coupled through a data transformer (T1). The PSE DC power is coupled on to the differential data lines through the differential mode inductor (DMI), L1. The CMC (L2) blocks common-mode signals at the MDI.

APPLICATIONS INFORMATION

The DMI (L1) and CMC (L2) must be selected to meet the droop, return loss, and mode conversion specifications as defined in the IEEE 802.3cg for the respective maximum power class.

Figure 55 shows a PHY-side PCN topology; power is injected through the DMI (L1) on the PHY side of the CMC (L2). Power and data are passed through the CMC. DC blocking capacitors (C8 and C9) with balancing resistors (R8 and R9) prevent the SPoE DC current from passing through the T1 transformer. This topology is recommended for Class 10 through Class 14.

Figure 56 shows a line-side (cable-side) PCN topology for Class 15; power is injected through the DMI (L1) on the line-side of the PHY CMC (L3). L2 is the power path CMC, and L3 is the data-only CMC. The C8 and C9 capacitors block the SPoE DC current from flowing through the T1 transformer.

Output-Power Snubber Selection

An output-power snubber, comprised of a 2.2 µF, X7R capacitor (C4) in-series with a resistance (R3 + R4) from the OUTP to OUTM pins of each port is required for current-limit stability during startup or overload. The C4 voltage rating must be at least twice the maximum operating voltage to account for capacitor voltage coefficients. For calculating R3 resistance, use the following equation:

$$R3 = 2 \times \sqrt{\frac{L_{DIFF}}{C4} - R4} \quad (5)$$

where L_{DIFF} is the differential inductance seen at the MDI. If L1 is a DMI (coupled inductor), use the calculated differential inductance of four times the single winding inductance.

Note that the 5 Ω resistor (R4) limits the current through M2. Choose the nearest 5% resistor values.

Low-Side Circuit Breaker Selection

A low-side circuit breaker can be implemented if protection against excessive low-side currents is required. This low-side circuit breaker disconnects the ground connection to all ports. See Figure 57.

The low-side circuit breaker controls the N-channel MOSFET (M4) gate-to-source voltage with the LGATE and LSRC pins. M4 is fully enhanced when the first port enters the idle state. Low-side current is monitored with the voltage across the R2 sense resistor measured at the LSNSx and OUTMx pins. Port 1 and Port 2 share the LSNS1/LSNS2 sense pin, and Port 3 and Port 4 share the LSNS3/LSNS4 sense pin. A low-side current causing any of the low-side, sense-resistor voltage to exceed $\Delta V_{LSNSx(FCB)}$ for t_{LSNS_FAULT} trips the circuit breaker; all LTC4296-1 ports that are out of the disabled state are forced to the overload state.

The low-side R2 sense resistor of each port sets the low-side circuit breaker current threshold for that port. This current threshold must be set for over 50% higher than the high-side ACL threshold for the corresponding port. To calculate the R2 value, use the following equation:

$$R2 = < \Delta V_{LSNSx(FCB)(MIN)} / I_{CB} \ (\Omega) \quad (6)$$

where I_{CB} is the circuit breaker current threshold.

Appropriate wattage must be selected for the sense resistors per the following equation:

$$P_{R2} > 2 \times (\Delta V_{LSNSx(FCB)(MAX)})^2 / R2 \ (W) \quad (7)$$

It is good practice to select a power rating for at least double the resistor application power.

Refer to the Layout Guidelines section for proper Kelvin sensing with the sense resistor.

Figure 58 provides the recommended R2 resistor values and power ratings per the maximum port power class. Refer to the Layout Guidelines section for the proper Kelvin sense layout with the low-side sense resistor.

The low-side circuit breaker MOSFET must have an adequate V_{DS} rating for the maximum system application and fault conditions. Because this MOSFET is for fast circuit breaking and not current limiting, high SOA is not required compared to the high-side MOSFET. Low $R_{DS(ON)}$ helps minimize losses.

An internal switch from LSNS0 to GND establishes a return path for all the OUTMx pins to ground when the low-side MOSFET is disabled, for example disabled or deep sleep. R_{SLP_LSNS0} is the on resistance for the deep-sleep return. The deep-sleep return switch is always on unless the low-side circuit breaker trips, or an overcurrent fault occurs and turns back on after a restart delay.

MDI FAULT TOLERANCE

Most applications with isolation only require the high-side circuit breaker as shown in Figure 1. For applications requiring MDI fault tolerance from an external positive or negative, forced voltage at the MDI, Figure 58 provides a protection solution.

A rectifying circuit or device before the IN pin protects components at the supply from a positive backfeed voltage greater than the supply voltage.

The low-side circuit breaker, C10 capacitor, D2 current steering diode, D3 current steering diode, and D1 TVS protect the PSE from negative voltages at the MDI. When a forced negative voltage is applied, the current through M1 is limited by the port foldback ACL, and D2 provides a return path for the remaining low-side current through M4. When the low-side circuit breaker trips, M4 is open and capacitor C10 absorbs the inductive kickback. D2 continues to conduct until C10 is charged to the forced negative voltage. High voltage ringing at LSNSx is steered by D3 to the TVS D1. All ports are held in the overload state during this fault.

APPLICATIONS INFORMATION

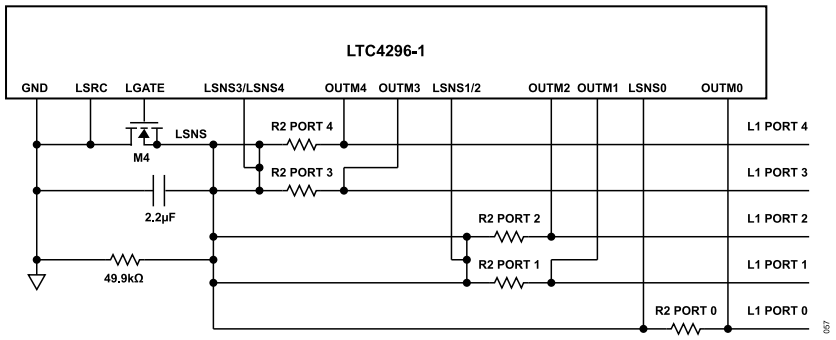
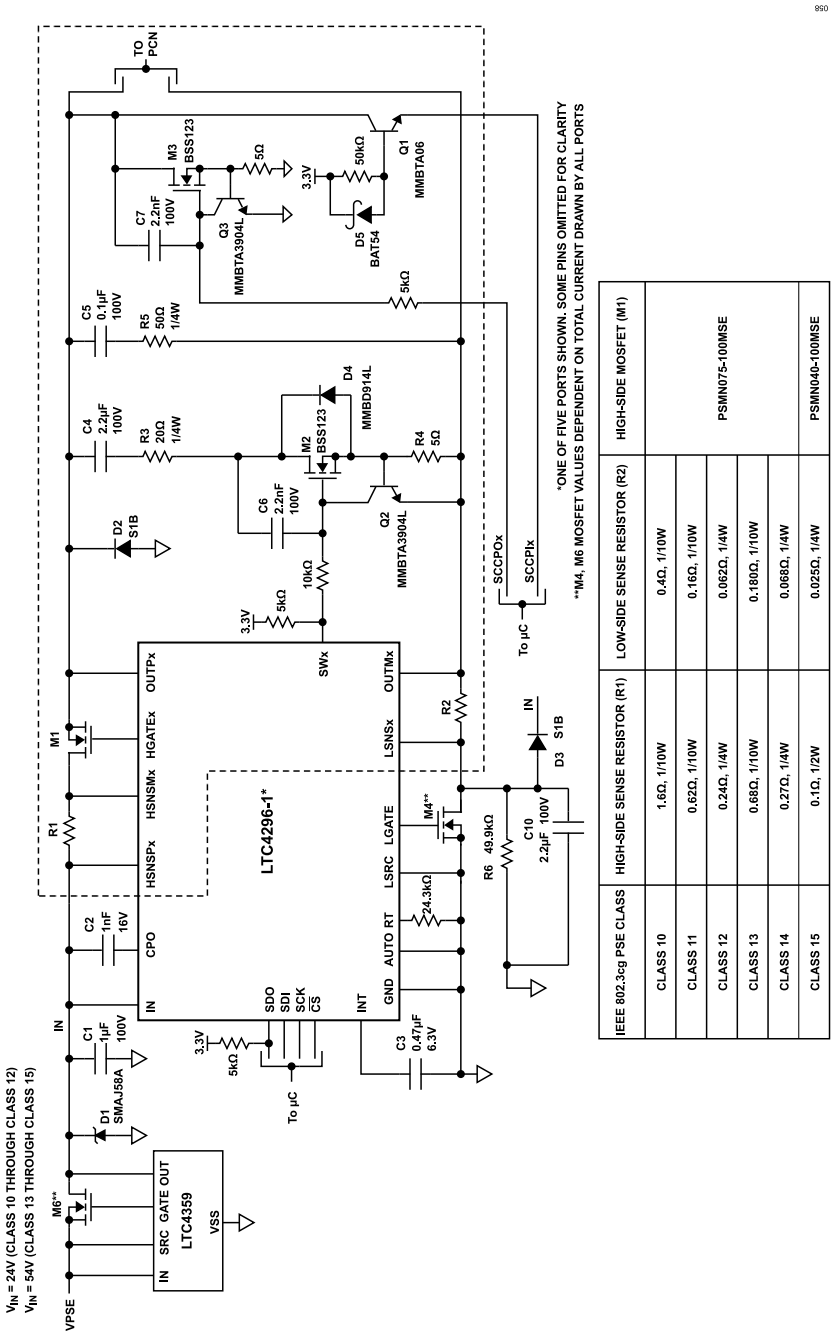


Figure 57. Low-Side Circuit Breaker

APPLICATIONS INFORMATION



IEEE 802.3cg PSE CLASS	HIGH-SIDE SENSE RESISTOR (R1)	LOW-SIDE SENSE RESISTOR (R2)	HIGH-SIDE MOSFET (M1)
CLASS 10	1.8Ω, 1/10W	0.4Ω, 1/10W	PSMN075-100MSE
CLASS 11	0.62Ω, 1/10W	0.16Ω, 1/10W	
CLASS 12	0.24Ω, 1/4W	0.062Ω, 1/4W	
CLASS 13	0.68Ω, 1/10W	0.180Ω, 1/10W	
CLASS 14	0.27Ω, 1/4W	0.068Ω, 1/4W	
CLASS 15	0.1Ω, 1/2W	0.025Ω, 1/4W	PSMN040-100MSE

Figure 58. LTC4296-1 PSE Port with MDI Fault Tolerance

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

Refer to the EVAL-SPoE-KIT-AZ Evaluation Kit User Guide for the layout reference. Standard power layout guidelines apply to the LTC4296-1, such as placing the decoupling capacitors for the IN, V_{INT}, and CPO supplies near their respective supply pins, use of ground planes, and use of wide traces wherever there are significant currents.

Kelvin Sense

Kelvin-sense connections to the current-sense resistors must always be used to ensure that the specified current-threshold accuracy is achieved. Figure 59 shows an example of proper Kelvin sensing for the high-side sense pins, HSNSPx and HSNSMx, to the respective sense resistor.

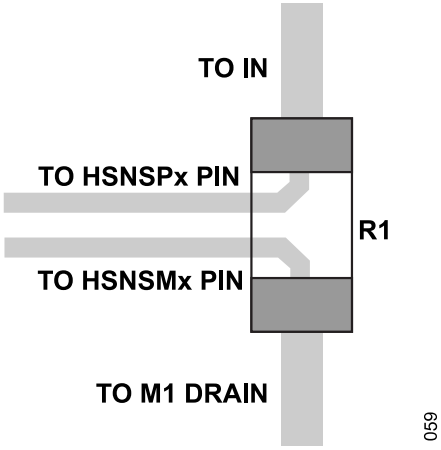


Figure 59. HSNSPx and HSNSMx Pin Kelvin Connection

For applications that implement the optional low-side circuit breaker, care must be taken to minimize stray currents at the shared Kelvin signal LSNS1/LSNS2 between Port 1 and Port 2, and LSNS3/LSNS4 between Port 3 and Port 4. The OUTM1, OUTM2, OUTM3, and OUTM4 pins must also have proper Kelvin sense to the respective sense resistor (see Figure 60).

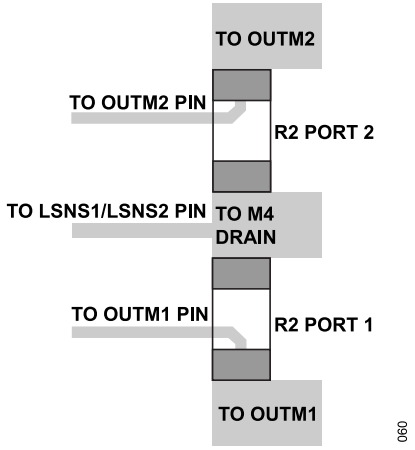


Figure 60. Shared LSNS1/LSNS2 and OUTM1 and OUTM2 Pins Example Kelvin Sense Layout

For the LSNS0 and OUTM0 signals, use the same Kelvin-sense technique as shown for HSNSPx and HSNSMx in Figure 59.

DATA CONVERTERS

Internal Temperature Sensor

The internal junction temperature can be measured by programming the global ADC configuration register to select the temperature sensor as the ADC input and enable the ADC for single-shot or continuous mode measurement (Register GADCCFG, Bits[4:0], GADC_SEL and Register GADCCFG, Bits[6:5], GADC_SAMPLE_MODE, respectively). The ADC results are available in the global ADC data register when the measurement is completed (Register GADCDAT, Bits[11:0], GADC) after approximately 3.6 ms and is updated every 1.8 ms thereafter in continuous mode. The LTC4296-1 sets the GADC new data bit (Register GADCDAT, Bit 12, GADC_NEW) when the new measurement is available to read. The T_J readout in °C can be determined by the following equation:

$$T_J = \frac{GADC, Bits[11:0] - 2048}{4} - 273.15 \quad (8)$$

Port, High-Side Current Readback

The port, high-side, current-sense resistor voltage can be measured by reading the port ADC result register (Register PxADCDAT, Bits[11:0], SOURCE_CURRENT) while in the power-up and power-on states. The port ADC result register is updated every 1.8 ms. To determine the expression for the source current (I_{SOURCE}) readout as a function of the high-side, current-sense resistor (R1), use the following equation:

$$I_{SOURCE}(A) = \frac{(SOURCE\_CURRENT, Bits[11:0] - 2048) \times 10}{R1} \quad (9)$$

APPLICATIONS INFORMATION

Port, Low-Side Current Readback

The port, low-side current (I_{RETURN}) sense-resistor voltage can be measured by programming the global ADC configuration register to select a port, low-side current as the ADC input and enable the ADC for single-shot or continuous mode measurement (Register GADCCFG, Bits[4:0], GADC_SEL and Register GADCCFG, Bits[6:5], GADC_SAMPLE_MODE, respectively). The ADC results are available in the global ADC data register when the measurement is completed (Register GADCDAT, Bits[11:0], GADC) after approximately 3.6 ms and are updated every 1.8 ms thereafter in continuous mode. To determine the expression for current as a function of the high-side, current-sense resistor (R2), use the following equation:

$$I_{RETURN}(A) = \frac{(GADC, Bits[11:0] - 2048) \times 100\mu V}{R2} \quad (10)$$

Input and Port Output Voltage Readback

V_{IN} and the port output voltage (V_{PORT}) can be measured by programming the global ADC configuration register. Select the V_{IN} input voltage or the port output voltage ($V_{PORT} = V_{OUTPx} - V_{OUTMx}$) as the ADC input and enable the ADC for single-shot or continuous mode measurement (Register GADCCFG, Bits[4:0], GADC_SET and Register GADCCFG, Bits[6:5], GADC_SAMPLE_MODE, respectively). High-gain or low-gain resolution can be selected in continuous mode. The ADC results are available in the global ADC data register when the measurement is completed (Register GADCDAT, Bits[11:0], GADC) after approximately 3.6 ms and is updated every 1.8 ms thereafter in continuous mode. To determine the expression for the input and port output voltage, use the following equations:

Low-Gain V_{IN} (V), V_{PORT} (V) = (*GADC, Bits[11:0]* − 2048) x 35.2 mV (11)

High-Gain V_{IN} (V), V_{PORT} (V) = (*GADC, Bits[11:0]* − 2048) x 17.6 mV (12)

ISOLATION CONSIDERATIONS

Traditional IEEE 802.3 multipair Ethernet specifications require that network segments (including PoE circuitry) be electrically isolated from the chassis ground of each network interface device. However, IEEE 802.3bu (PoDL) and IEEE 802.3cg (SPoE) only require PDs provide at least 1 MΩ isolation between all accessible external conductors and the MDI, when measured using 5 V ± 20%. Both of these standards also require that all equipment complies with local, state, national, and application-specific standards, such as the applicable sections of IEC 61010-1 or IEC 62368-1:2018.

For simple devices with no electrically conducting pins other than the twisted-pair Ethernet MDI, the isolation requirement can be met by using a nonconductive chassis enclosure.

For SPoE applications that require galvanic isolation from chassis, an isolated power supply must be used to power the LTC4296-1 and SPoE. Any input/output crossing the isolation must have some form of high-voltage tolerant coupling. Proper layout techniques must be implemented to maintain the high voltage isolation on the PCB.

APPLICATIONS INFORMATION

LOW-DROOP APPLICATIONS

Figure 61 shows a high-current application circuit suitable for use cases where the PHY transmitter droop requirement is 10% as opposed to the 25% requirement for IEEE 802.3cg.

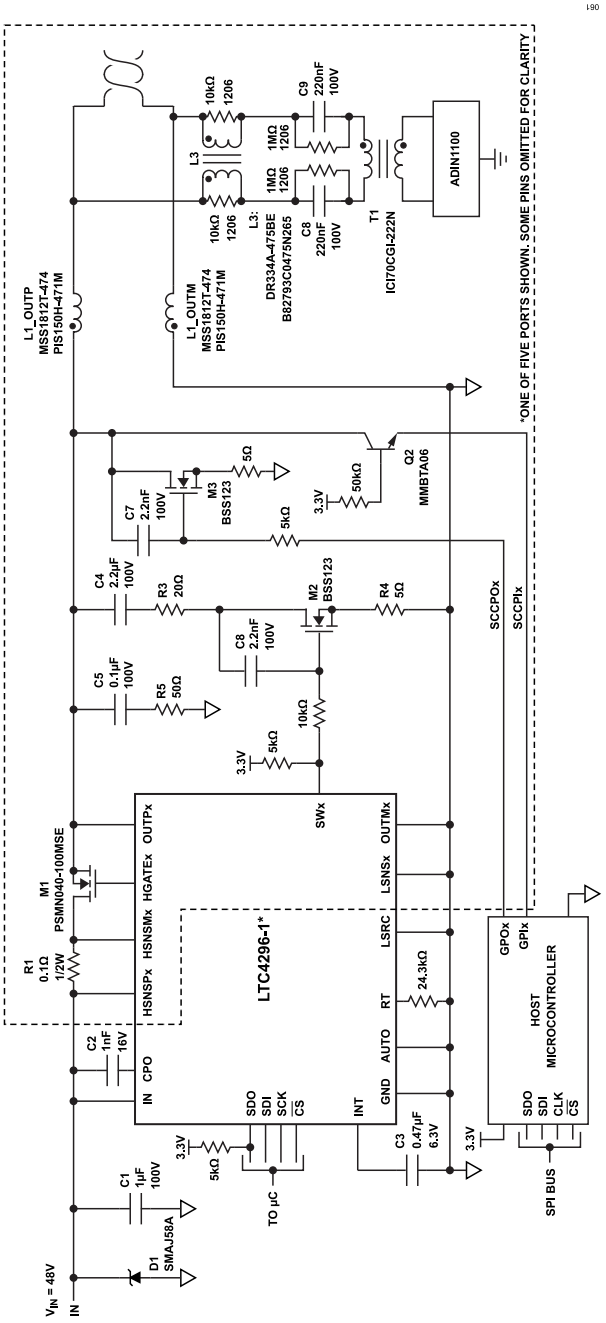


Figure 61. High-Current, Low-Droop Application Circuit

APPLICATIONS INFORMATION

CLASS 14 TYPICAL APPLICATION

Figure 62 shows the IEEE 802.3cg Class 14 PSE.

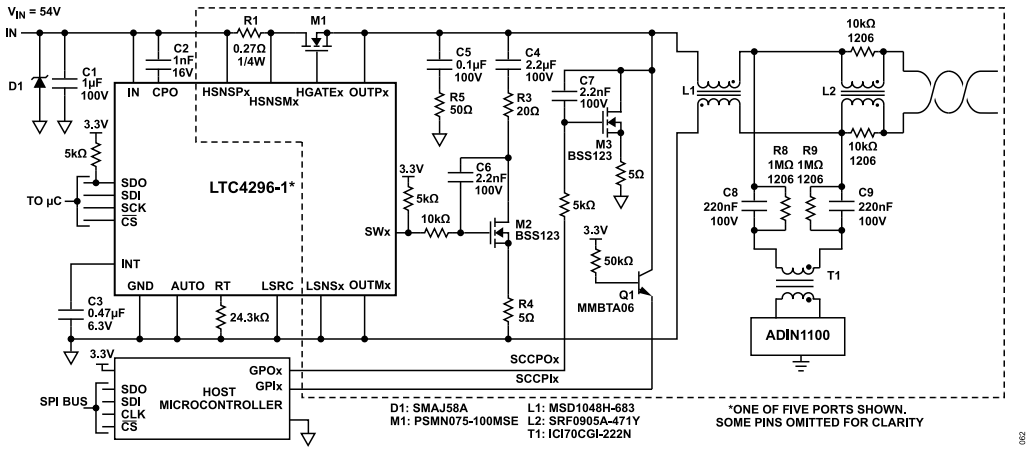


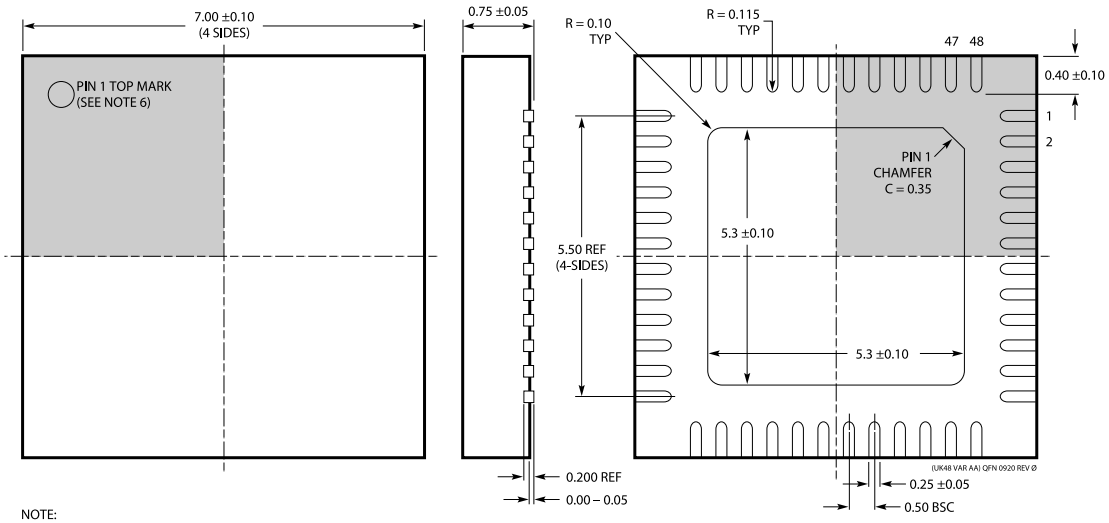
Figure 62. IEEE 802.3cg Class 14 PSE

RELATED PARTS

Table 24. Related Parts

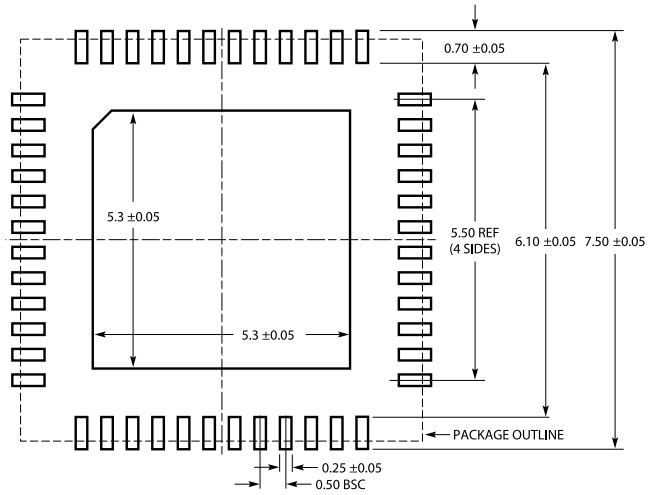
Part Number	Description	Comments
LTC9111	IEEE 802.3cg SPoE PD controller	IEEE 802.3cg-compliant, supports SCCP, external switch, low-side ideal bridge, pin-programmable class configuration, 2.3 V to 60 V input range
ADIN1100	Robust, industrial, low power 10BASE-T1L PHY	Low power, single port transceiver; compliant with IEEE 802.3cg-2019 Ethernet standard for long reach SPE
ADIN1110	Robust, industrial, low power 10BASE-T1L Ethernet MAC-PHY	Ultra low power, single port transceiver; compliant with IEEE 802.3cg-2019 Ethernet standard for long reach SPE
ADIN2111	Low complexity, 2-port Ethernet switch with integrated 10BASE-T1L PHYs	Low power, low complexity, two-Ethernet port switch and one SPI port
ADIN1200	Robust, industrial, low power, 10 Mbps and 100 Mbps Ethernet PHY	10BASE-Te/100BASE-TX IEEE 802.3 compliant; MII, RMII, and RGMII MAC interfaces
ADIN1300	Robust, industrial, low latency and low power 10 Mbps, 100 Mbps, and 1 Gbps Ethernet PHY	10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant; MII, RMII, and RGMII MAC interfaces
LTC4359	Ideal diode controller with reverse input protection	4 V to 80 V operation, –40 V reverse-input protection, low 13 µA shutdown current
LT8641	65 V, 3.5 A synchronous step-down Silent Switcher with 2.5 µA quiescent current	$V_{IN(MIN)}$ = 3 V, $V_{IN(MAX)}$ = 65 V, $V_{OUT(MIN)}$ = 0.81 V, I_Q = 2.5 µA, ISD < 1 µA, 3 mm × 4 mm QFN-18
LTC3630A	6 V, 500 mA synchronous step-down DC/DC converter	V_{IN}: 4 V to 76 V, $V_{OUT(MIN)}$ = 0.8 V, I_Q = 12 µA, ISD = 5 µA, 3 × 5 DFN-16, MSOP-16(12)E
LT8301	42 V_{IN} micropower isolated flyback converter with 65 V/1.2 A switch	Low I_Q Monolithic no-opto flyback 5-lead TSOT-23
ADUM1251	Hot swappable, dual I^2C isolators	Bidirectional I^2C communication, 1000 kHz operation, suitable for hot swap Applications
ADUM162N	Robust 3.0 kV rms six channel digital isolators with fail-safe and two reverse channels	Low propagation delay, 150 Mbps maximum guaranteed data rate

OUTLINE DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

BOTTOM VIEW—EXPOSED PAD



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Figure 63. 48-Lead, 7 mm x 7 mm, Plastic QFN
(05-08-7073)
Dimensions shown in millimeters

Updated: December 03, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC4296AUK-1#PBF	−40°C to +125°C	48-Lead Plastic QFN (7 mm × 7 mm)	Tray, 260	05-08-7073

[1] LTC4296AUK-1#PBF is a RoHS compliant part.

OUTLINE DIMENSIONS

EVALUATION BOARDS

Table 25. Evaluation Boards

Model[1]	Description
EVAL-SPoE-KIT-AZ	Evaluation Board Kit Featuring the LTC4296-1

[1] Z = RoHS-Compliant Part.