

FEATURES

- 10-bit temperature-to-digital converter
- 10-bit 8-channel ADC
- DC input bandwidth
- Input range: 0 V to 2.25 V, and 0 V to V_{DD}
- Temperature range: -40°C to +120°C
- Temperature sensor accuracy of ±0.5°C
- Supply range: 2.7 V to 5.5 V
- Power-down current 1 µA
- Internal 2.25 V_{REF} option
- Double-buffered input logic
- I²C, SPI, QSPI™, MICROWIRE™, and DSP compatible
- 4-wire serial interface
- SMBus packet error checking (PEC) compatible
- 16-lead QSOP package

APPLICATIONS

- Portable battery-powered instruments
- Personal computers
- Smart battery chargers
- Telecommunications systems electronic test equipment
- Domestic appliances
- Process control

GENERAL DESCRIPTION

The ADT7411 combines a 10-bit temperature-to-digital converter and a 10-bit 8-channel ADC in a 16-lead QSOP package. This includes a band gap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of 0.25°C. The ADT7411 operates from a single 2.7 V to 5.5 V supply. The input voltage on the ADC channels has a range of 0 V to 2.25 V and the input bandwidth is dc. The reference for the ADC channels is derived internally. The ADT7411 provides two serial interface options: a 4-wire serial interface compatible

with SPI, QSPI, MICROWIRE, and DSP interface standards, and a 2-wire SMBus/I²C interface. It features a standby mode that is controlled via the serial interface.

The ADT7411's wide supply voltage range, low supply current, and SPI/I²C compatible interface make it ideal for a variety of applications, including personal computers, office equipment, and domestic appliances.

PIN CONFIGURATION

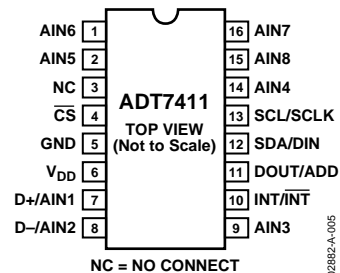


Figure 1.

02882-A-005

*Protected by the following U.S. Patent Numbers: 6,169,442; 5,867,012; 5,764,174. Other patents pending.

Rev. A

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REVISION HISTORY

Revision A

3/04—Data Sheet Changed from Rev. 0 to Rev. A

Format Updated Universal

Change to Equation.....17

8/03—Revision 0: Initial Version

SPECIFICATIONS

Table 1. $V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted. Temperature ranges are $-40^{\circ}\text{C to }+120^{\circ}\text{C}$.

| Parameter ¹ | Min | Typ | Max | Unit | Conditions/Comments |
|---|-----|-----------|-----------|--------------------|---|
| ADC DC ACCURACY | | | | | Max $V_{DD} = 5\text{ V}$. |
| Resolution | | | 10 | Bits | |
| Total Unadjusted Error (TUE) | | 2 | 3 | % of FSR | |
| Offset Error | | | ± 0.5 | % of FSR | |
| Gain Error | | | ± 2 | % of FSR | |
| ADC BANDWIDTH | | | DC | Hz | |
| ANALOG INPUTS | | | | | |
| Input Voltage Range | 0 | | 2.25 | V | AIN1 to AIN8. C4 = 0 in Control Configuration 3. |
| | 0 | | V_{DD} | V | AIN1 to AIN8. C4 = 1 in Control Configuration 3. |
| DC Leakage Current | | | ± 1 | μA | |
| Input Capacitance | | 5 | 20 | pF | |
| Input Resistance | | 10 | | M Ω | |
| THERMAL CHARACTERISTICS | | | | | Internal reference used. Averaging on. |
| Internal Temperature Sensor | | | | | |
| Accuracy @ $V_{DD} = 3.3\text{ V} \pm 10\%$ | | | ± 1.5 | $^{\circ}\text{C}$ | $T_A = 85^{\circ}\text{C}$. |
| | | ± 0.5 | ± 3 | $^{\circ}\text{C}$ | $T_A = 0^{\circ}\text{C to }85^{\circ}\text{C}$. |
| | | ± 2 | ± 5 | $^{\circ}\text{C}$ | $T_A = -40^{\circ}\text{C to }+120^{\circ}\text{C}$. |
| Accuracy @ $V_{DD} = 5\text{ V} \pm 5\%$ | | ± 2 | ± 3 | $^{\circ}\text{C}$ | $T_A = 0^{\circ}\text{C to }85^{\circ}\text{C}$. |
| | | ± 3 | ± 5 | $^{\circ}\text{C}$ | $T_A = -40^{\circ}\text{C to }+120^{\circ}\text{C}$. |
| Resolution | | | 10 | Bits | Equivalent to 0.25°C . |
| Long-term Drift | | 0.25 | | $^{\circ}\text{C}$ | Drift over 10 years if part is operated at 55°C . |
| External Temperature Sensor | | | | | External transistor = 2N3906. |
| Accuracy @ $V_{DD} = 3.3\text{ V} \pm 10\%$ | | | ± 1.5 | $^{\circ}\text{C}$ | $T_A = 85^{\circ}\text{C}$. |
| | | | ± 3 | $^{\circ}\text{C}$ | $T_A = 0^{\circ}\text{C to }85^{\circ}\text{C}$. |
| | | | ± 5 | $^{\circ}\text{C}$ | $T_A = -40^{\circ}\text{C to }+120^{\circ}\text{C}$. |
| Accuracy @ $V_{DD} = 5\text{ V} \pm 5\%$ | | ± 2 | ± 3 | $^{\circ}\text{C}$ | $T_A = 0^{\circ}\text{C to }85^{\circ}\text{C}$. |
| | | ± 3 | ± 5 | $^{\circ}\text{C}$ | $T_A = -40^{\circ}\text{C to }+120^{\circ}\text{C}$. |
| Resolution | | | 10 | Bits | Equivalent to 0.25°C . |
| Output Source Current | | 180 | | μA | High Level. |
| | | 11 | | μA | Low Level. |
| CONVERSION TIMES | | | | | Single-channel Mode. |
| Slow ADC | | | | | |
| V_{DD}/AIN | | 11.4 | | ms | Averaging (16 samples) on. |
| | | 712 | | μs | Averaging off. |
| Internal Temperature | | 11.4 | | ms | Averaging (16 samples) on. |
| | | 712 | | μs | Averaging off. |
| External Temperature | | 24.22 | | ms | Averaging (16 samples) on. |
| | | 1.51 | | ms | Averaging off. |
| Fast ADC | | | | | |
| V_{DD}/AIN | | 712 | | μs | Averaging (16 samples) on. |
| | | 44.5 | | μs | Averaging off. |
| Internal Temperature | | 2.14 | | ms | Averaging (16 samples) on. |
| | | 134 | | μs | Averaging off. |
| External Temperature | | 14.25 | | ms | Averaging (16 samples) on. |
| | | 890 | | μs | Averaging off. |

¹ See the Terminology section.

ADT7411

| Parameter ¹ | Min | Typ | Max | Unit | Conditions/Comments |
|---|------|--------|-----|--------|--|
| ROUND ROBIN UPDATE RATE ² | | | | | Time to complete one measurement cycle through all channels. |
| Slow ADC @ 25°C | | | | | |
| Averaging On | | 125.4 | | ms | AIN1 and AIN2 are selected on Pins 7 and 8. |
| Averaging Off | | 17.1 | | ms | AIN1 and AIN2 are selected on Pins 7 and 8. |
| Averaging On | | 140.36 | | ms | D+ and D- are selected on Pins 7 and 8. |
| Averaging Off | | 12.11 | | ms | D+ and D- are selected on Pins 7 and 8. |
| Fast ADC @ 25°C | | | | | |
| Averaging On | | 9.26 | | ms | AIN1 and AIN2 are selected on Pins 7 and 8. |
| Averaging Off | | 578.96 | | μs | AIN1 and AIN2 are selected on pins 7 and 8. |
| Averaging On | | 24.62 | | ms | D+ and D- are selected on Pins 7 and 8. |
| Averaging Off | | 3.25 | | ms | D+ and D- are selected on Pins 7 and 8. |
| ON-CHIP REFERENCE ³ | | | | | |
| Reference Voltage | | 2.25 | | V | |
| Temperature Coefficient | | 80 | | ppm/°C | |
| DIGITAL INPUTS ^{1,3} | | | | | |
| Input Current | | | ±1 | μA | V _{IN} = 0 V to V _{DD} . |
| V _{IL} , Input Low Voltage | | | 0.8 | V | |
| V _{IH} , Input High Voltage | 1.89 | | | V | |
| Pin Capacitance | | 3 | 10 | pF | All Digital Inputs. |
| SCL, SDA Glitch Rejection | | | 50 | ns | Input filtering suppresses noise spikes of less than 50 ns. |
| DIGITAL OUTPUT | | | | | |
| Output High Voltage, V _{OH} | 2.4 | | | V | I _{SOURCE} = I _{SINK} = 200 μA. |
| Output Low Voltage, V _{OL} | | | 0.4 | V | I _{OL} = 3 mA. |
| Output High Current, I _{OH} | | | 1 | mA | V _{OH} = 5 V. |
| Output Capacitance, C _{OUT} | | | 50 | pF | |
| INT/ $\overline{\text{INT}}$ Output Saturation Voltage | | | 0.8 | V | I _{OUT} = 4 mA. |
| I ² C TIMING CHARACTERISTICS ^{4,5} | | | | | |
| Serial Clock Period, t ₁ | 2.5 | | | μs | Fast-Mode I ² C. See Figure 2. |
| Data In Setup Time to SCL High, t ₂ | 50 | | | ns | |
| Data Out Stable after SCL Low, t ₃ | 0 | | | ns | See Figure 2. |
| SDA Low Setup Time to SCL Low (Start Condition), t ₄ | 50 | | | ns | See Figure 2. |
| SDA High Hold Time after SCL High (Stop Condition), t ₅ | 50 | | | ns | See Figure 2. |
| SDA and SCL Fall Time, t ₆ | | | 90 | ns | See Figure 2. |
| SPI TIMING CHARACTERISTICS ^{1,3,6} | | | | | |
| $\overline{\text{CS}}$ to SCLK Setup Time, t ₁ | 0 | | | ns | See Figure 3. |
| SCLK High Pulse Width, t ₂ | 50 | | | ns | See Figure 3. |
| SCLK Low Pulse Width, t ₃ | 50 | | | ns | See Figure 3. |
| Data Access Time after SCLK Falling Edge, t ₄ ⁶ | | | 35 | ns | See Figure 3. |
| Data Setup Time Prior to SCLK Rising Edge, t ₅ | 20 | | | ns | See Figure 3. |
| Data Hold Time after SCLK Rising Edge, t ₆ | 0 | | | ns | See Figure 3. |

² Round robin is the continuous sequential measurement of the following channels: V_{DD}, internal temperature, external temperature (AIN1, AIN2), AIN3, AIN4, AIN5, AIN6, AIN7, and AIN8.

³ Guaranteed by design and characterization, not production tested.

⁴ The SDA and SCL timing is measured with the input filters turned on so as to meet the FAST-Mode I²C specification. Switching off the input filters improves the transfer rate, but has a negative effect on the EMC behavior of the part.

⁵ Guaranteed by design. Not tested in production.

⁶ All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}), and timed from a voltage level of 1.6 V.

| Parameter ¹ | Min | Typ | Max | Unit | Conditions/Comments |
|--|-----|-----|-----|---------------|---|
| $\overline{\text{CS}}$ to SCLK Hold Time, t_7 | 0 | | | ns | See Figure 3. |
| $\overline{\text{CS}}$ to DOUT High Impedance, t_8 | | | 40 | ns | See Figure 3. |
| POWER REQUIREMENTS | | | | | |
| V_{DD} | 2.7 | | 5.5 | V | |
| V_{DD} Settling Time | | | 50 | ms | V_{DD} settles to within 10% of its final voltage level. |
| I_{DD} (Normal Mode) ⁷ | | | 3 | mA | $V_{\text{DD}} = 3.3\text{ V}$, $V_{\text{IH}} = V_{\text{DD}}$ and $V_{\text{IL}} = \text{GND}$. |
| | | 2.2 | 3 | mA | $V_{\text{DD}} = 5\text{ V}$, $V_{\text{IH}} = V_{\text{DD}}$ and $V_{\text{IL}} = \text{GND}$. |
| I_{DD} (Power-Down Mode) | | | 10 | μA | $V_{\text{DD}} = 3.3\text{ V}$, $V_{\text{IH}} = V_{\text{DD}}$ and $V_{\text{IL}} = \text{GND}$. |
| | | | 10 | μA | $V_{\text{DD}} = 5\text{ V}$, $V_{\text{IH}} = V_{\text{DD}}$ and $V_{\text{IL}} = \text{GND}$. |
| Power Dissipation | | | 10 | mW | $V_{\text{DD}} = 3.3\text{ V}$. Using normal mode. |
| | | | 33 | μW | $V_{\text{DD}} = 3.3\text{ V}$. Using shutdown mode. |

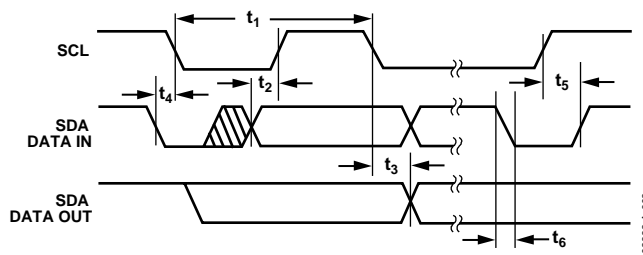


Figure 2. I²C Bus Timing Diagram

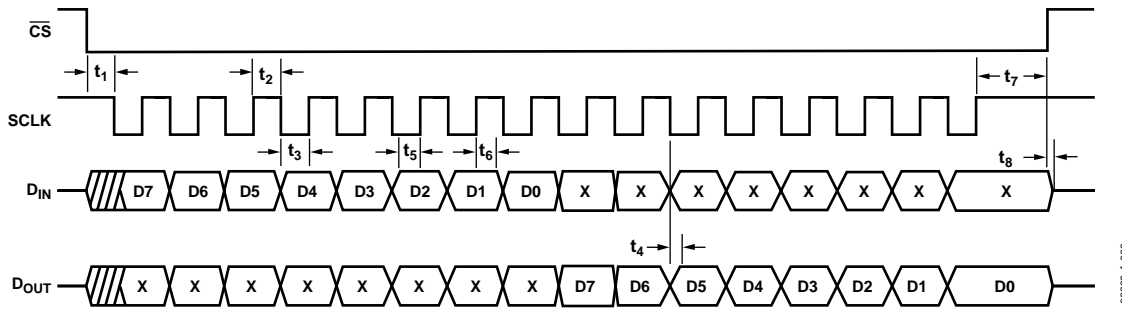


Figure 3. SPI Bus Timing Diagram

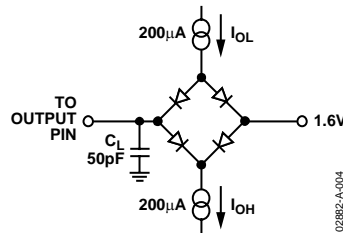


Figure 4. Load Circuit for Access Time and Bus Relinquish Time

⁷ I_{DD} specification is valid for full-scale analog input voltages. Interface inactive. ADC active. Load currents excluded.

FUNCTIONAL BLOCK DIAGRAM

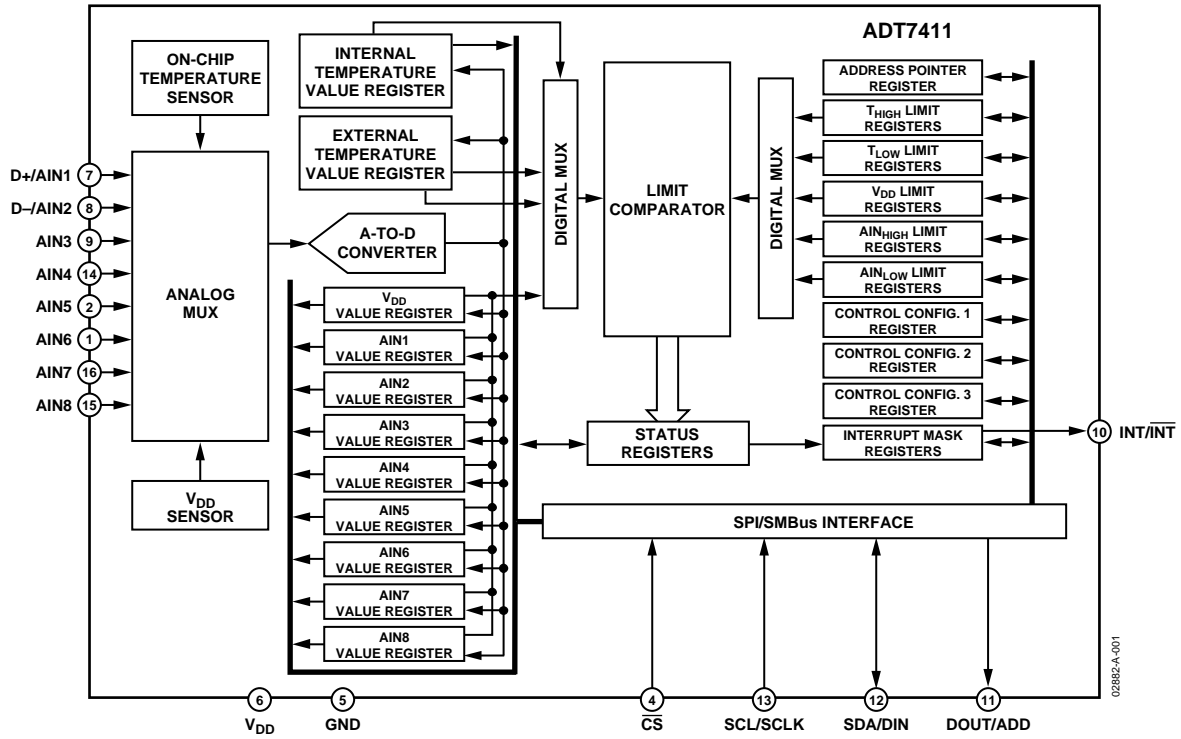


Figure 5. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|-------------------------------------|--|
| V _{DD} to GND | −0.3 V to +7 V |
| Analog Input Voltage to GND | −0.3 V to V _{DD} + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to V _{DD} + 0.3 V |
| Operating Temperature Range | −40°C to +120°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| 16-Lead QSOP Package | |
| Power Dissipation ⁸ | (T _{Jmax} − TA)/θ _{JA} |
| Thermal Impedance ⁹ | |
| θ _{JA} Junction-to-Ambient | 105.44°C/W |
| θ _{JC} Junction-to-Case | 38.8°C/W |
| IR Reflow Soldering | |
| Peak Temperature | 220°C (0°C/5°C) |
| Time at Peak Temperature | 10 sec to 20 sec |
| Ramp-Up Rate | 2°C/sec to 3°C/sec |
| Ramp-Down Rate | −6°C/sec |

⁸ Values relate to package being used on a 4-layer board

⁹ Junction-to-case resistance is applicable to components featuring a preferential flow direction, e.g., components mounted on a heat sink. Junction-to-ambient resistance is more useful for air-cooled PCB-mounted components.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electro-static discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 3. I²C Address Selection

| ADD Pin | I ² C Address |
|---------|--------------------------|
| Low | 1001 000 |
| Float | 1001 010 |
| High | 1001 011 |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTION

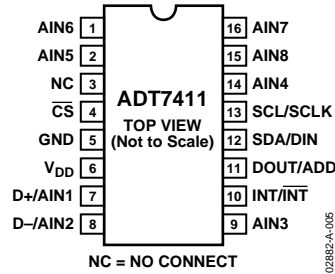


Figure 6. Pin Configuration

Table 4. Pin Function Description

| Pin No. | Mnemonic | Description |
|---------|-----------------------|---|
| 1 | AIN6 | Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD} . |
| 2 | AIN5 | Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD} . |
| 3 | NC | No Connection to This Pin. |
| 4 | \overline{CS} | SPI—Active Low Control Input. This is the frame synchronization signal for the input data. When \overline{CS} goes low, it enables the input register and data is transferred in on the rising edges and out on the falling edges of the subsequent serial clocks. It is recommended that this pin be tied high to V_{DD} when operating the serial interface in I ² C mode. |
| 5 | GND | Ground Reference Point for All Circuitry on the Part. Analog and digital ground. |
| 6 | V_{DD} | Positive Supply Voltage, 2.7 V to 5.5 V. The supply should be decoupled to ground. |
| 7 | D+/AIN | D+. Positive connection to external temperature sensor. AIN1. Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to 5 V. |
| 8 | D-/AIN2 | D-. Negative connection to external temperature sensor. AIN2. Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to 5 V. |
| 9 | AIN3 | Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD} . |
| 10 | INT/ \overline{INT} | Over Limit Interrupt. The output polarity of this pin can be set to give an active low or active high interrupt when temperature, V_{DD} , or AIN limits are exceeded. Default is active low. Open-drain output, needs a pull-up resistor. |
| 11 | DOUT/ADD | SPI. Serial Data Output. Logic output. Data is clocked out of any register at this pin. Data is clocked out on the falling edge of SCLK. Open-drain output, needs a pull-up resistor. ADD. I ² C serial bus address selection pin. Logic input. A low on this pin gives the Address 1001 000. Leaving it floating gives the address 1001 010, and setting it high gives the Address 1001 011. The I ² C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. Any subsequent changes on this pin will have no effect on the I ² C serial bus address. |
| 12 | SDA/DIN | SDA. I ² C serial data input. I ² C serial data to be loaded into the part's registers is provided on this input. An open-drain configuration, it needs a pull-up resistor. DIN. SPI serial data input. Serial data to be loaded into the part's registers is provided on this input. Data is clocked into a register on the rising edge of SCLK. Open-drain configuration, needs a pull-up resistor. |
| 13 | SCL/SCLK | Serial Clock Input. This is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7411 and also to clock data into any register that can be written to. An open-drain configuration, it needs a pull-up resistor. |
| 14 | AIN4 | Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD} . |
| 15 | AIN8 | Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD} . |
| 16 | AIN7 | Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD} . |

TERMINOLOGY

Relative Accuracy

Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the ADC transfer function. A typical INL versus code plot can be seen in Figure 10.

Total Unadjusted Error (TUE)

Total unadjusted error is a comprehensive specification that includes the sum of the relative accuracy error, gain error, and offset error under a specified set of conditions.

Offset Error

This is a measure of the offset error of the ADC. It can be negative or positive. It is expressed in mV.

Gain Error

This is a measure of the span error of the ADC. It is the deviation in slope of the actual ADC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Offset Error Drift

This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Long-term Temperature Drift

This is a measure of the change in temperature error with the passage of time. It is expressed in degrees Celsius. The concept of long-term stability has been used for many years to describe by what amount an IC's parameter would shift during its lifetime. This is a concept that has been typically applied to both voltage references and monolithic temperature sensors. Unfortunately, integrated circuits cannot be evaluated at room temperature (25°C) for 10 years or so to determine this shift. As a result, manufacturers typically perform accelerated lifetime testing of integrated circuits by operating ICs at elevated temperatures (between 125°C and 150°C) over a shorter period of time (typically, between 500 and 1,000 hours). As a result of this operation, the lifetime of an integrated circuit is significantly accelerated due to the increase in rates of reaction within the semiconductor material.

DC Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio (PSRR) is defined as the ratio of the power in the ADC output at full-scale frequency f , to the power of a 100 mV sine wave applied to the V_{DD} supply of frequency f_s :

$$PSRR (dB) = 10 \log (P_f / P_{f_s})$$

P_f = power at frequency f in ADC output

P_{f_s} = power at frequency f_s coupled into the V_{DD} supply

Round Robin

This term is used to describe the ADT7411 cycling through the available measurement channels in sequence, taking a measurement on each channel.

TYPICAL PERFORMANCE CHARACTERISTICS

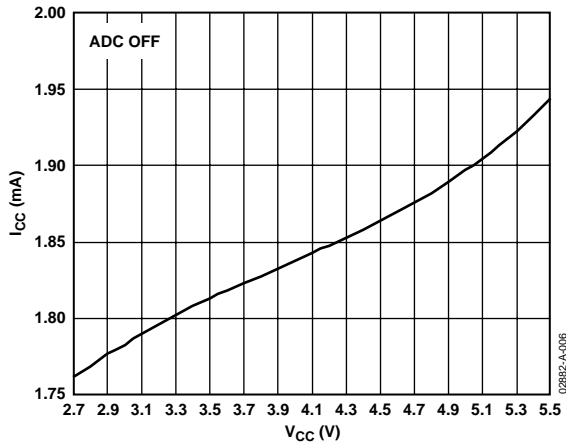


Figure 7. Supply Current vs. Supply Voltage at 25°C

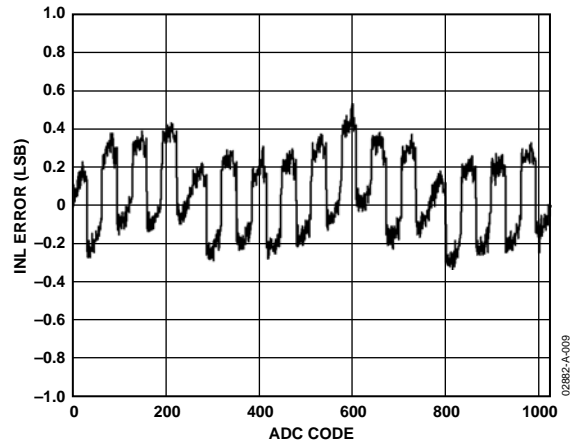


Figure 10. ADC INL with Ref = V_{DD} (3.3V)

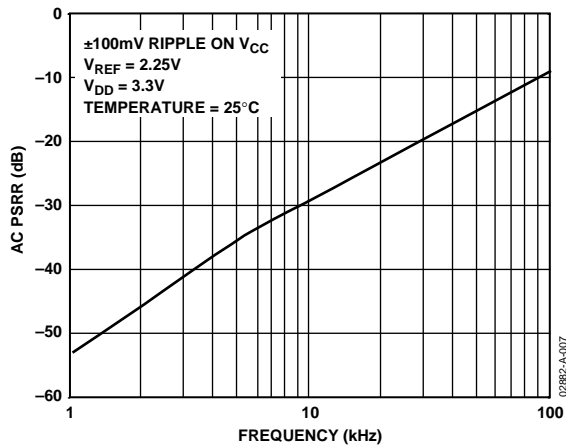


Figure 8. PSRR vs. Supply Ripple Frequency

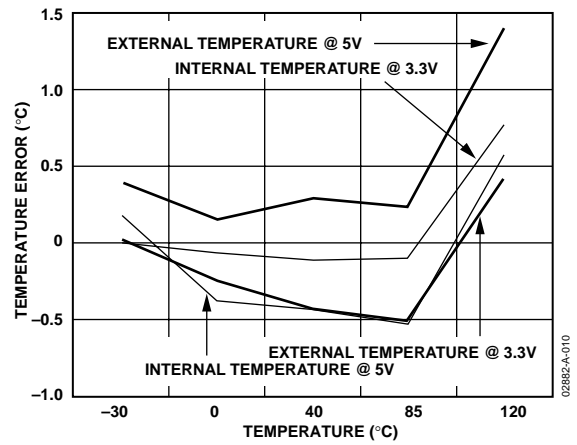


Figure 11. Temperature Error at 3.3V and 5V

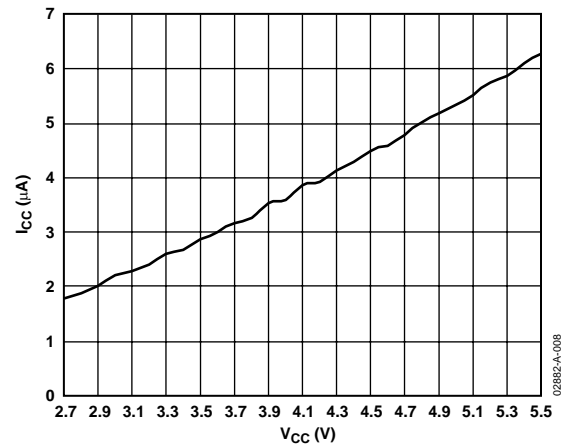


Figure 9. Power-Down Current vs. Supply Voltage at 25°C

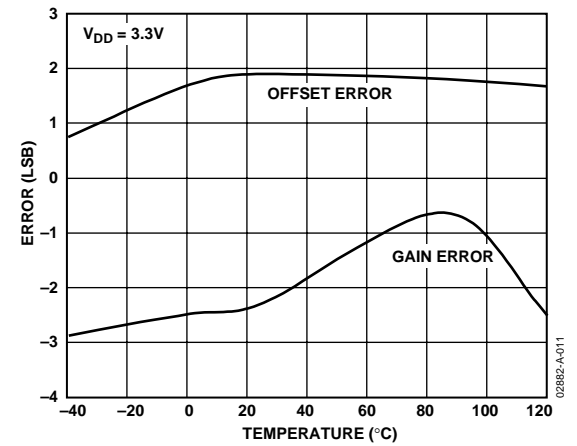


Figure 12. ADC Offset Error and Gain Error vs. Temperature

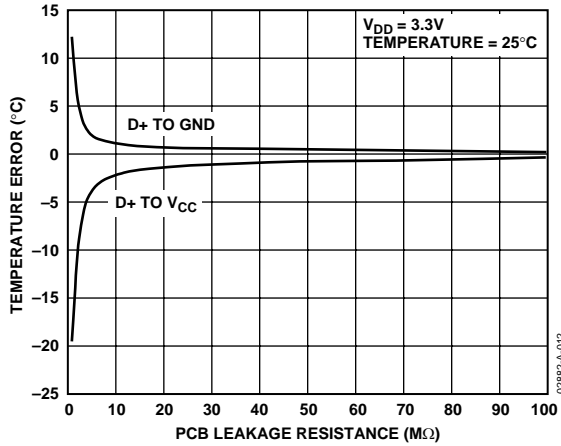


Figure 13. External Temperature Error vs. PCB Track Resistance

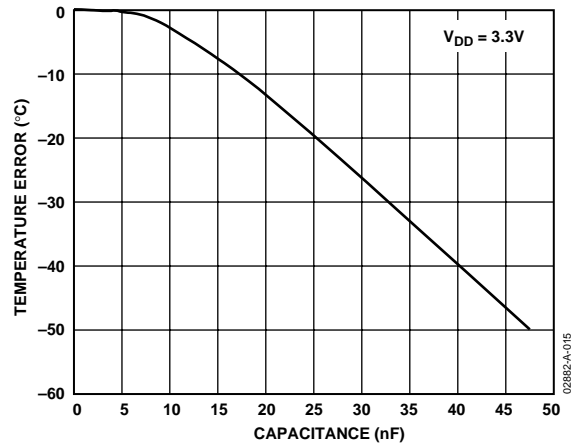


Figure 16. External Temperature Error vs. Capacitance between D+ and D-

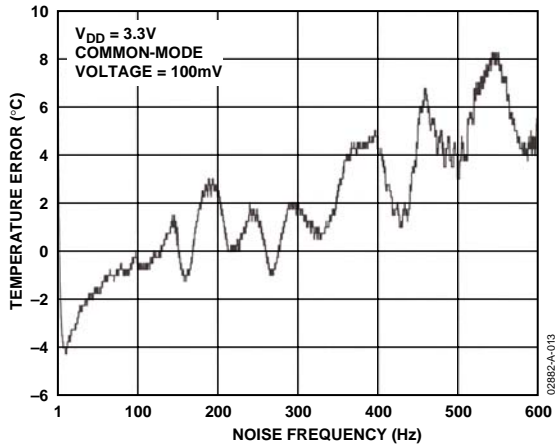


Figure 14. External Temperature Error vs. Common-Mode Noise Frequency

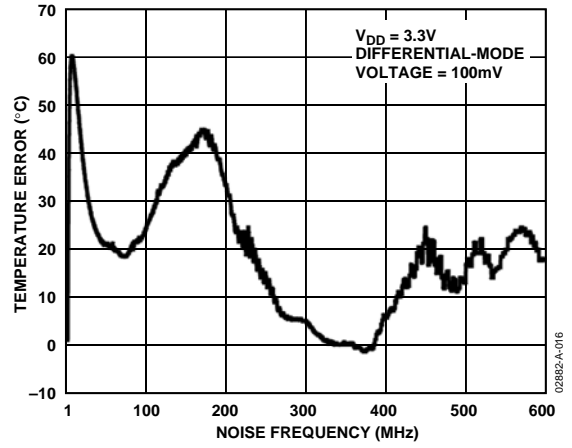


Figure 17. External Temperature Error vs. Differential Mode Noise Frequency

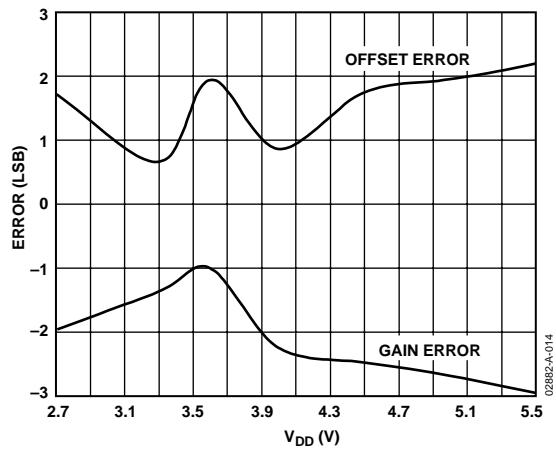


Figure 15. ADC Offset Error and Gain Error vs. V_{DD}

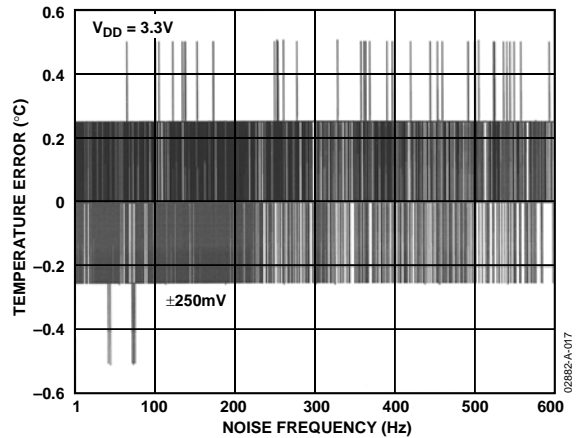


Figure 18. Internal Temperature Error vs. Power Supply Noise Frequency

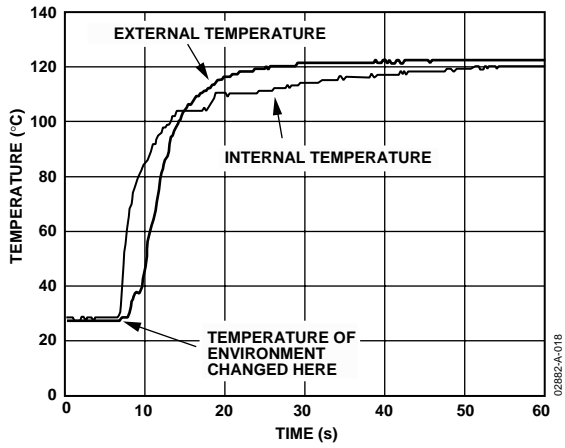


Figure 19. Temperature Sensor Response to Thermal Shock

THEORY OF OPERATION

Directly after the power-up calibration routine, the ADT7411 goes into idle mode. In this mode, the device is not performing any measurements and is fully powered up.

To begin monitoring, write to the Control Configuration 1 register (Address 18h) and set Bit C0 = 1. The ADT7411 goes into its power-up default measurement mode, which is round robin. The device proceeds to take measurements on the V_{DD} channel, internal temperature sensor channel, external temperature sensor channel, or AIN1 and AIN2, AIN3, AIN4, AIN5, AIN6, AIN7, and finally AIN8. Once it finishes taking measurements on the AIN8 channel, the device immediately loops back to start taking measurements on the V_{DD} channel and repeats the same cycle as before. This loop continues until the monitoring is stopped by resetting Bit C0 of the Control Configuration 1 register to 0. It is also possible to continue monitoring as well as switching to single-channel mode by writing to the Control Configuration 2 register (Address 19h) and setting Bit C4 = 1. Further explanations of the single-channel and round robin measurement modes are given in later sections. All measurement channels have averaging enabled on them at power-up. Averaging forces the device to take an average of 16 readings before giving a final measured result. To disable averaging and consequently decrease the conversion time by a factor of 16, set C5 = 1 in the Control Configuration 2 register.

There are eight single-ended analog input channels on the ADT7411: AIN1 to AIN8. AIN1 and AIN2 are multiplexed with the external temperature sensors D+ and D- terminals. Bits C1 and C2 of the Control Configuration 1 register (Address 18h) are used to select between AIN1/2 and the external temperature sensor. The input range on the analog input channels is dependent on whether the ADC reference used is the internal V_{REF} or V_{DD} . To meet linearity specifications, it is recommended that the maximum V_{DD} value is 5 V. Bit C4 of the Control Configuration 3 register is used to select between the internal reference and V_{DD} as the analog inputs' ADC reference.

The dual serial interface defaults to the I²C protocol on power-up. To select and lock in the SPI protocol, follow the selection process as described in the Serial Interface Selection section. The I²C protocol cannot be locked in, while the SPI protocol on selection is automatically locked in. The interface can only be switched back to I²C when the device is powered off and on. When using I²C, the \overline{CS} pin should be tied to either V_{DD} or GND.

There are a number of different operating modes on the ADT7411 devices and all of them can be controlled by the configuration registers. These features consist of enabling and disabling interrupts, polarity of the INT/ \overline{INT} pin, enabling and disabling the averaging on the measurement channels, SMBus timeout, and software reset.

POWER-UP CALIBRATION

It is recommended that no communication to the part is initiated until approximately 5 ms after V_{DD} has settled to within 10% of its final value. It is generally accepted that most systems take a maximum of 50 ms to power up. Power-up time is directly related to the amount of decoupling on the voltage supply line.

During the 5 ms after V_{DD} has settled the part is performing a calibration routine; any communication to the device will interrupt this routine and could cause erroneous temperature measurements. If it is not possible to have V_{DD} at its nominal value by the time 50 ms has elapsed or that communication to the device has started prior to V_{DD} settling, then it is recommended that a measurement be taken on the V_{DD} channel before a temperature measurement is taken. The V_{DD} measurement is used to calibrate out any temperature measurement error due to different supply voltage values.

CONVERSION SPEED

The internal oscillator circuit used by the ADC has the capability to output two different clock frequencies. This means that the ADC is capable of running at two different speeds when doing a conversion on a measurement channel. Thus the time taken to perform a conversion on a channel can be reduced by setting C0 of the Control Configuration 3 register (Address 1Ah). This increases the ADC clock speed from 1.4 kHz to 22 kHz. At the higher clock speed, the analog filters on the D+ and D- input pins (external temperature sensor) are switched off. This is why the power-up default setting is to have the ADC working at the slow speed. The typical times for fast and slow ADC speeds are given in the specification pages.

The ADT7411 powers up with averaging on. This means every channel is measured 16 times and internally averaged to reduce noise. The conversion time can also be reduced by turning the averaging off. This is done by setting Bit C5 of the Control Configuration 2 register (Address 19h) to a 1.

FUNCTIONAL DESCRIPTION

ANALOG INPUTS

Single-Ended Inputs

The ADT7411 offers eight single-ended analog input channels. The analog input range is from 0 V to 2.25 V or 0 V to V_{DD} . To maintain the linearity specification it is recommended that the maximum V_{DD} value be set at 5 V. Selection between the two input ranges is done by Bit C4 of the Control Configuration 3 register (Address 1Ah). Setting this bit to 0 sets up the analog input ADC reference to be sourced from the internal voltage reference of 2.25 V. Setting the bit to 1 sets up the ADC reference to be sourced from V_{DD} .

The ADC resolution is 10 bits and is mostly suitable for dc input signals or very slowly varying ac signals. Bits C1:2 of the Control Configuration 1 register (Address 18h) are used to set up Pins 7 and 8 as AIN1 and AIN2. Figure 20 shows the overall view of the 8-channel analog input path.

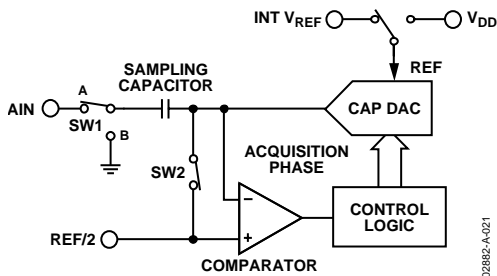


Figure 20. Octal Analog Input Path

Converter Operation

The analog input channels use a successive approximation ADC based around a capacitor DAC. Figure 21 and Figure 22 show simplified schematics of the ADC. Figure 21 shows the ADC during acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on AIN.

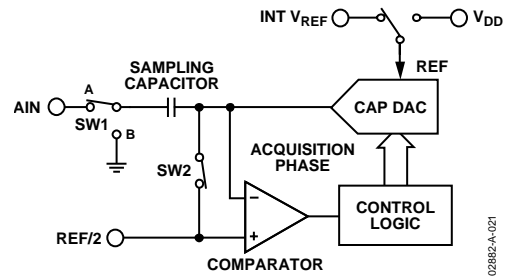


Figure 21. ADC Acquisition Phase

When the ADC eventually goes into conversion phase (see Figure 22) SW2 opens and SW1 moves to position B, causing the comparator to become unbalanced. The control logic and the DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 24 shows the ADC transfer function for single-ended analog inputs.

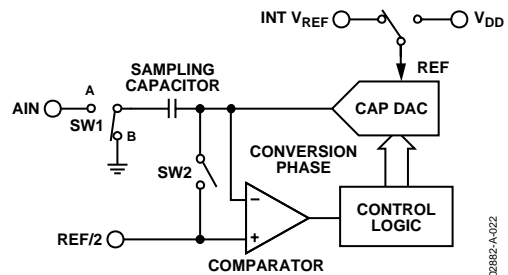


Figure 22. ADC Conversion Phase

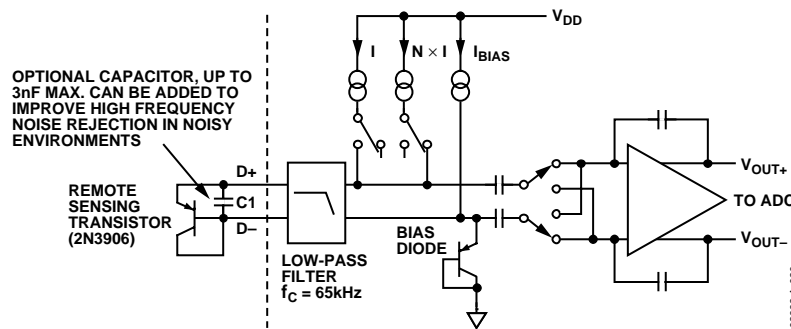


Figure 23. Signal Conditioning for External Diode Temperature Sensor

ADC Transfer Function

The output coding of the ADT7411 analog inputs is straight binary. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB). The LSB is $V_{DD}/1024$ or $\text{Int } V_{REF}/1024$, $\text{Int } V_{REF} = 2.25 \text{ V}$. The ideal transfer characteristic is shown in Figure 24.

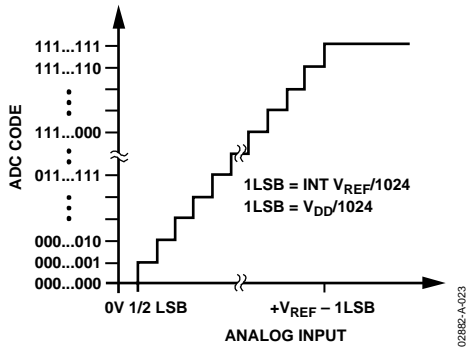


Figure 24. Transfer Function

To work out the voltage on any analog input channel, the following method can be used:

$$1 \text{ LSB} = \text{Reference (V)} / 1024$$

Convert the value read back from the AIN value register into decimal.

$$\text{AINVoltage} = \text{AINValue}(d) \times \text{LSB size}$$

where d = decimal

Example:

Internal reference used. Therefore, $V_{REF} = 2.25 \text{ V}$.

$$\text{AIN value} = 512d$$

$$1 \text{ LSB size} = 2.25 \text{ V} / 1024 = 2.197 \times 10^{-3}$$

$$\begin{aligned} \text{AINVoltage} &= 512 \times 2.197 \times 10^{-3} \\ &= 1.125 \text{ V} \end{aligned}$$

Analog Input ESD Protection

Figure 26 shows the input structure that provides ESD protection on any of the analog input pins. The diode provides the main ESD protection for the analog inputs. Care must be taken that the analog input signal never drops below the GND rail by more than 200 mV. If this happens, the diode will become forward biased and start conducting current into the substrate. The 4 pF capacitor is the typical pin capacitance and the resistor is a lumped component made up of the on resistance of the multiplexer switch.

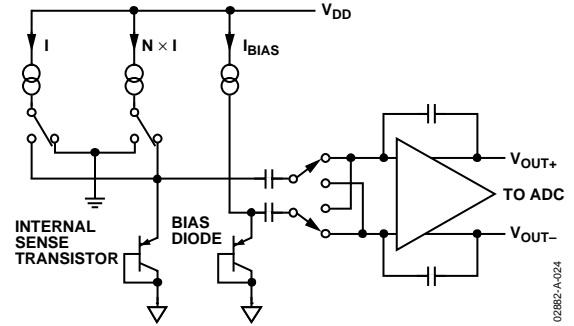


Figure 25. Top Level Structure of Internal Temperature Sensor

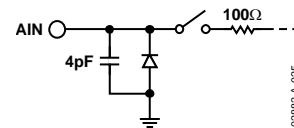


Figure 26. Equivalent Analog Input ESD Circuit

AIN Interrupts

The measured results from the AIN inputs are compared with the AIN V_{HIGH} (greater than comparison) and V_{LOW} (less than or equal to comparison) limits. An interrupt occurs if the AIN inputs exceed or equal the limit registers. These voltage limits are stored in on-chip registers. Note that the limit registers are eight bits long while the AIN conversion result is 10 bits long. If the voltage limits are not masked out, any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register (Address 00h) and one or more out-of-limit results will cause the INT/INT \bar{N} output to pull either high or low, depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application. Figure 27 shows the interrupt structure for the ADT7411. It shows a block diagram representation of how the various measurement channels affect the INT/INT \bar{N} pin.

FUNCTIONAL DESCRIPTION—MEASUREMENT Temperature Sensor

The ADT7411 contains an A/D converter with special input signal conditioning to enable operation with external and on-chip diode temperature sensors. When the ADT7411 is operating in single-channel mode, the A/D converter continually processes the measurement taken on one channel only. This channel is preselected by bits C0:C3 in the Control Configuration 2 register (Address 19h). When in round robin mode the analog input multiplexer sequentially selects the V_{DD} input channel, on-chip temperature sensor to measure its internal temperature, the external temperature sensor, or an AIN channel, and then the rest of the AIN channels. These signals are digitized by the ADC and the results stored in the various value registers.

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The measured results from the temperature sensors are compared with the internal and external, T_{HIGH} , T_{LOW} , limits. These temperature limits are stored in on-chip registers. If the temperature limits are not masked out, any out-of-limit comparisons generate flags that are stored in Interrupt Status 1 register. One or more out-of-limit results will cause the INT/ \overline{INT} output to pull either high or low, depending on the output polarity setting.

Theoretically, the temperature measuring circuit can measure temperatures from -128°C to $+127^{\circ}\text{C}$ with a resolution of 0.25°C . However, temperatures outside T_A are outside the guaranteed operating temperature range of the device. Temperature measurement from -128°C to $+127^{\circ}\text{C}$ is possible using an external sensor.

Temperature measurement is initiated by three methods. The first method is applicable when the part is in single-channel measurement mode. The temperature is measured 16 times and internally averaged to reduce noise. In single-channel mode, the part is continuously monitoring the selected channel, i.e., as soon as one measurement is taken, another one is started on the same channel. The total time to measure a temperature channel with the ADC operating at slow speed is typically 11.4 ms ($712\ \mu\text{s} \times 16$) for the internal temperature sensor and 24.22 ms ($1.51\ \text{ms} \times 16$) for the external temperature sensor. The new

temperature value is stored in two 8-bit registers and ready for reading by the I²C or SPI interface. The user has the option of disabling the averaging by setting Bit 5 in the Control Configuration 2 register (Address 19h). The ADT7411 defaults on power-up with the averaging enabled.

The second method is applicable when the part is in round robin measurement mode. The part measures both the internal and external temperature sensors as it cycles through all possible measurement channels. The two temperature channels are measured each time the part runs a round robin sequence. In round robin mode, the part is continuously measuring all channels.

Temperature measurement is also initiated after every read or write to the part when the part is in either single-channel measurement mode or round robin measurement mode. Once serial communication has started, any conversion in progress is stopped and the ADC is reset. Conversion will start again immediately after the serial communication has finished. The temperature measurement proceeds normally as described previously.

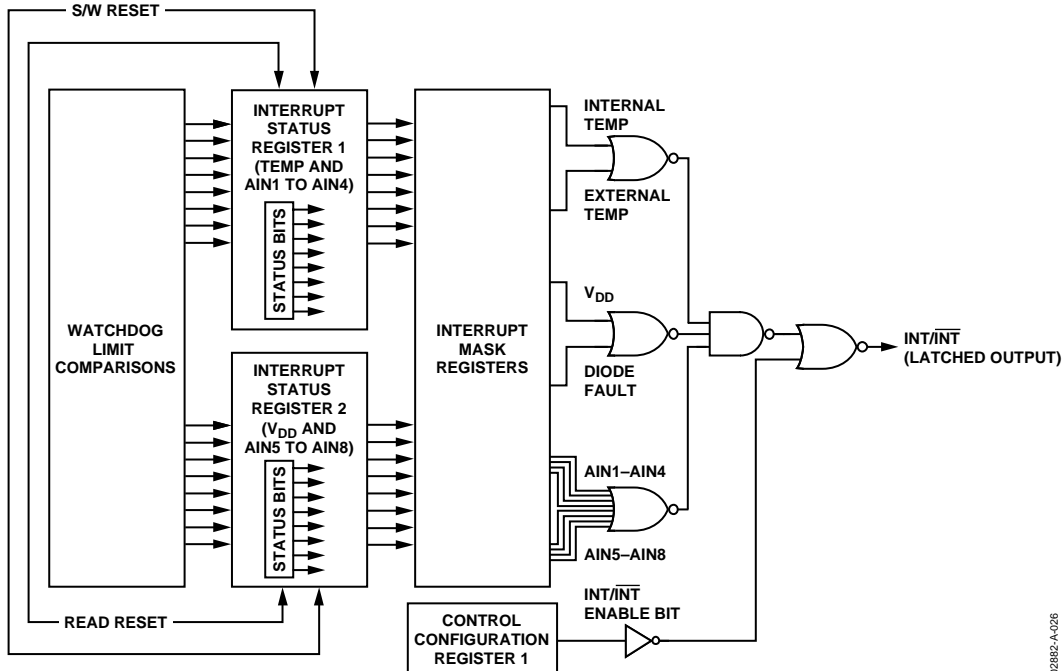


Figure 27. ADT7411 Interrupt Structure

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V_{DD} Monitoring

The ADT7411 also has the capability of monitoring its own power supply. The part measures the voltage on its V_{DD} pin to a resolution of 10 bits. The resulting value is stored in two 8-bit registers, with the 2 LSBs stored in register Address 03h and the 8 MSBs stored in register Address 06h. This allows the user to have the option of just doing a 1-byte read if 10-bit resolution is not important. The measured result is compared with the V_{HIGH} and V_{LOW} limits. If the V_{DD} interrupt is not masked out then any out-of-limit comparison generates a flag in the Interrupt Status 2 register, and one or more out-of-limit results will cause the INT/INT output to pull either high or low, depending on the output polarity setting.

Measuring the voltage on the V_{DD} pin is regarded as monitoring a channel along with the internal, external, and AIN channels. The user can select the V_{DD} channel for single-channel measurement by setting Bit C4 = 1 and setting Bits C0 to C2 to all 0s in the Control Configuration 2 register.

When measuring the V_{DD} value, the reference for the ADC is sourced from the internal reference. Table 5 shows the data format. As the max V_{DD} voltage measurable is 7 V, internal scaling is performed on the V_{DD} voltage to match the 2.25 V internal reference value. The following is an example of how the transfer function works:

$$ADC\ Reference = 2.25\ V$$

$$1\ LSB = ADC\ Reference / 2^{10} = 2.25 / 1024 = 2.197\ mV$$

$$Scale\ Factor = Fullscale\ V_{CC} / ADC\ Reference = 7 / 2.25 = 3.11$$

$$Conversion\ Result = V_{DD} / (Scale\ Factor \times LSB\ Size)$$

$$= 5 / (3.11 \times 2.197\ mV)$$

$$= 2DBh$$

Table 5. V_{DD} Data Format, $V_{REF} = 2.25\ V$

| V_{DD} Value (V) | Digital Output | |
|--------------------------------------|-----------------------|------------|
| | Binary | Hex |
| 2.5 | 01 0110 1110 | 16E |
| 2.7 | 01 1000 1011 | 18B |
| 3.0 | 01 1011 0111 | 1B7 |
| 3.5 | 10 0000 0000 | 200 |
| 4.0 | 10 0100 1001 | 249 |
| 4.5 | 10 1001 0010 | 292 |
| 5.0 | 10 1101 1011 | 2DB |
| 5.5 | 11 0010 0100 | 324 |
| 6.0 | 11 0110 1101 | 36D |
| 6.5 | 11 1011 0110 | 3B6 |
| 7.0 | 11 1111 1111 | 3FF |

On-Chip Reference

The ADT7411 has an on-chip 1.125 V band gap reference that is gained up by a switched capacitor amplifier to give an output of 2.25 V. The amplifier is powered up for the duration of the device monitoring phase and is powered down once monitoring is disabled. This saves on current consumption. The internal reference is used as the reference for the ADC.

Round Robin Measurement

Upon power-up, the ADT7411 goes into round robin mode, but monitoring is disabled. Setting Bit C0 of the Configuration 1 register to 1 enables conversions. It sequences through all available channels, taking a measurement from each in the following order: V_{DD} , internal temperature sensor, external temperature sensor/(AIN1 and AIN2), AIN3, AIN4, AIN5, AIN6, AIN7, and AIN8. Pin 7 and Pin 8 can be configured as either external temperature sensor pins or standalone analog input pins. Once conversion is completed on the AIN8 channel, the device loops around for another measurement cycle. This method of taking a measurement on all the channels in one cycle is called round robin. Setting Bit 4 of the Control Configuration 2 register (Address 19h) disables the round robin mode and in turn sets up the single-channel mode. The single-channel mode is where only one channel, e.g., the internal temperature sensor, is measured in each conversion cycle.

The time taken to monitor all channels will normally not be of interest, as the most recently measured value can be read at any time. For applications where the round robin time is important, typical times at 25°C are given in the specification pages.

Single-Channel Measurement

Setting Bit C4 of the Control Configuration 2 register enables the single-channel mode and allows the ADT7411 to focus on one channel only. A channel is selected by writing to Bits C0:C3 in the Control Configuration 2 register. For example, to select the V_{DD} channel for monitoring, write to the Control Configuration 2 register and set C4 to 1 (if not done so already), then write all 0s to Bits C0 to C3. All subsequent conversions will be done on the V_{DD} channel only. To change the channel selection to the internal temperature channel, write to the Control Configuration 2 register and set C0 = 1. When measuring in single-channel mode, conversions on the channel selected occur directly after each other. Any communication to the ADT7411 stops the conversions, but they are restarted once the read or write operation is completed.

Temperature Measurement Method

Internal Temperature Measurement

The ADT7411 contains an on-chip, band gap temperature sensor whose output is digitized by the on-chip ADC. The temperature data is stored in the internal temperature value register. As both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table 6. The thermal characteristics of the

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measurement sensor could change and therefore an offset is added to the measured value to enable the transfer function to match the thermal characteristics. This offset is added before the temperature data is stored. The offset value used is stored in the internal temperature offset register.

External Temperature Measurement

The ADT7411 can measure the temperature of one external diode sensor or diode-connected transistor.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about $-2 \text{ mV}/^\circ\text{C}$. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass production.

The technique used in the ADT7411 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by:

$$\Delta V_{BE} = KT/q \times \ln(N)$$

where:

K is Boltzmann's constant

q is the charge on the carrier

T is the absolute temperature in Kelvin

N is the ratio of the two currents

Figure 23 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used, the base is connected to the D- input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D- input and the base to the D+ input. A 2N3906 is recommended as the external transistor.

To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D- input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the Layout Considerations section for more information on C1.

To measure ΔV_{BE} , the sensor is switched between operating currents of I, and $N \times I$. The resulting waveform is passed through a low-pass filter to remove noise, then to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE} . This voltage is measured by the ADC to give a temperature output in 10-bit twos complement format. To

further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

Layout Considerations

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADT7411 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses, and CRTs are avoided, this distance can be 4 inches to 8 inches.
2. Route the D+ and D- tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended (see Figure 28).

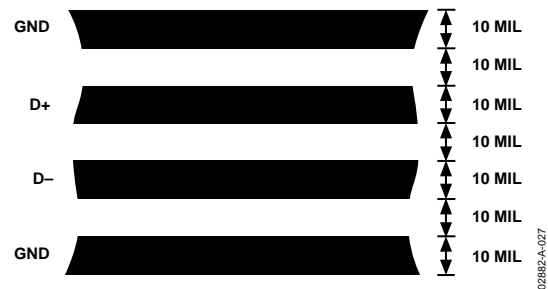


Figure 28. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D- path and at the same temperature.

Thermocouple effects should not be a major problem as 1°C corresponds to about $240 \mu\text{V}$, and thermocouple voltages are about $3 \mu\text{V}/^\circ\text{C}$ of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.

5. Place $0.1 \mu\text{F}$ bypass and 2200 pF input filter capacitors close to the ADT7411.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted-pair cable is recommended. This will work up to about 6 feet to 12 feet.
7. For long distances (up to 100 feet) use shielded twisted-pair cable, such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D- and the shield to GND close to the ADT7411. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. 1 Ω series resistance introduces about 0.5°C error.

Temperature Value Format

One LSB of the ADC corresponds to 0.25°C. The ADC can theoretically measure a temperature span of 255°C. The internal temperature sensor is guaranteed to a low value limit of -40°C. It is possible to measure the full temperature span using the external temperature sensor. The temperature data format is shown in Table 6.

The result of the internal or external temperature measurements is stored as twos complement format in the temperature value registers, and is compared with limits programmed into the internal or external high and low registers.

Table 6. Temperature Data Format (Internal and External Temperature)

| Temperature (°C) | Digital Output |
|------------------|----------------|
| -40 | 11 0110 0000 |
| -25 | 11 1001 1100 |
| -10 | 11 1101 1000 |
| -0.25 | 11 1111 1111 |
| 0 | 00 0000 0000 |
| +0.25 | 00 0000 0001 |
| +10 | 00 0010 1000 |
| +25 | 00 0110 0100 |
| +50 | 00 1100 1000 |
| +75 | 01 0010 1100 |
| +100 | 01 1001 0000 |
| +105 | 01 1010 0100 |
| +125 | 01 1111 0100 |

Temperature Conversion Formula:

$$\text{Positive Temperature} = \text{ADC Code} / 4$$

$$\text{Negative Temperature} = (\text{ADC Code}^* - 512) / 4$$

*DB9 is removed from the ADC Code.

Interrupts

The measured results from the internal temperature sensor, external temperature sensor, VDD pin, and AIN inputs are compared with their THIGH/VHIGH (greater than comparison) and TLOW/VLOW (less than or equal to comparison) limits. An interrupt occurs if the measurement exceeds or equals the limit registers. These limits are stored in on-chip registers. Note that the limit registers are eight bits long while the conversion results are 10 bits long. If the limits are not masked out, then any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register (Address 00h) and the Interrupt

Status 2 register (Address 01h). One or more out-of limit results will cause the INT/ $\overline{\text{INT}}$ output to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application.

Figure 27 shows the interrupt structure for the ADT7411. It gives a block diagram representation of how the various measurement channels affect the INT/ $\overline{\text{INT}}$ pin.

ADT7411 REGISTERS

The ADT7411 contains registers that are used to store the results of external and internal temperature measurements, VDD value measurements, analog input measurements, high and low temperature limits, supply voltage and analog input limits, configure multipurpose pins, and generally control the device. See Table 7 for a detailed description of these registers.

The register map is divided into registers of 8 bits. Each register has its own individual address but some consist of data that is linked with other registers. These registers hold the 10-bit conversion results of measurements taken on the temperature, V_{DD}, and AIN channels. For example, the MSBs of the V_{DD} measurement are stored in Register Address 06h while the two LSBs are stored in Register Address 03h. The link involved between these types of registers is that when the LSB register is read first, the MSB registers associated with that LSB register are locked out to prevent any updates. To unlock these MSB registers the user has only to read any one of them, which will have the effect of unlocking all previously locked out MSB registers. So for the example given above, if Register 03h was read first, MSB Registers 06h and 07h would be locked out to prevent any updates to them. If Register 06h was read this register and Register 07h would be subsequently unlocked.

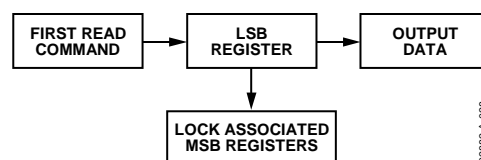


Figure 29. Phase 1 of 10-Bit Read

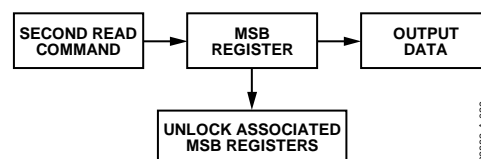


Figure 30. Phase 2 of 10-Bit Read

If an MSB register is read first, its corresponding LSB register is not locked out, thus leaving the user with the option of just reading back 8 bits (MSB) of a 10-bit conversion result. Reading an MSB register first does not lock out other MSB registers, and likewise reading an LSB register first does not lock out other LSB registers.

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Table 7. ADT7411 Registers

| RD/WR Address | Name | Power-On Default |
|---------------|---|------------------|
| 00h | Interrupt Status 1 | 00h |
| 01h | Interrupt Status 2 | 00h |
| 02h | Reserved | |
| 03h | Internal Temp and V _{DD} LSBs | 00h |
| 04h | External Temp and AIN1–4 LSBs | 00h |
| 05h | AIN5–8 LSBs | 00h |
| 06h | V _{DD} MSBs | xxh |
| 07h | Internal Temperature MSBs | 00h |
| 08h | External Temp MSBs/AIN1 MSBs | 00h |
| 09h | AIN2 MSBs | 00h |
| 0Ah | AIN3 MSBs | 00h |
| 0Bh | AIN4 MSBs | 00h |
| 0Ch | AIN5 MSBs | 00h |
| 0Dh | AIN6 MSBs | 00h |
| 0Eh | AIN7 MSBs | 00h |
| 0Fh | AIN8 MSBs | 00h |
| 10h–17h | Reserved | |
| 18h | Control CONFIG 1 | 08h |
| 19h | Control CONFIG 2 | 00h |
| 1Ah | Control CONFIG 3 | 00h |
| 1Bh–1Ch | Reserved | |
| 1Dh | Interrupt Mask 1 | 00h |
| 1Eh | Interrupt Mask 2 | 00h |
| 1Fh | Internal Temp Offset | 00h |
| 20h | External Temp Offset | 00h |
| 21h | Reserved | |
| 22h | Reserved | |
| 23h | V _{DD} V _{HIGH} Limit | C7h |
| 24h | V _{DD} V _{LOW} Limit | 62h |
| 25h | Internal T _{HIGH} Limit | 64h |
| 26h | Internal T _{LOW} Limit | C9h |
| 27h | External T _{HIGH} /AIN1 V _{HIGH} Limits | FFh |
| 28h | External T _{LOW} /AIN1 V _{LOW} Limits | 00h |
| 29h–2Ah | Reserved | |
| 2Bh | AIN2 V _{HIGH} Limit | FFh |
| 2Ch | AIN2 V _{LOW} Limit | 00h |
| 2Dh | AIN3 V _{HIGH} Limit | FFh |
| 2Eh | AIN3 V _{LOW} Limit | 00h |
| 2Fh | AIN4 V _{HIGH} Limit | FFh |
| 30h | AIN4 V _{LOW} Limit | 00h |
| 31h | AIN5 V _{HIGH} Limit | FFh |
| 32h | AIN5 V _{LOW} Limit | 00h |
| 33h | AIN6 V _{HIGH} Limit | FFh |
| 34h | AIN6 V _{LOW} Limit | 00h |
| 35h | AIN7 V _{HIGH} Limit | FFh |
| 36h | AIN7 V _{LOW} Limit | 00h |
| 37h | AIN8 V _{HIGH} Limit | FFh |
| 38h | AIN8 V _{LOW} Limit | 00h |
| 39h–4Ch | Reserved | |
| 4Dh | Device ID | 02h |
| 4Eh | Manufacturer's ID | 41h |
| 4Fh | Silicon Revision | 04h |
| 50h–7Eh | Reserved | 00h |
| 7F | SPI Lock Status | 00h |
| 80h–FFh | Reserved | 00h |

Interrupt Status 1 Register (Read-Only) [Address = 00h]

This 8-bit read-only register reflects the status of some of the interrupts that can cause the INT/INT pin to go active. This register is reset by a read operation, provided that any out-of-limit event has been corrected. It is also reset by a software reset.

Table 8. Interrupt Status 1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Table 9.

| Bit | Function |
|-----|--|
| D0 | 1 when internal temperature value exceeds T _{HIGH} limit. Any internal temperature reading greater than the set limit will cause an out-of-limit event. |
| D1 | 1 when internal temperature value exceeds T _{LOW} limit. Any internal temperature reading less than or equal to the set limit will cause an out-of-limit event. |
| D2 | This status bit is linked to the configuration of pins 7 and 8. If configured for external temperature sensor, this bit is 1 when external temperature value exceeds T _{HIGH} limit. The default value for this limit register is –1°C, so any external temperature reading greater than the limit set will cause an out-of-limit event. If configured for AIN1 and AIN2, this bit is 1 when AIN1 Input Voltage exceeds V _{HIGH} or V _{LOW} limits. |
| D3 | 1 when external temperature value exceeds T _{LOW} limit. The default value for this limit register is 0°C, so any external temperature reading less than or equal to the limit set will cause an out-of-limit event. |
| D4 | 1 indicates a fault (open or short) for the external temperature sensor. |
| D5 | 1 when AIN2 voltage is greater than corresponding V _{HIGH} limit. 1 when AIN2 voltage is less than or equal to corresponding V _{LOW} limit. |
| D6 | 1 when AIN3 voltage is greater than corresponding V _{HIGH} limit. 1 when AIN3 voltage is less than or equal to corresponding V _{LOW} limit. |
| D7 | 1 when AIN4 voltage is greater than corresponding V _{HIGH} limit. 1 when AIN4 voltage is less than or equal to corresponding V _{LOW} limit. |

Interrupt Status 2 Register (Read-Only) [Address = 01h]

This 8-bit read-only register reflects the status of the V_{DD} and AIN5–AIN8 interrupts that can cause the INT/INT pin to go active. This register is reset by a read operation provided that any out-of-limit event has been corrected. It is also reset by a software reset.

Table 10. Interrupt Status 2 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|----|----|----|----|----|
| N/A | N/A | N/A | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Table 11.

| Bit | Function |
|-------|---|
| D0 | 1 when AIN5 voltage is greater than the corresponding V _{HIGH} limit. 1 when AIN5 voltage is less than or equal to the corresponding V _{LOW} limit. |
| D1 | 1 when AIN6 voltage is greater than the corresponding V _{HIGH} limit. 1 when AIN6 voltage is less than or equal to the corresponding V _{LOW} limit. |
| D2 | 1 when AIN7 voltage is greater than the corresponding V _{HIGH} limit. 1 when AIN7 voltage is less than or equal to the corresponding V _{LOW} limit. |
| D3 | 1 when AIN8 voltage is greater than the corresponding V _{HIGH} limit. 1 when AIN8 voltage is less than or equal to the corresponding V _{LOW} limit. |
| D4 | 1 when V _{DD} value is greater than the corresponding V _{HIGH} limit. 1 when V _{DD} is less than or equal to the corresponding V _{LOW} limit. |
| D5:D7 | Reserved |

Internal Temperature Value/V_{DD} Value Register LSBs (Read-Only) [Add. = 03h]

This internal temperature value and V_{DD} value register is an 8-bit read-only register. It stores the 2 LSBs of the 10-bit temperature reading from the internal temperature sensor and also the 2 LSBs of the 10-bit supply voltage reading.

Table 12. Internal Temperature/V_{DD} LSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|----|-----|----|-----|
| N/A | N/A | N/A | N/A | V1 | LSB | T1 | LSB |
| N/A | N/A | N/A | N/A | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Table 13.

| Bit | Function |
|-----|------------------------------------|
| D0 | LSB of Internal Temperature Value. |
| D1 | B1 of Internal Temperature Value. |
| D2 | LSB of V _{DD} Value. |
| D3 | B1 of V _{DD} Value. |

External Temperature Value and Analog Inputs 1 to 4 Register LSBs (Read-Only) [Address = 04h]

This is an 8-bit read-only register. Bits D2–D7 store the 2 LSBs of the analog inputs AIN2–AIN4. Bits D0 and D1 are used to store the 2 LSBs of either the external temperature value or AIN1 input value. The type of input for D0 and D1 is selected by Bits 1:2 of the Control Configuration 1 register.

Table 14. External Temperature and AIN1–4 LSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|-------------------|----|-------------------|----|-------------------|-----|--------------------|
| A4 | A4 _{LSB} | A3 | A3 _{LSB} | A2 | A2 _{LSB} | T/A | T/A _{LSB} |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Table 15

| Bit | Function |
|-----|--|
| D0 | LSB of External Temperature Value or AIN1 Value. |
| D1 | Bit 1 of External Temperature Value or AIN1 Value. |
| D2 | LSB of AIN2 Value. |
| D3 | Bit 1 of AIN2 Value. |
| D4 | LSB of AIN3 Value. |
| D5 | Bit 1 of AIN3 Value. |
| D6 | LSB of AIN4 Value. |
| D7 | Bit 1 of AIN4 Value. |

Analog Inputs 5 to 8 Registers LSBs (Read-Only) [Add. = 05h]

This is an 8-bit read-only register. Bits D0 to D7 store the 2 LSBs of the analog inputs AIN5 to AIN8. The MSBs are stored in Registers 0Ch to 0Fh.

Table 16. External Temperature and AIN5 to AIN8 LSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|-------------------|----|-------------------|----|-------------------|----|-------------------|
| A8 | A8 _{LSB} | A7 | A7 _{LSB} | A6 | A6 _{LSB} | A5 | A5 _{LSB} |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Table 17.

| Bit | Function |
|-----|----------------------|
| D0 | LSB of AIN5 Value. |
| D1 | Bit 1 of AIN5 Value. |
| D2 | LSB of AIN6 Value. |
| D3 | Bit 1 of AIN6 Value. |
| D4 | LSB of AIN7 Value. |
| D5 | Bit 1 of AIN7 Value. |
| D6 | LSB of AIN8 Value. |
| D7 | Bit 1 of AIN8 Value. |

V_{DD} Value Register MSBs (Read-Only) [Address = 06h]

This 8-bit read-only register stores the supply voltage value. The 8 MSBs of the 10-bit value are stored in this register.

Table 18. V_{DD} Value MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| V9 | V8 | V7 | V6 | V5 | V4 | V3 | V2 |
| x* | x* | x* | x* | x* | x* | x* | x* |

*Loaded with V_{DD} value after power-up.

Internal Temperature Value Register MSBs (Read-Only) [Address = 07h]

This 8-bit read-only register stores the internal temperature value from the internal temperature sensor in twos complement format. This register stores the 8 MSBs of the 10-bit value.

Table 19. Internal Temperature Value MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| T9 | T8 | T7 | T6 | T5 | T4 | T3 | T2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

External Temperature Value or Analog Input AIN1 Register MSBs (Read-Only) [Address = 08h]

This 8-bit read-only register stores, if selected, the external temperature value or the analog input AIN1 value. Selection is done in Control Configuration 1 register. The external temperature value is stored in twos complement format. The 8 MSBs of the 10-bit value are stored in this register.

Table 20. External Temperature Value/Analog Inputs MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------|------|------|------|------|------|------|
| T/A9 | T/A8 | T/A7 | T/A6 | T/A5 | T/A4 | T/A3 | T/A2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN2 Register MSBs (Read) [Address = 09h]

This 8-bit read register contains the 8 MSBs of the AIN2 analog input voltage word. The value in this register is combined with Bits D2:3 of the external temperature value and Analog Inputs 1 to 4 register LSBs, Address 04h, to give the full 10-bit conversion result of the analog value on the AIN2 pin.

Table 21. AIN2 MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----|
| MSB | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN3 Register MSBs (Read) [Address = 0Ah]

This 8-bit read register contains the 8 MSBs of the AIN3 analog input voltage word. The value in this register is combined with Bits D4:5 of the external temperature value and Analog Inputs 1 to 4 register LSBs, Address 04h, to give the full 10-bit conversion result of the analog value on the AIN3 pin.

Table 22. AIN3 MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----|
| MSB | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN4 Register MSBs (Read) [Address = 0Bh]

This 8-bit read register contains the 8 MSBs of the AIN4 analog input voltage word. The value in this register is combined with Bits D6:7 of the external temperature value and Analog Inputs 1 to 4 register LSBs, Address 04h, to give the full 10-bit conversion result of the analog value on the AIN4 pin.

Table 23. AIN4 MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----|
| MSB | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN5 Register MSBs (Read) [Address = 0Ch]

This 8-bit read register contains the 8 MSBs of the AIN5 analog input voltage word. The value in this register is combined with Bits D0:1 of the Analog Inputs 5 to 8 register LSBs, Address 05h,

to give the full 10-bit conversion result of the analog value on the AIN5 pin.

Table 24. AIN5 MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----|
| MSB | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN6 Register MSBs (Read) [Address = 0Dh]

This 8-bit read register contains the 8 MSBs of the AIN6 analog input voltage word. The value in this register is combined with Bits D2:3 of the Analog Inputs 5 to 8 register LSBs, Address 05h, to give the full 10-bit conversion result of the analog value on the AIN6 pin.

Table 25. AIN6 MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----|
| MSB | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN7 Register MSBs (Read) [Address = 0Eh]

This 8-bit read register contains the 8 MSBs of the AIN7 analog input voltage word. The value in this register is combined with Bits D4:5 of the Analog Inputs 5 to 8 register LSBs, Address 05h, to give the full 10-bit conversion result of the analog value on the AIN7 pin.

Table 26. AIN7 MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----|
| MSB | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN8 Register MSBs (Read) [Address = 0Fh]

This 8-bit read register contains the 8 MSBs of the AIN8 analog input voltage word. The value in this register is combined with Bits D6:7 of the Analog Inputs 5 to 8 register LSBs, Address 05h, to give the full 10-bit conversion result of the analog value on the AIN8 pin.

Table 27. AIN8 MSBs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----|----|----|----|----|----|----|
| MSB | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Control Configuration 1 Register (Read/Write) [Address = 18h]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7411.

Table 28. Control Configuration 1

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| PD | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 0* | 0* | 0* | 0* | 1* | 0* | 0* | 0* |

*Default settings at power-up.

Table 29.

| Bit | Function |
|-------|---|
| C0 | This bit enables/disables conversions in round robin and single-channel mode. ADT7411 powers up in round robin mode, but monitoring is not initiated until this bit is set. Default = 0. 0 = Stop monitoring. 1 = Start monitoring. |
| C2:C1 | Selects between the two different analog inputs on Pins 7 and 8. The ADT7411 powers up with AIN1 and AIN2 selected. 00: AIN1 and AIN2 selected. 01: Undefined. 10: External TDM selected. 11: Undefined. |
| C3 | Reserved. Write 1 only to this bit. |
| C4 | Reserved. Write 0 only. |
| C5 | 0: Enable INT/ $\overline{\text{INT}}$ output. 1: Disable INT/ $\overline{\text{INT}}$ output. |
| C6 | Configures INT/ $\overline{\text{INT}}$ output polarity. 0: Active low. 1: Active high. |
| PD | Power-Down Bit. Setting this bit to 1 puts the ADT7411 into standby mode. In this mode, the analog circuitry is fully powered down, but the serial interface is still operational. To power up the part again, write 0 to this bit. |

Control Configuration 2 Register (Read/Write)
[Address = 19h]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7411.

Table 30. Control Configuration 2

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Table 31.

| Bit | Function |
|------|---|
| C3:0 | In single-channel mode, these bits select between V_{DD} , the internal temperature sensor, external temperature sensor/AIN1, AIN2 to AIN8 for conversion. The default is V_{DD} . 0000 = V_{DD} . 0001 = Internal Temperature Sensor. 0010 = External Temperature Sensor/AIN1. (Bits C1:C2 of Control Configuration 1 affect this selection.) 0011 = AIN2. 0100 = AIN3. 0101 = AIN4. 0110 = AIN5. 0111 = AIN6. 1000 = AIN7. 1001 = AIN8. |

| Bit | Function |
|-----|---|
| | 1010 to 1111 = Reserved. |
| C4 | Selects between single-channel and round robin conversion cycle. Default is round robin. 0 = Round robin. 1 = Single-channel. |
| C5 | Default condition is to average every measurement on all channels 16 times. This bit disables this averaging. Channels affected are temperature, analog inputs, and V_{DD} . 0 = Enable averaging. 1 = Disable averaging. |
| C6 | SMBus timeout on the serial clock puts a 25 ms limit on the pulse width of the clock, ensuring that a fault on the master SCL does not lock up the SDA line. 0 = Disable SMBus timeout. 1 = Enable SMBus timeout. |
| C7 | Software Reset. Setting this bit to a 1 causes a software reset. All registers will reset to their default settings. |

Control Configuration 3 Register (Read/Write)
[Address = 1Ah]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7411.

Table 32. Control Configuration 3

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 0* | 0* | 0* | 0* | 1* | 0* | 0* | 0* |

*Default settings at power-up.

Table 33.

| Bit | Function |
|-------|--|
| C0 | Selects between fast and normal ADC conversion speeds. 0 = ADC clock at 1.4 kHz. 1 = ADC clock at 22.5 kHz. D+ and D- analog filters are disabled. |
| C1:2 | Reserved. Only write 0s. |
| C3 | Reserved. Write only 1 to this bit. |
| C4 | Selects the ADC reference to be either Internal V_{REF} or V_{DD} for analog inputs. 0 = Int V_{REF} 1 = V_{DD} |
| C5:C7 | Reserved. Only write 0s. |

Interrupt Mask 1 Register (Read/Write) [Address = 1Dh]

This mask register is an 8-bit read/write register that can be used to mask out any interrupts that can cause the INT/ $\overline{\text{INT}}$ pin to go active.

Table 34. Interrupt Mask 1

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Table 35.

| Bit | Function |
|-----|---|
| D0 | 0 = Enable internal T _{HIGH} interrupt. 1 = Disable internal T _{HIGH} interrupt. |
| D1 | 0 = Enable internal T _{LOW} interrupt. 1 = Disable internal T _{LOW} interrupt. |
| D2 | 0 = Enable external T _{HIGH} interrupt or AIN1 interrupt. 1 = Disable external T _{HIGH} interrupt or AIN1 interrupt. |
| D3 | 0 = Enable external T _{LOW} interrupt. 1 = Disable external T _{LOW} interrupt. |
| D4 | 0 = Enable external temperature fault interrupt. 1 = Disable external temperature fault interrupt. |
| D5 | 0 = Enable AIN2 interrupt. 1 = Disable AIN2 interrupt. |
| D6 | 0 = Enable AIN3 interrupt. 1 = Disable AIN3 interrupt. |
| D7 | 0 = Enable AIN4 interrupt. 1 = Disable AIN4 interrupt. |

Interrupt Mask 2 Register (Read/Write) [Address = 1Eh]

This mask register is an 8-bit read/write register that can be used to mask out any interrupts that can cause the INT/INT pin to go active.

Table 36. Interrupt Mask 2

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Table 37.

| Bit | Function |
|-------|---|
| D0 | 0 = Enable AIN5 interrupt. 1 = Disable AIN5 interrupt. |
| D1 | 0 = Enable AIN6 interrupt. 1 = Disable AIN6 interrupt. |
| D2 | 0 = Enable AIN7 interrupt. 1 = Disable AIN7 interrupt. |
| D3 | 0 = Enable AIN8 interrupt. 1 = Disable AIN8 interrupt. |
| D4 | 0 = Enable V _{DD} interrupts. 1 = Disable V _{DD} interrupts. |
| D5:D7 | Reserved. Only write 0s. |

Internal Temperature Offset Register (Read/Write) [Address = 1Fh]

This register contains the offset value for the internal temperature channel. A twos complement number can be written to this register, which is then added to the measured result before it is stored or compared to limits. In this way, a sort of one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view this may be a very simple method to vary the characteristics of the measurement channel if the

thermal characteristics change. Because it is an 8-bit register, the temperature resolution is 1°C.

Table 38. Internal Temperature Offset

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

External Temperature Offset Register (Read/Write) [Address = 20h]

This register contains the offset value for the external temperature channel. A twos complement number can be written to this register, which is then added to the measured result before it is stored or compared to limits. In this way, a sort of one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. Because it is an 8-bit register, the temperature resolution is 1°C.

Table 39. External Temperature Offset

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

V_{DD} V_{HIGH} Limit Register (Read/Write) [Address = 23h]

This limit register is an 8-bit read/write register that stores the V_{DD} upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured V_{DD} value has to be greater than the value in this register. The default value is 5.46 V.

Table 40. V_{DD} V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 0* | 0* | 0* | 1* | 1* | 1* |

*Default settings at power-up.

V_{DD} V_{LOW} Limit Register (Read/Write) [Address = 24h]

This limit register is an 8-bit read/write register that stores the V_{DD} lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured V_{DD} value has to be less than or equal to the value in this register. The default value is 2.7 V.

Table 41. V_{DD} V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 1* | 1* | 0* | 0* | 0* | 1* | 0* |

*Default settings at power-up.

Internal T_{HIGH} Limit Register (Read/Write) [Address = 25h]

This limit register is an 8-bit read/write register that stores the two's complement of the internal temperature upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured internal temperature value has to be greater than the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is +100°C.

Table 42. Internal T_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 1* | 1* | 0* | 0* | 1* | 0* | 0* |

*Default settings at power-up.

Internal T_{LOW} Limit Register (Read/Write) [Address = 26h]

This limit register is an 8-bit read/write register that stores the two's complement of the internal temperature lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured internal temperature value has to be more negative than or equal to the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is -55°C.

Table 43. Internal T_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 0* | 0* | 1* | 0* | 0* | 1* |

*Default settings at power-up.

External T_{HIGH} /AIN1 V_{HIGH} Limit Register (Read/Write) [Address = 27h]

If Pins 7 and 8 are configured for the external temperature sensor, this limit register is an 8-bit read/write register that stores the two's complement of the external temperature upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured external temperature value has to be greater than the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is -1°C.

If Pins 7 and 8 are configured for AIN1 and AIN2 single-ended inputs, this limit register is an 8-bit read/write register that stores the AIN1 input upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN1 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. Since the power-up default settings for Pins 7 and 8 are AIN1 and AIN2 single-ended inputs, the default value for this limit register is full-scale voltage.

Table 44. AIN1 V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 1* | 1* | 1* | 1* | 1* | 1* |

*Default settings at power-up.

External T_{LOW} /AIN1 V_{LOW} Limit Register (Read/Write) [Address = 28h]

If Pins 7 and 8 are configured for the external temperature sensor, this limit register is an 8-bit read/write register that stores the two's complement of the external temperature lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured external temperature value has to be more negative than or equal to the value in this register. Since it is an 8-bit register, the temperature resolution is 1°C. The default value is 0°C.

If Pins 7 and 8 are configured for AIN1 and AIN2 single-ended inputs, this limit register is an 8-bit read/write register that stores the AIN1 input lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN1 value has to be less than or equal to the value in this register. Because it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Since the power-up default settings for Pins 7 and 8 are AIN1 and AIN2 single-ended inputs, the default value for this limit register is 0 V.

Table 45. AIN1 V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN2 V_{HIGH} Limit Register (Read/Write) [Address = 2Bh]

This limit register is an 8-bit read/write register that stores the AIN2 input upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN2 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 46. AIN2 V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 1* | 1* | 1* | 1* | 1* | 1* |

*Default settings at power-up.

AIN2 V_{LOW} Limit Register (Read/Write) [Address = 2Ch]

This limit register is an 8-bit read/write register that stores the AIN2 input lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN2 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 47. AIN2 V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN3 V_{HIGH} Limit Register (Read/Write) [Address = 2Dh]

This limit register is an 8-bit read/write register that stores the AIN3 input upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN3 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 48. AIN3 V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 1* | 1* | 1* | 1* | 1* | 1* |

*Default settings at power-up.

AIN3 V_{LOW} Limit Register (Read/Write) [Address = 2Eh]

This limit register is an 8-bit read/write register that stores the AIN3 input lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN3 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 49. AIN3 V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN4 V_{HIGH} Limit Register (Read/Write) [Address = 2Fh]

This limit register is an 8-bit read/write register that stores the AIN4 input upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN4 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 50. AIN4 V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 1* | 1* | 1* | 1* | 1* | 1* |

*Default settings at power-up.

AIN4 V_{LOW} Limit Register (Read/Write) [Address = 30h]

This limit register is an 8-bit read/write register that stores the AIN4 input lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN4 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 51. AIN4 V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN5 V_{HIGH} Limit Register (Read/Write) [Address = 31h]

This limit register is an 8-bit read/write register that stores the AIN5 input upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN5 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 52. AIN5 V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 1* | 1* | 1* | 1* | 1* | 1* |

*Default settings at power-up.

AIN5 V_{LOW} Limit Register (Read/Write) [Address = 32h]

This limit register is an 8-bit read/write register that stores the AIN5 input lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN5 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 53. AIN5 V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN6 V_{HIGH} Limit Register (Read/Write) [Address = 33h]

This limit register is an 8-bit read/write register that stores the AIN3 input upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN6 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 54. AIN6 V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 1* | 1* | 1* | 1* | 1* | 1* |

*Default settings at power-up at power-up.

AIN6 V_{LOW} Limit Register (Read/Write) [Address = 34h]

This limit register is an 8-bit read/write register that stores the AIN6 input lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the mea-

sured AIN6 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 55. AIN6 V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN7 V_{HIGH} Limit Register (Read/Write) [Address = 35h]

This limit register is an 8-bit read/write register that stores the AIN7 input upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN7 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 56. AIN7 V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 1* | 1* | 1* | 1* | 1* | 1* |

*Default settings at power-up.

AIN7 V_{LOW} Limit Register (Read/Write) [Address = 36h]

This limit register is an 8-bit read/write register that stores the AIN7 input lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN7 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 57. AIN7 V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

AIN8 V_{HIGH} Limit Register (Read/Write) [Address = 37h]

This limit register is an 8-bit read/write register that stores the AIN8 input upper limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN8 value has to be greater than the value in this register. As it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 58. AIN8 V_{HIGH} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1* | 1* | 1* | 1* | 1* | 1* | 1* | 1* |

*Default settings at power-up.

AIN8 V_{LOW} Limit Register (Read/Write) [Address = 38h]

This limit register is an 8-bit read/write register that stores the AIN8 input lower limit that will cause an interrupt and activate the INT/INT output (if enabled). For this to happen, the measured AIN8 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 59. AIN8 V_{LOW} Limit

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* |

*Default settings at power-up.

Device ID Register (Read-Only) [Address = 4Dh]

This 8-bit read-only register gives a unique identification number for this part. ADT7411 = 02h.

Manufacturer's ID Register (Read-Only) [Address = 4Eh]

This register contains the manufacturer's identification number. ADI's is 41h.

Silicon Revision Register (Read-Only) [Address = 4Fh]

This register is divided into the four LSBs representing the stepping and the four MSBs representing the version. The stepping contains the manufacturer's code for minor revisions or steppings to the silicon. The version is the ADT7411 version number, 0100b (4h).

SPI Lock Status Register (Read-Only) [Address = 7Fh]

Bit D0 (LSB) of this read-only register indicates whether the SPI interface is locked or not. Writing to this register will cause the device to malfunction. Default value is 00h.

0 = I²C interface.

1 = SPI interface selected and locked.

SERIAL INTERFACE

There are two serial interfaces that can be used on this part: I²C and SPI. The device will power up with the serial interface in I²C mode but it is not locked into this mode. To stay in I²C mode, it is recommended that the user tie the $\overline{\text{CS}}$ line to either V_{CC} or GND. It is not possible to lock the I²C mode, but it is possible to select and lock the SPI mode.

To select and lock the interface into the SPI mode, a number of pulses must be sent down the $\overline{\text{CS}}$ (Pin 4) line. The following section describes how this is done.

Once the SPI communication protocol has been locked in, it cannot be unlocked while the device is still powered up. Bit D0 of the SPI Lock Status register (Address 7Fh) is set to 1 when a successful SPI interface lock has been accomplished. To reset the serial interface, the user must power down the part and power up again. A software reset does not reset the serial interface.

Serial Interface Selection

The \overline{CS} line controls the selection between I²C and SPI.

Figure 16 shows the selection process necessary to lock the SPI interface mode.

To communicate to the ADT7411 using the SPI protocol, send three pulses down the \overline{CS} line as shown in Figure 33. On the third rising edge (marked as C in Figure 33), the part selects and locks the SPI interface. Communication to the device is now limited to the SPI protocol.

As per most SPI standards, the \overline{CS} line must be low during every SPI communication to the ADT7411, and high at all other times. Typical examples of how to connect the dual interface as I²C or SPI are shown in Figure 31 and Figure 32.

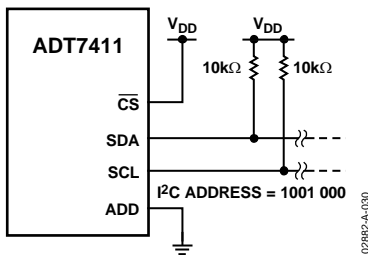


Figure 31. Typical I²C Interface Connection

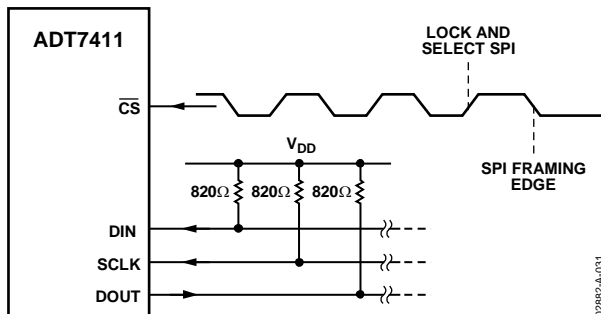


Figure 32. Typical SPI Interface Connection

The following sections describe in detail how to use the I²C and SPI protocols associated with the ADT7411.

I²C Serial Interface

Like all I²C compatible devices, the ADT7411 has a 7-bit serial address. The four MSBs of this address for the ADT7411 are set to 1001. The three LSBs are set by Pin 11, ADD. The ADD pin can be configured three ways to give three different address options: low, floating, and high. Setting the ADD pin low gives a serial bus address of 1001 000, leaving it floating gives the Address 1001 010, and setting it high gives the Address 1001 011. The recommended pull-up resistor value is 10 kΩ.

There is an enable/disable bit for the SMBus timeout. When this is enabled, the SMBus will timeout after 25 ms of no activity. To enable it, set Bit 6 of the Control Configuration 2 register. The power-up default is with the SMBus timeout disabled.

The ADT7411 supports SMBus packet error checking (PEC) and its use is optional. It is triggered by supplying the extra clocks for the PEC byte. The PEC is calculated using CRC-8. The frame clock sequence (FCS) conforms to CRC-8 by the polynomial

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult the SMBus specification (www.smbus.org) for more information.

The serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/W bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is 0, the master will write to the slave device. If the R/W bit is 1, the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master will pull the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device will pull the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation. This is because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

The I²C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. This is the SCL cycle directly after the device has seen its own I²C serial bus address. Any subsequent changes on this pin will have no effect on the I²C serial bus address.

Writing to the ADT7411

Depending on the register being written to, there are two different writes for the ADT7411. It is not possible to do a block write to this part, i.e., no I²C auto-increment.

Writing to the Address Pointer Register for a Subsequent Read

In order to read data from a particular register, the address pointer register must contain the address of that register. If it does not, the correct address must be written to the address pointer register by performing a single-byte write operation, as shown in Figure 34. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation is then performed to read the register.

Writing Data to a Register

All registers are 8-bit registers so only one byte of data can be written to each register. Writing a single byte of data to one of these read/write registers consists of the serial bus address, the data register address written to the address pointer register,

followed by the data byte written to the selected data register. This is illustrated in Figure 35. To write to a different register, another START or repeated START is required. If more than one byte of data is sent in one communication operation, the addressed register will be repeatedly loaded until the last data byte has been sent.

Reading Data From the ADT7411

Reading data from the ADT7411 is done in a one-byte operation. Reading back the contents of a register is shown in Figure 36. The register address had previously been set up by a single-byte write operation to the Address Pointer register. To read from another register, write to the Address Pointer register again to set up the relevant register address. Thus, block reads are not possible, i.e., no I²C auto-increment.

SPI Serial Interface

The SPI serial interface of the ADT7411 consists of four wires: \overline{CS} , SCLK, DIN, and DOUT. The \overline{CS} is used to select the device when more than one device is connected to the serial clock and data lines. The \overline{CS} is also used to distinguish between any two separate serial communications (see Figure 41 for a graphical explanation). The SCLK is used to clock data in and out of the part. The DIN line is used to write to the registers, and the DOUT line is used to read data back from the registers. The recommended pull-up resistor value is between 500 Ω and 820 Ω .

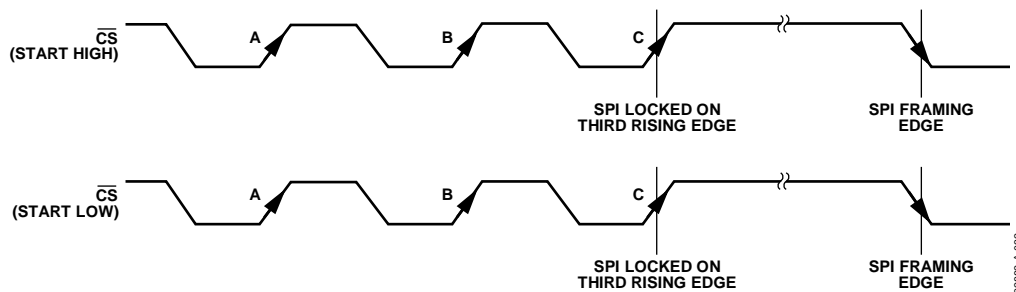


Figure 33. Serial Interface—Selecting and Locking SPI Protocol

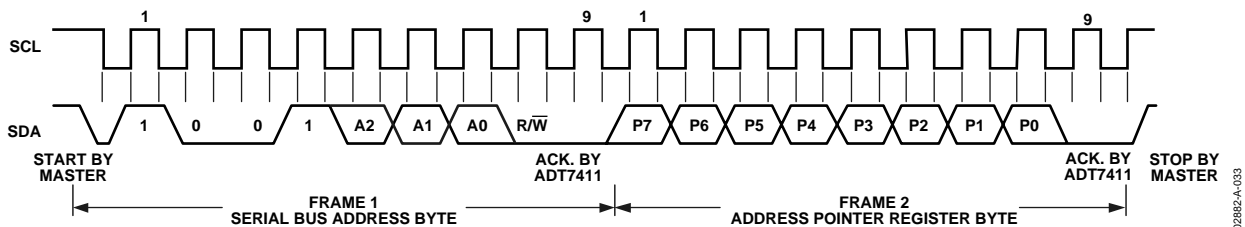


Figure 34. I²C—Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation

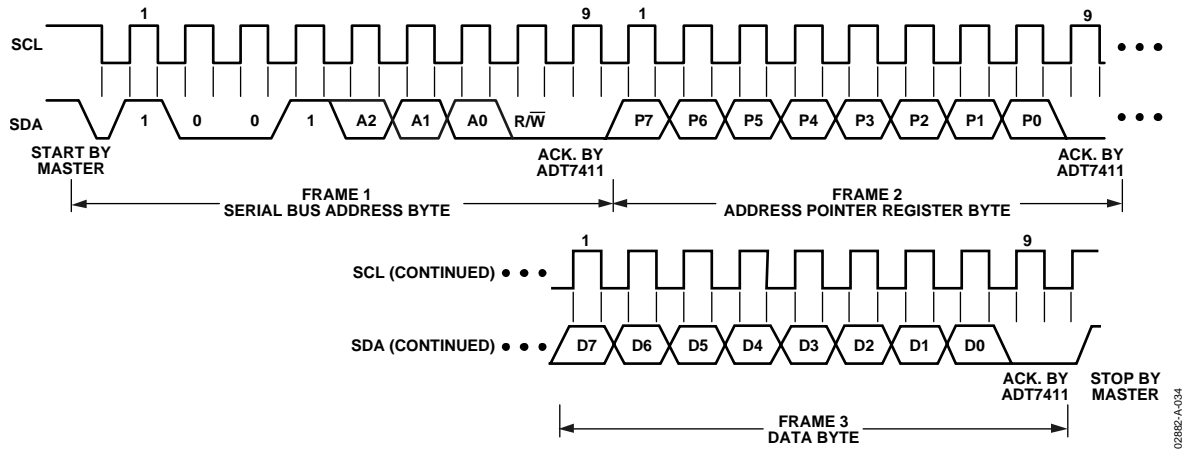


Figure 35. I²C—Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register

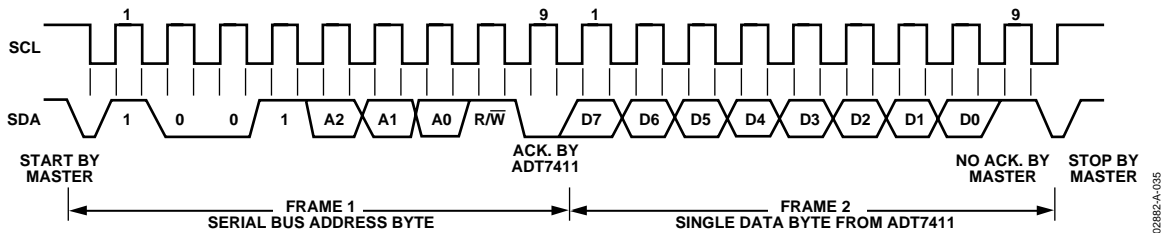


Figure 36. I²C—Reading a Single Byte of Data from a Selected Register

The part operates in a slave mode and requires an externally applied serial clock to the SCLK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

There are two types of serial operation: a read and a write. Command words are used to distinguish between a read and a write operation. These command words are given in Table 60. Address auto-incrementing is possible in SPI mode.

Table 60. SPI Command Words

| Write | Read |
|-----------------|-----------------|
| 90h (1001 0000) | 91h (1001 0001) |

Write Operation

Figure 37 shows the timing diagram for a write operation to the ADT7411. Data is clocked into the registers on the rising edge of SCLK. When the \overline{CS} line is high, the DIN and DOUT lines are in three-state mode. Only when the \overline{CS} goes from a high to a low does the part accept any data on the DIN line. In SPI mode, the address pointer register is capable of auto-incrementing to the next register in the register map without having to load the address pointer register each time. In Figure 37, the register address portion of the diagram gives the first register that will be written to. Subsequent data bytes will be written into sequential writable registers. Thus, after each data byte has been written into a register, the address pointer register auto-increments its value to the next available register. The address pointer

register will auto-increment from 00h to 3Fh and then loop back to start over again at 00h.

Read Operation

Figure 38 to Figure 40 show the timing diagrams of correct read operations. To read back from a register, first write to the address pointer register with the address to be read from. This operation is shown in Figure 38. Figure 39 shows the procedure for reading back a single byte of data. The read command is first sent to the part during the first eight clock cycles, during the following eight clock cycles the data contained in the register selected by the address pointer register is output onto the DOUT line. Data is output onto the DOUT line on the falling edge of SCLK. Figure 40 shows the procedure when reading data from two sequential registers.

Multiple data reads are possible in SPI interface mode as the address pointer register is auto-incremental. The address pointer register will auto-increment from 00h to 3Fh and will loop back to start all over again at 00h when it reaches 3Fh.

SMBus/SPI INT/ \overline{INT}

The ADT7411 INT/ \overline{INT} output is an interrupt line for devices that want to trade their ability to master for an extra pin. The ADT7411 is a slave-only device and uses the SMBus/SPI INT/ \overline{INT} to signal the host device that it wants to talk. The SMBus/SPI INT/ \overline{INT} on the ADT7411 is used as an over/under limit indicator.

The $\overline{\text{INT/INT}}$ pin has an open-drain configuration that allows the outputs of several devices to be wired-AND together when the $\overline{\text{INT/INT}}$ pin is active low. Use C6 of the Control Configuration 1 register to set the active polarity of the $\overline{\text{INT/INT}}$ output. The power-up default is active low. The $\overline{\text{INT/INT}}$ output can be disabled or enabled by setting C5 of Control Configuration 1 register to a 1 or 0, respectively.

The $\overline{\text{INT/INT}}$ output becomes active when either the internal temperature value, the external temperature value, V_{DD} value, or any of the AIN input values exceed the values in their corresponding $T_{\text{HIGH}}/V_{\text{HIGH}}$ or $T_{\text{LOW}}/V_{\text{LOW}}$ registers. The $\overline{\text{INT/INT}}$ output goes inactive again when a conversion result has the measured value back within the trip limits and when the status register associated with the out-of-limit event is read. The two Interrupt Status registers show which event caused the $\overline{\text{INT/INT}}$ pin to go active.

The $\overline{\text{INT/INT}}$ output requires an external pull-up resistor. This can be connected to a voltage different from V_{DD} , provided the maximum voltage rating of the $\overline{\text{INT/INT}}$ output pin is not exceeded. The value of the pull-up resistor depends on the application, but should be as large enough to avoid excessive sink currents at the $\overline{\text{INT/INT}}$ output, which can heat the chip and affect the temperature reading.

SMBus Alert Response

The $\overline{\text{INT/INT}}$ pin behaves the same way as an SMBus alert pin when the SMBus/I²C interface is selected. It is an open-drain output and requires a pull-up to V_{DD} . Several $\overline{\text{INT/INT}}$ outputs can be wire-AND together, so that the common line will go low if one or more of the $\overline{\text{INT/INT}}$ outputs goes low. The polarity of the $\overline{\text{INT/INT}}$ pin must be set for active low for a number of outputs to be wire-AND together.

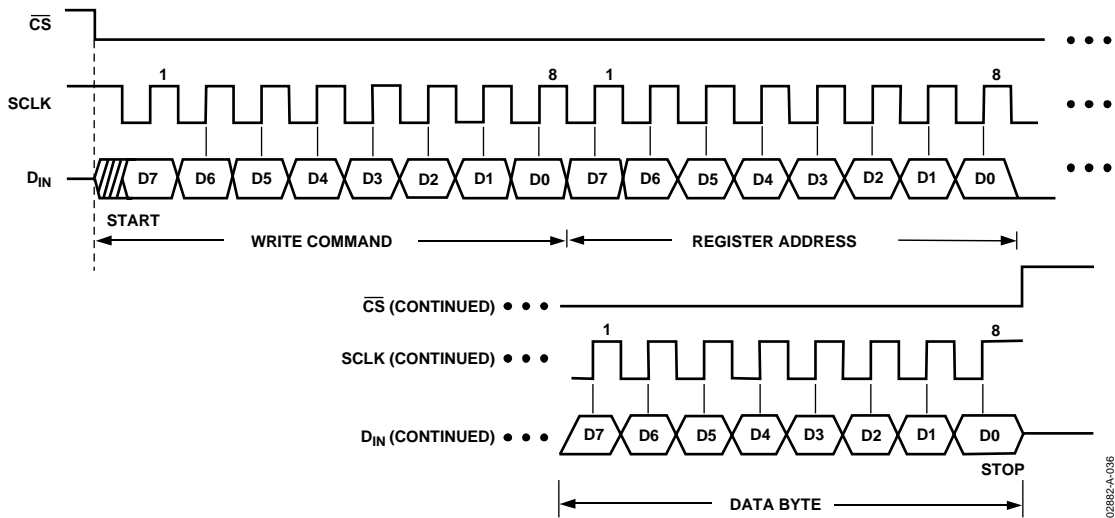


Figure 37. SPI—Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register

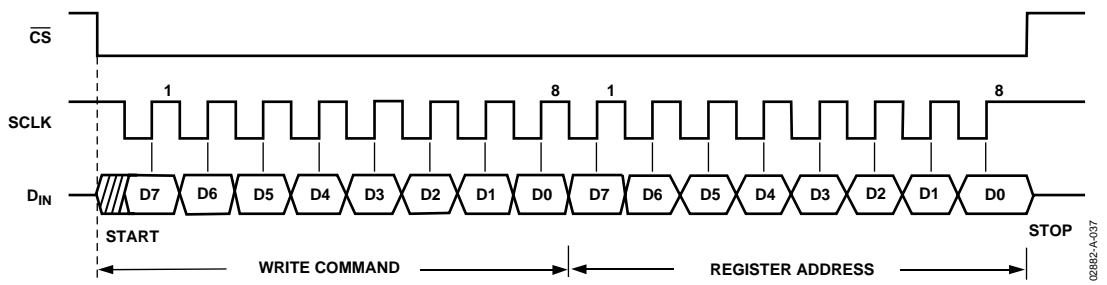


Figure 38. SPI—Writing to the Address Pointer Register to Select a Register for Subsequent Read Operation

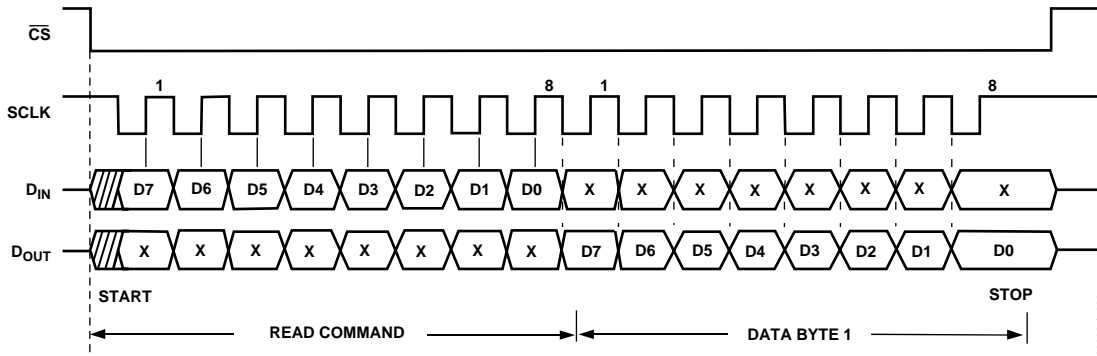


Figure 39. SPI—Reading a Single Byte of Data from a Selected Register

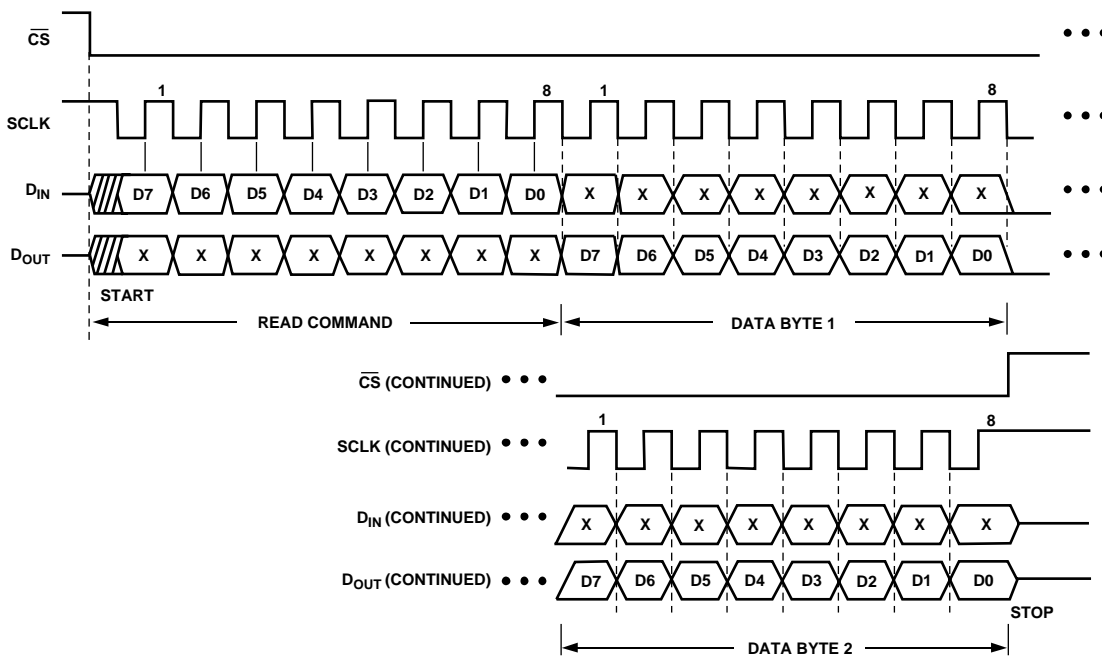


Figure 40. SPI—Reading Two Bytes of Data from Two Sequential Registers

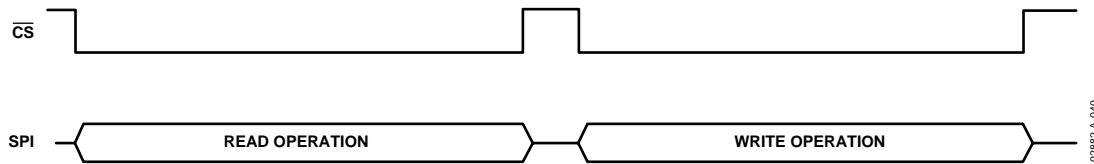


Figure 41. SPI—Correct Use of \overline{CS} during SPI Communications

The $\overline{INT}/\overline{INT}$ output can operate as an $\overline{SMBALERT}$ function. Slave devices on the SMBus can normally not signal to the master that they want to talk, but the $\overline{SMBALERT}$ function allows them to do so. $\overline{SMBALERT}$ is used in conjunction with the SMBus general call address.

One or more $\overline{INT}/\overline{INT}$ outputs can be connected to a common $\overline{SMBALERT}$ line connected to the master. When the $\overline{SMBALERT}$ line is pulled low by one of the devices, the following procedure occurs, as shown in Figure 42.

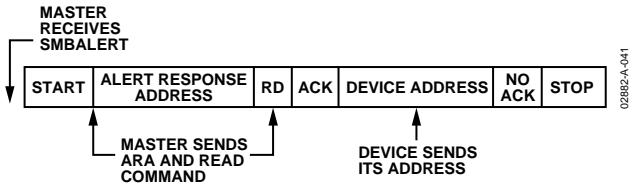


Figure 42. INT/INT Responds to SMBALERT ARA

1. SMBALERT is pulled low.
2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose INT/INT output is low responds to the alert response address and the master reads its device address. As the device address is seven bits long, an LSB of 1 is added. The address of the device is now known and it can be interrogated in the usual way.

4. If more than one device's INT/INT output is low, the one with the lowest device address will have priority, in accordance with normal SMBus specifications.
5. Once the ADT7411 has responded to the alert response address, it will reset its INT/INT output, provided that the condition that caused the out-of-limit event no longer exists and the status register associated with the out-of-limit event is read. If the SMBALERT line remains low, the master will send the ARA again. It will continue to do this until all devices whose SMBALERT outputs were low have responded.

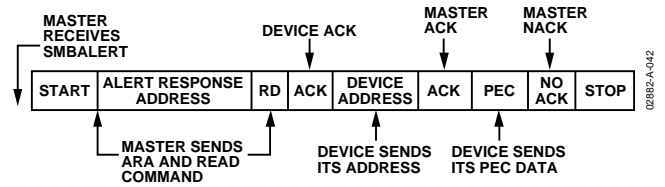


Figure 43. INT/INT Responds to SMBALERT ARA with Packet Error Checking (PEC)

OUTLINE DIMENSIONS

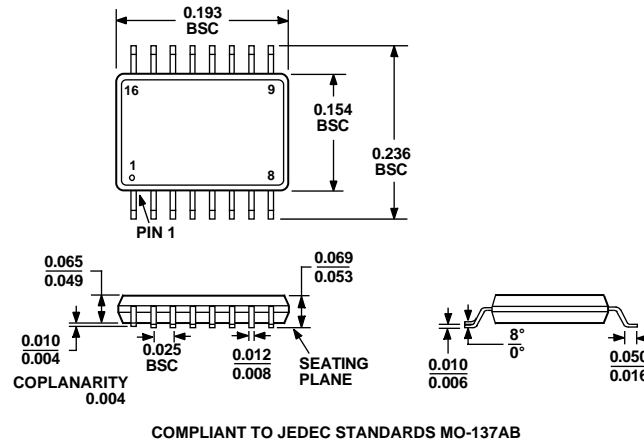


Figure 44. 16-Lead Shrink Small Outline Package [QSOP] (RQ-16)

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ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Minimum Quantities/Reel |
|--------------------------------|-------------------|---------------------|----------------|-------------------------|
| ADT7411ARQ | -40°C to +120°C | 16-Lead QSOP | RQ-16 | N/A |
| ADT7411ARQ-REEL | -40°C to +120°C | 16-Lead QSOP | RQ-16 | 2500 |
| ADT7411ARQ-REEL7 | -40°C to +120°C | 16-Lead QSOP | RQ-16 | 1000 |
| ADT7411ARQZ ¹⁰ | -40°C to +120°C | 16-Lead QSOP | RQ-16 | N/A |
| ADT7411ARQZ-REEL ¹ | -40°C to +120°C | 16-Lead QSOP | RQ-16 | 2500 |
| ADT7411ARQZ-REEL7 ¹ | -40°C to +120°C | 16-Lead QSOP | RQ-16 | 1000 |

¹⁰ Z = Pb-free part.

NOTES

ADT7411

NOTES