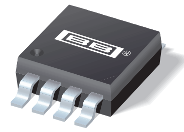
BURR - BROWN®



ADS8321

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16-Bit, High Speed, MicroPower Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **BIPOLAR INPUT RANGE**
- **100kHz SAMPLING RATE**
- **MICRO POWER:**
  4.5mW at 100kHz
  1mW at 10kHz
- **POWER DOWN: 3µA max**
- **8-LEAD MSOP PACKAGE**
- **PIN-COMPATIBLE TO ADS7816 AND ADS7822**
- **SERIAL (SPI/SSI) INTERFACE**

APPLICATIONS

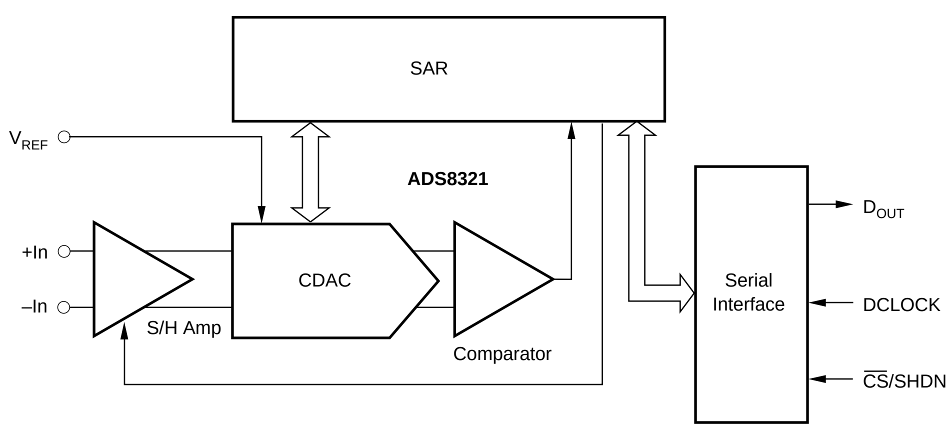
- **BATTERY OPERATED SYSTEMS**
- **REMOTE DATA ACQUISITION**
- **ISOLATED DATA ACQUISITION**
- **SIMULTANEOUS SAMPLING, MULTI-CHANNEL SYSTEMS**
- **INDUSTRIAL CONTROLS**
- **ROBOTICS**
- **VIBRATION ANALYSIS**

DESCRIPTION

The ADS8321 is a 16-bit sampling analog-to-digital converter with guaranteed specifications over a 4.75V to 5.25V supply range. It requires very little power even when operating at the full 100kHz data rate. At lower data rates, the high speed of the device enables it to spend most of its time in the power-down mode—the average power dissipation is less than 1mW at 10kHz data rate.

The ADS8321 also features a synchronous serial (SPI/SSI compatible) interface, and a differential input. The reference voltage can be set to any level within the range of 500mV to 2.5V.

Ultra-low power and small size make the ADS8321 ideal for portable and battery-operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multi-channel systems, and isolated data acquisition. The ADS8321 is available in an 8-lead MSOP package.



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SPECIFICATIONS: $+V_{CC} = +5V$

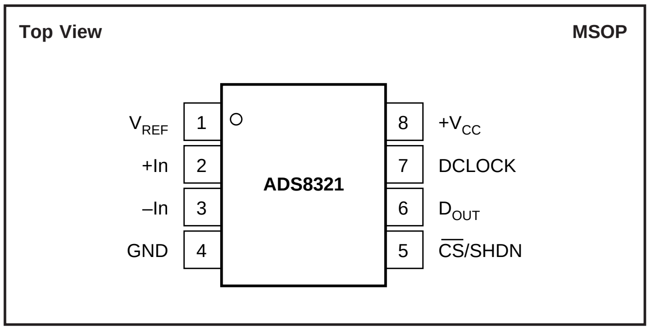
At –40°C to +85°C, V_{REF} = +2.5V, –In = 2.5V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE}, unless otherwise specified.

PARAMETER	CONDITIONS	ADS8321E MIN	ADS8321E TYP	ADS8321E MAX	ADS8321EB MIN	ADS8321EB TYP	ADS8321EB MAX	UNITS
RESOLUTION				16			✻	Bits
ANALOG INPUT								
Full-Scale Input Span	+In – (–In)	$-V_{REF}$		$+V_{REF}$	✻		✻	V
Absolute Input Range	+In	–0.1		V_{CC} + 0.1	✻		✻	V
	–In	–0.1		+4.0	✻		✻	V
Capacitance			25			✻		pF
Leakage Current			1			✻		nA
SYSTEM PERFORMANCE								
No Missing Codes		14			15			Bits
Integral Linearity Error			±0.008	±0.018		±0.006	±0.012	% of FSR
Offset Error			±0.4	±2		±0.2	±1	mV
Offset Temperature Drift			±1			✻		µV/°C
Gain Error, Positive				±0.05			±0.024	%
Negative				±0.05			±0.024	%
Gain Temperature Drift			±0.3			✻		ppm/°C
Noise			60			✻		µVrms
Common-Mode Rejection Ratio			80			✻		dB
Power Supply Rejection Ratio	+4.7V < V_{CC} < 5.25V		3			✻		LSB(1)
SAMPLING DYNAMICS								
Conversion Time				16			✻	Clk Cycles
Acquisition Time		4.5			✻			Clk Cycles
Throughput Rate				100			✻	kHz
Clock Frequency Range		0.024		2.9	✻		✻	MHz
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion	V_{IN} = 5Vp-p at 10kHz		–84			–86		dB
SINAD	V_{IN} = 5Vp-p at 10kHz		82			84		dB
Spurious Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz		84			86		dB
SNR			85			87		dB
REFERENCE INPUT								
Voltage Range		0.5		$V_{CC}/2$	✻		✻	V
Resistance	$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			✻		GΩ
	$\overline{CS}$ = V_{CC}		5			✻		GΩ
Current Drain			40	80		✻	✻	µA
	f_{SAMPLE} = 10kHz		0.8			✻		µA
	$\overline{CS}$ = V_{CC}		0.1	3		✻		µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			✻		
Logic Levels:								
V_{IH}	I_{IH} = +5µA	3.0		V_{CC} + 0.3	✻		✻	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	✻		✻	V
V_{OH}	I_{OH} = –250µA	4.0			✻			V
V_{OL}	I_{OL} = 250µA			0.4			✻	V
Data Format			Binary Two's Complement			✻		
POWER SUPPLY REQUIREMENTS								
V_{CC}	Specified Performance	4.75		5.25	✻		✻	V
V_{CC} Range(2)		2.7		5.25	✻		✻	V
Quiescent Current			1100	1700		✻	✻	µA
	f_{SAMPLE} = 10kHz(3, 4)		250			✻		µA
Power Dissipation			5.5	8.5		✻	✻	mW
Power Down	$\overline{CS}$ = V_{CC}		0.3	3		✻	✻	µA
TEMPERATURE RANGE								
Specified Performance		–40		+85	✻		✻	°C

✻ Specifications same as grade to the left.

NOTES: (1) LSB means Least Significant Bit. (2) See Typical Performance Curves for more information. (3) f_{CLK} = 2.4MHz, $\overline{CS}$ = V_{CC} for 216 clock cycles out of every 240. (4) See the Power Dissipation section for more information regarding lower sample rates.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V_{REF}	Reference Input
2	+In	Non Inverting Input
3	–In	Inverting Input
4	GND	Ground
5	$\overline{CS}$/SHDN	Chip Select when LOW, Shutdown Mode when HIGH.
6	D_{OUT}	The serial output data word is comprised of 16 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit, data is valid for the next 16 edges.
7	DCLOCK	Data Clock synchronizes the serial data transfer and determines conversion speed.
8	$+V_{CC}$	Power Supply.

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC}	+6V
Analog Input	–0.3V to (V_{CC} + 0.3V)
Logic Input	–0.3V to 6V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Reference Voltage	+5.5V

NOTE: (1) Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

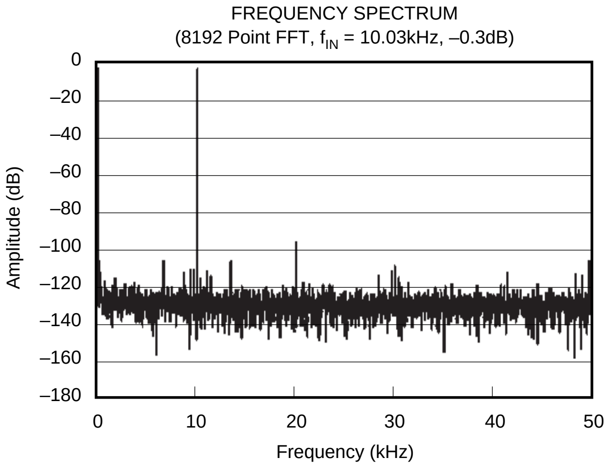
PACKAGE/ORDERING INFORMATION

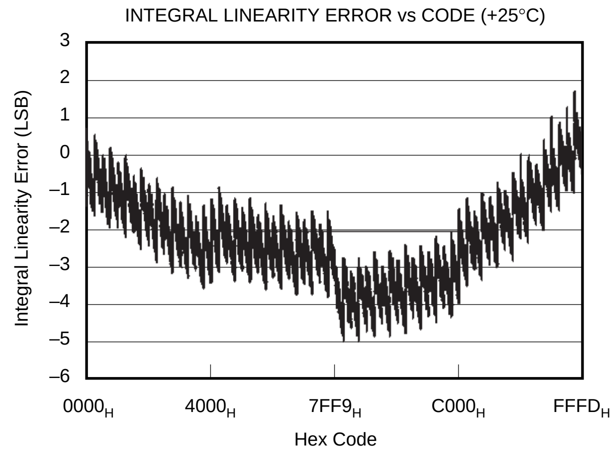
PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA
ADS8321E	0.018%	14	MSOP	337	–40°C to +85°C	ADS8321E/250	Tape and Reel
"	"	"	"	"	"	ADS8321E/2K5	Tape and Reel
ADS8321EB	0.012%	15	MSOP	337	–40°C to +85°C	ADS8321EB/250	Tape and Reel
"	"	"	"	"	"	ADS8321EB/2K5	Tape and Reel

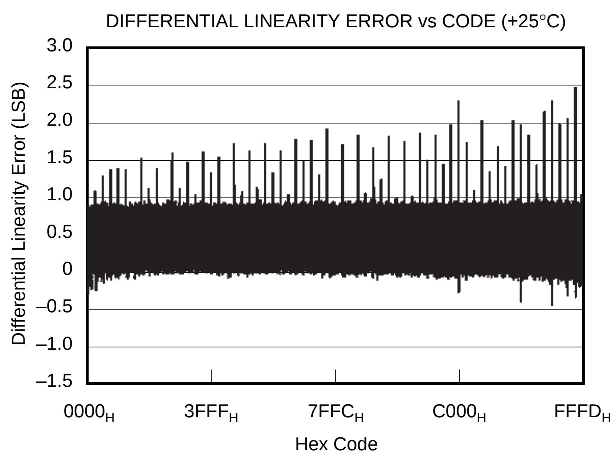
NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS8321EB/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

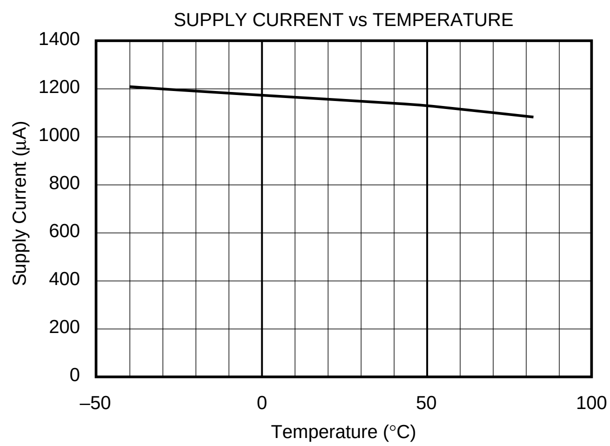
TYPICAL PERFORMANCE CURVES

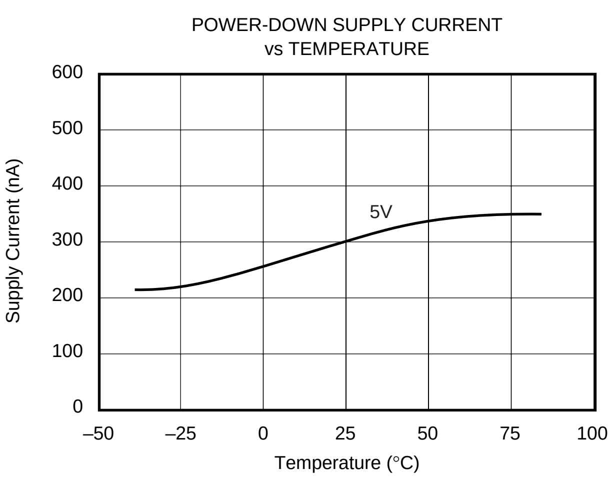
At $T_A = +25°C$, $V_{CC} = +5V$, $V_{REF} = +2.5V$, $f_{SAMPLE} = 100kHz$, $f_{CLK} = 24 \bullet f_{SAMPLE}$, unless otherwise specified.

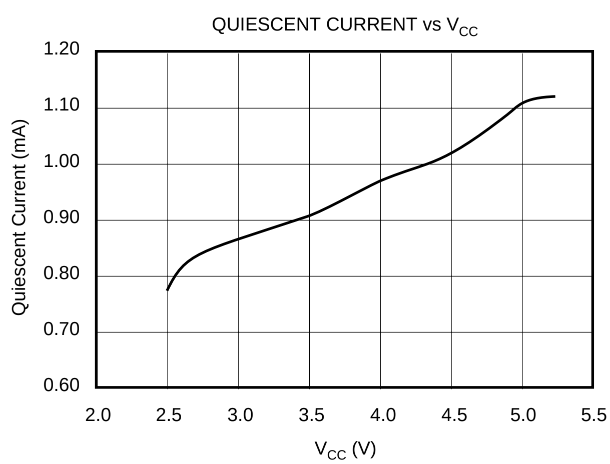






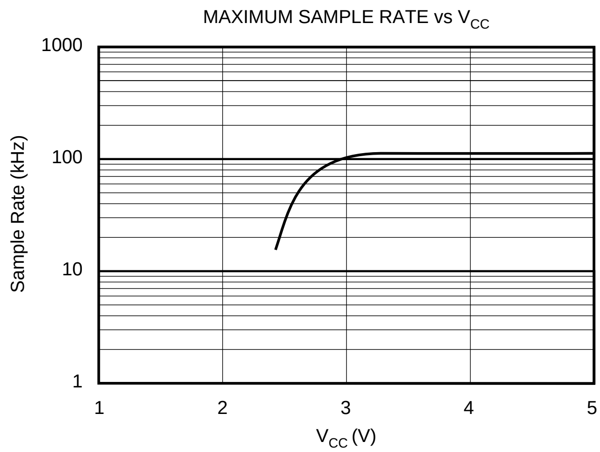


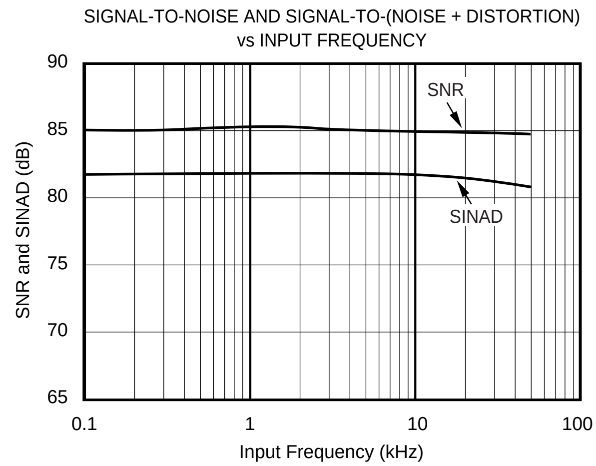


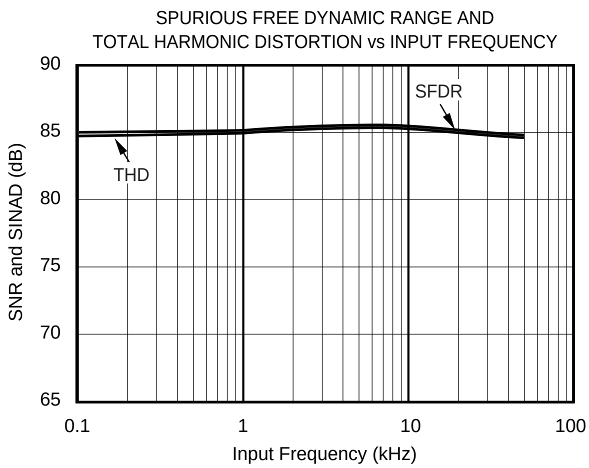


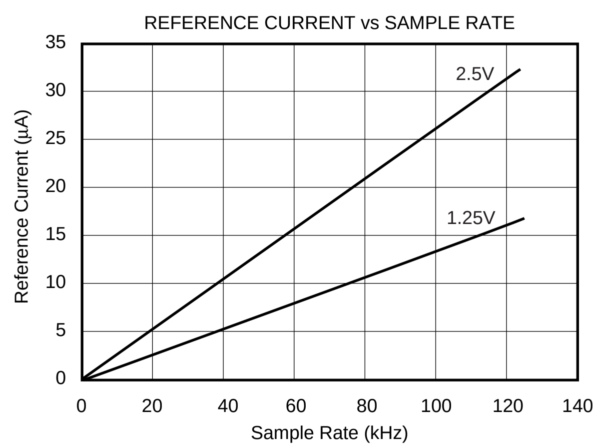
TYPICAL PERFORMANCE CURVES (Cont.)

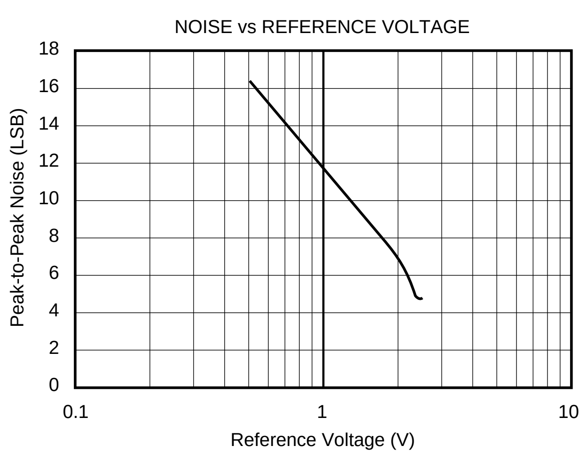
At $T_A = +25°C$, $V_{CC} = +5V$, $V_{REF} = +2.5V$, $f_{SAMPLE} = 100kHz$, $f_{CLK} = 24 \bullet f_{SAMPLE}$, unless otherwise specified.

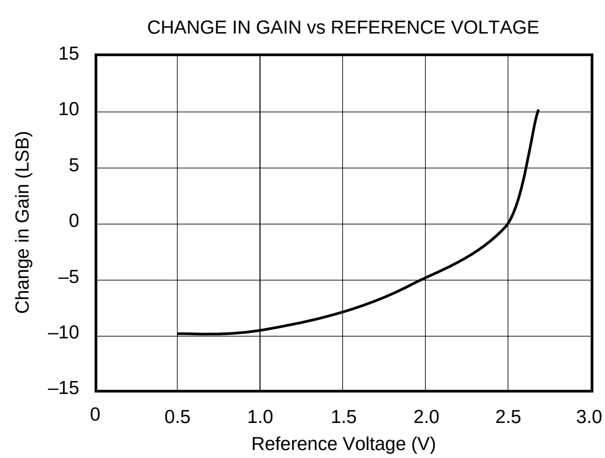






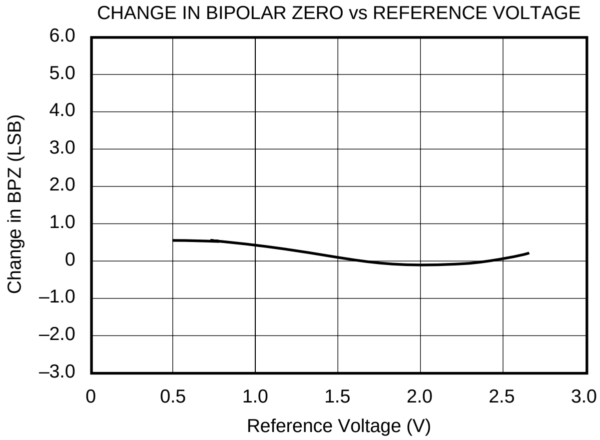


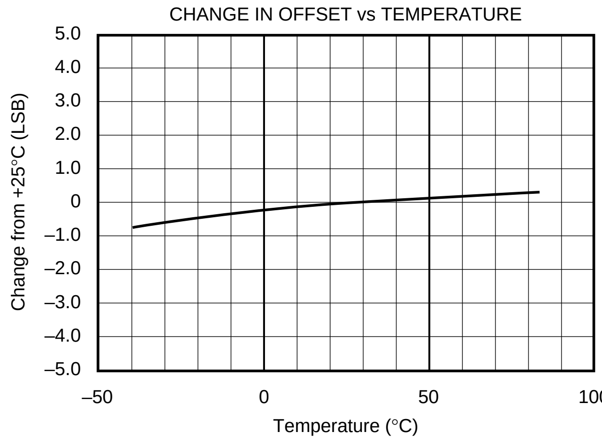


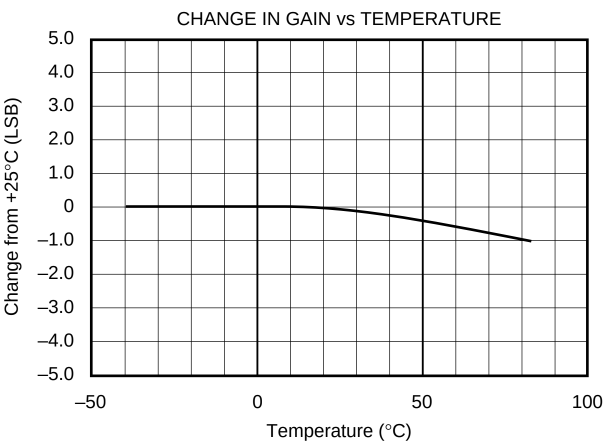


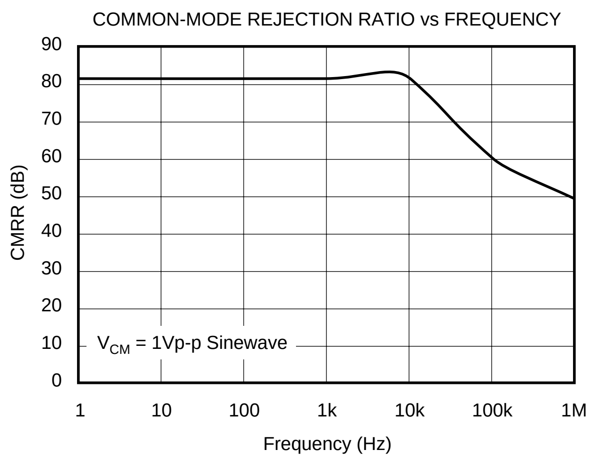
TYPICAL PERFORMANCE CURVES (Cont.)

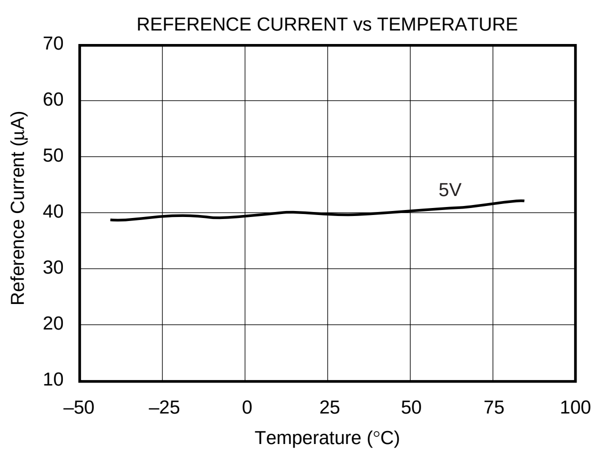
At $T_A = +25°C$, $V_{CC} = +5V$, $V_{REF} = +2.5V$, $f_{SAMPLE} = 100kHz$, $f_{CLK} = 24 \bullet f_{SAMPLE}$, unless otherwise specified.











THEORY OF OPERATION

The ADS8321 is a classic Successive Approximation Register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µ CMOS process. The architecture and process allow the ADS8321 to acquire and convert an analog signal at up to 100,000 conversions per second while consuming less than 5.5mW from $+V_{CC}$.

The ADS8321 requires an external reference, an external clock, and a single power source (V_{CC}). The external reference can be any voltage between 500mV and 2.5V. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS8321.

The external clock can vary between 24kHz (1kHz throughput) and 2.4MHz (100kHz throughput). The duty cycle of the clock is essentially unimportant as long as the minimum high and low times are at least 200ns (4.75V or greater). The minimum clock frequency is set by the leakage on the capacitors internal to the ADS8321.

The analog input is provided to two input pins: +In and –In. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS8321 after the conversion is complete and to obtain the serial data least significant bit first. See the digital timing section for more information.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8321: single-ended or differential (see Figure 1). When the input is single-ended, the –In input is held at a fixed voltage. The +In input swings around the same voltage and the peak-to-peak amplitude is $2 \cdot V_{REF}$. The value of V_{REF} determines the range over which the common voltage may vary (see Figure 2).

When the input is differential, the amplitude of the input is the difference between the +In and –In input, or; +In – (–In). A voltage or signal is common to both of these inputs. The peak-to-peak amplitude of each input is V_{REF} about this common voltage. However, since the input are 180°C out-of-phase, the peak-to-peak amplitude of the difference voltage is $2 \cdot V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs (see Figure 3).

In each case, care should be taken to ensure that the output impedance of the sources driving the +In and –In inputs are matched. If this is not observed, the two inputs could have

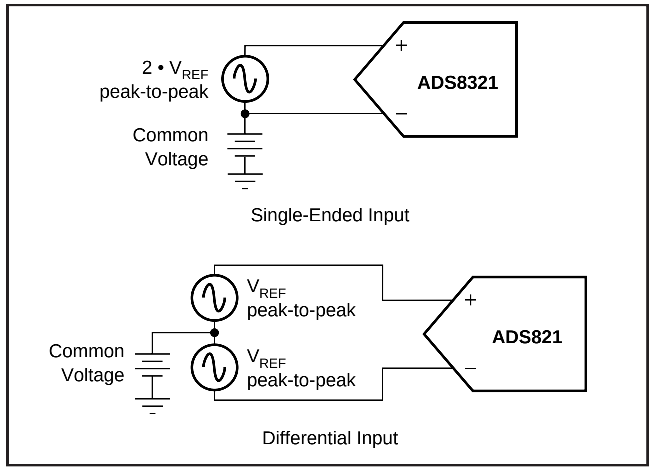


FIGURE 1. Methods of Driving the ADS8321—Single-Ended or Differential.

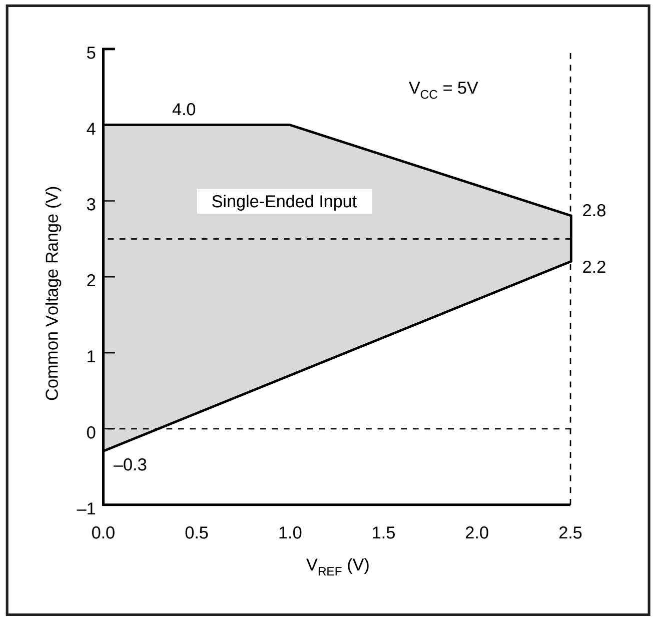


FIGURE 2. Single-Ended Input—Common Voltage Range vs V_{REF}.

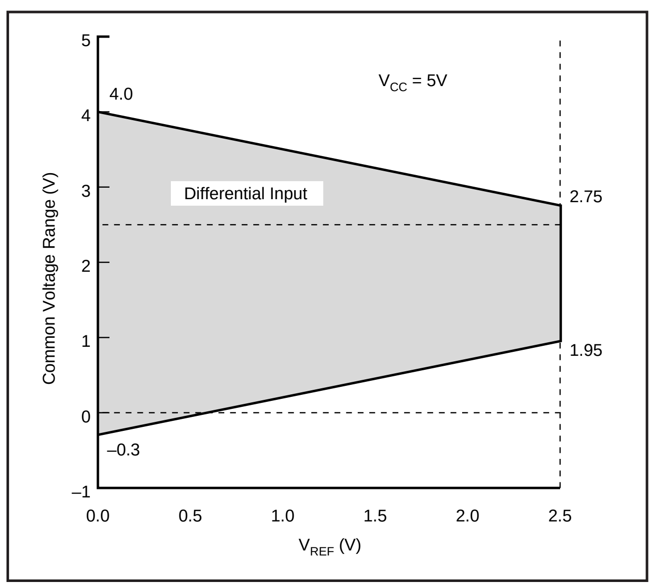


FIGURE 3. Differential Input—Common Voltage Range vs V_{REF}.

different settling times. This may result in offset error, gain error, and linearity error which change with both temperature and input voltage. If the impedance cannot be matched, the errors can be lessened by giving the ADS8321 additional acquisition time.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8321 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to 16-bit settling level within 4.5 clock cycles. When the converter goes into the hold mode or while it is in the power-down mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +In input should always remain within the range of GND – 300mV to V_{CC} + 300mW. The –In input should always remain within the range of GND – 300mV to 4V. Outside of these ranges, the converter's linearity may not meet specifications.

REFERENCE INPUT

The external reference sets the analog input range. The ADS8321 will operate with a reference in the range of 500mV to 2.5V. There are several important implications of this. As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the Least Significant Bit (LSB) size and is equal to 2 • V_{REF} divided by 65,535. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter will also appear to increase with lower LSB size. With a +2.5V reference, the internal noise of the converter typically contributes only 5 LSB peak-to-peak of potential error to the output code. When the external reference is 500mV, the potential error contribution from the internal noise will be 10 times larger—15 LSBs. The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical performance curve "Noise vs Reference Voltage." Note that the Effective Number of Bits (ENOB) figure is calculated based on the converter's signal-to-(noise + distortion) ratio with a 1kHz, 0dB input signal. SINAD is related to ENOB as follows:

$$\text{SINAD} = 6.02 \cdot \text{ENOB} + 1.76$$

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.

NOISE

The noise floor of the ADS8321 itself is extremely low, as can be seen from Figures 4 and 5, and is much lower than competing A/D converters. It was tested by applying a low noise DC input and a 2.5V reference to the ADS8321 and initiating 5,000 conversions. The digital output of the A/D converter will vary in output code due to the internal noise of the ADS8321. This is true for all 16-bit SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions will represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this will yield the ±3σ distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the distribution when executing 1000 conversions. The ADS8321, with five output codes for the ±3σ distribution, will yield a ±0.8LSB transition noise. Remember, to achieve this low noise performance, the peak-to-peak noise of the input signal and reference must be < 50μV.

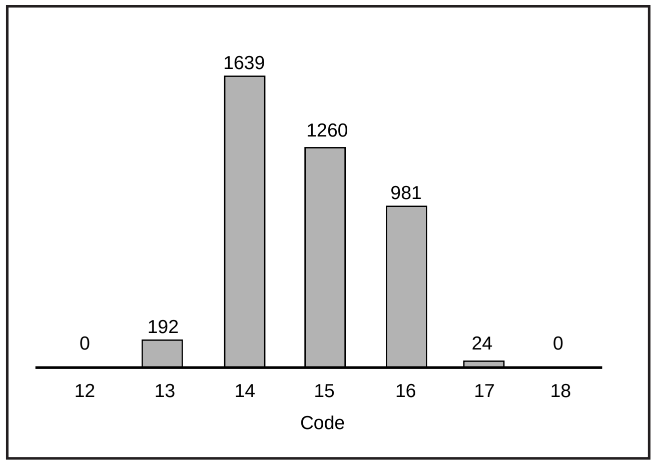


FIGURE 4. Histogram of 5,000 Conversions of a DC Input at the Code Transition.

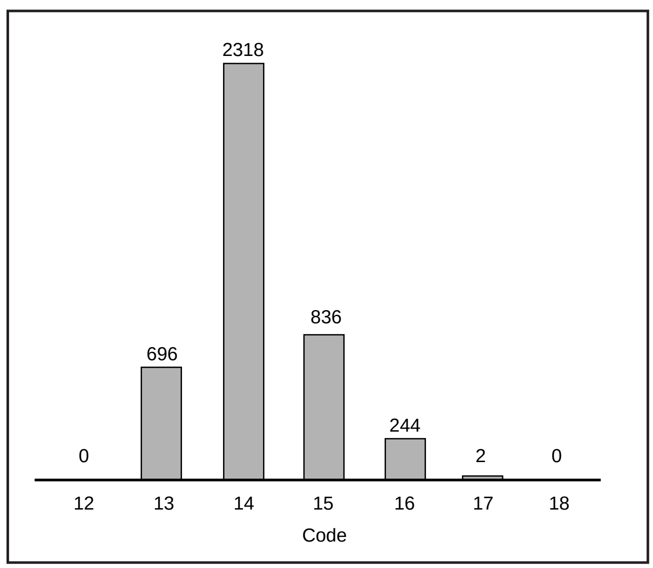


FIGURE 5. Histogram of 5,000 Conversions of a DC Input at the Code Center.

AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging 4 conversion results will reduce the transition noise by 1/2 to ±0.25 LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low pass filter and decimate the output codes. This works in a similar manner to averaging; for every decimation by 2, the signal-to-noise ratio will improve 3dB.

DIGITAL INTERFACE

SIGNAL LEVELS

The digital inputs of the ADS8321 can accommodate logic levels up to 5.5V regardless of the value of V_{CC}.

The CMOS digital output (D_{OUT}) will swing 0V to V_{CC}. If V_{CC} is 3V and this output is connected to a 5V CMOS logic input, then that IC may require more supply current than normal and may have a slightly longer propagation delay.

SERIAL INTERFACE

The ADS8321 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface as shown in Figure 6 and Table I. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	4.5		5.0	Clk Cycles
t_{CONV}	Conversion Time		16		Clk Cycles
t_{CYC}	Throughput Rate			100	kHz
t_{CSD}	$\overline{CS}$ Falling to DCLOCK LOW			0	ns
t_{SUCS}	$\overline{CS}$ Falling to DCLOCK Rising	20			ns
t_{hDO}	DCLOCK Falling to Current D_{OUT} Not Valid	5	15		ns
t_{dDO}	DCLOCK Falling to Next D_{OUT} Valid		30	50	ns
t_{dis}	$\overline{CS}$ Rising to D_{OUT} Tri-State		70	100	ns
t_{en}	DCLOCK Falling to D_{OUT} Enabled		20	50	ns
t_f	D_{OUT} Fall Time		5	25	ns
t_r	D_{OUT} Rise Time		7	25	ns

TABLE I. Timing Specifications (V_{CC} = 5V) –40°C to +85°C.

A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 4.5 to 5.0 clock periods of the conversion cycle are used to sample the input signal. After the fifth falling DCLOCK edge, D_{OUT} is enabled and will output a LOW value for one clock period. For the next 16 DCLOCK periods, D_{OUT} will output the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks will repeat the output data but in a least significant bit first format.

After the most significant bit (B15) has been repeated, D_{OUT} will tri-state. Subsequent clocks will have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

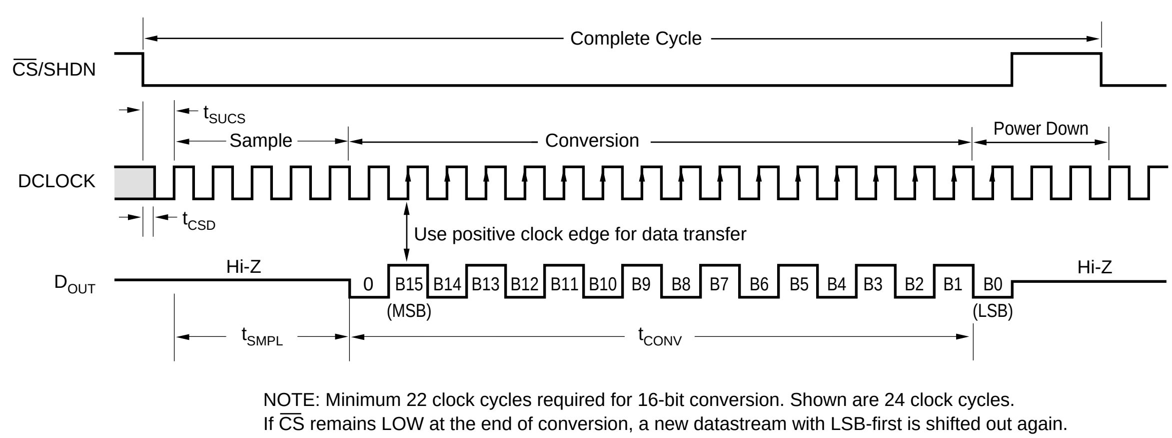


FIGURE 6. ADS8321 Basic Timing Diagrams.

DATA FORMAT

The output data from the ADS8321 is in Binary Two's Complement format as shown in Table II. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
Full-Scale Range	$2 \cdot V_{REF}$		
Least Significant Bit (LSB)	$2 \cdot V_{REF}/65536$	BINARY CODE	HEX CODE
+Full Scale	$+V_{REF}$ – 1 LSB	0111 1111 1111 1111	7FFF
Midscale	0V	0000 0000 0000 0000	0000
Midscale – 1LSB	0V – 1 LSB	1111 1111 1111 1111	FFFF
–Full Scale	$-V_{REF}$	1000 0000 0000 0000	8000

TABLE II. Ideal Input Voltages and Output Codes.

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS8321 to convert at up to a 100kHz rate while requiring very little power. Still, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS8321 scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that will satisfy the requirements of the system.

In addition, the ADS8321 is in power-down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH (see Figure 6). Ideally, each conversion should occur as quickly as possible, preferably at a 2.4MHz clock rate. This way, the converter spends the longest possible time in the power-down mode. This is very important as the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components) but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power down mode is entered.

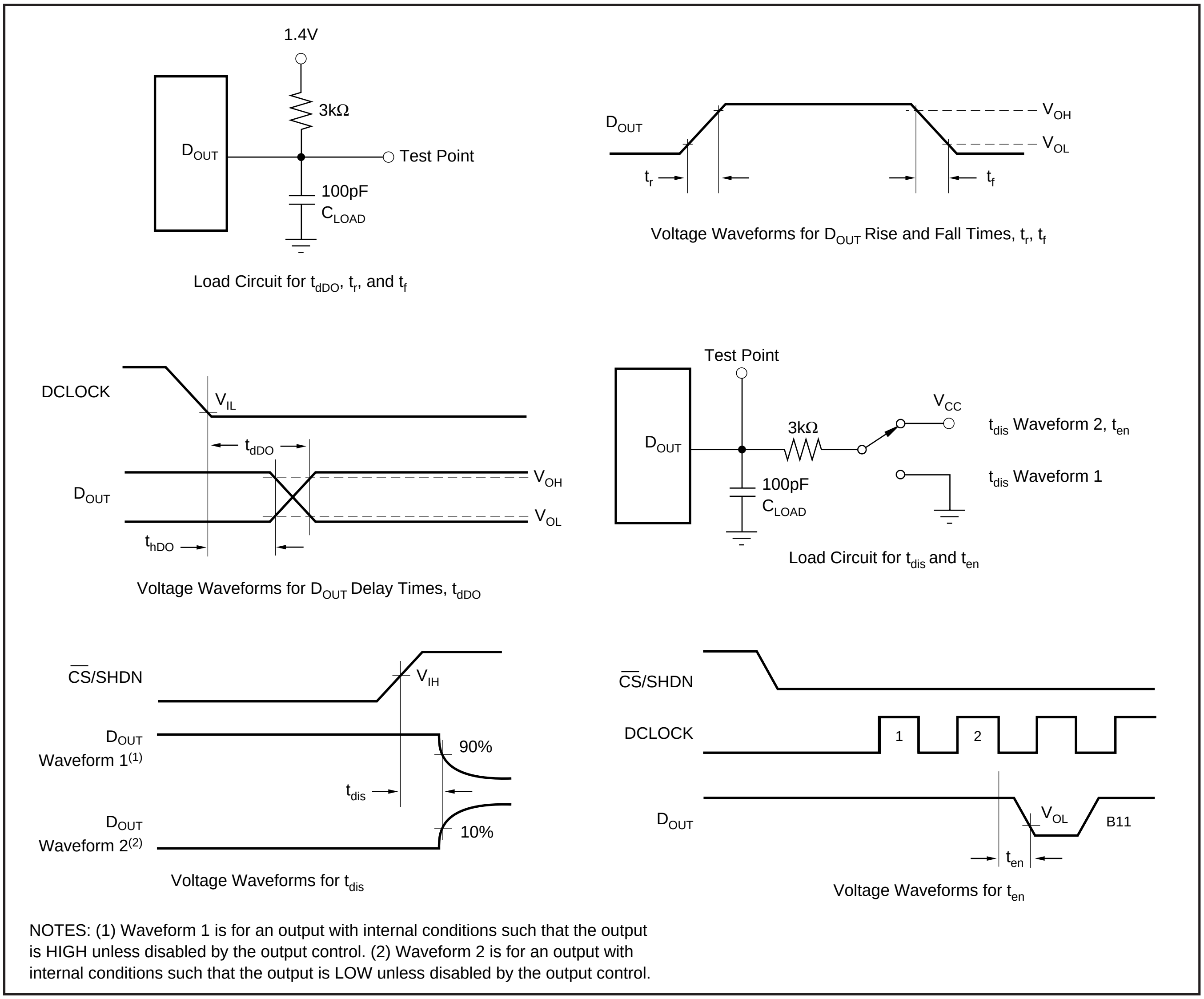


FIGURE 7. Timing Diagrams and Test Circuits for the Parameters in Table I.

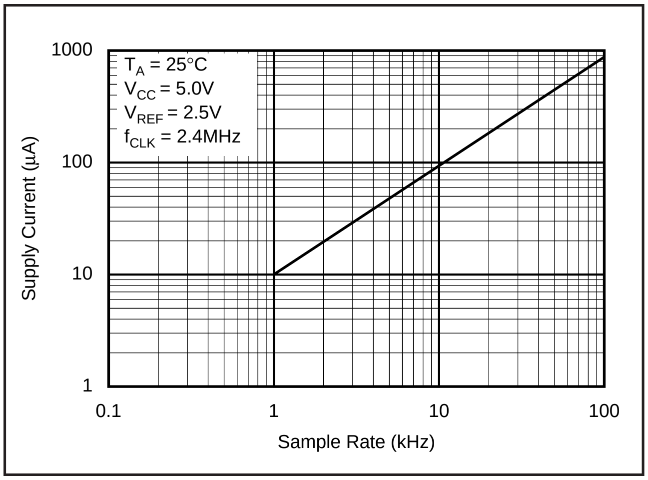


FIGURE 8. Maintaining f_{CLK} at the Highest Possible Rate Allows Supply Current to Drop Linearly with Sample Rate.

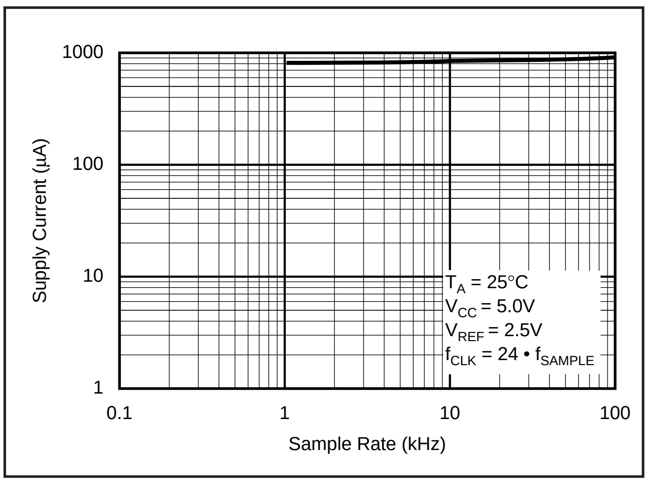


FIGURE 9. Scaling f_{CLK} Reduces Supply Current Only Slightly with Sample Rate.

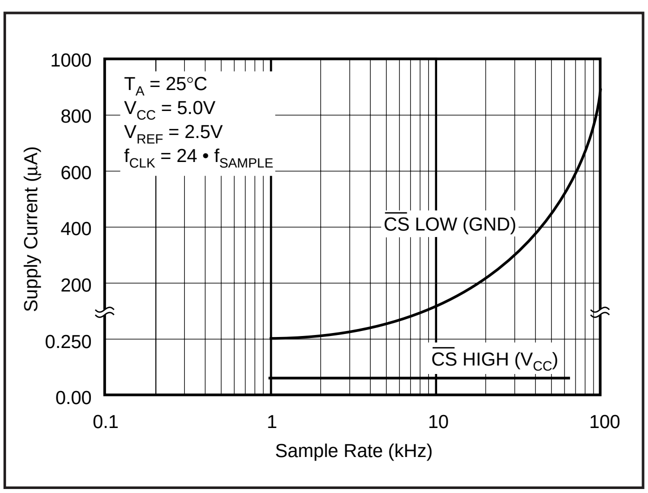


FIGURE 10. Shutdown Current with $\overline{CS}$ HIGH is 50nA Typically, Regardless of the Clock. Shutdown Current with $\overline{CS}$ LOW Varies with Sample Rate.

Figure 8 shows the current consumption of the ADS8321 versus sample rate. For this graph, the converter is clocked at 2.4MHz regardless of the sample rate—$\overline{CS}$ is HIGH for the remaining sample period. Figure 9 also shows current consumption versus sample rate. However, in this case, the DCLOCK period is 1/24th of the sample period—$\overline{CS}$ is HIGH for one DCLOCK cycle out of every 16.

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode which is enabled when $\overline{CS}$ is HIGH. $\overline{CS}$ LOW will shut down only the analog section. The digital section is completely shutdown only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is HIGH. See Figure 10 for more information.

SHORT CYCLING

Another way of saving power is to utilize the $\overline{CS}$ signal to short cycle the conversion. Because the ADS8321 places the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short cycled. This term means that the conversion can be terminated at any time. For example, if only 14 bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ HIGH) after the 14th bit has been clocked out.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 16-bit conversion result may not be needed. If so, the conversion can be terminated after the first n bits, where n might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system, as they spend more time in the power-down mode.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8321 circuitry. This will be particularly true if the reference voltage is low and/or the conversion rate is high. At a 100kHz conversion rate, the ADS8321 makes a bit decision every 416ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 16-bit level all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter's DCLOCK signal—as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS8321 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the ADS8321 package as possible. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, be careful that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS8321 draws very little current from the reference on average, there are still instantaneous current demands placed on the external input and reference circuitry.

Burr-Brown's OPA627 op amp provides optimum performance for buffering both the signal and reference inputs. For low cost, low voltage, single-supply applications, the OPA2350 or OPA2340 dual op amps are recommended.

Also, keep in mind that the ADS8321 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50Hz or 60Hz), can be difficult to remove.

The GND pin on the ADS8321 should be placed on a clean ground point. In many cases, this will be the "analog" ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power supply connection point. The ideal layout will include an analog ground plane for the converter and associated analog circuitry.

APPLICATION CIRCUITS

Figure 11 shows a basic data acquisition system. The ADS8321 input range is 0V to V_{CC}, as the reference input is connected directly to the power supply. The 5Ω resistor and 1µF to 10µF capacitor filter the microcontroller "noise" on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of the noise.

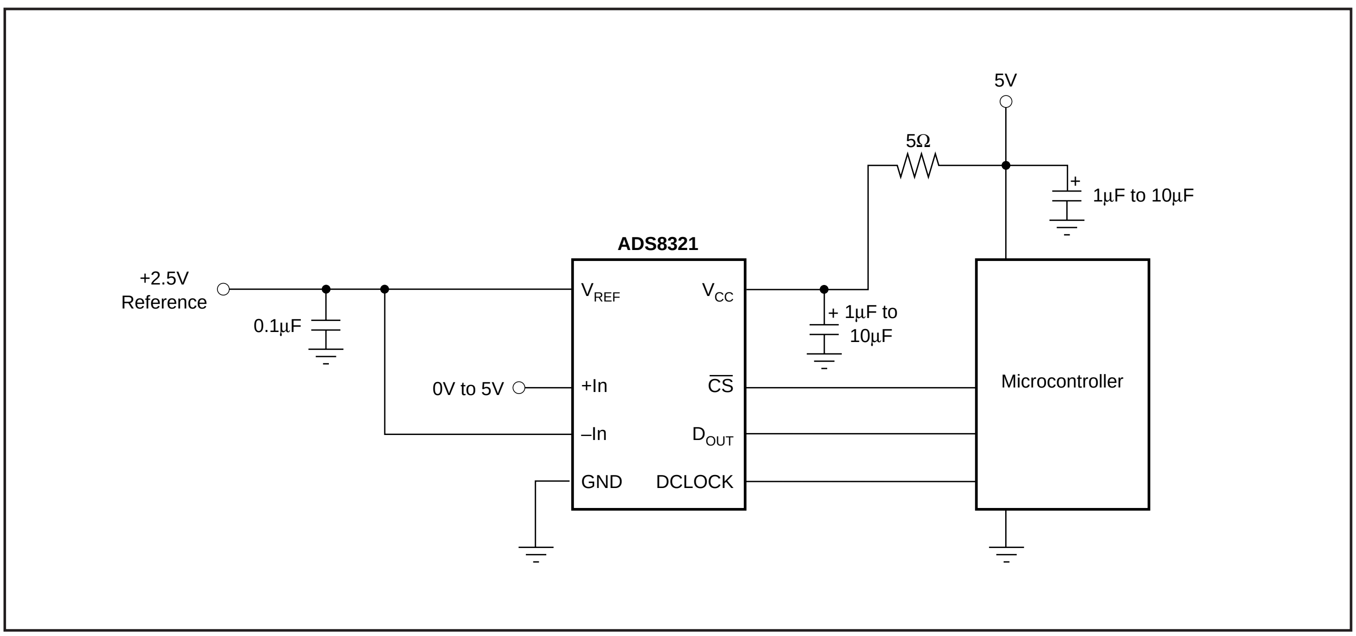


FIGURE 11. Basic Data Acquisition System.