# Dual-Channel, 12-/14-Bit, 65/125/160MSPS Ultralow-Power ADC

**Check for Samples: ADS4222, ADS4225, ADS4226, ADS4242, ADS4245, ADS4246**

## FEATURES

- **Ultralow Power with Single 1.8V Supply, CMOS Output:**
  - **211mW total power at 65MSPS**
  - **326mW total power at 125MSPS**
  - **391mW total power at 160MSPS**
- **High Dynamic Performance:**
  - **82dBc SFDR at 170MHz**
  - **71.2dBFS SNR at 170MHz**
- **Crosstalk: > 90dB at 185MHz**
- **Programmable Gain up to 6dB for SNR/SFDR Trade-off**
- **DC Offset Correction**
- **Output Interface Options:**
  - **1.8V parallel CMOS interface**
  - **Double data rate (DDR) LVDS with programmable swing:**
    - **Standard swing: 350mV**
    - **Low swing: 200mV**
- **Supports Low Input Clock Amplitude Down to 200mV$_{PP}$**
- **Package: QFN-64 (9mm × 9mm)**

## APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**

## DESCRIPTION

The ADS422x/424x are low-speed variants of the ADS42xx ultralow-power family of dual-channel, 12-bit/14-bit analog-to-digital converters (ADCs). Innovative design techniques are used to achieve high-dynamic performance, while consuming extremely low power with 1.8V supply. This topology makes the ADS422x/424x well-suited for multi-carrier, wide-bandwidth communications applications.

The ADS422x/424x have gain options that can be used to improve SFDR performance at lower full-scale input ranges. These devices include a dc offset correction loop that can be used to cancel the ADC offset. Both DDR (double data rate) LVDS and parallel CMOS digital output interfaces are available in a compact QFN-64 PowerPAD™ package.

The devices include internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. All devices are specified over the industrial temperature range (–40°C to +85°C).

**ADS424x/2x Family Comparison(1)**

| | 65MSPS | 125MSPS | 160MSPS | 250MSPS |
|---|---|---|---|---|
| ADS422x 12-bit family | ADS4222 | ADS4225 | ADS4226 | ADS4229 |
| ADS424x 14-bit family | ADS4242 | ADS4245 | ADS4246 | ADS4249 |

(1) See for details on migrating from the ADS62P49 family.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | ECO PLAN(2) | LEAD/BALL FINISH | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|---|---|
| ADS4222(3) | QFN-64 | RGC | –40°C to +85°C | GREEN (RoHS, no Sb/Br) | Cu/NiPdAu | AZ4222 | ADS4222IRGCT | Tape and reel |
| | | | | | | | ADS4222IRGCR | Tape and reel |
| ADS4225(3) | QFN-64 | RGC | –40°C to +85°C | GREEN (RoHS, no Sb/Br) | Cu/NiPdAu | AZ4225 | ADS4225IRGCT | Tape and reel |
| | | | | | | | ADS4225IRGCR | Tape and reel |
| ADS4226 | QFN-64 | RGC | –40°C to +85°C | GREEN (RoHS, no Sb/Br) | Cu/NiPdAu | AZ4226 | ADS4226IRGCT | Tape and reel |
| | | | | | | | ADS4226IRGCR | Tape and reel |
| ADS4242(3) | QFN-64 | RGC | –40°C to +85°C | GREEN (RoHS, no Sb/Br) | Cu/NiPdAu | AZ4242 | ADS4242IRGCT | Tape and reel |
| | | | | | | | ADS4242IRGCR | Tape and reel |
| ADS4245(3) | QFN-64 | RGC | –40°C to +85°C | GREEN (RoHS, no Sb/Br) | Cu/NiPdAu | AZ4245 | ADS4245IRGCT | Tape and reel |
| | | | | | | | ADS4245IRGCR | Tape and reel |
| ADS4246(3) | QFN-64 | RGC | –40°C to +85°C | GREEN (RoHS, no Sb/Br) | Cu/NiPdAu | AZ4246 | ADS4246IRGCT | Tape and reel |
| | | | | | | | ADS4246IRGCR | Tape and reel |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines *Green* to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information.
(3) Product preview device.

The ADS422x/424x are pin-compatible with the previous generation ADS62P49 data converter; this architecture enables easy migration. However, there are some important differences between the two device generations, summarized in Table 1.

**Table 1. Migrating from the ADS62P49**

| ADS62P49 FAMILY | ADS422x/424x FAMILY |
|---|---|
| **PINS** | |
| Pin 22 is NC (not connected) | Pin 22 is AVDD |
| Pins 38 and 58 are DRVDD | Pins 38 and 58 are NC (do not connect pins) |
| Pins 39 and 59 are DRGND | Pins 39 and 59 are NC (do not connect pins) |
| **SUPPLY** | |
| AVDD is 3.3V | AVDD is 1.8V |
| DRVDD is 1.8V | No change |
| **INPUT COMMON-MODE VOLTAGE** | |
| VCM is 1.5V | VCM is 0.95V |
| **SERIAL INTERFACE** | |
| Protocol: 8-bit register address and 8-bit register data | No change in protocol<br>New serial register map |
| **EXTERNAL REFERENCE** | |
| Supported | Not supported |

## ABSOLUTE MAXIMUM RATINGS(1)

| | | ADS422x/424x | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Supply voltage range, AVDD | | –0.3 | 2.1 | V |
| Supply voltage range, DRVDD | | –0.3 | 2.1 | V |
| Voltage between AGND and DRGND | | –0.3 | 0.3 | V |
| Voltage between AVDD to DRVDD (when AVDD leads DRVDD) | | –2.4 | 2.4 | V |
| Voltage between DRVDD to AVDD (when DRVDD leads AVDD) | | –2.4 | 2.4 | V |
| Voltage applied to input pins | INP_A, INM_A, INP_B, INM_B | –0.3 | Minimum (1.9, AVDD + 0.3) | V |
| | CLKP, CLKM(2) | –0.3 | AVDD + 0.3 | V |
| | RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3 | –0.3 | 3.9 | V |
| Operating free-air temperature range, $T_A$ | | –40 | +85 | °C |
| Operating junction temperature range, $T_J$ | | | +125 | °C |
| Storage temperature range, $T_{stg}$ | | –65 | +150 | °C |
| ESD rating | Human body model (HBM) | | 2 | kV |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | ADS42xx RGC 64 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 23.9 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 10.9 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 4.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 4.4 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 0.6 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

| PARAMETER | | ADS422x/424x MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **SUPPLIES** | | | | | |
| Analog supply voltage, AVDD | | 1.7 | 1.8 | 1.9 | V |
| Digital supply voltage, DRVDD | | 1.7 | 1.8 | 1.9 | V |
| **ANALOG INPUTS** | | | | | |
| Differential input voltage range | | | 2 | | $V_{PP}$ |
| Input common-mode voltage | | | VCM ± 0.05 | | V |
| Maximum analog input frequency with $2V_{PP}$ input amplitude(1) | | | 400 | | MHz |
| Maximum analog input frequency with $1V_{PP}$ input amplitude(1) | | | 600 | | MHz |
| **CLOCK INPUT** | | | | | |
| **Input clock sample rate (ADS4222/ADS4242)** | | | | | |
| Low-speed mode enabled (by default after reset) | | 1 | | 65 | MSPS |
| **Input clock sample rate (ADS4225/ADS4245)** | | | | | |
| Low-speed mode enabled(2) | | 1 | | 80 | MSPS |
| Low-speed mode disabled(2) (by default after reset) | | 80 | | 125 | MSPS |
| **Input clock sample rate (ADS4226/ADS4246)** | | | | | |
| Low-speed mode enabled(2) | | 1 | | 80 | MSPS |
| Low-speed mode disabled(2) (by default after reset) | | 80 | | 160 | MSPS |
| Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$) | Sine wave, ac-coupled | 0.2 | 1.5 | | $V_{PP}$ |
| | LVPECL, ac-coupled | | 1.6 | | $V_{PP}$ |
| | LVDS, ac-coupled | | 0.7 | | $V_{PP}$ |
| | LVCMOS, single-ended, ac-coupled | | 1.5 | | V |
| **Input clock duty cycle** | | | | | |
| Low-speed mode disabled | | 35 | 50 | 65 | % |
| Low-speed mode enabled | | 40 | 50 | 60 | % |
| **DIGITAL OUTPUTS** | | | | | |
| Maximum external load capacitance from each output pin to DRGND, $C_{LOAD}$ | | | 5 | | pF |
| Differential load resistance between the LVDS output pairs (LVDS mode), $R_{LOAD}$ | | | 100 | | Ω |
| **HIGH-PERFORMANCE MODES(3)(4)** | | | | | |
| High-performance mode | Set the HIGH PERF MODE register bit to obtain best performance across sample clock and input signal frequencies. Register address = 03h, data = 03h | | | | |
| High-frequency mode | Set the HIGH FREQ MODE CH A and HIGH FREQ MODE CH B register bits for high input signal frequencies greater than 200MHz. Register address = 4Ah, data = 01h Register address = 58h, data = 01h | | | | |
| Operating free-air temperature, $T_A$ | | –40 | | +85 | °C |

(1) See the *Theory of Operation* section in the Application Information.
(2) See the *Serial Interface Configuration* section for details on programming the low-speed mode.
(3) It is recommended to use these modes to obtain best performance.
(4) See the *Serial Interface Configuration* section for details on register programming.

## ELECTRICAL CHARACTERISTICS: ADS4222/ADS4225/ADS4226

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, LVDS interface, and 0dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8V, and DRVDD = 1.8V.

| PARAMETER | | TEST CONDITIONS | ADS4222 (65MSPS) | | | ADS4225 (125MSPS) | | | ADS4226 (160MSPS) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Resolution | | | | | 12 | | | 12 | | | 12 | Bits |
| Signal-to-noise ratio | SNR | $f_{IN}$ = 20MHz | | 70.9 | | | 70.8 | | | 70.5 | | dBFS |
| | | $f_{IN}$ = 70MHz | | 70.3 | | | 70.5 | | | 70.3 | | dBFS |
| | | $f_{IN}$ = 100MHz | | 70.2 | | | 70.3 | | | 70.1 | | dBFS |
| | | $f_{IN}$ = 170MHz | | 69.9 | | | 69.9 | | 67.5 | 69.5 | | dBFS |
| | | $f_{IN}$ = 300MHz | | 68.2 | | | 68.1 | | | 68.2 | | dBFS |
| Signal-to-noise and distortion ratio | SINAD | $f_{IN}$ = 20MHz | | 70.8 | | | 70.7 | | | 70.4 | | dBFS |
| | | $f_{IN}$ = 70MHz | | 70.2 | | | 70.3 | | | 70.1 | | dBFS |
| | | $f_{IN}$ = 100MHz | | 70.1 | | | 70.1 | | | 69.8 | | dBFS |
| | | $f_{IN}$ = 170MHz | | 68.7 | | | 69.5 | | 66.5 | 69.3 | | dBFS |
| | | $f_{IN}$ = 300MHz | | 67.2 | | | 67.5 | | | 67.6 | | dBFS |
| Spurious-free dynamic range | SFDR | $f_{IN}$ = 20MHz | | 91.8 | | | 88.9 | | | 86.6 | | dBc |
| | | $f_{IN}$ = 70MHz | | 88.8 | | | 86.7 | | | 84.7 | | dBc |
| | | $f_{IN}$ = 100MHz | | 87.3 | | | 85.3 | | | 82.2 | | dBc |
| | | $f_{IN}$ = 170MHz | | 85.3 | | | 88.0 | | 70 | 82.0 | | dBc |
| | | $f_{IN}$ = 300MHz | | 74 | | | 78.1 | | | 78.4 | | dBc |
| Total harmonic distortion | THD | $f_{IN}$ = 20MHz | | 88.1 | | | 86.2 | | | 84.4 | | dBc |
| | | $f_{IN}$ = 70MHz | | 85.6 | | | 84.0 | | | 81.6 | | dBc |
| | | $f_{IN}$ = 100MHz | | 85.1 | | | 83.0 | | | 81.2 | | dBc |
| | | $f_{IN}$ = 170MHz | | 82.2 | | | 84.2 | | 68.5 | 80.8 | | dBc |
| | | $f_{IN}$ = 300MHz | | 73.2 | | | 75.5 | | | 76.5 | | dBc |
| Second-harmonic distortion | HD2 | $f_{IN}$ = 20MHz | | 91.8 | | | 88.9 | | | 86.6 | | dBc |
| | | $f_{IN}$ = 70MHz | | 88.8 | | | 86.7 | | | 84.7 | | dBc |
| | | $f_{IN}$ = 100MHz | | 87.3 | | | 85.3 | | | 82.2 | | dBc |
| | | $f_{IN}$ = 170MHz | | 85.3 | | | 88.0 | | 70 | 82.0 | | dBc |
| | | $f_{IN}$ = 300MHz | | 74.0 | | | 78.1 | | | 78.4 | | dBc |
| Third-harmonic distortion | HD3 | $f_{IN}$ = 20MHz | | 95.2 | | | 93.9 | | | 92.3 | | dBc |
| | | $f_{IN}$ = 70MHz | | 90.7 | | | 89.5 | | | 86.4 | | dBc |
| | | $f_{IN}$ = 100MHz | | 96.2 | | | 89.4 | | | 93.2 | | dBc |
| | | $f_{IN}$ = 170MHz | | 87.0 | | | 90.8 | | 70 | 94.2 | | dBc |
| | | $f_{IN}$ = 300MHz | | 81.9 | | | 81.6 | | | 80.7 | | dBc |
| Worst spur (other than second and third harmonics) | | $f_{IN}$ = 20MHz | | 98.9 | | | 95.8 | | | 90.8 | | dBc |
| | | $f_{IN}$ = 70MHz | | 97.5 | | | 94.4 | | | 92.8 | | dBc |
| | | $f_{IN}$ = 100MHz | | 95.2 | | | 93.9 | | | 89.8 | | dBc |
| | | $f_{IN}$ = 170MHz | | 93.1 | | | 91.0 | | 75 | 89.7 | | dBc |
| | | $f_{IN}$ = 300MHz | | 92.7 | | | 89.4 | | | 91.7 | | dBc |
| Two-tone intermodulation distortion | IMD | $f_1$ = 46MHz, $f_2$ = 50MHz, each tone at –7dBFS | | 98 | | | 96.9 | | | 96.2 | | dBFS |
| | | $f_1$ = 185MHz, $f_2$ = 190MHz, each tone at –7dBFS | | 92.9 | | | 92.8 | | | 83.6 | | dBFS |
| Crosstalk | | 20-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel | | 95 | | | 95 | | | 95 | | dB |
| Input overload recovery | | Recovery to within 1% (of full-scale) for 6dB overload with sine-wave input | | 1 | | | 1 | | | 1 | | Clock cycle |
| AC power-supply rejection ratio | PSRR | For 100$mV_{PP}$ signal on AVDD supply, up to 10MHz | | 30 | | | 30 | | | 30 | | dB |
| Effective number of bits | ENOB | $f_{IN}$ = 170MHz | | 11.1 | | | 11.3 | | | 11.2 | | LSBs |
| Differential nonlinearity | DNL | $f_{IN}$ = 170MHz | | ±0.13 | | | ±0.13 | | –0.8 | ±0.13 | 1.5 | LSBs |
| Integrated nonlinearity | INL | $f_{IN}$ = 170MHz | | ±0.5 | | | ±0.5 | | | ±0.5 | 3.5 | LSBs |

## ELECTRICAL CHARACTERISTICS: ADS4242/ADS4245/ADS4246

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, LVDS interface, and 0dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8V, and DRVDD = 1.8V.

| PARAMETER | | TEST CONDITIONS | ADS4242 (65MSPS) | | | ADS4245 (125MSPS) | | | ADS4246 (160MSPS) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Resolution | | | | | 14 | | | 14 | | | 14 | Bits |
| Signal-to-noise ratio | SNR | $f_{IN}$ = 20MHz | | 73.6 | | | 73.4 | | | 72.8 | | dBFS |
| | | $f_{IN}$ = 70MHz | | 72.5 | | | 72.9 | | | 72.5 | | dBFS |
| | | $f_{IN}$ = 100MHz | | 72.3 | | | 72.6 | | | 72.2 | | dBFS |
| | | $f_{IN}$ = 170MHz | | 70.4 | | | 71.4 | | | 71.2 | | dBFS |
| | | $f_{IN}$ = 300MHz | | 69.4 | | | 69.3 | | | 69.4 | | dBFS |
| Signal-to-noise and distortion ratio | SINAD | $f_{IN}$ = 20MHz | | 73.5 | | | 73.2 | | | 72.6 | | dBFS |
| | | $f_{IN}$ = 70MHz | | 72.3 | | | 72.6 | | | 72.1 | | dBFS |
| | | $f_{IN}$ = 100MHz | | 72.1 | | | 72.3 | | | 71.7 | | dBFS |
| | | $f_{IN}$ = 170MHz | | 70.2 | | | 71.2 | | | 70.8 | | dBFS |
| | | $f_{IN}$ = 300MHz | | 68.2 | | | 68.5 | | | 68 | | dBFS |
| Spurious-free dynamic range | SFDR | $f_{IN}$ = 20MHz | | 91.8 | | | 88.9 | | | 86.6 | | dBc |
| | | $f_{IN}$ = 70MHz | | 88.8 | | | 86.7 | | | 84.7 | | dBc |
| | | $f_{IN}$ = 100MHz | | 87.3 | | | 85.3 | | | 82.2 | | dBc |
| | | $f_{IN}$ = 170MHz | | 85.3 | | | 88.0 | | | 82.0 | | dBc |
| | | $f_{IN}$ = 300MHz | | 74 | | | 78.1 | | | 78.4 | | dBc |
| Total harmonic distortion | THD | $f_{IN}$ = 20MHz | | 88.1 | | | 86.2 | | | 84.4 | | dBc |
| | | $f_{IN}$ = 70MHz | | 85.6 | | | 84.0 | | | 81.6 | | dBc |
| | | $f_{IN}$ = 100MHz | | 85.1 | | | 83.0 | | | 81.2 | | dBc |
| | | $f_{IN}$ = 170MHz | | 82.2 | | | 84.2 | | | 80.8 | | dBc |
| | | $f_{IN}$ = 300MHz | | 73.2 | | | 75.5 | | | 76.5 | | dBc |
| Second-harmonic distortion | HD2 | $f_{IN}$ = 20MHz | | 91.8 | | | 88.9 | | | 86.6 | | dBc |
| | | $f_{IN}$ = 70MHz | | 88.8 | | | 86.7 | | | 84.7 | | dBc |
| | | $f_{IN}$ = 100MHz | | 87.3 | | | 85.3 | | | 82.2 | | dBc |
| | | $f_{IN}$ = 170MHz | | 85.3 | | | 88.0 | | | 82.0 | | dBc |
| | | $f_{IN}$ = 300MHz | | 74.0 | | | 78.1 | | | 78.4 | | dBc |
| Third-harmonic distortion | HD3 | $f_{IN}$ = 20MHz | | 95.2 | | | 93.9 | | | 92.3 | | dBc |
| | | $f_{IN}$ = 70MHz | | 90.7 | | | 89.5 | | | 86.4 | | dBc |
| | | $f_{IN}$ = 100MHz | | 96.2 | | | 89.4 | | | 93.2 | | dBc |
| | | $f_{IN}$ = 170MHz | | 87.0 | | | 90.8 | | | 94.2 | | dBc |
| | | $f_{IN}$ = 300MHz | | 81.9 | | | 81.6 | | | 80.7 | | dBc |
| Worst spur (other than second and third harmonics) | | $f_{IN}$ = 20MHz | | 98.9 | | | 95.8 | | | 90.8 | | dBc |
| | | $f_{IN}$ = 70MHz | | 97.5 | | | 94.4 | | | 92.8 | | dBc |
| | | $f_{IN}$ = 100MHz | | 95.2 | | | 93.9 | | | 89.8 | | dBc |
| | | $f_{IN}$ = 170MHz | | 93.1 | | | 91.0 | | | 89.7 | | dBc |
| | | $f_{IN}$ = 300MHz | | 92.7 | | | 89.4 | | | 91.7 | | dBc |
| Two-tone intermodulation distortion | IMD | $f_1$ = 46MHz, $f_2$ = 50MHz, each tone at –7dBFS | | 98 | | | 96.9 | | | 96.2 | | dBFS |
| | | $f_1$ = 185MHz, $f_2$ = 190MHz, each tone at –7dBFS | | 92.2 | | | 92.8 | | | 83.6 | | dBFS |
| Crosstalk | | 20-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel | | 95 | | | 95 | | | 95 | | dB |
| Input overload recovery | | Recovery to within 1% (of full-scale) for 6dB overload with sine-wave input | | 1 | | | 1 | | | 1 | | Clock cycle |
| AC power-supply rejection ratio | PSRR | For 100$mV_{PP}$ signal on AVDD supply, up to 10MHz | | > 30 | | | > 30 | | | > 30 | | dB |
| Effective number of bits | ENOB | $f_{IN}$ = 170MHz | | 11.4 | | | 11.5 | | | 11.5 | | LSBs |
| Differential nonlinearity | DNL | $f_{IN}$ = 170MHz | | ±0.5 | | | ±0.5 | | | ±0.5 | | LSBs |
| Integrated nonlinearity | INL | $f_{IN}$ = 170MHz | | ±2 | | | ±2 | | | ±2 | | LSBs |

## ELECTRICAL CHARACTERISTICS: GENERAL

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, 50% clock duty cycle, and –1dBFS differential analog input, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8V, and DRVDD = 1.8V.

| PARAMETER | ADS4222/ADS4242 (65MSPS) | | | ADS4225/ADS4245 (125MSPS) | | | ADS4226/ADS4246 (160MSPS) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ANALOG INPUTS** | | | | | | | | | | |
| Differential input voltage range (0dB gain) | | 2 | | | 2 | | | 2 | | $V_{PP}$ |
| Differential input resistance (at 200MHz) | | 0.75 | | | 0.75 | | | 0.75 | | kΩ |
| Differential input capacitance (at 200MHz) | | 3.7 | | | 3.7 | | | 3.7 | | pF |
| Analog input bandwidth (with 50Ω source impedance, and 50Ω termination) | | 550 | | | 550 | | | 550 | | MHz |
| Analog input common-mode current (per input pin of each channel) | | 1.5 | | | 1.5 | | | 1.5 | | µA/MSPS |
| Common-mode output voltage VCM | | 0.95 | | | 0.95 | | | 0.95 | | V |
| VCM output current capability | | 4 | | | 4 | | | 4 | | mA |
| **DC ACCURACY** | | | | | | | | | | |
| Offset error | | 2.5 | | | 2.5 | | –15 | 2.5 | 15 | mV |
| Temperature coefficient of offset error | | 0.003 | | | 0.003 | | | 0.003 | | mV/°C |
| Gain error as a result of internal reference inaccuracy alone $E_{GREF}$ | –2 | | 2 | –2 | | 2 | –2 | | 2 | %FS |
| Gain error of channel alone $E_{GCHAN}$ | | ±0.1 | –1 | | ±0.1 | | | ±0.1 | –1 | %FS |
| Temperature coefficient of $E_{GCHAN}$ | | 0.002 | | | 0.002 | | | 0.002 | | Δ%/°C |
| **POWER SUPPLY** | | | | | | | | | | |
| IAVDD<br>Analog supply current | | 73 | | | 105 | | | 123 | 150 | mA |
| IDRVDD<br>Output buffer supply current<br>LVDS interface, 350mV swing with 100Ω external termination, $f_{IN}$ = 2.5MHz | | 96 | | | 99 | | | 111 | 135 | mA |
| IDRVDD<br>Output buffer supply current<br>CMOS interface, 8pF external load capacitance, $f_{IN}$ = 2.5MHz(1) | | 44 | | | 76 | | | 94 | | mA |
| Analog power | | 133 | | | 189 | | | 222 | | mW |
| Digital power<br>LVDS interface, 350mV swing with 100Ω external termination, $f_{IN}$ = 2.5MHz | | 173 | | | 179 | | | 199 | | mW |
| Digital power<br>CMOS interface, 8pF external load capacitance(1)<br>$f_{IN}$ = 2.5MHz | | 80 | | | 137 | | | 169 | | mW |
| Global power-down | | | 25 | | | 25 | | | 25 | mW |

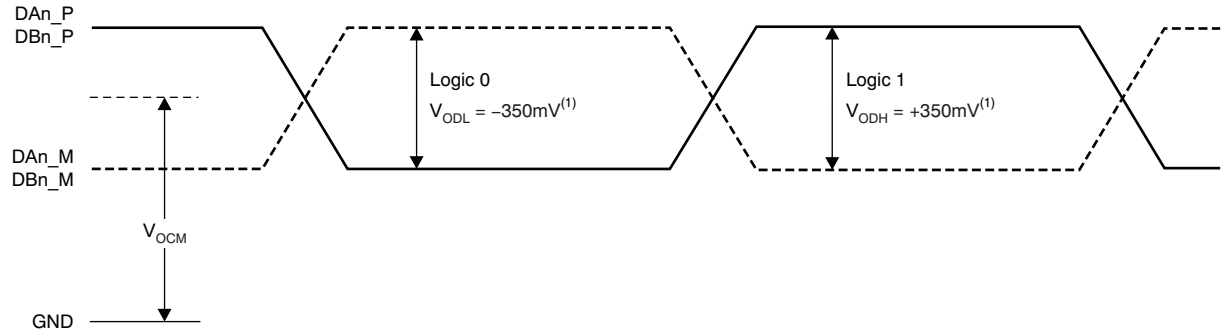
(1) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Application Information*).

## DIGITAL CHARACTERISTICS

At AVDD = 1.8V and DRVDD = 1.8V, unless otherwise noted. DC specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level '0' or '1'.

| PARAMETER | | TEST CONDITIONS | ADS422x/424x MIN | ADS422x/424x TYP | ADS422x/424x MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3)(1)** | | | | | | |
| High-level input voltage | | All digital inputs support 1.8V and 3.3V CMOS logic levels | 1.3 | | | V |
| Low-level input voltage | | | | | 0.4 | V |
| High-level input current | SDATA, SCLK(2) | $V_{HIGH}$ = 1.8V | | 10 | | µA |
| | SEN(3) | $V_{HIGH}$ = 1.8V | | 0 | | µA |
| Low-level input current | SDATA, SCLK | $V_{LOW}$ = 0V | | 0 | | µA |
| | SEN | $V_{LOW}$ = 0V | | 10 | | µA |
| **DIGITAL OUTPUTS, CMOS INTERFACE (DA[13:0], DB[13:0], CLKOUT, SDOUT)** | | | | | | |
| High-level output voltage | | | DRVDD – 0.1 | DRVDD | | V |
| Low-level output voltage | | | | 0 | 0.1 | V |
| Output capacitance (internal to device) | | | | | | pF |
| **DIGITAL OUTPUTS, LVDS INTERFACE** | | | | | | |
| High-level output differential voltage | $V_{ODH}$ | With an external 100Ω termination | 270 | 350 | 430 | mV |
| Low-level output differential voltage | $V_{ODL}$ | With an external 100Ω termination | –430 | –350 | –270 | mV |
| Output common-mode voltage | $V_{OCM}$ | | 0.9 | 1.05 | 1.25 | V |

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.
(2) SDATA, SCLK have internal 150kΩ pull-down resistor.
(3) SEN has an internal 150kΩ pull-up resistor to AVDD. Because the pull-up is weak, SEN can also be driven by 1.8V or 3.3V CMOS buffers.

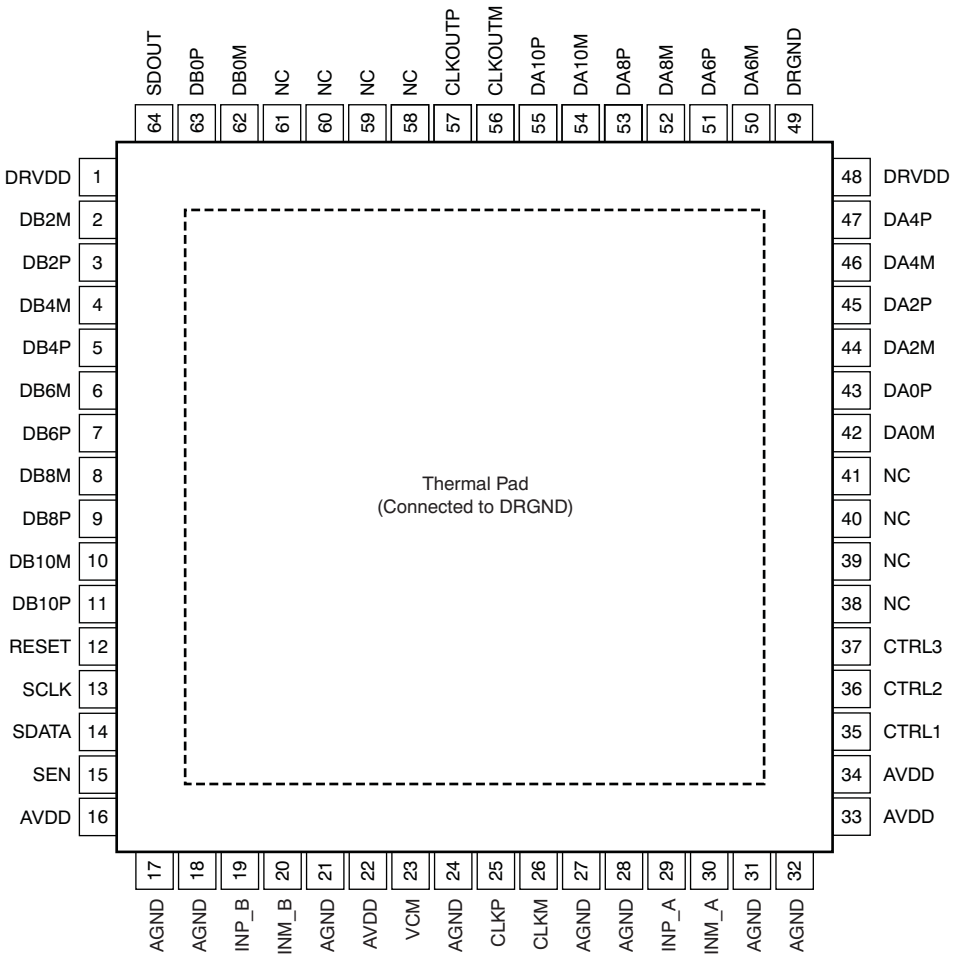



(1) With external 100Ω termination.

**Figure 1. LVDS Output Voltage Levels**

## PIN CONFIGURATION (LVDS MODE)

**RGC PACKAGE(2)**
**QFN-64**
**(TOP VIEW)**

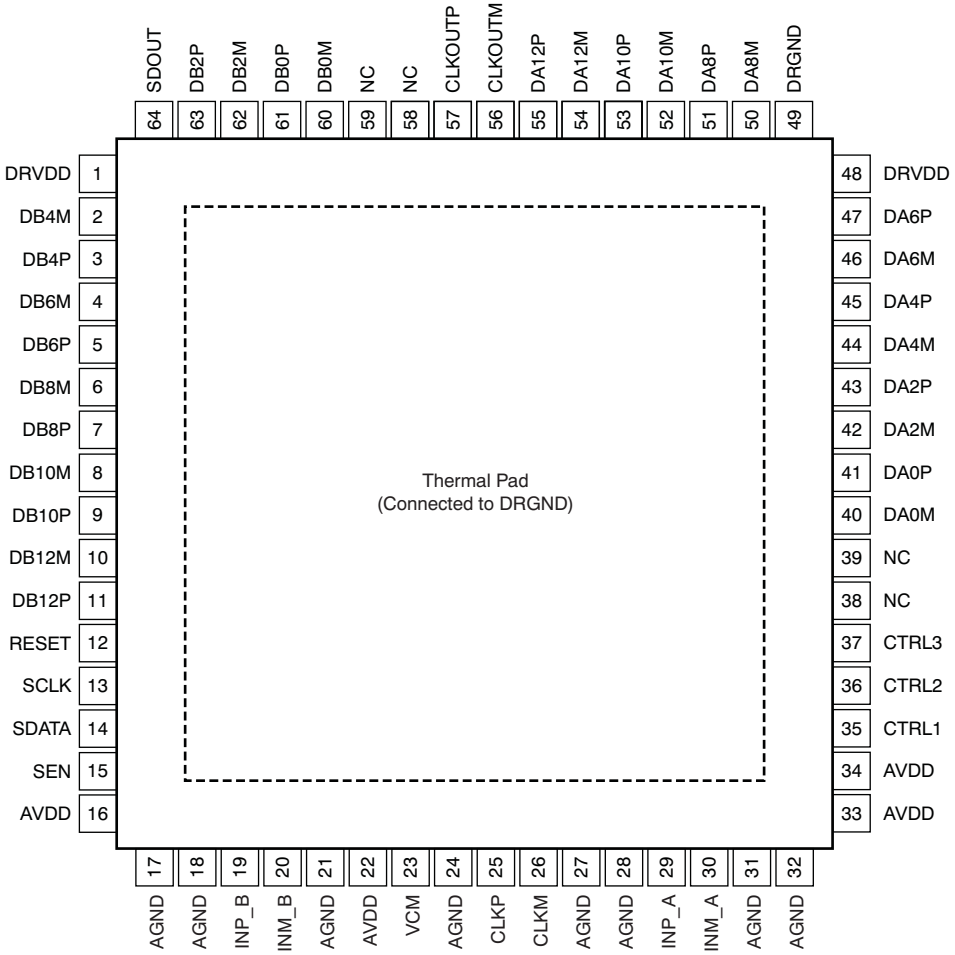



(2) The PowerPAD is connected to DRGND.

NOTE: NC = do not connect.

**Figure 2. ADS4222/ADS4225/ADS4226 LVDS Pinout**

**RGC PACKAGE(3)**
**QFN-64**
**(TOP VIEW)**




(3) The PowerPAD is connected to DRGND.

NOTE: NC = do not connect.

**Figure 3. ADS4242/ADS4245/ADS4246 LVDS Pinout**

**Pin Descriptions (LVDS Mode)**

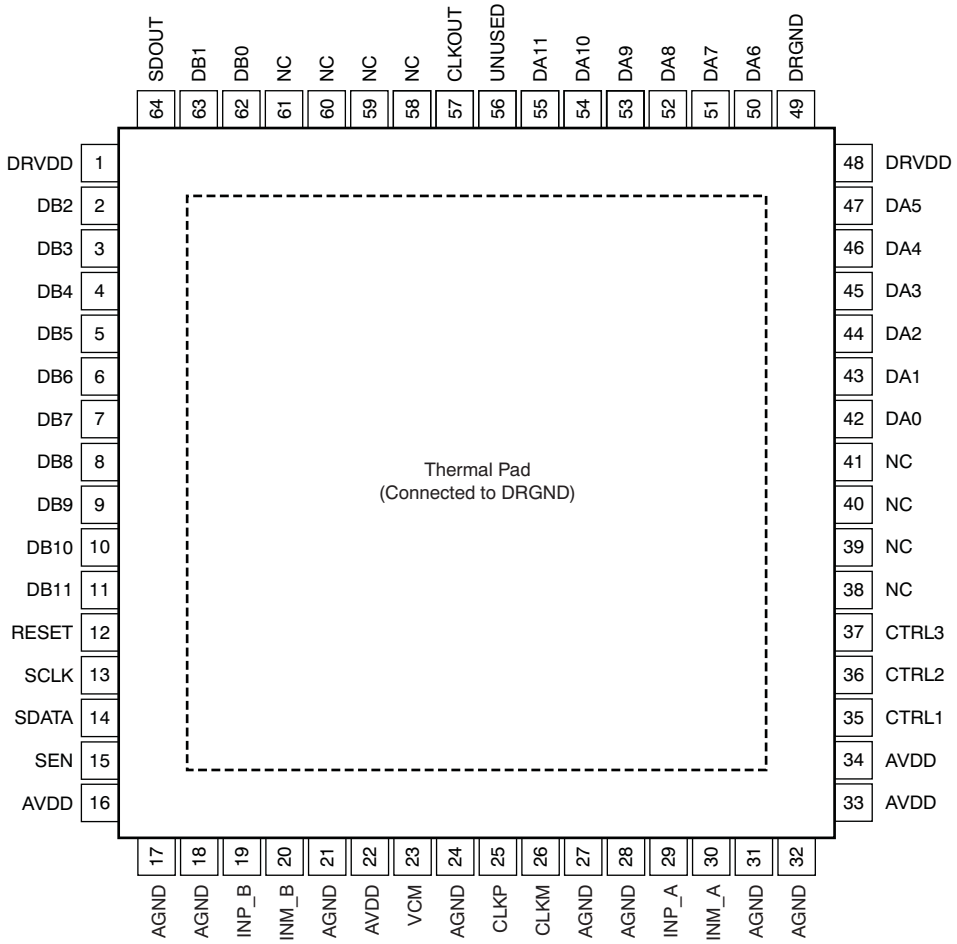
| PIN NAME | PIN NUMBER | # OF PINS | FUNCTION | DESCRIPTION |
|---|---|---|---|---|
| AVDD | 16, 22, 33, 34 | 4 | Input | Analog power supply |
| AGND | 17, 18, 21, 24, 27, 28, 31, 32 | 8 | Input | Analog ground |
| CLKP | 25 | 1 | Input | Differential clock positive input |
| CLKM | 26 | 1 | Input | Differential clock negative input |
| INP_A | 29 | 1 | Input | Differential analog positive input, channel A |
| INM_A | 30 | 1 | Input | Differential analog negative input, channel A |
| INP_B | 19 | 1 | Input | Differential analog positive input, channel B |
| INM_B | 20 | 1 | Input | Differential analog negative input, channel B |
| VCM | 23 | 1 | Output | This pin outputs the common-mode voltage (0.95V) that can be used externally to bias the analog input pins |

## Pin Descriptions (LVDS Mode) (continued)

| PIN NAME | PIN NUMBER | # OF PINS | FUNCTION | DESCRIPTION |
|---|---|---|---|---|
| RESET | 12 | 1 | Input | Serial interface RESET input.<br>When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section.<br>In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 150kΩ pull-down resistor. |
| SCLK | 13 | 1 | Input | This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode selection when RESET is tied high; see Table 5 for detailed information. This pin has an internal 150kΩ pull-down resistor. |
| SDATA | 14 | 1 | Input | Serial interface data input; this pin has an internal 150kΩ pull-down resistor. |
| SEN | 15 | 1 | Input | This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 6 for detailed information. This pin has an internal 150kΩ pull-up resistor to AVDD. |
| SDOUT | 64 | 1 | Output | This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin forces a logic low and is not put in 3-state. |
| CTRL1 | 35 | 1 | Input | Digital control input pins. Together, they control the various power-down modes. |
| CTRL2 | 36 | 1 | Input | Digital control input pins. Together, they control the various power-down modes. |
| CTRL3 | 37 | 1 | Input | Digital control input pins. Together, they control the various power-down modes. |
| CLKOUTP | 57 | 1 | Output | Differential output clock, true |
| CLKOUTM | 56 | 1 | Output | Differential output clock, complement |
| DA0P, DA0M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel A differential output data pair, D0 and D1 multiplexed |
| DA2P, DA2M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel A differential output data D2 and D3 multiplexed |
| DA4P, DA4M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel A differential output data D4 and D5 multiplexed |
| DA6P, DA6M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel A differential output data D6 and D7 multiplexed |
| DA8P, DA8M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel A differential output data D8 and D9 multiplexed |
| DA10P, DA10M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel A differential output data D10 and D11 multiplexed |
| DA12P, DA12M | Refer to Figure 3 | 2 | Output | Channel A differential output data D12 and D13 multiplexed (ADS424x only) |
| DB0P, DB0M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel B differential output data pair, D0 and D1 multiplexed |
| DB2P, DB2M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel B differential output data D2 and D3 multiplexed |
| DB4P, DB4M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel B differential output data D4 and D5 multiplexed |
| DB6P, DB6M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel B differential output data D6 and D7 multiplexed |
| DB8P, DB8M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel B differential output data D8 and D9 multiplexed |
| DB10P, DB10M | Refer to Figure 2 and Figure 3 | 2 | Output | Channel B differential output data D10 and D11 multiplexed |
| DB12P, DB12M | Refer to Figure 3 | 2 | Output | Channel B differential output data D12 and D13 multiplexed (ADS424x only) |
| DRVDD | 1, 48 | 2 | Input | Output buffer supply |
| DRGND | 49, PAD | 2 | Input | Output buffer ground |
| NC | Refer to Figure 98, Figure 99, Figure 116, and Figure 117 | 8 (ADS422x)<br>4 (ADS424x) | — | Do not connect |

## PIN CONFIGURATION (CMOS MODE)

**RGC PACKAGE(4)**
**QFN-64**
**(TOP VIEW)**

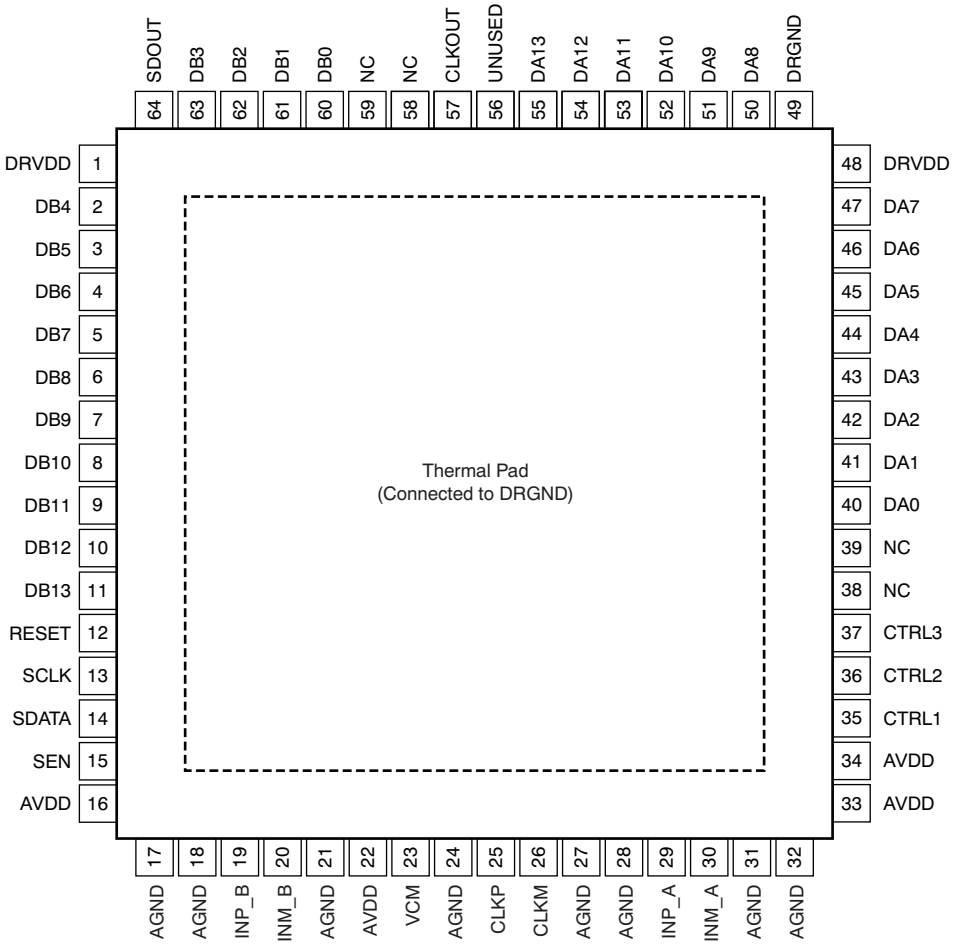



(4) The PowerPAD is connected to DRGND.

NOTE: NC = do not connect.

**Figure 4. ADS4222/ADS4225/ADS4226 CMOS Pinout**

**RGC PACKAGE(5)**
**QFN-64**
**(TOP VIEW)**




(5) The PowerPAD is connected to DRGND.

NOTE: NC = do not connect.

**Figure 5. ADS4242/ADS4245/ADS4246 CMOS Pinout**

## Pin Descriptions (CMOS Mode)

| PIN NAME | PIN NUMBER | # OF PINS | FUNCTION | DESCRIPTION |
|---|---|---|---|---|
| AVDD | 16, 22, 33, 34 | 4 | Input | Analog power supply |
| AGND | 17, 18, 21, 24, 27, 28, 31, 32 | 8 | Input | Analog ground |
| CLKP | 25 | 1 | Input | Differential clock positive input |
| CLKM | 26 | 1 | Input | Differential clock negative input |
| INP_A | 29 | 1 | Input | Differential analog positive input, channel A |
| INM_A | 30 | 1 | Input | Differential analog negative input, channel A |
| INP_B | 19 | 1 | Input | Differential analog positive input, channel B |
| INM_B | 20 | 1 | Input | Differential analog negative input, channel B |
| VCM | 23 | 1 | Output | This pin outputs the common-mode voltage (0.95V) that can be used externally to bias the analog input pins |
| RESET | 12 | 1 | Input | Serial interface RESET input.<br>When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section.<br>In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 150kΩ pull-down resistor. |
| SCLK | 13 | 1 | Input | This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high; see Table 5 for detailed information. This pin has an internal 150kΩ pull-down resistor. |
| SDATA | 14 | 1 | Input | Serial interface data input; this pin has an internal 150kΩ pull-down resistor. |
| SEN | 15 | 1 | Input | This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 6 for detailed information. This pin has an internal 150kΩ pull-up resistor to AVDD. |
| SDOUT | 64 | 1 | Output | This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin forces a logic low and is not put in 3-state. |
| CTRL1 | 35 | 1 | Input | Digital control input pins. Together, they control various power-down modes. |
| CTRL2 | 36 | 1 | Input | Digital control input pins. Together, they control various power-down modes. |
| CTRL3 | 37 | 1 | Input | Digital control input pins. Together, they control various power-down modes. |
| CLKOUT | 57 | 1 | Output | CMOS output clock |
| DA0 to DA11 | Refer to Figure 4 and Figure 5 | 12 | Output | Channel A ADC output data bits, CMOS levels |
| DA12 to DA13 | Refer to Figure 5 | 2 | Output | Channel A ADC output data bits, CMOS levels (ADS424x only) |
| DB0 to DB11 | Refer to Figure 4 and Figure 5 | 12 | Output | Channel B ADC output data bits, CMOS levels |
| DB12 to DB13 | Refer to Figure 5 | 2 | Output | Channel B ADC output data bits, CMOS levels (ADS424x only) |
| DRVDD | 1, 48 | 2 | Input | Output buffer supply |
| DRGND | 49, PAD | 2 | Input | Output buffer ground |
| NC | | 1 | — | Do not connect |
| UNUSED | 56 | 1 | — | This pin is not used in the CMOS interface |

## FUNCTIONAL BLOCK DIAGRAM

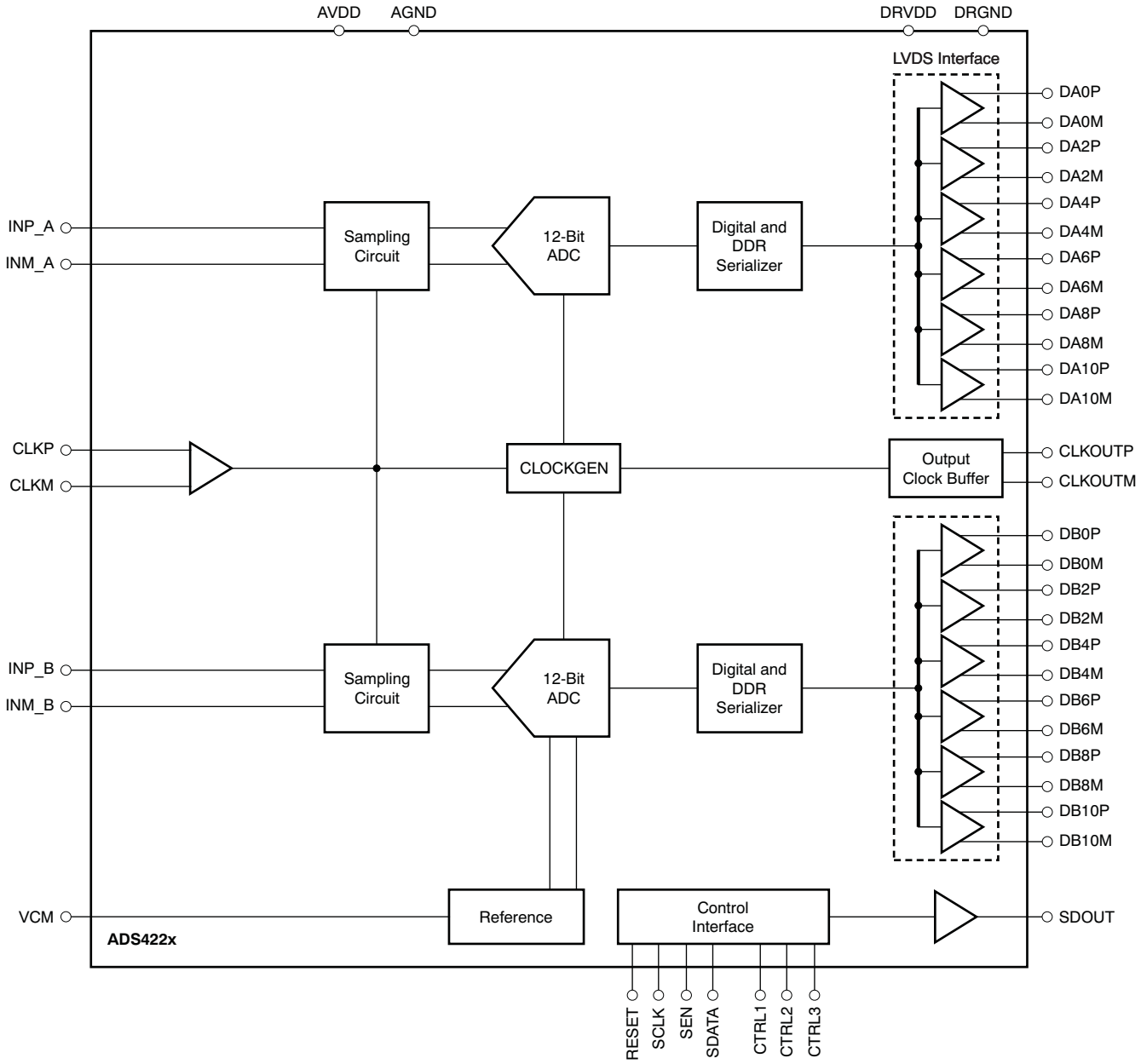



**Figure 6. ADS4222/25/26 Block Diagram**

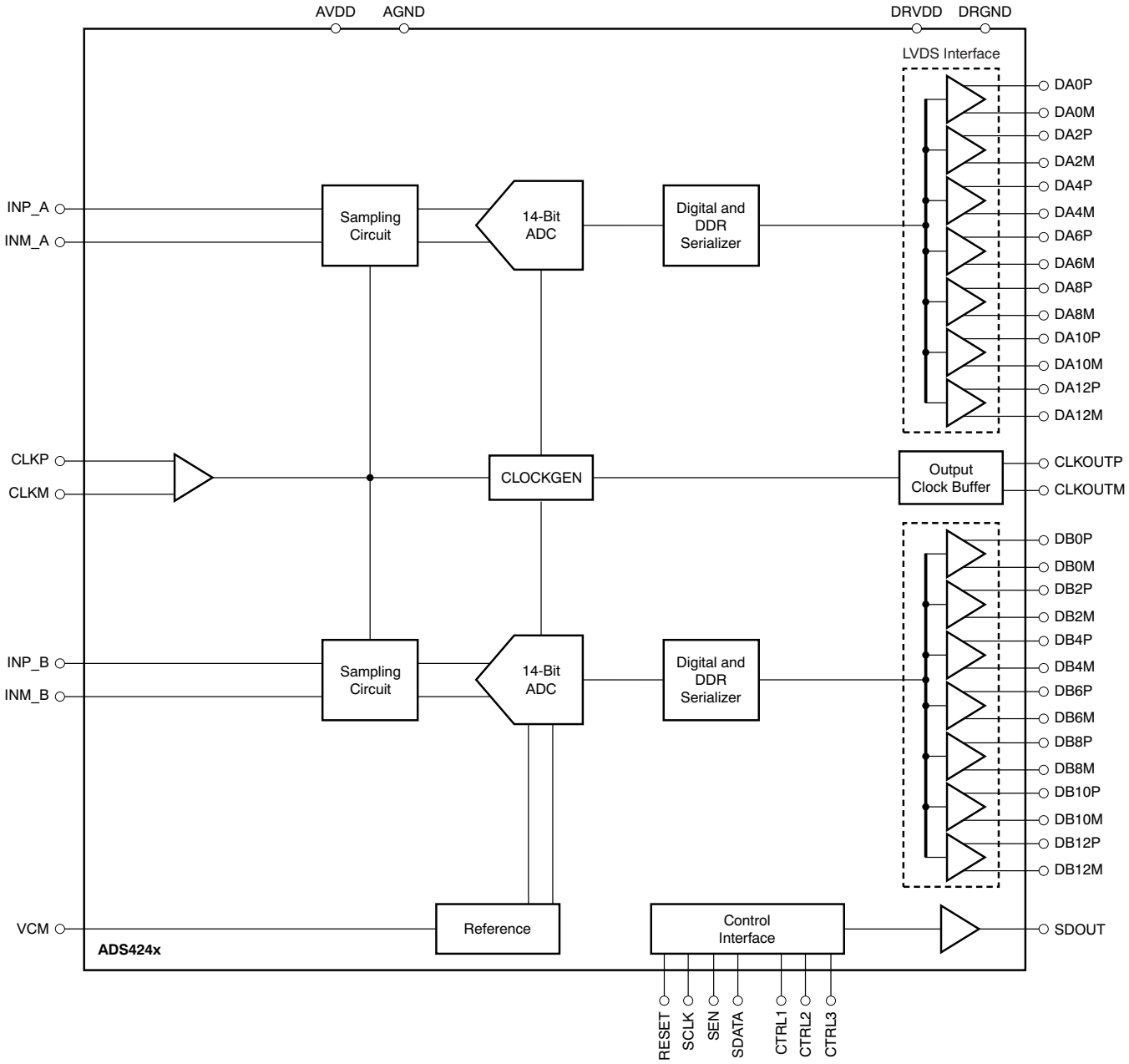



**Figure 7. ADS4242/45/46 Block Diagram**

## TIMING CHARACTERISTICS: LVDS AND CMOS MODES(1)

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8V, sampling frequency = 160MSPS, sine wave input clock, $1.5V_{PP}$ clock amplitude, $C_{LOAD}$ = 5pF(2), and $R_{LOAD}$ = 100Ω(3), unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8V, and DRVDD = 1.7V to 1.9V.

| PARAMETER | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_A$ | Aperture delay | | 0.5 | 0.8 | 1.1 | ns |
| | Aperture delay matching | Between the two channels of the same device | | ±70 | | ps |
| | Variation of aperture delay | Between two devices at the same temperature and DRVDD supply | | ±150 | | ps |
| $t_J$ | Aperture jitter | | | 140 | | $f_S$ rms |
| | Wakeup time | Time to valid data after coming out of STANDBY mode | | 50 | 100 | µs |
| | | Time to valid data after coming out of GLOBAL power-down mode | | 100 | 500 | µs |
| | ADC latency(4) | Default latency after reset | | 16 | | Clock cycles |
| | | Digital functions enabled (EN DIGITAL = 1) | | 24 | | Clock cycles |
| **DDR LVDS MODE(5)** | | | | | | |
| $t_{SU}$ | Data setup time | Data valid(6) to zero-crossing of CLKOUTP | 1.5 | 2.0 | | ns |
| $t_H$ | Data hold time | Zero-crossing of CLKOUTP to data becoming invalid(6) | 0.35 | 0.6 | | ns |
| $t_{PDI}$ | Clock propagation delay | Input clock rising edge cross-over to output clock rising edge cross-over | 5.0 | 6.1 | 7.5 | ns |
| | LVDS bit clock duty cycle | Duty cycle of differential clock, (CLKOUTP-CLKOUTM) | | 49 | | % |
| $t_{RISE}$, $t_{FALL}$ | Data rise time, Data fall time | Rise time measured from –100mV to +100mV<br>Fall time measured from +100mV to –100mV<br>*1MSPS ≤ Sampling frequency ≤ 160MSPS* | | 0.13 | | ns |
| $t_{CLKRISE}$, $t_{CLKFALL}$ | Output clock rise time, Output clock fall time | Rise time measured from –100mV to +100mV<br>Fall time measured from +100mV to –100mV<br>*1MSPS ≤ Sampling frequency ≤ 160MSPS* | | 0.13 | | ns |
| **PARALLEL CMOS MODE** | | | | | | |
| $t_{SU}$ | Data setup time | Data valid(7) to zero-crossing of CLKOUT | 1.6 | 2.5 | | ns |
| $t_H$ | Data hold time | Zero-crossing of CLKOUT to data becoming invalid(7) | 2.3 | 2.7 | | ns |
| $t_{PDI}$ | Clock propagation delay | Input clock rising edge cross-over to output clock rising edge cross-over | 4.5 | 6.4 | 8.5 | ns |
| | Output clock duty cycle | Duty cycle of output clock, CLKOUT<br>*1MSPS ≤ Sampling frequency ≤ 160MSPS* | | 46 | | % |
| $t_{RISE}$, $t_{FALL}$ | Data rise time, Data fall time | Rise time measured from 20% to 80% of DRVDD<br>Fall time measured from 80% to 20% of DRVDD<br>*1MSPS ≤ Sampling frequency ≤ 160MSPS* | | 1 | | ns |
| $t_{CLKRISE}$, $t_{CLKFALL}$ | Output clock rise time<br>Output clock fall time | Rise time measured from 20% to 80% of DRVDD<br>Fall time measured from 80% to 20% of DRVDD<br>*1MSPS ≤ Sampling frequency ≤ 160MSPS* | | 1 | | ns |

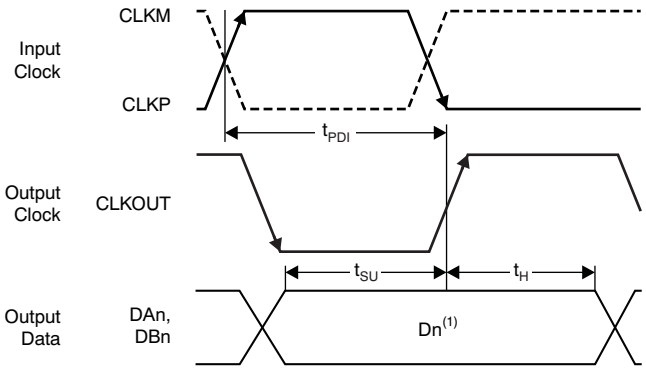
(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) $C_{LOAD}$ is the effective external single-ended load capacitance between each output pin and ground
(3) $R_{LOAD}$ is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, $t_{PDI}$ is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to a logic high of +100mV and a logic low of –100mV.
(7) Data valid refers to a logic high of 1.26V and a logic low of 0.54V

**Table 2. LVDS Timings at Lower Sampling Frequencies**

| SAMPLING FREQUENCY (MSPS) | SETUP TIME (ns) | | | HOLD TIME (ns) | | | $t_{PDI}$, CLOCK PROPAGATION DELAY (ns) | | |
|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 5.9 | 6.6 | | 0.35 | 0.6 | | 5.0 | 6.1 | 7.5 |
| 80 | 4.5 | 5.2 | | 0.35 | 0.6 | | 5.0 | 6.1 | 7.5 |
| 105 | 3.1 | 3.6 | | 0.35 | 0.6 | | 5.0 | 6.1 | 7.5 |
| 125 | 2.3 | 2.9 | | 0.35 | 0.6 | | 5.0 | 6.1 | 7.5 |
| 150 | 1.7 | 2.2 | | 0.35 | 0.6 | | 5.0 | 6.1 | 7.5 |

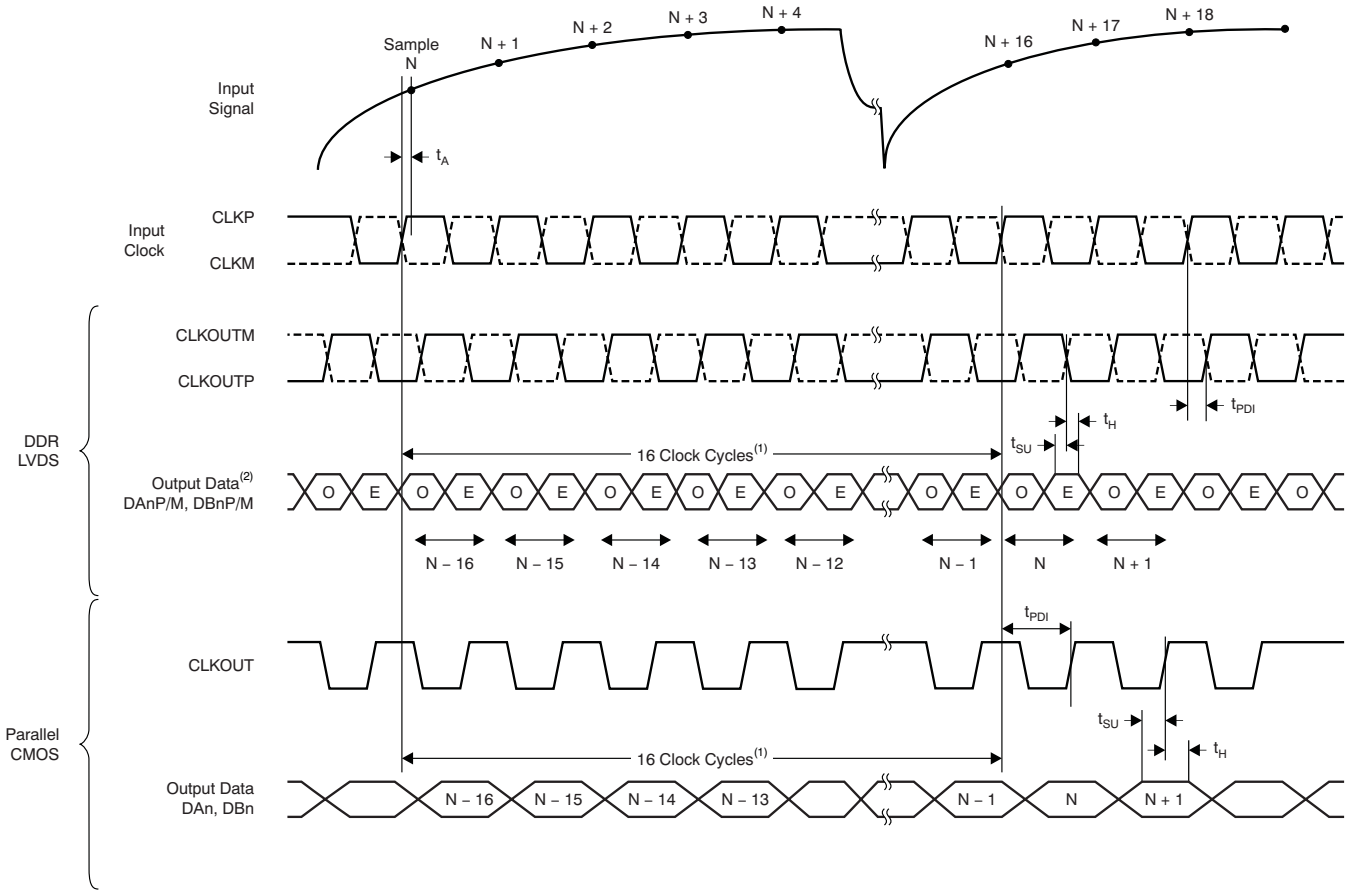
**Table 3. CMOS Timings at Lower Sampling Frequencies**

| SAMPLING FREQUENCY (MSPS) | TIMINGS SPECIFIED WITH RESPECT TO CLKOUT | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | SETUP TIME (ns) | | | HOLD TIME (ns) | | | $t_{PDI}$, CLOCK PROPAGATION DELAY (ns) | | |
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 6.1 | 7.2 | | 6.7 | 7.1 | | 4.5 | 6.4 | 8.5 |
| 80 | 4.7 | 5.8 | | 5.3 | 5.8 | | 4.5 | 6.4 | 8.5 |
| 105 | 3.4 | 4.3 | | 3.8 | 4.3 | | 4.5 | 6.4 | 8.5 |
| 125 | 2.7 | 3.6 | | 3.1 | 3.6 | | 4.5 | 6.4 | 8.5 |
| 150 | 1.9 | 2.8 | | 2.5 | 2.9 | | 4.5 | 6.4 | 8.5 |




(1) Dn = bits D0, D1, D2, etc. of channels A and B.

**Figure 8. CMOS Interface Timing Diagram**




(1) ADC latency after reset. At higher sampling frequencies, $t_{PDI}$ is greater than one clock cycle, which then makes the overall latency = ADC latency + 1.

(2) E = even bits (D0, D2, D4, etc.); O = odd bits (D1, D3, D5, etc.).

**Figure 9. Latency Timing Diagram**

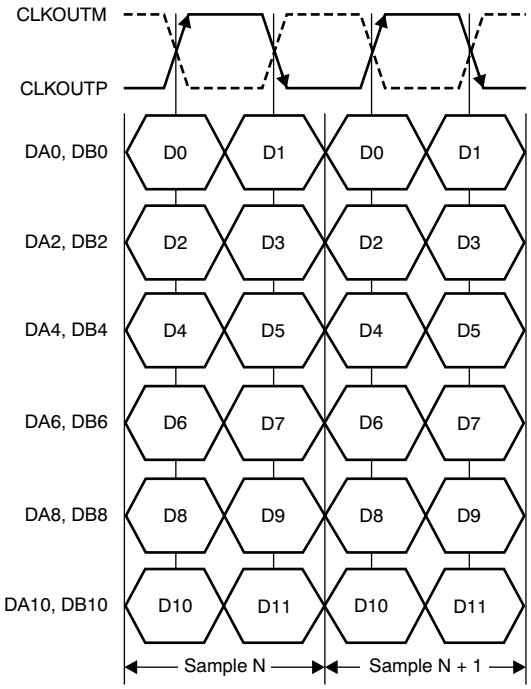



**Figure 10. ADS4222/25/26 LVDS Interface Timing Diagram**

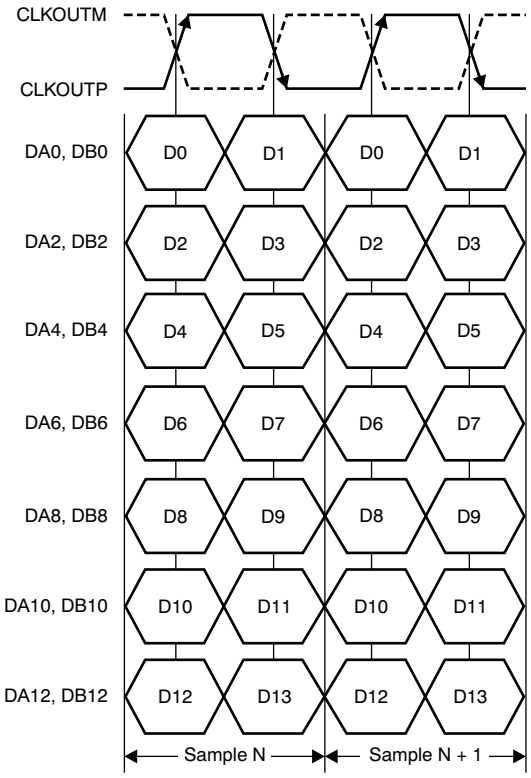



**Figure 11. ADS4242/45/46 LVDS Interface Timing Diagram**

## DEVICE CONFIGURATION

The ADS422x/424x can be configured independently using either parallel interface control or serial interface programming.

### PARALLEL CONFIGURATION ONLY

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 4 to Table 7). There is no need to apply a reset and SDATA can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Some frequently-used functions can be controlled using these pins. Table 4 describes the modes controlled by the parallel pins.

**Table 4. Parallel Pin Definition**

| PIN | CONTROL MODE |
|---|---|
| SCLK | Low-speed mode selection |
| SEN | Output data format and output interface selection |
| CTRL1 | Together, these pins control the power-down modes |
| CTRL2 | |
| CTRL3 | |

### SERIAL INTERFACE CONFIGURATION ONLY

To enable this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The *Serial Register Map* section describes the register programming and the register reset process in more detail.

### USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this option, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these pins (see Table 7). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RESET bit to '1'. After reset, the RESET pin must be kept low. The *Serial Register Map* section describes register programming and the register reset process in more detail.

## PARALLEL CONFIGURATION DETAILS

The functions controlled by each parallel pin are described in Table 5, Table 6, and Table 7. A simple way of configuring the parallel pins is shown in Figure 12.

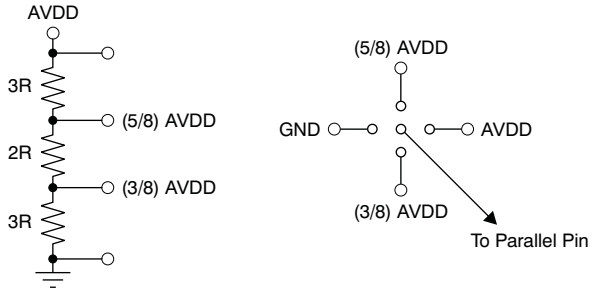



**Figure 12. Simple Scheme to Configure the Parallel Pins**

**Table 5. SCLK Control Pin**

| VOLTAGE APPLIED ON SCLK | DESCRIPTION |
|---|---|
| Low | Low-speed mode is disabled |
| High | Low-speed mode is enabled(1) |

(1) Low-speed mode is enabled in the ADS4222/42 by default.

**Table 6. SEN Control Pin**

| VOLTAGE APPLIED ON SEN | DESCRIPTION |
|---|---|
| 0<br>(+50mV/0mV) | Twos complement and parallel CMOS output |
| (3/8) AVDD<br>(±50mV) | Offset binary and parallel CMOS output |
| (5/8) 2AVDD<br>(±50mV) | Offset binary and DDR LVDS output |
| AVDD<br>(0mV/–50mV) | Twos complement and DDR LVDS output |

**Table 7. CTRL1, CTRL2, and CTRL3 Pins**

| CTRL1 | CTRL2 | CTRL3 | DESCRIPTION |
|---|---|---|---|
| Low | Low | Low | Normal operation |
| Low | Low | High | Not available |
| Low | High | Low | Not available |
| Low | High | High | Not available |
| High | Low | Low | Global power-down |
| High | Low | High | Channel A standby, channel B is active |
| High | High | Low | Not available |
| High | High | High | MUX mode of operation, channel A and B data are multiplexed and output on the DB[13:0] pins. |

## SERIAL INTERFACE DETAILS

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

### Register Initialization

After power-up, the internal registers must be initialized to the default values. Initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET pin (of width greater than 10ns), as shown in Figure 13; or
2. By applying a software reset. When using the serial interface, set the RESET bit high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

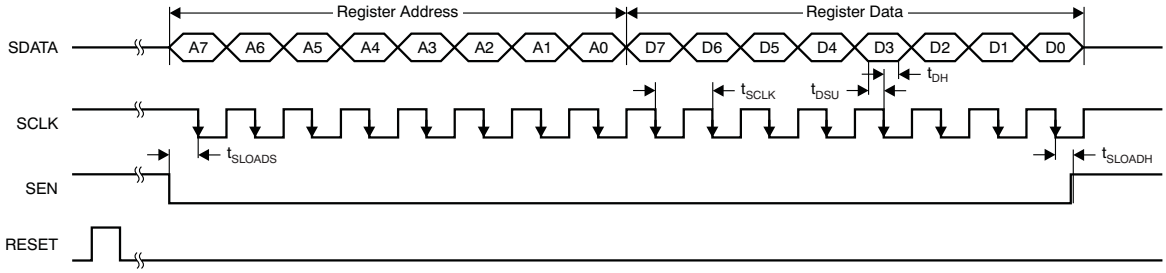



**Figure 13. Serial Interface Timing**

**Table 8. Serial Interface Timing Characteristics(1)**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK frequency (equal to $1/t_{SCLK}$) | > DC | | 20 | MHz |
| $t_{SLOADS}$ | SEN to SCLK setup time | 25 | | | ns |
| $t_{SLOADH}$ | SCLK to SEN hold time | 25 | | | ns |
| $t_{DSU}$ | SDATA setup time | 25 | | | ns |
| $t_{DH}$ | SDATA hold time | 25 | | | ns |

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8V, and DRVDD = 1.8V, unless otherwise noted.

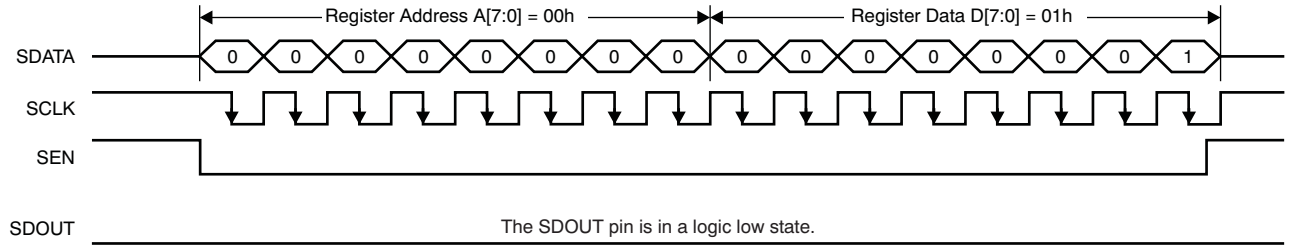
### Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. To use readback mode, follow this procedure:

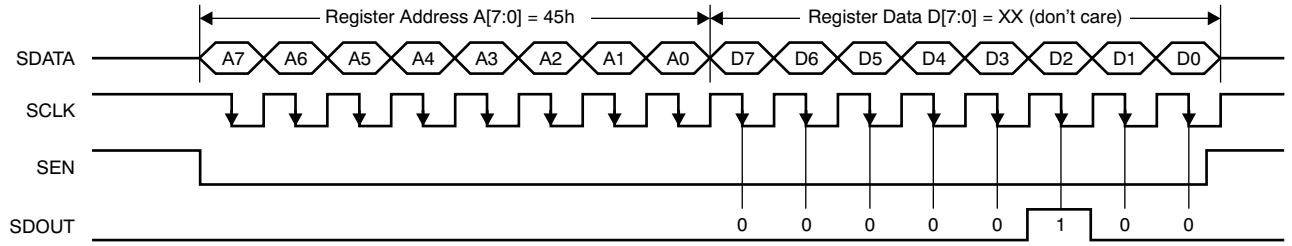
1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 64).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to '0'.

The serial register readout works with both CMOS and LVDS interfaces on pin 64.

When READOUT is disabled, the SDOUT pin is in a logic low state. If serial readout is not used, the SDOUT pin must float.




**a) Enable serial readout (READOUT = 1)**



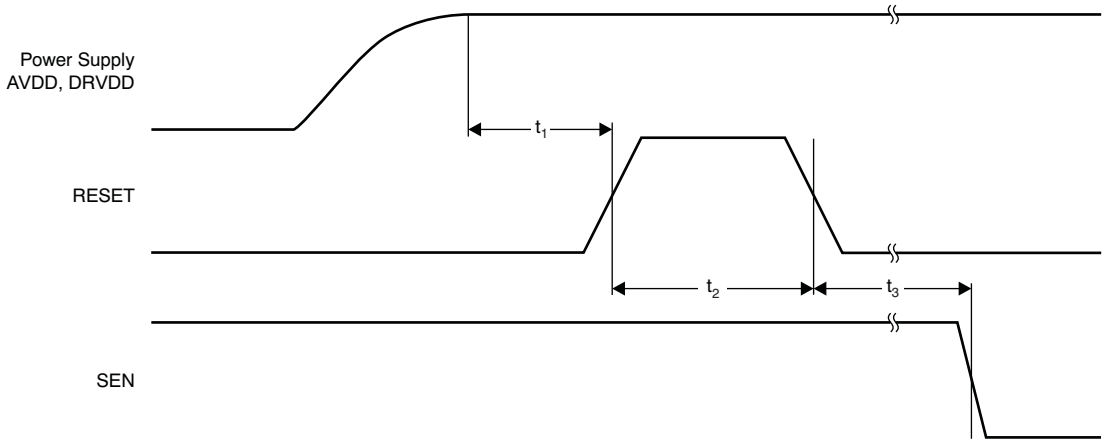

**b) Read contents of Register 45h. This register has been initialized with 04h (device is put into global power-down mode.)**

**Figure 14. Serial Readout Timing Diagram**

**Table 9. Reset Timing (Only when Serial Interface is Used)(1)**

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_1$ | Power-on delay | Delay from AVDD and DRVDD power-up to active RESET pulse | 1 | | | ms |
| $t_2$ | Reset pulse width | Active RESET signal pulse width | 10 | | | ns |
| | | | | | 1 | µs |
| $t_3$ | Register write delay | Delay from RESET disable to SEN active | 100 | | | ns |

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, unless otherwise noted.




NOTE: A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

**Figure 15. Reset Timing Diagram**

## SERIAL REGISTER MAP

Table 10 summarizes the functions supported by the serial interface.

**Table 10. Serial Interface Register Map(1)**

| REGISTER ADDRESS | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| A[7:0] (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | RESET | READOUT |
| 01 | LVDS SWING | | | | | | 0 | 0 |
| 03 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH PERF MODE | |
| 25 | CH A GAIN | | | | 0 | CH A TEST PATTERNS | | |
| 29 | 0 | 0 | 0 | DATA FORMAT | | 0 | 0 | 0 |
| 2B | CH B GAIN | | | | 0 | CH B TEST PATTERNS | | |
| 3D | 0 | 0 | ENABLE OFFSET CORR | 0 | 0 | 0 | 0 | 0 |
| 3F | 0 | 0 | CUSTOM PATTERN D[13:8] | | | | | |
| 40 | CUSTOM PATTERN D[7:0] | | | | | | | |
| 41 | LVDS CMOS | | CMOS CLKOUT STRENGTH | | 0 | 0 | DIS OBUF | |
| 42 | CLKOUT FALL POSN | | CLKOUT RISE POSN | | EN DIGITAL | 0 | 0 | 0 |
| 45 | STBY | LVDS CLKOUT STRENGTH | LVDS DATA STRENGTH | 0 | 0 | PDN GLOBAL | 0 | 0 |
| 4A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH B(2) |
| 58 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH A(2) |
| BF | CH A OFFSET PEDESTAL | | | | | | 0 | 0 |
| C1 | CH B OFFSET PEDESTAL | | | | | | 0 | 0 |
| CF | FREEZE OFFSET CORR | 0 | OFFSET CORR TIME CONSTANT | | | | 0 | 0 |
| DB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH B(3) |
| EF | 0 | 0 | 0 | EN LOW SPEED MODE(3) | 0 | 0 | 0 | 0 |
| F1 | 0 | 0 | 0 | 0 | 0 | 0 | EN LVDS SWING | |
| F2 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH A(3) | 0 | 0 | 0 |

(1) Multiple functions in a register can be programmed in a single write operation. All registers default to '0' after reset.
(2) These bits improve SFDR on high frequencies. The frequency limit is 200MHz.
(3) Low-speed mode is not applicable for the ADS4222 and ADS4242.

## DESCRIPTION OF SERIAL REGISTERS

**Register Address 00h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | RESET | READOUT |

**Bits[7:2]** **Always write '0'**

**Bit 1** **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

**Bit 0** **READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the SDOUT pin is placed in a logic low state.
1 = Serial readout enabled; the SDOUT pin functions as a serial data readout with CMOS logic levels running from the DRVDD supply. See the *Serial Register Readout* section.

**Register Address 01h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LVDS SWING | | | | | | 0 | 0 |

**Bits[7:2]** **LVDS SWING: LVDS swing programmability**

These bits program the LVDS swing. Set the EN LVDS SWING bit to '1' before programming swing.
000000 = Default LVDS swing; ±350mV with external 100Ω termination
011011 = LVDS swing increases to ±410mV
110010 = LVDS swing increases to ±465mV
010100 = LVDS swing increases to ±570mV
111110 = LVDS swing increases to ±200mV
001111 = LVDS swing increases to ±125mV

**Bits[1:0]** **Always write '0'**

**Register Address 03h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | HIGH PERF MODE | |

**Bits[7:2]** **Always write '0'**

**Bits[1:0]** **HIGH PERF MODE: High-performance mode**

00 = Default performance
01 = Do not use
10 = Do not use
11 = Obtain best performance across sample clock and input signal frequencies

**Register Address 25h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH A GAIN | | | | 0 | CH A TEST PATTERNS | | |

**Bits[7:4] CH A GAIN: Channel A gain programmability**

These bits set the gain programmability in 0.5dB steps for channel A.

0000 = 0dB gain (default after reset)
0001 = 0.5dB gain
0010 = 1dB gain
0011 = 1.5dB gain
0100 = 2dB gain
0101 = 2.5dB gain
0110 = 3dB gain
0111 = 3.5dB gain
1000 = 4dB gain
1001 = 4.5dB gain
1010 = 5dB gain
1011 = 5.5dB gain
1100 = 6dB gain

**Bit 3 Always write '0'**

**Bits[2:0] CH A TEST PATTERNS: Channel A data capture**

These bits verify data capture for channel A.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
For the ADS424x, output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.
For the ADS422x, the output data D[11:0] are an alternating sequence of *101010101010* and *010101010101*.
100 = Outputs digital ramp.
For the ADS424x, output data increment by one LSB (14-bit) every clock cycle from code 0 to code 16383.
For the ADS422x, output data increment by one LSB (12-bit) every fourth clock cycle from code 0 to code 4095.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

**Register Address 29h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | DATA FORMAT | | 0 | 0 | 0 |

**Bits[7:5] Always write '0'**

**Bits[4:3] DATA FORMAT: Data format selection**

00 = Twos complement
01 = Twos complement
10 = Twos complement
11 = Offset binary

**Bits[2:0] Always write '0'**

**Register Address 2Bh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH B GAIN | | | | 0 | CH B TEST PATTERNS | | |

**Bits[7:4] CH B GAIN: Channel B gain programmability**

These bits set the gain programmability in 0.5dB steps for channel B.

0000 = 0dB gain (default after reset)
0001 = 0.5dB gain
0010 = 1dB gain
0011 = 1.5dB gain
0100 = 2dB gain
0101 = 2.5dB gain
0110 = 3dB gain
0111 = 3.5dB gain
1000 = 4dB gain
1001 = 4.5dB gain
1010 = 5dB gain
1011 = 5.5dB gain
1100 = 6dB gain

**Bit 3 Always write '0'**

**Bits[2:0] CH B TEST PATTERNS: Channel B data capture**

These bits verify data capture for channel B.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
For the ADS424x, output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.
For the ADS422x, the output data D[11:0] are an alternating sequence of *101010101010* and *010101010101*.
100 = Outputs digital ramp.
For the ADS424x, output data increment by one LSB (14-bit) every clock cycle from code 0 to code 16383.
For the ADS422x, output data increment by one LSB (12-bit) every fourth clock cycle from code 0 to code 4095.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

**Register Address 3Dh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | ENABLE OFFSET CORR | 0 | 0 | 0 | 0 | 0 |

**Bits[7:6] Always write '0'**

**Bit 5 ENABLE OFFSET CORR: Offset correction setting**

This bit enables the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

**Bits[4:0] Always write '0'**

**Register Address 3Fh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | CUSTOM PATTERN D13 | CUSTOM PATTERN D12 | CUSTOM PATTERN D11 | CUSTOM PATTERN D10 | CUSTOM PATTERN D9 | CUSTOM PATTERN D8 |

**Bits[7:6] Always write '0'**

**Bits[5:0] CUSTOM PATTERN D[13:8]**

These are the six upper bits of the custom pattern available at the output instead of ADC data. Note that for the ADS424x, the custom pattern is 14-bit. The ADS422x custom pattern is 12-bit.

**Register Address 40h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOM PATTERN D7 | CUSTOM PATTERN D6 | CUSTOM PATTERN D5 | CUSTOM PATTERN D4 | CUSTOM PATTERN D3 | CUSTOM PATTERN D2 | CUSTOM PATTERN D1 | CUSTOM PATTERN D0 |

**Bits[7:0] CUSTOM PATTERN D[7:0]**

These are the eight upper bits of the custom pattern available at the output instead of ADC data. Note that for the ADS424x, the custom pattern is 14-bit. The ADS422x custom pattern is 12-bit; use the CUSTOM PATTERN D[13:2] register bits.

**Register Address 41h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LVDS CMOS | | CMOS CLKOUT STRENGTH | | 0 | 0 | DIS OBUF | |

**Bits[7:6] LVDS CMOS: Interface selection**

These bits select the interface.
00 = DDR LVDS interface
01 = DDR LVDS interface
10 = DDR LVDS interface
11 = Parallel CMOS interface

**Bits[5:4] CMOS CLKOUT STRENGTH**

These bits control the strength of the CMOS output clock.
00 = Maximum strength (recommended)
01 = Medium strength
10 = Low strength
11 = Very low strength

**Bits[3:2] Always write '0'**

**Bits[1:0] DIS OBUF**

These bits power down data and clock output buffers for both the CMOS and LVDS output interface. When powered down, the output buffers are in 3-state.
00 = Default
01 = Power-down data output buffers for channel B
10 = Power-down data output buffers for channel A
11 = Power-down data output buffers for both channels as well as the clock output buffer

**Register Address 42h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLKOUT FALL POSN | | CLKOUT RISE POSN | | EN DIGITAL | 0 | 0 | 0 |

**Bits[7:6] CLKOUT FALL POSN**

00 = Default
01 = Do not use
10 = The falling edge of the output clock advances by 650ps
11 = The falling edge of the output clock advances by 1.1ns

**Bits[5:6] CLKOUT RISE POSN**

00 = Default
01 = The rising edge of the output clock advances by 650ps
10 = The rising edge of the output clock is delayed by 650ps
11 = Do not use

**Bit 3 EN DIGITAL: Digital function enable**

0 = All digital functions disabled
1 = All digital functions (such as test patterns, gain, and offset correction) enabled

**Bits[2:0] Always write '0'**

**Register Address 45h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STBY | LVDS CLKOUT STRENGTH | LVDS DATA STRENGTH | 0 | 0 | PDN GLOBAL | 0 | 0 |

**Bit 7** **STBY: Standby setting**

0 = Normal operation
1 = Both channels are put in standby; wakeup time from this mode is fast (typically 50µs).

**Bit 6** **LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting**

0 = LVDS output clock buffer at default strength to be used with 100Ω external termination
1 = LVDS output clock buffer has double strength to be used with 50Ω external termination

**Bit 5** **LVDS DATA STRENGTH**

0 = All LVDS data buffers at default strength to be used with 100Ω external termination
1 = All LVDS data buffers have double strength to be used with 50Ω external termination

**Bits[4:3]** **Always write '0'**

**Bit 2** **PDN GLOBAL**

0 = Normal operation
1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wakeup time from this mode is slow (typically 100µs).

**Bits[1:0]** **Always write '0'**

**Register Address 4Ah (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH B |

**Bits[7:1]** **Always write '0'**

**Bit 0** **HIGH FREQ MODE CH B: High-frequency mode for channel B**

0 = Default
1 = Use this mode for high input frequencies

**Register Address 58h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH A |

**Bits[7:1]** **Always write '0'**

**Bit 0** **HIGH FREQ MODE CH A: High-frequency mode for channel A**

0 = Default
1 = Use this mode for high input frequencies

**Register Address BFh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH A OFFSET PEDESTAL | | | | | | 0 | 0 |

**Bits[7:2] CH A OFFSET PEDESTAL: Channel A offset pedestal selection**

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
For the ADS424x, the pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+32 by adding pedestal D7-D2.
For the ADS422x, the pedestal ranges from –8 to +7, so the output code can vary from midcode-8 to midcode+7 by adding pedestal D7-D4.

| ADS422x (Program Bits D[7:4]) | ADS424x (Program Bits D[7:2]) |
|---|---|
| 0111 = Midcode+7 | 011111 = Midcode+31 |
| 0110 = Midcode+6 | 011110 = Midcode+30 |
| 0101 = Midcode+5 | 011101 = Midcode+29 |
| … | … |
| 0000 = Midcode | 000000 = Midcode |
| 1111 = Midcode-1 | 111111 = Midcode-1 |
| 1110 = Midcode-2 | 111110 = Midcode-2 |
| 1101 = Midcode-3 | 111101 = Midcode-3 |
| … | … |
| 1000 = Midcode-8 | 100000 = Midcode-32 |

**Bits[1:0] Always write '0'**

**Register Address C1h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH B OFFSET PEDESTAL | | | | | | 0 | 0 |

**Bits[7:2] CH B OFFSET PEDESTAL: Channel B offset pedestal selection**

When offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits; see the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
For the ADS422x, the pedestal ranges from –8 to +7, so the output code can vary from midcode-8 to midcode+7 by adding pedestal D[7:4]. For the ADS424x, the pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+32 by adding pedestal D[7:2].

| ADS422x (Program Bits D[7:4]) | ADS424x (Program Bits D[7:2]) |
|---|---|
| 0111 = Midcode+7 | 011111 = Midcode+31 |
| 0110 = Midcode+6 | 011110 = Midcode+30 |
| 0101 = Midcode+5 | 011101 = Midcode+29 |
| … | … |
| 0000 = Midcode | 000000 = Midcode |
| 1111 = Midcode-1 | 111111 = Midcode-1 |
| 1110 = Midcode-2 | 111110 = Midcode-2 |
| 1101 = Midcode-3 | 111101 = Midcode-3 |
| … | … |
| 1000 = Midcode-8 | 100000 = Midcode-32 |

**Bits[1:0] Always write '0'**

**Register Address CFh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FREEZE OFFSET CORR | 0 | OFFSET CORR TIME CONSTANT | | | | 0 | 0 |

**Bit 7** **FREEZE OFFSET CORR: Freeze offset correction setting**

This bit sets the freeze offset correction estimation.
0 = Estimation of offset correction is not frozen (the EN OFFSET CORR bit must be set)
1 = Estimation of offset correction is frozen (the EN OFFSET CORR bit must be set); when frozen, the last estimated value is used for offset correction of every clock cycle. See the *Offset Correction* section.

**Bit 6** **Always write '0'**

**Bits[5:2]** **OFFSET CORR TIME CONSTANT**

The offset correction loop time constant in number of clock cycles. Refer to the *Offset Correction* section.

**Bits[1:0]** **Always write '0'**

**Register Address DBh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH B |

**Bits[7:1]** **Always write '0'**

**Bit 0** **LOW SPEED MODE CH B: Channel B low-speed mode enable**

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel B
1 = Low-speed mode is enabled for channel B

**Register Address EFh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | EN LOW SPEED MODE | 0 | 0 | 0 | 0 |

**Bits[7:5]** **Always write '0'**

**Bit 4** **EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits (ADS42x5 and ADS42x6 only)**

This bit enables the control of the low-speed mode using the LOW SPEED MODE CH B and LOW SPEED MODE CH A register bits.
0 = Low-speed mode is disabled
1 = Low-speed mode is controlled by serial register bits

**Bits[3:0]** **Always write '0'**

**Register Address F1h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | EN LVDS SWING | |

**Bits[7:2] Always write '0'**

**Bits[1:0] EN LVDS SWING: LVDS swing enable**

These bits enable LVDS swing control using the LVDS SWING register bits.
00 = LVDS swing control using the LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using the LVDS SWING register bits is enabled

**Register Address F2h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | LOW SPEED MODE CH A | 0 | 0 | 0 |

**Bits[7:4] Always write '0'**

**Bit 3 LOW SPEED MODE CH A: Channel A low-speed mode enable**

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel A
1 = Low-speed mode is enabled for channel A

**Bits[2:0] Always write '0'**

## TYPICAL CHARACTERISTICS: ADS4222

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR 20MHz INPUT SIGNAL**

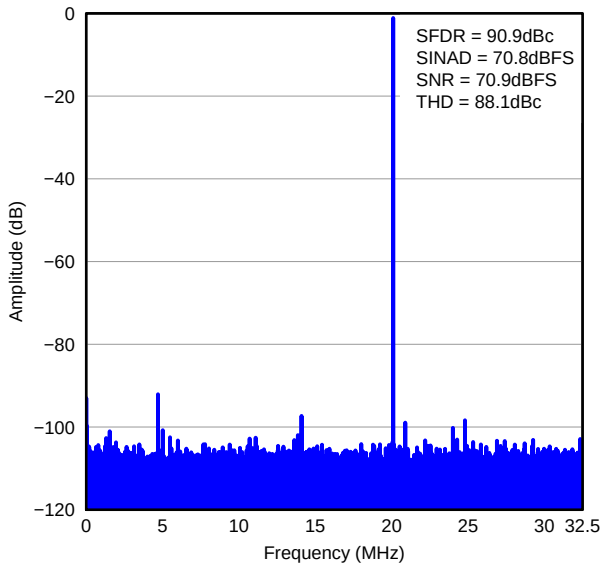



**Figure 16.**

**FFT FOR 170MHz INPUT SIGNAL**

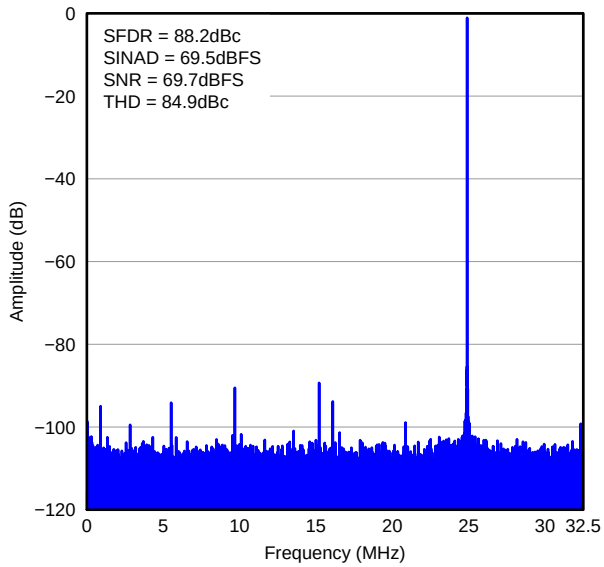



**Figure 17.**

**FFT FOR 300MHz INPUT SIGNAL**

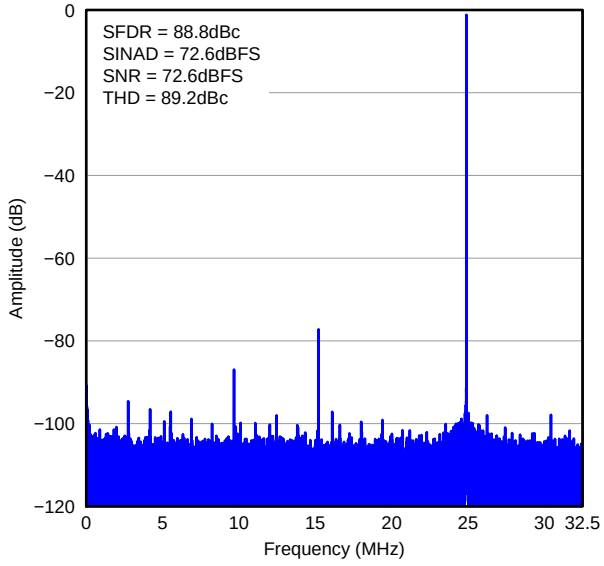



**Figure 18.**

**FFT FOR TWO-TONE INPUT SIGNAL**

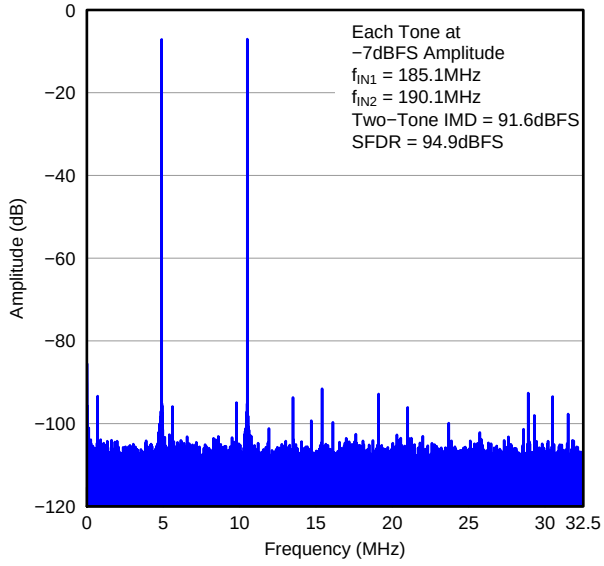



**Figure 19.**

## TYPICAL CHARACTERISTICS: ADS4222 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR TWO-TONE INPUT SIGNAL**

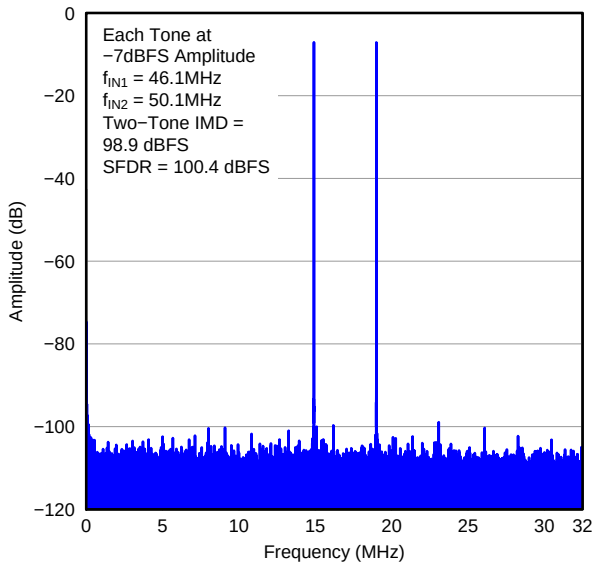



**Figure 20.**

**SFDR vs INPUT FREQUENCY**

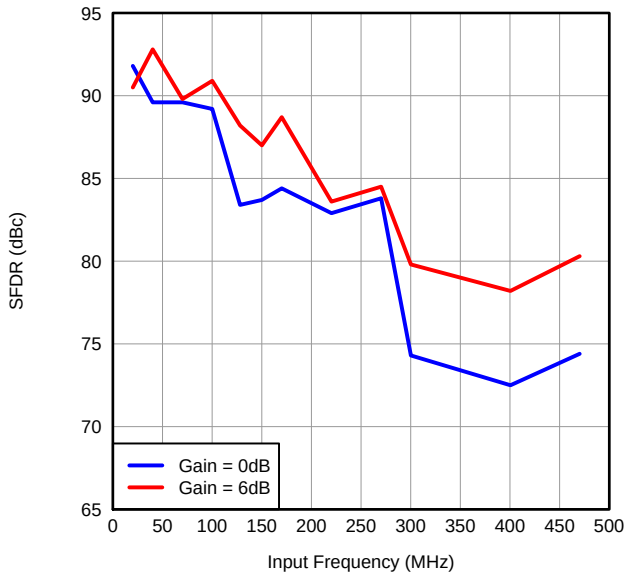



**Figure 21.**

**SNR vs INPUT FREQUENCY**

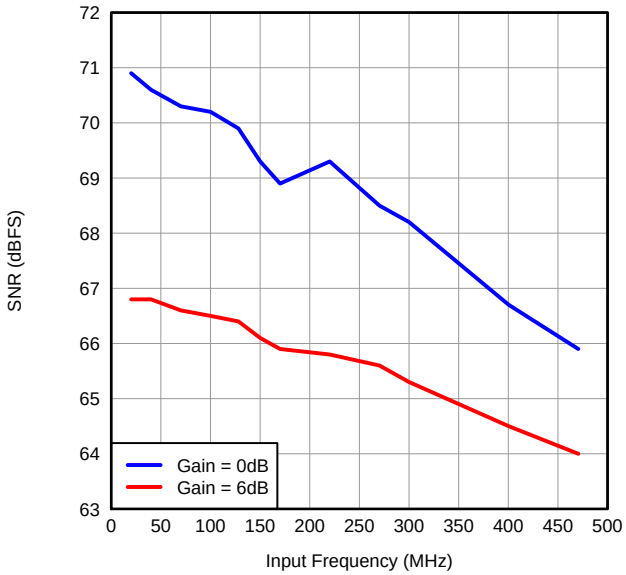



**Figure 22.**

**SNR vs INPUT FREQUENCY (CMOS)**

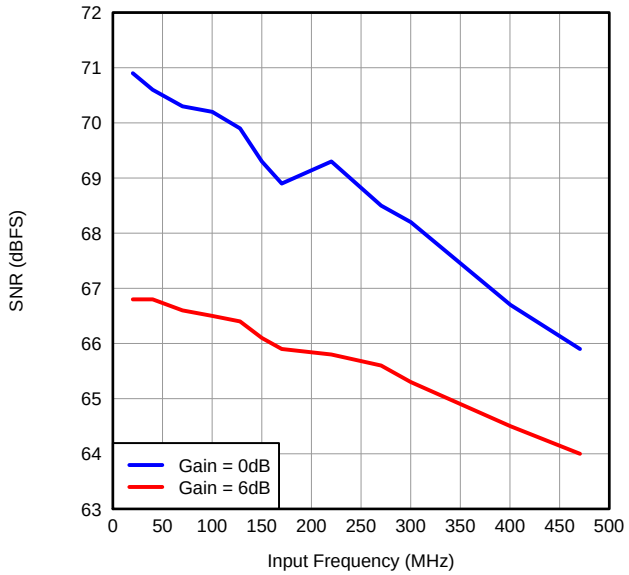



**Figure 23.**

## TYPICAL CHARACTERISTICS: ADS4222 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**SFDR vs GAIN AND INPUT FREQUENCY**

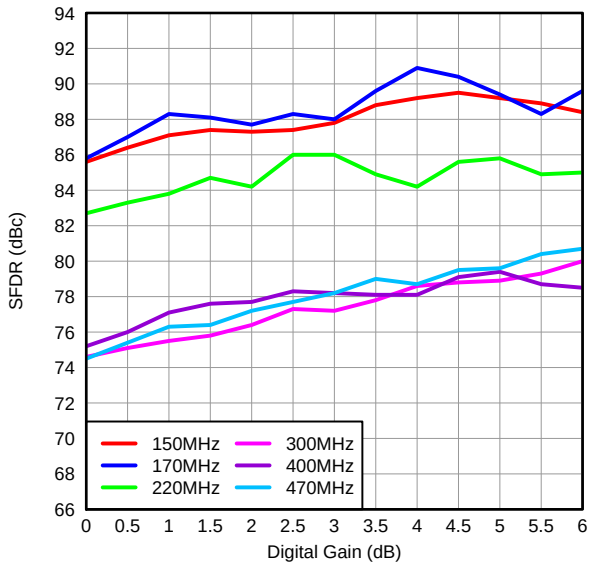



**Figure 24.**

**SINAD vs GAIN AND INPUT FREQUENCY**

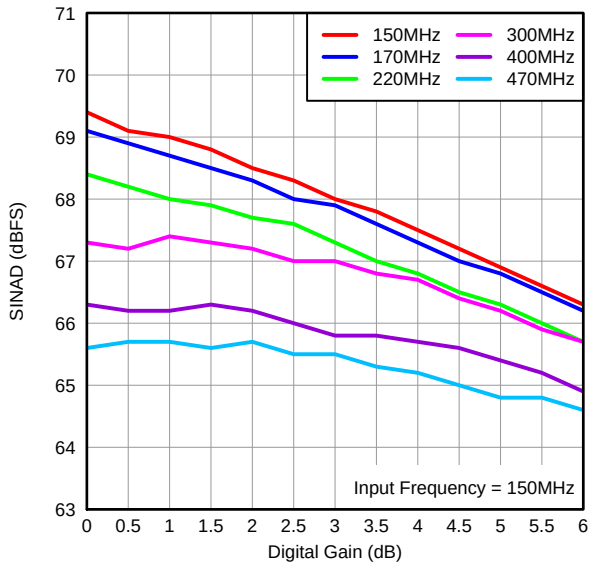



**Figure 25.**

**PERFORMANCE vs INPUT AMPLITUDE**

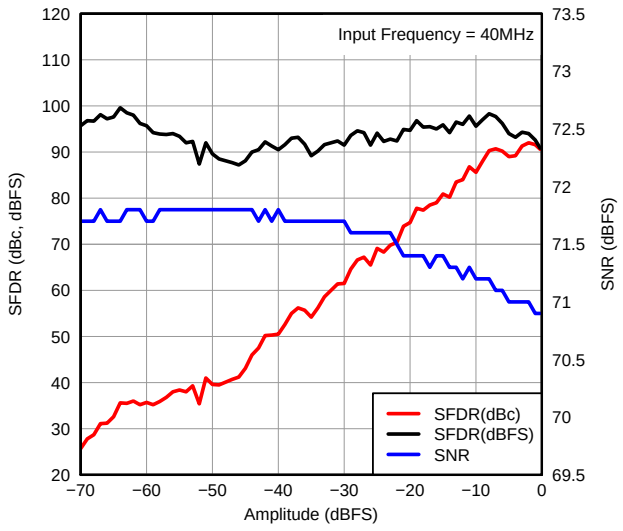



**Figure 26.**

**PERFORMANCE vs INPUT AMPLITUDE**

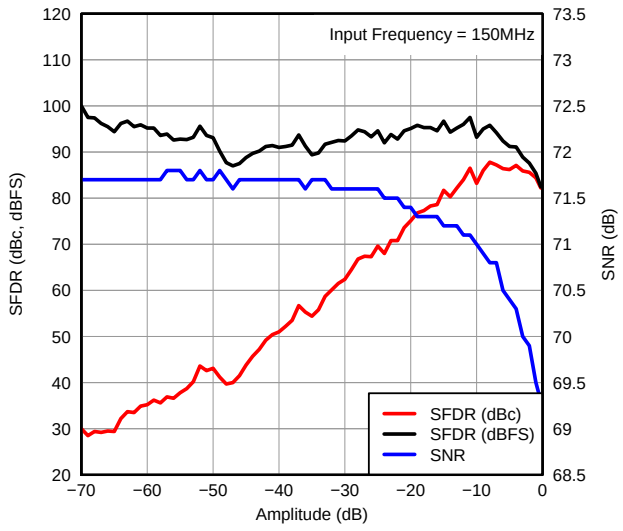



**Figure 27.**

## TYPICAL CHARACTERISTICS: ADS4222 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

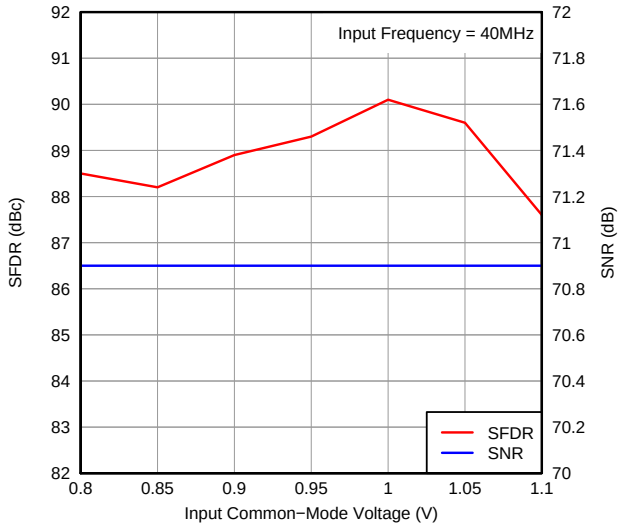



**Figure 28.**

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

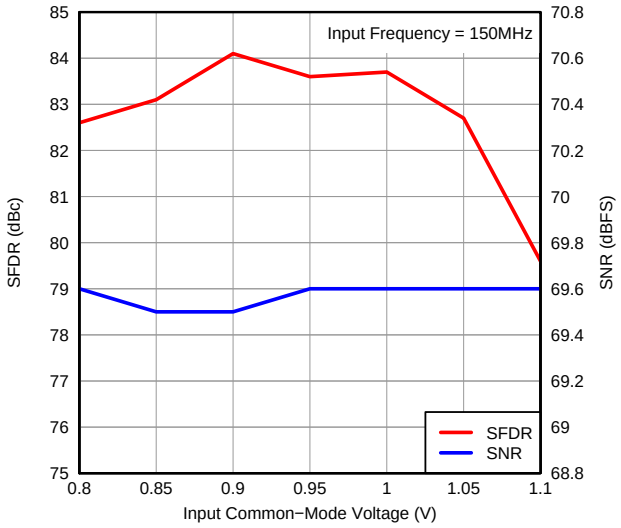



**Figure 29.**

**SFDR vs TEMPERATURE AND AVDD SUPPLY**

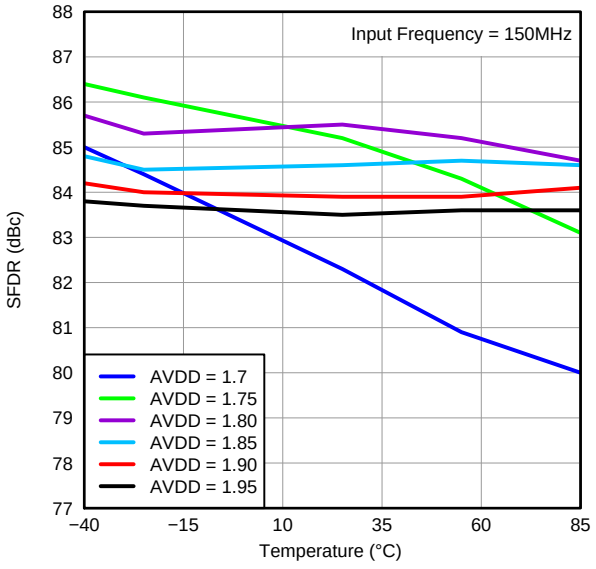



**Figure 30.**

**SNR vs TEMPERATURE AND AVDD SUPPLY**

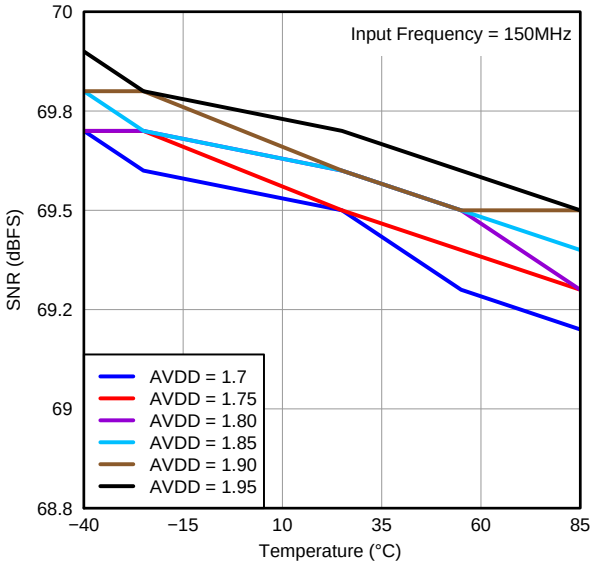



**Figure 31.**

## TYPICAL CHARACTERISTICS: ADS4222 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs DRVDD SUPPLY VOLTAGE**

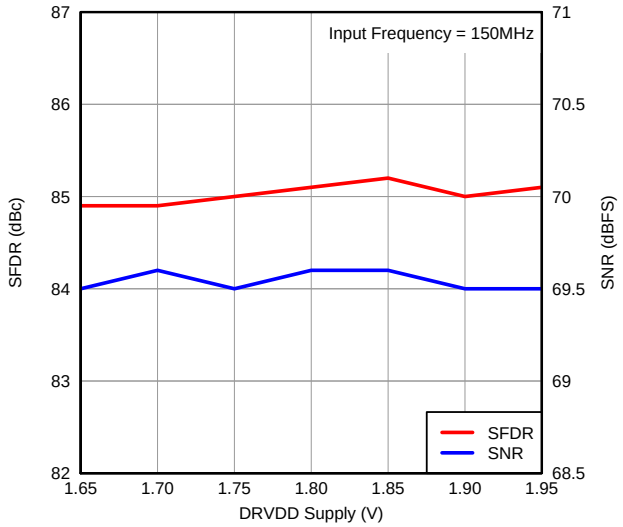



**Figure 32.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

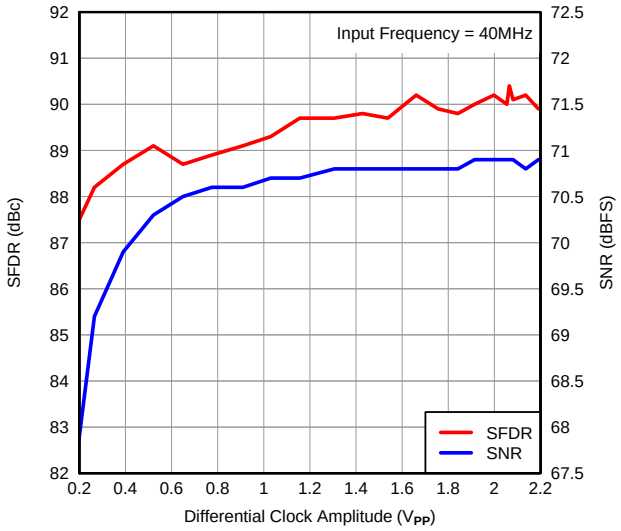



**Figure 33.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

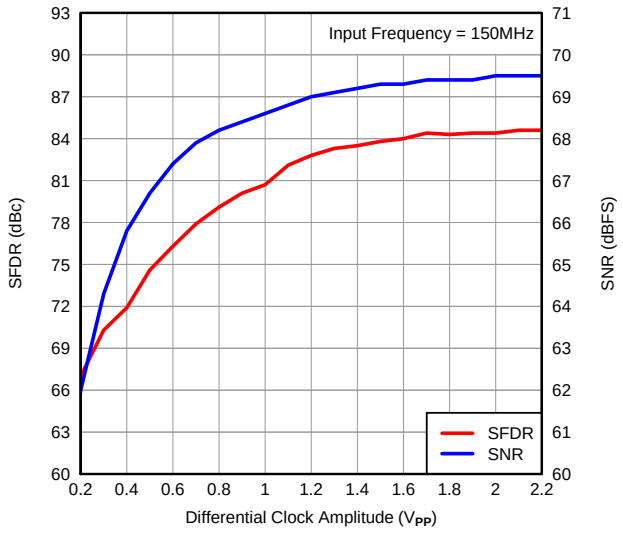



**Figure 34.**

**PERFORMANCE vs INPUT CLOCK DUTY CYCLE**

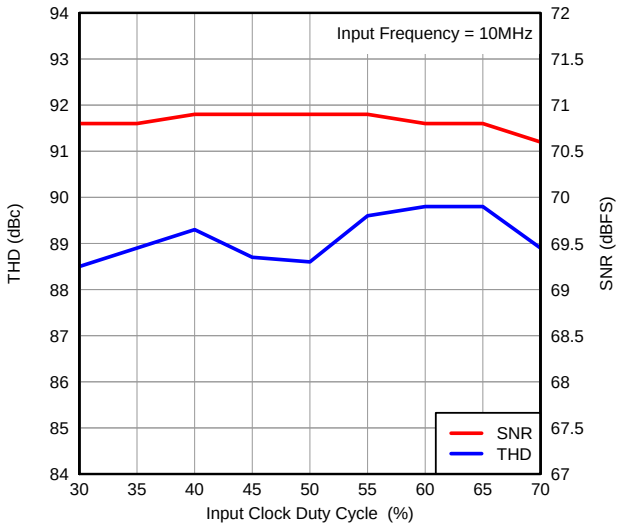



**Figure 35.**

## TYPICAL CHARACTERISTICS: ADS4225

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR 20MHz INPUT SIGNAL**

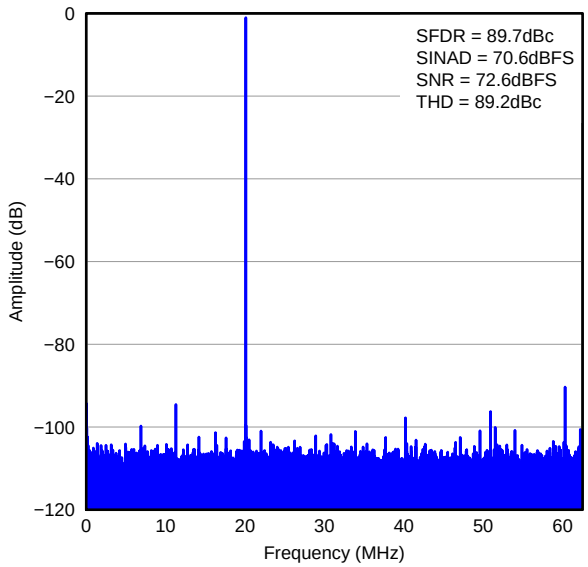



**Figure 36.**

**FFT FOR 170MHz INPUT SIGNAL**

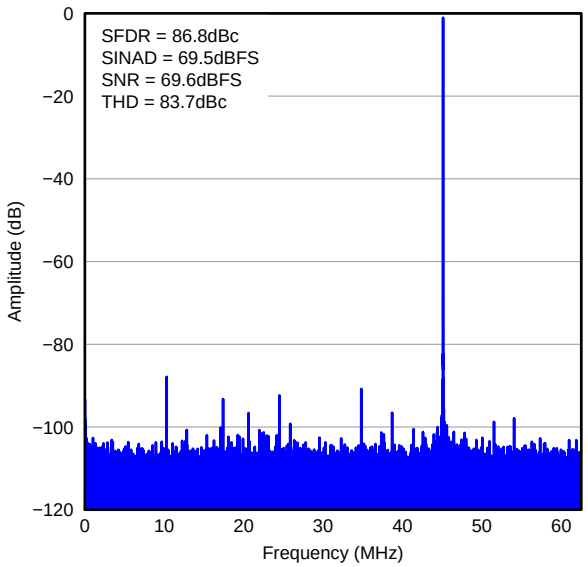



**Figure 37.**

**FFT FOR 300MHz INPUT SIGNAL**

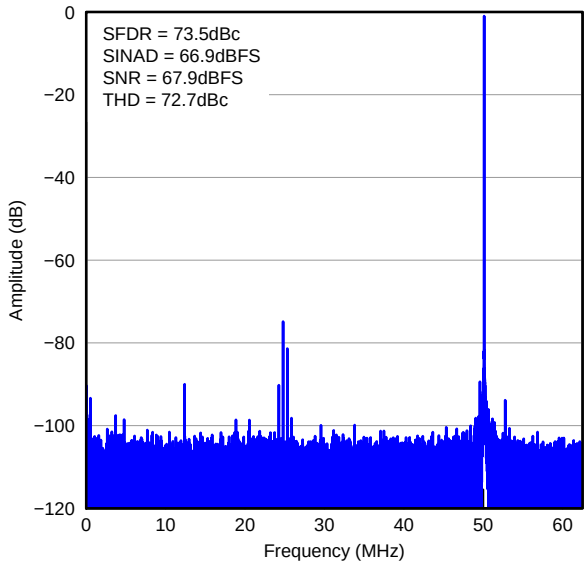



**Figure 38.**

**FFT FOR TWO-TONE INPUT SIGNAL**

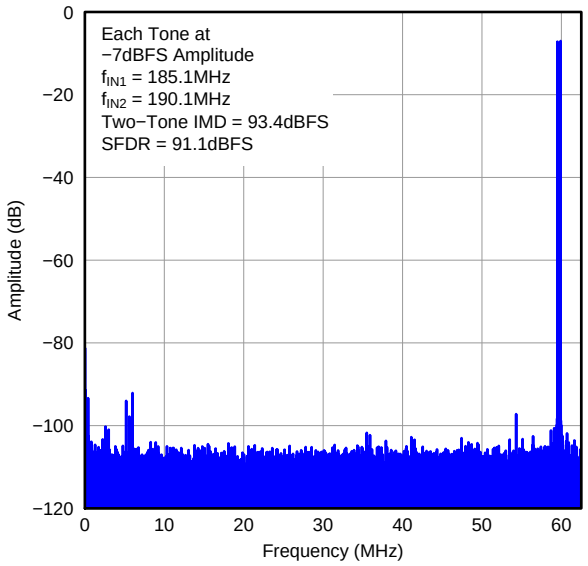



**Figure 39.**

## TYPICAL CHARACTERISTICS: ADS4225 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR TWO-TONE INPUT SIGNAL**

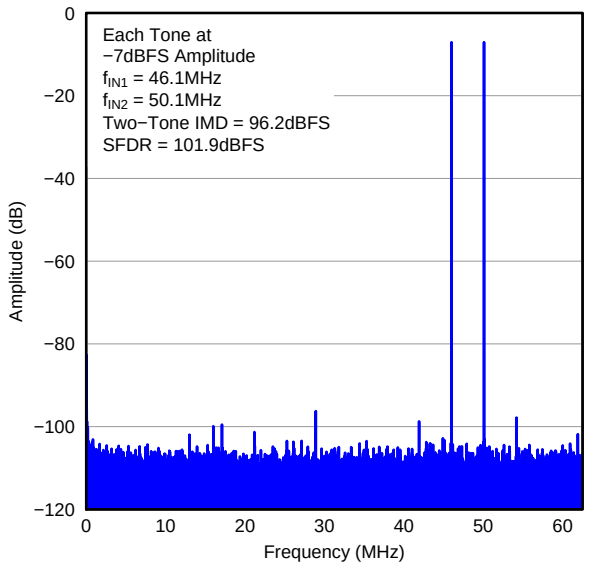



**Figure 40.**

**SFDR vs INPUT FREQUENCY**

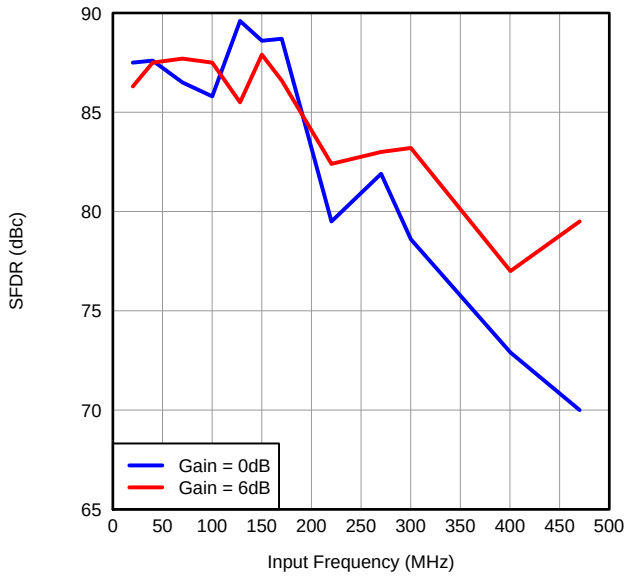



**Figure 41.**

**SNR vs INPUT FREQUENCY**

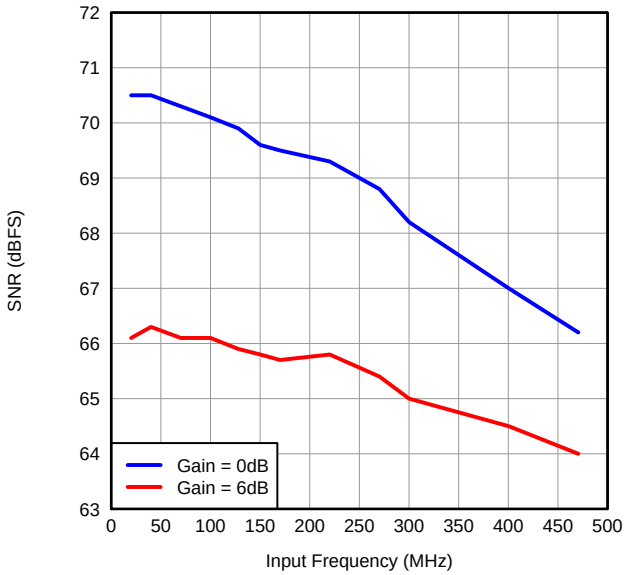



**Figure 42.**

**SNR vs INPUT FREQUENCY (CMOS)**

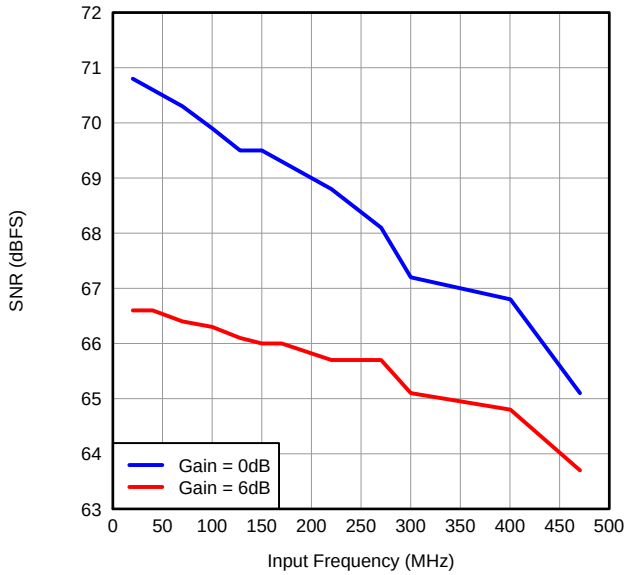



**Figure 43.**

## TYPICAL CHARACTERISTICS: ADS4225 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**SFDR vs GAIN AND INPUT FREQUENCY**

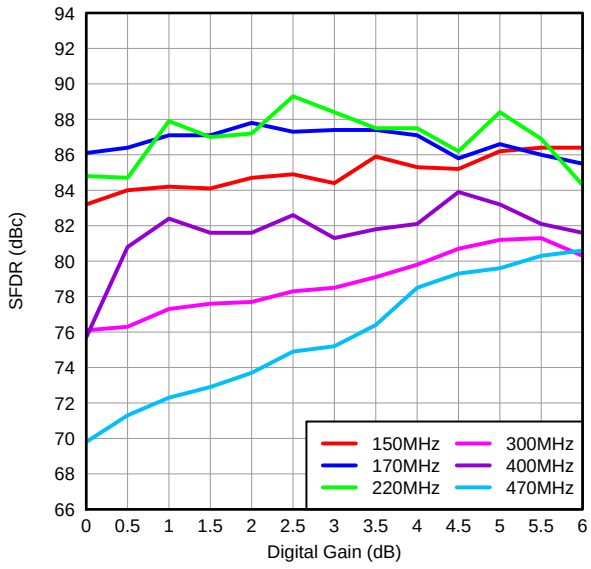



**Figure 44.**

**SINAD vs GAIN AND INPUT FREQUENCY**

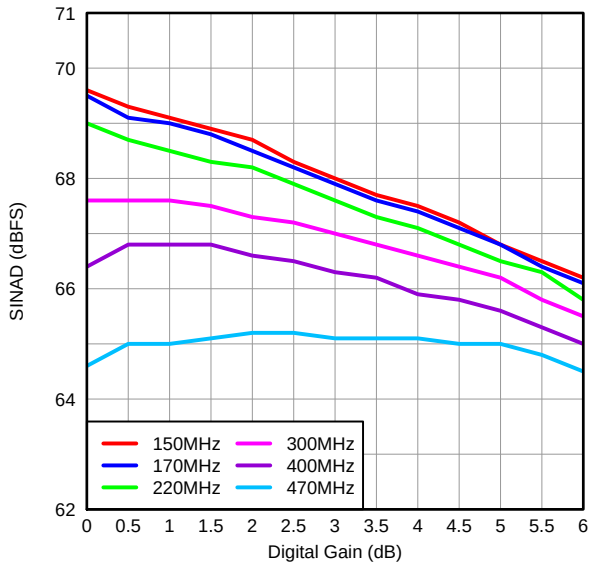



**Figure 45.**

**PERFORMANCE vs INPUT AMPLITUDE**

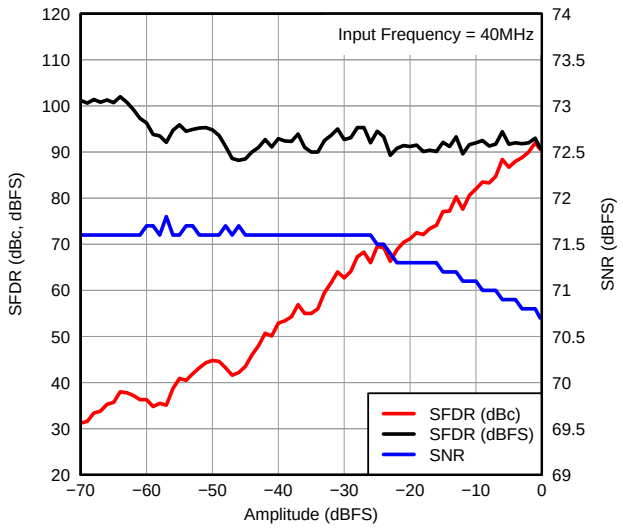



**Figure 46.**

**PERFORMANCE vs INPUT AMPLITUDE**

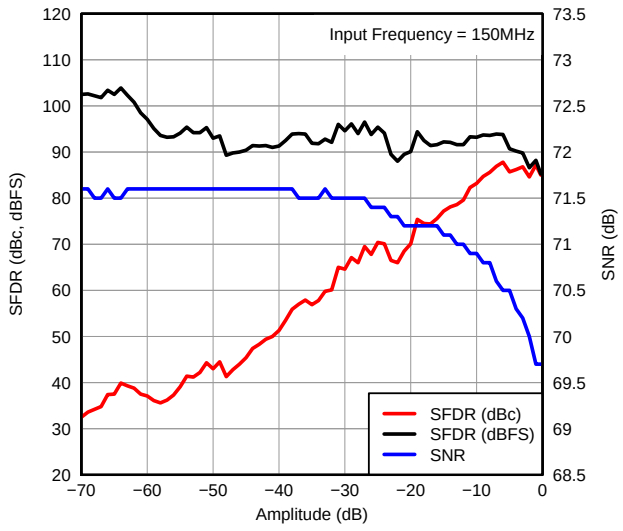



**Figure 47.**

## TYPICAL CHARACTERISTICS: ADS4225 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

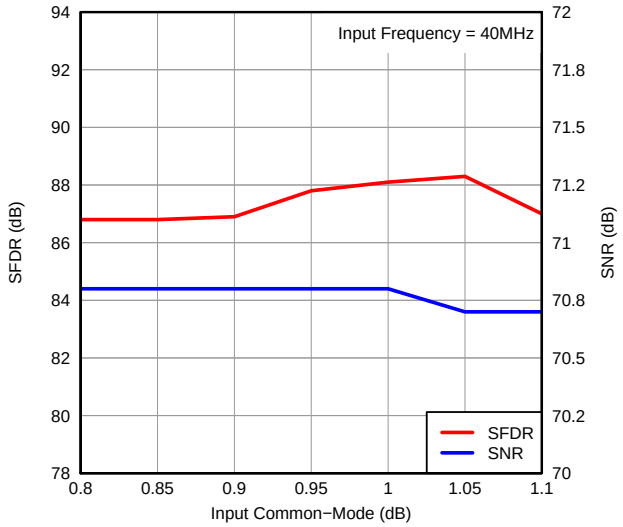



**Figure 48.**

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

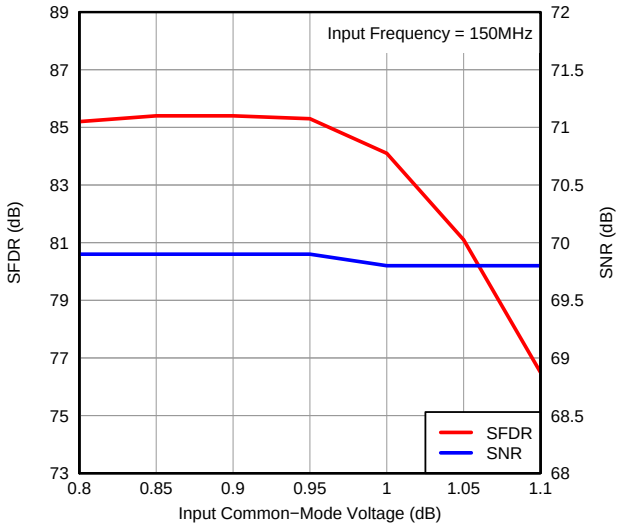



**Figure 49.**

**SFDR vs TEMPERATURE AND AVDD SUPPLY**

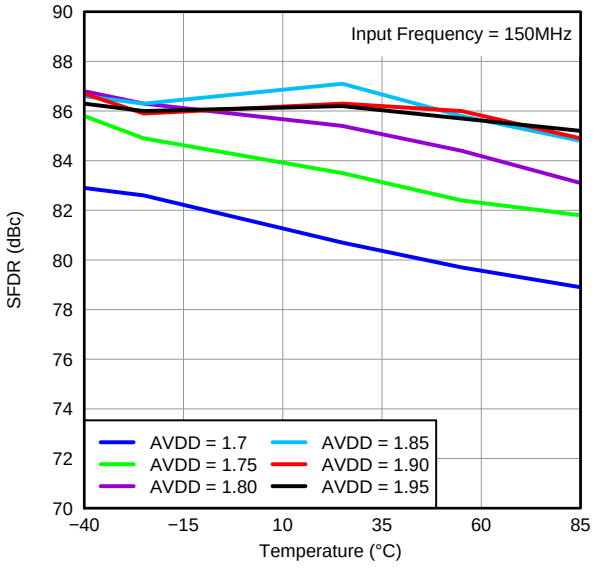



**Figure 50.**

**SNR vs TEMPERATURE AND AVDD SUPPLY**

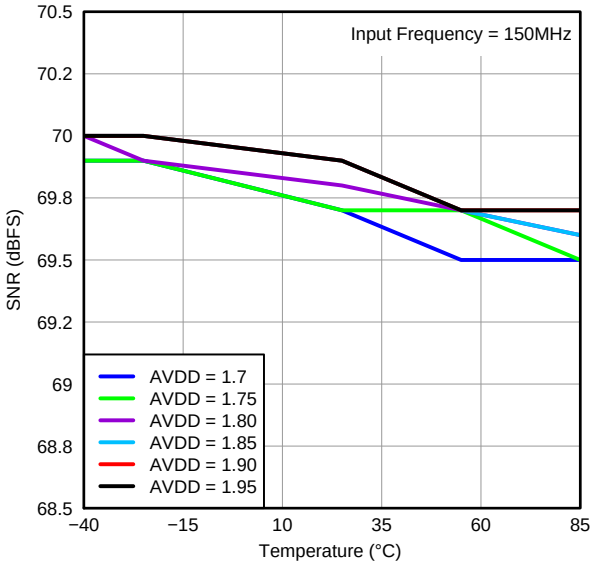



**Figure 51.**

## TYPICAL CHARACTERISTICS: ADS4225 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs DRVDD SUPPLY VOLTAGE**

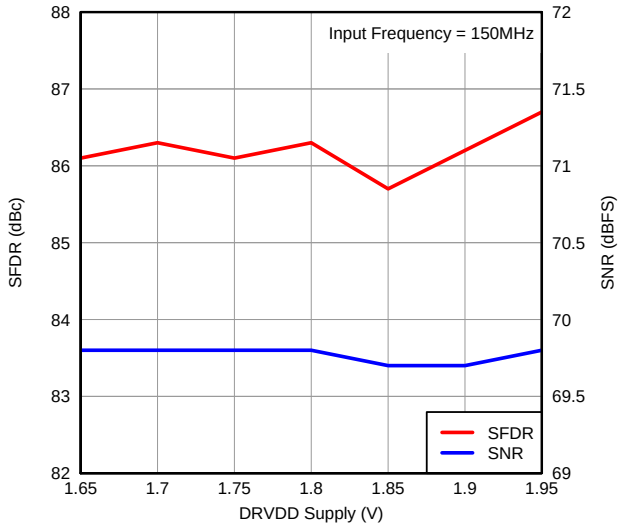



**Figure 52.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

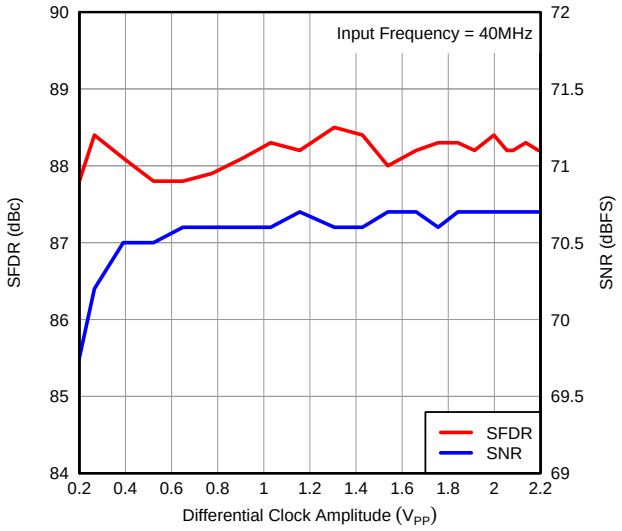



**Figure 53.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

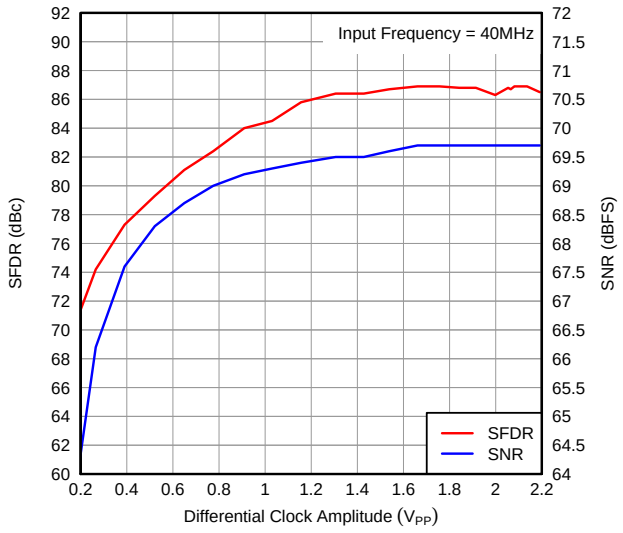



**Figure 54.**

**PERFORMANCE vs INPUT CLOCK DUTY CYCLE**

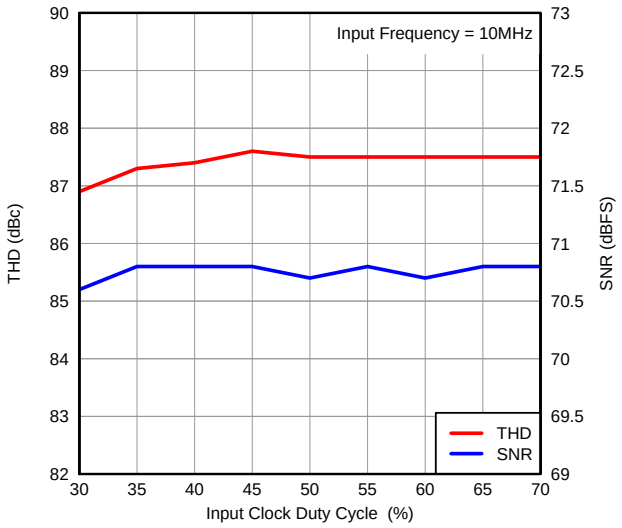



**Figure 55.**

## TYPICAL CHARACTERISTICS: ADS4226

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR 20MHz INPUT SIGNAL**

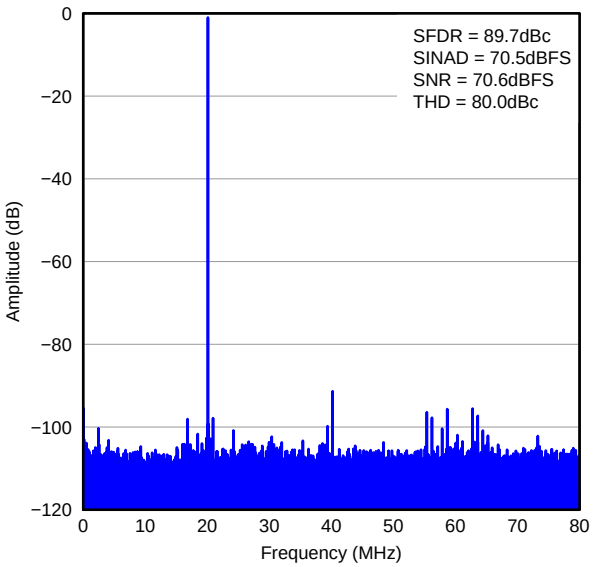



**Figure 56.**

**FFT FOR 170MHz INPUT SIGNAL**

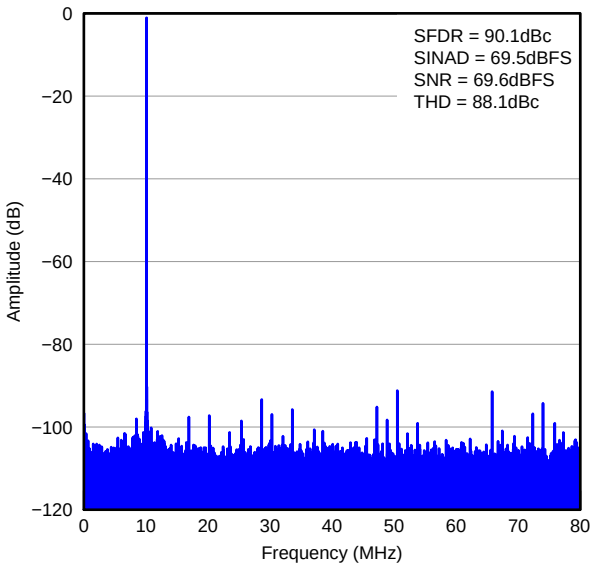



**Figure 57.**

**FFT FOR 300MHz INPUT SIGNAL**

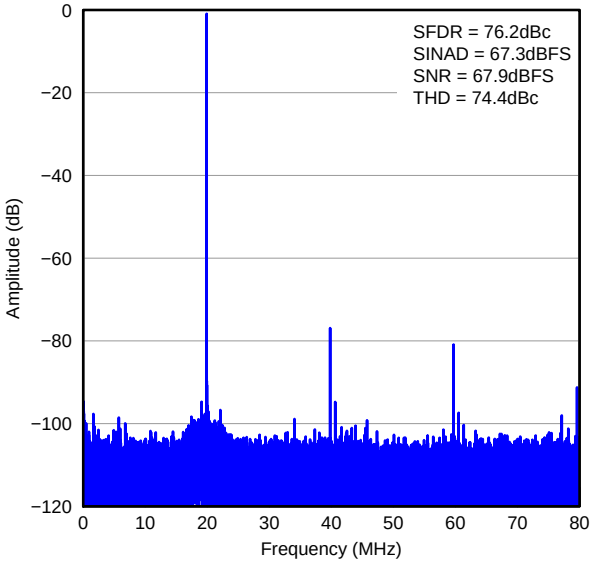



**Figure 58.**

**FFT FOR TWO-TONE INPUT SIGNAL**

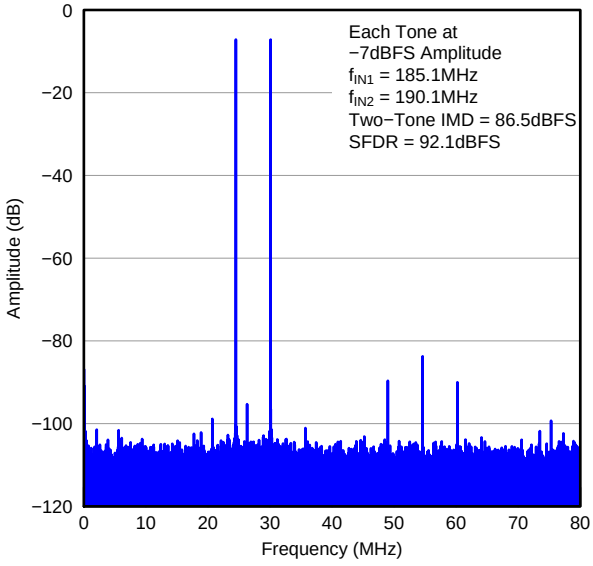



**Figure 59.**

## TYPICAL CHARACTERISTICS: ADS4226 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR TWO-TONE INPUT SIGNAL**

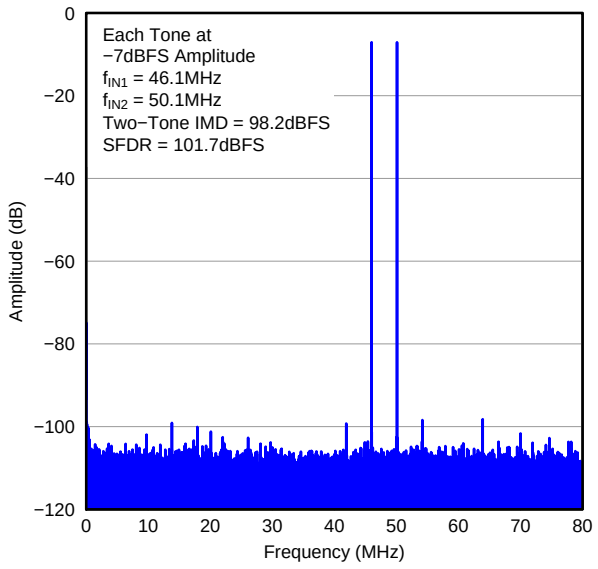



**Figure 60.**

**SFDR vs INPUT FREQUENCY**

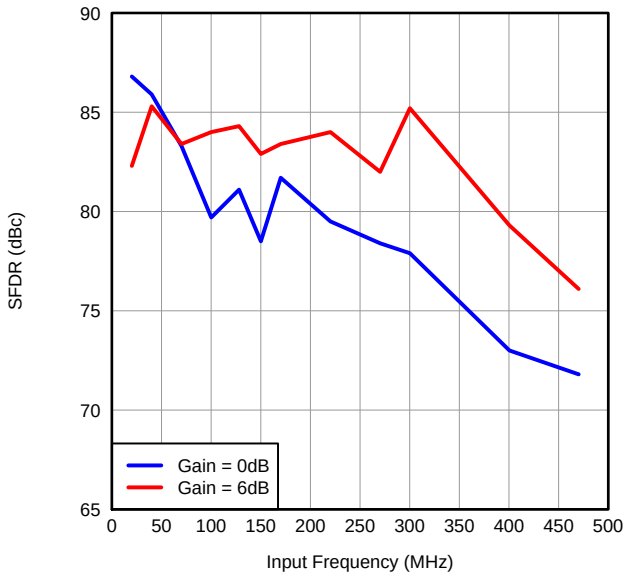



**Figure 61.**

**SNR vs INPUT FREQUENCY**

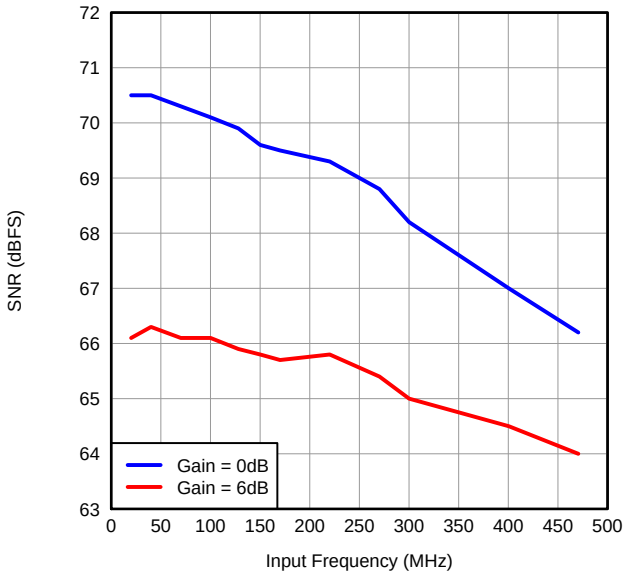



**Figure 62.**

**SNR vs INPUT FREQUENCY (CMOS)**

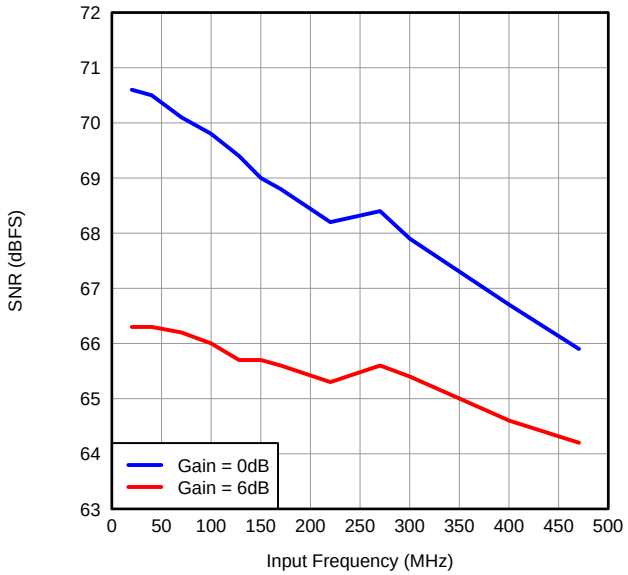



**Figure 63.**

## TYPICAL CHARACTERISTICS: ADS4226 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**SFDR vs GAIN AND INPUT FREQUENCY**

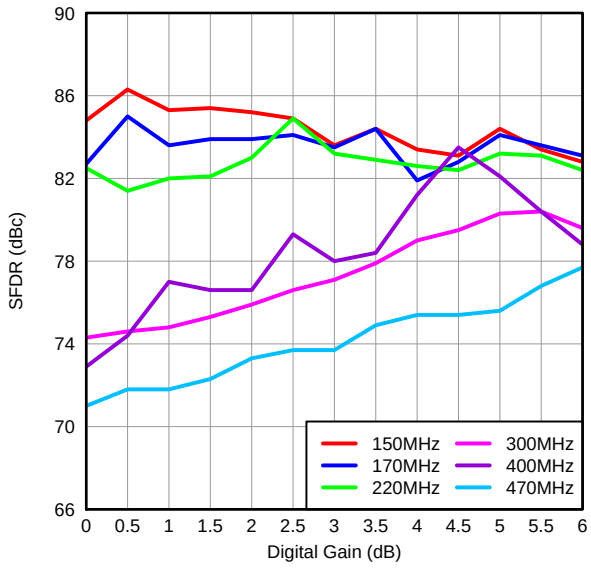



**Figure 64.**

**SINAD vs GAIN AND INPUT FREQUENCY**

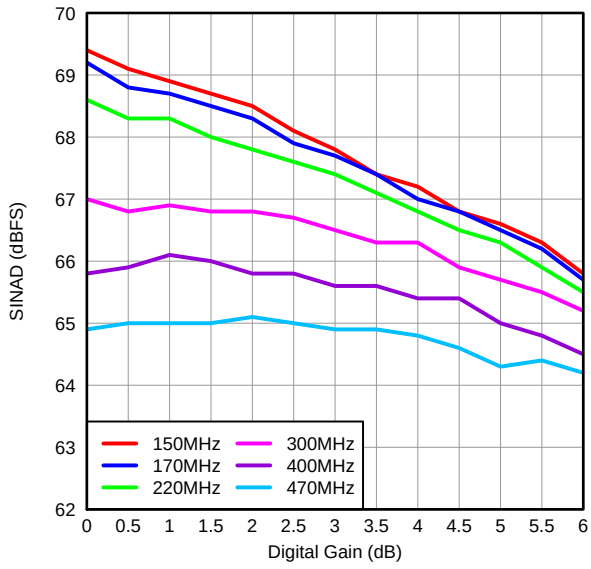



**Figure 65.**

**PERFORMANCE vs INPUT AMPLITUDE**

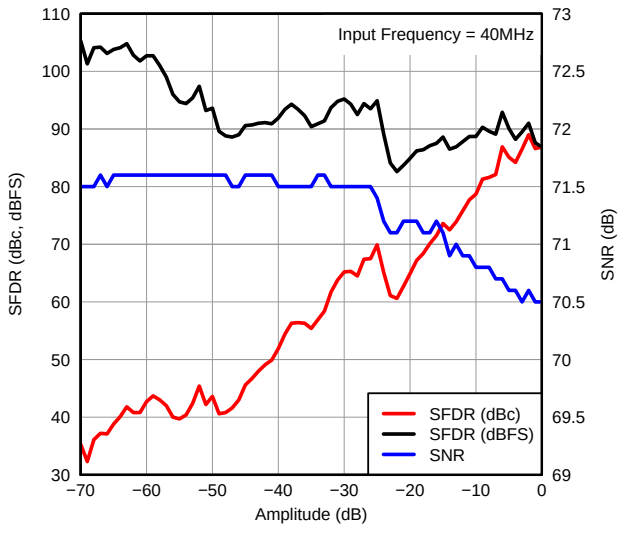



**Figure 66.**

**PERFORMANCE vs INPUT AMPLITUDE**

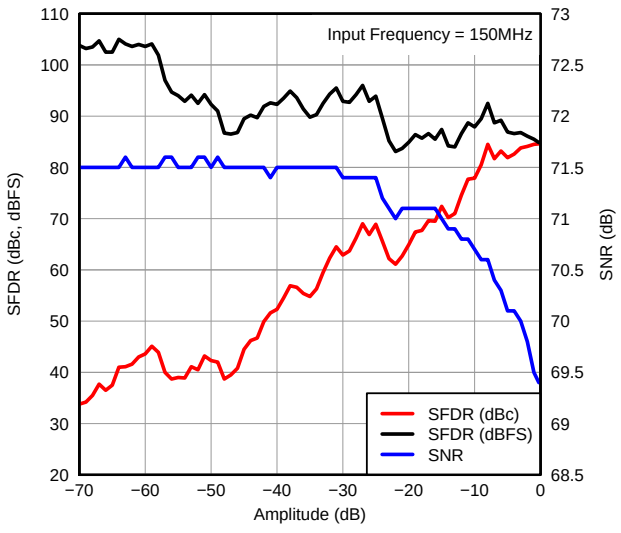



**Figure 67.**

## TYPICAL CHARACTERISTICS: ADS4226 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

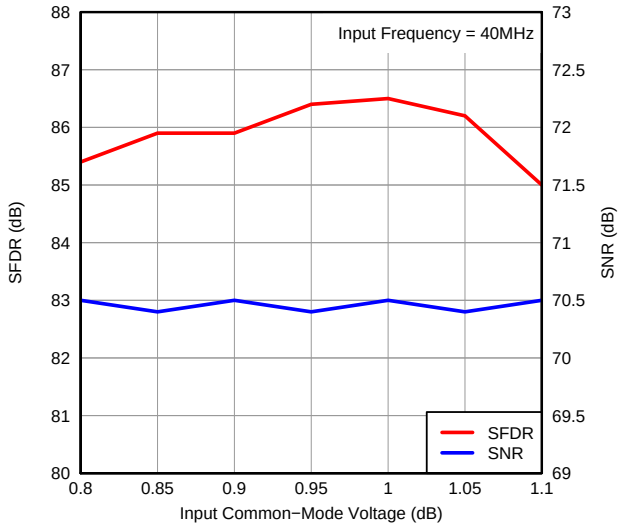



**Figure 68.**

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

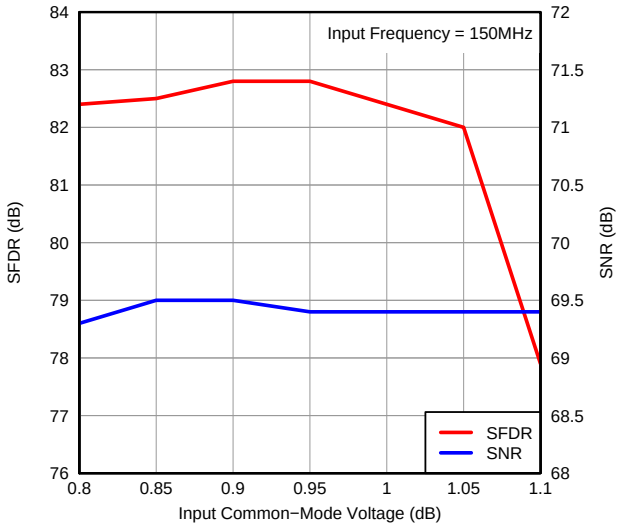



**Figure 69.**

**SFDR vs TEMPERATURE AND AVDD SUPPLY**

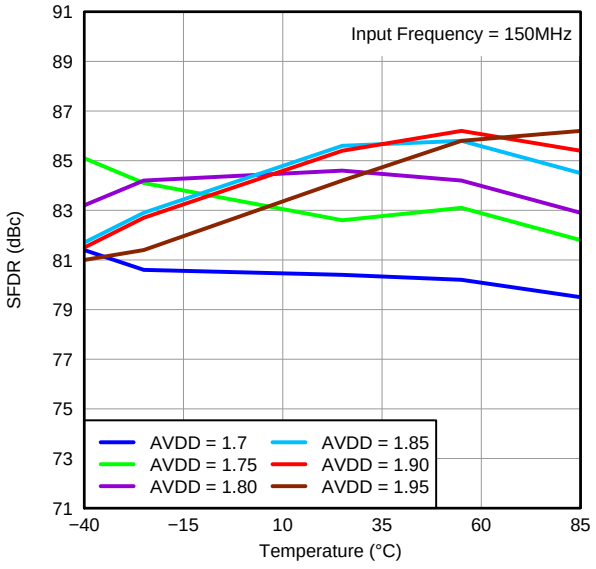



**Figure 70.**

**SNR vs TEMPERATURE AND AVDD SUPPLY**

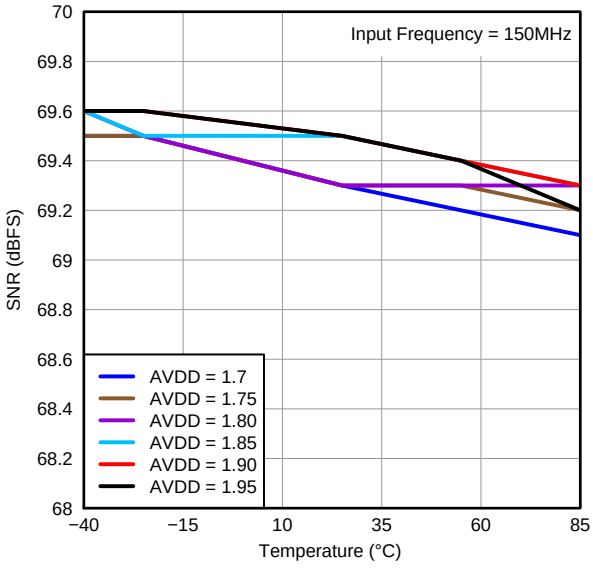



**Figure 71.**

## TYPICAL CHARACTERISTICS: ADS4226 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs DRVDD SUPPLY VOLTAGE**

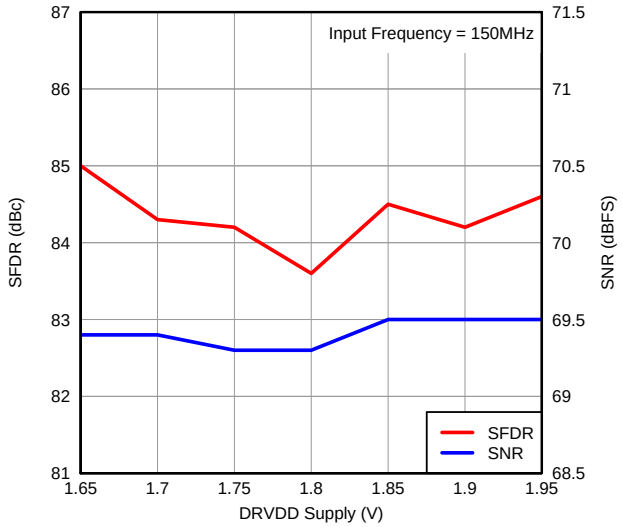



**Figure 72.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

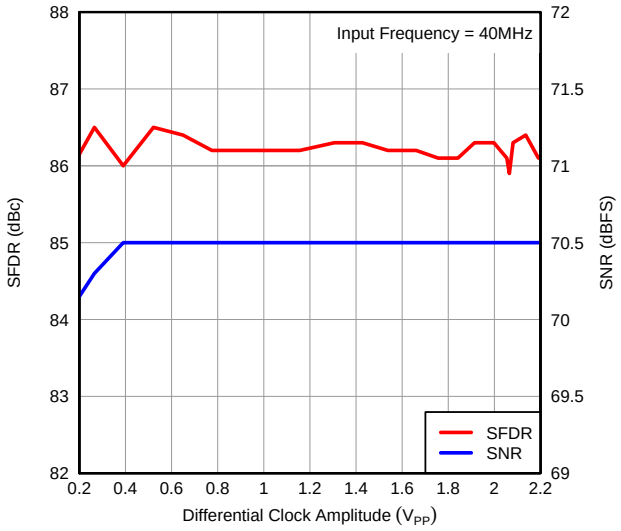



**Figure 73.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

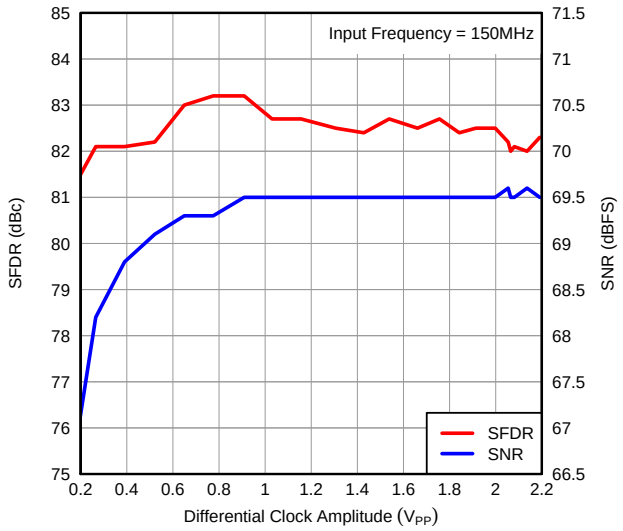



**Figure 74.**

**PERFORMANCE vs INPUT CLOCK DUTY CYCLE**

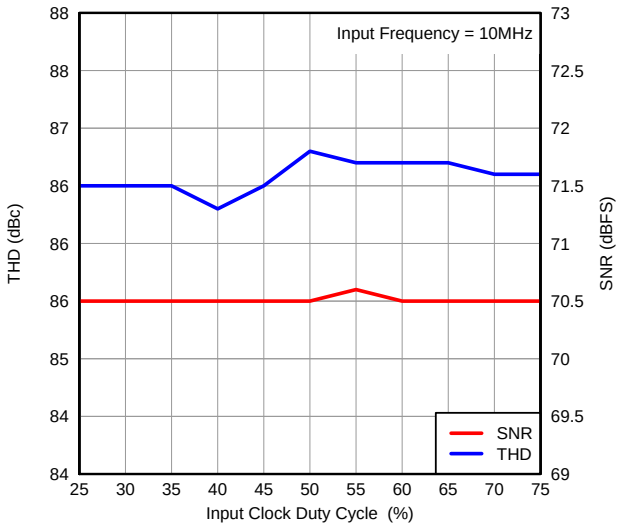



**Figure 75.**

## TYPICAL CHARACTERISTICS: ADS4242

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR 20MHz INPUT SIGNAL**

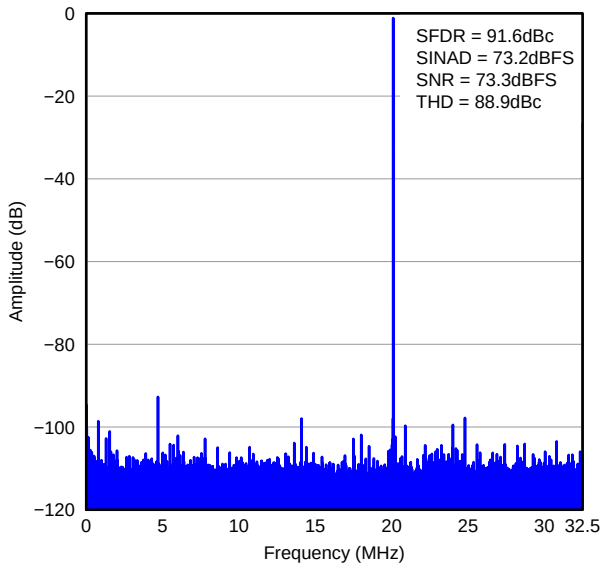



**Figure 76.**

**FFT FOR 170MHz INPUT SIGNAL**

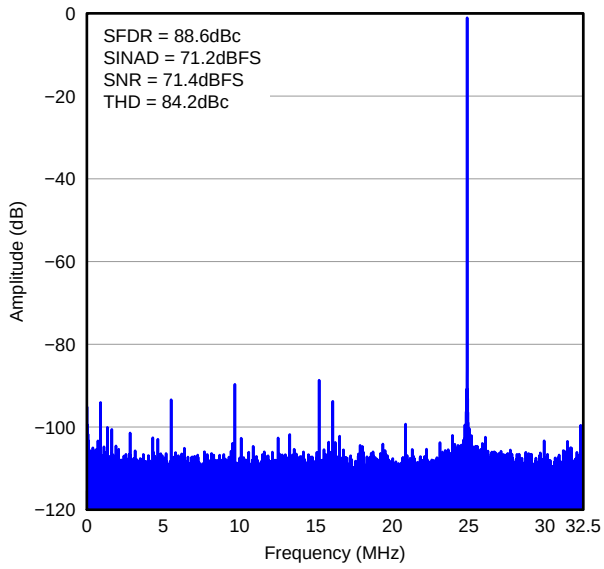



**Figure 77.**

**FFT FOR 300MHz INPUT SIGNAL**

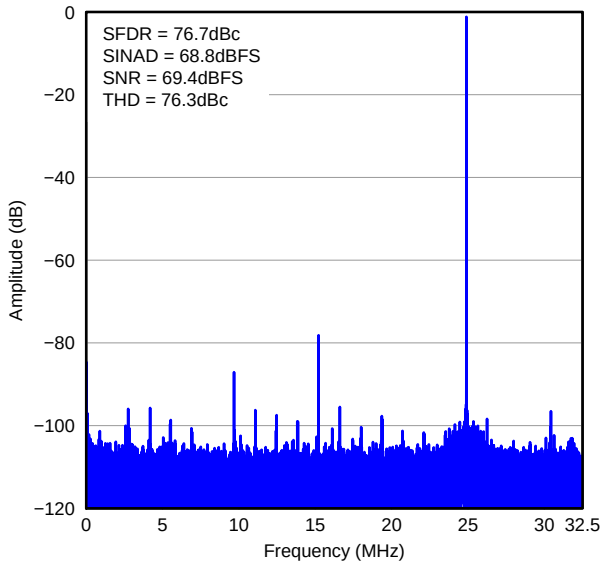



**Figure 78.**

**FFT FOR TWO-TONE INPUT SIGNAL**

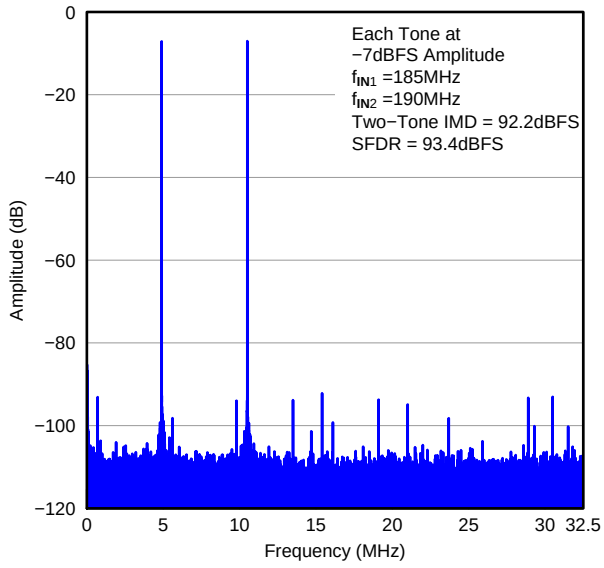



**Figure 79.**

## TYPICAL CHARACTERISTICS: ADS4242 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR TWO-TONE INPUT SIGNAL**

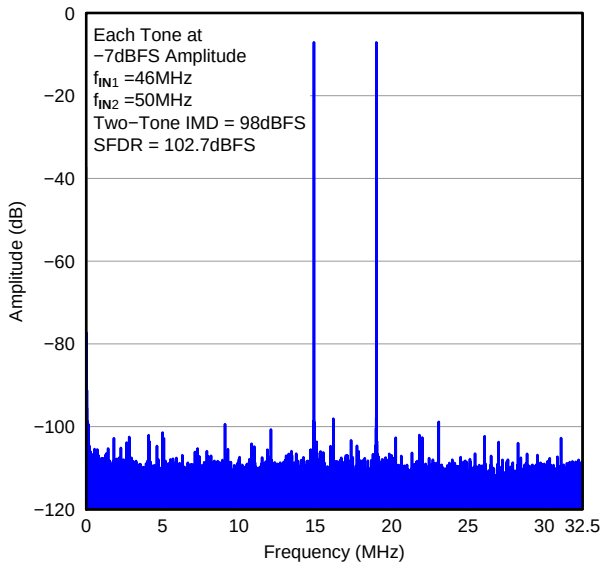



**Figure 80.**

**SFDR vs INPUT FREQUENCY**

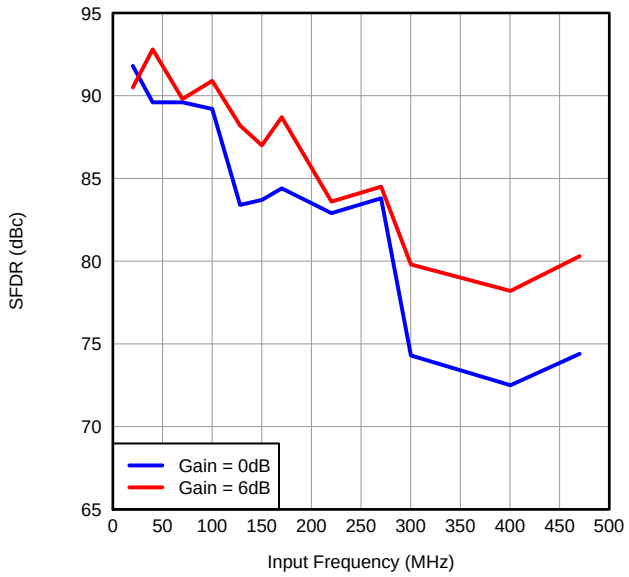



**Figure 81.**

**SNR vs INPUT FREQUENCY**

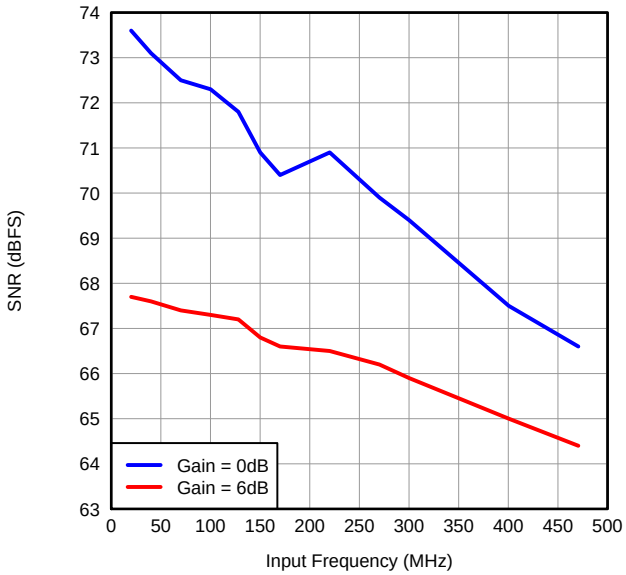



**Figure 82.**

**SNR vs INPUT FREQUENCY (CMOS)**

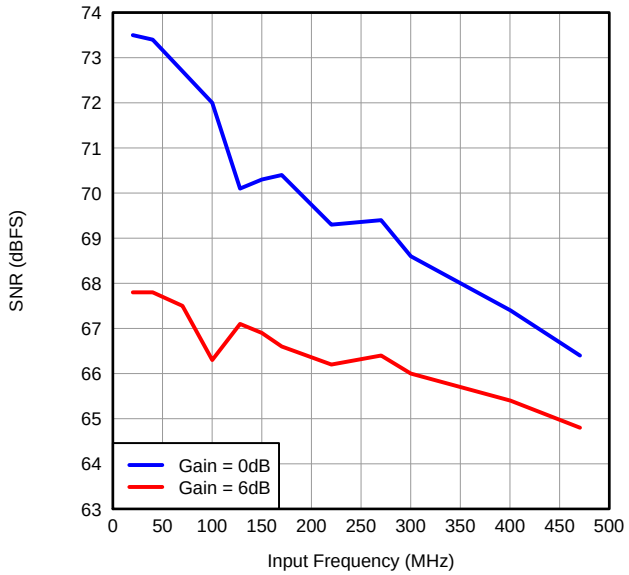



**Figure 83.**

## TYPICAL CHARACTERISTICS: ADS4242 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**SFDR vs GAIN AND INPUT FREQUENCY**

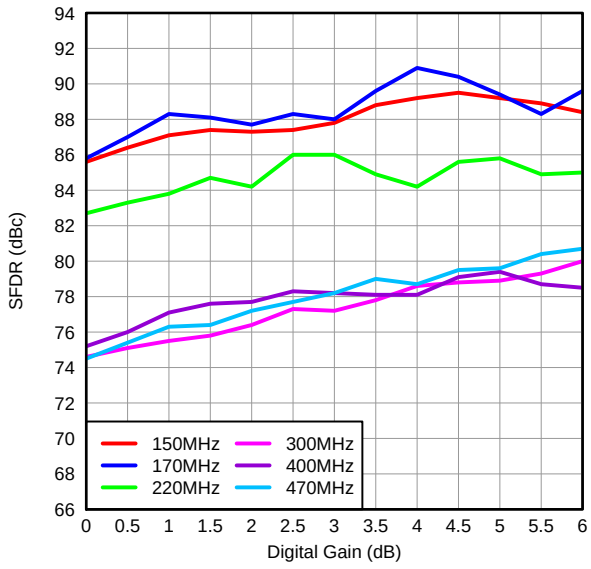



**Figure 84.**

**SINAD vs GAIN AND INPUT FREQUENCY**

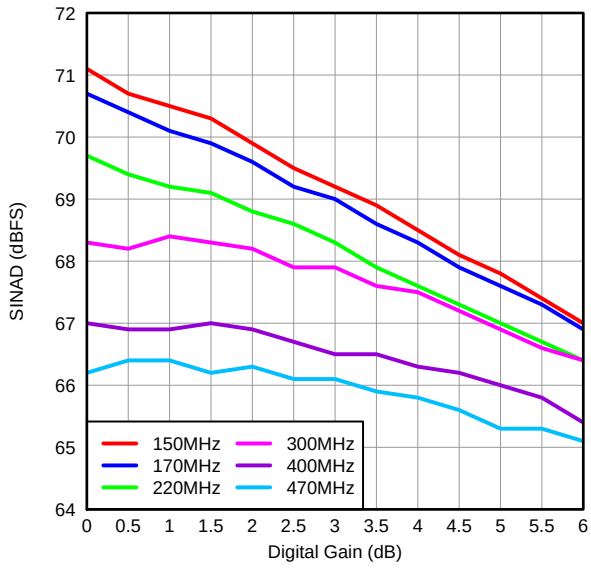



**Figure 85.**

**PERFORMANCE vs INPUT AMPLITUDE**

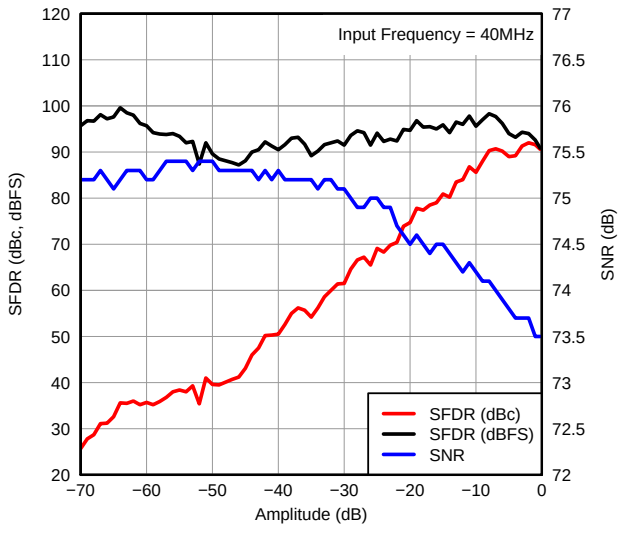



**Figure 86.**

**PERFORMANCE vs INPUT AMPLITUDE**

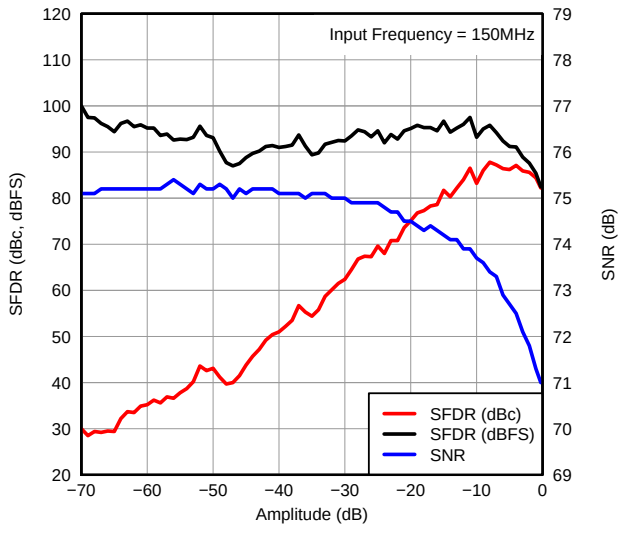



**Figure 87.**

## TYPICAL CHARACTERISTICS: ADS4242 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

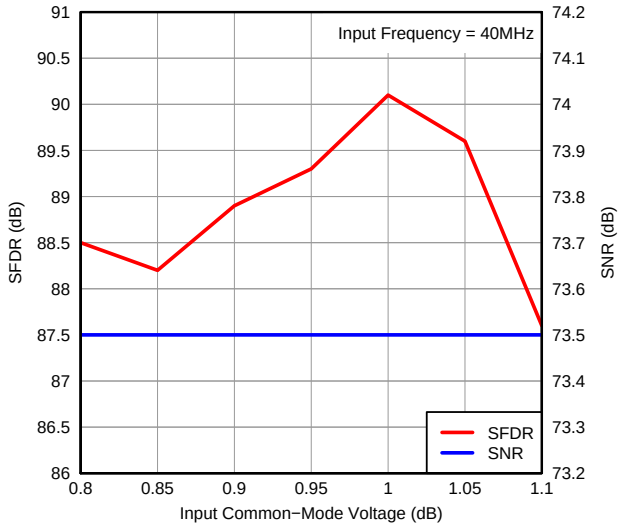



**Figure 88.**

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

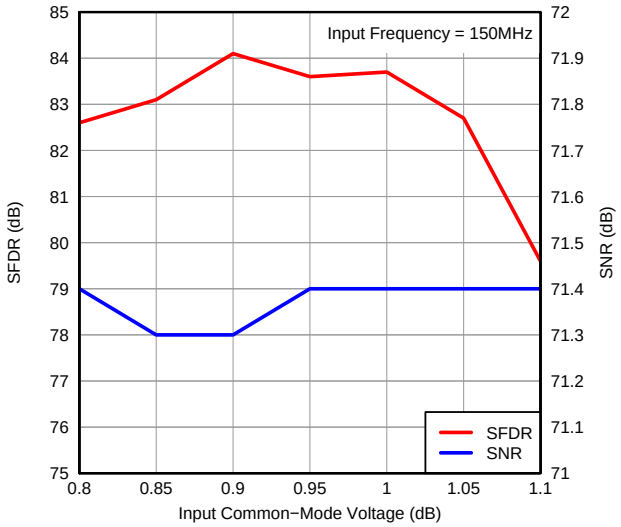



**Figure 89.**

**SFDR vs TEMPERATURE AND AVDD SUPPLY**

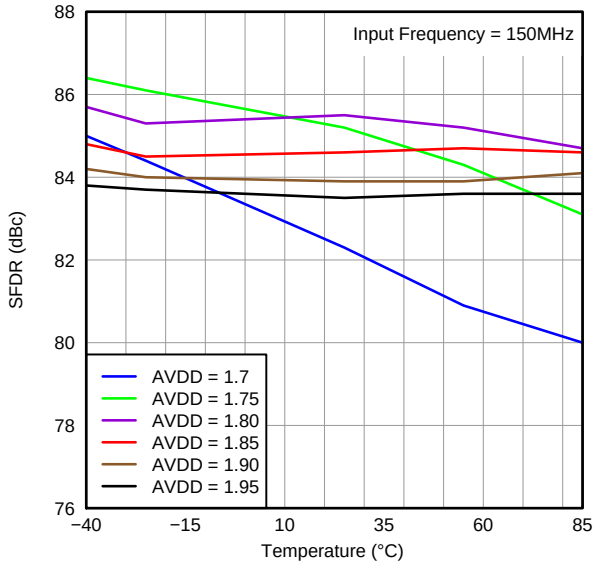



**Figure 90.**

**SNR vs TEMPERATURE AND AVDD SUPPLY**

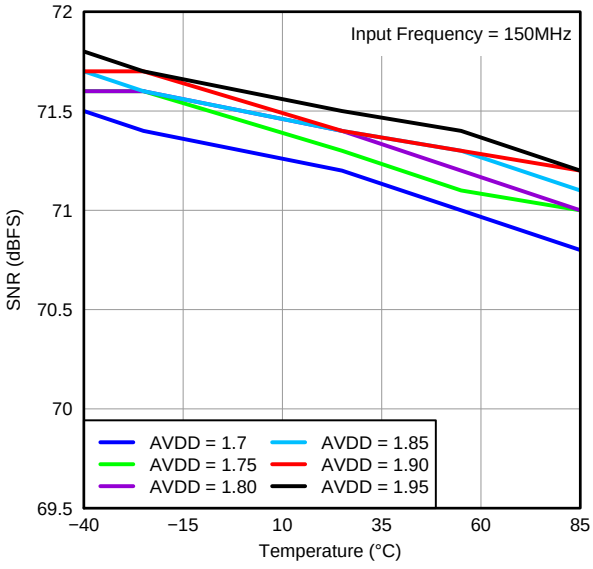



**Figure 91.**

## TYPICAL CHARACTERISTICS: ADS4242 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs DRVDD SUPPLY VOLTAGE**

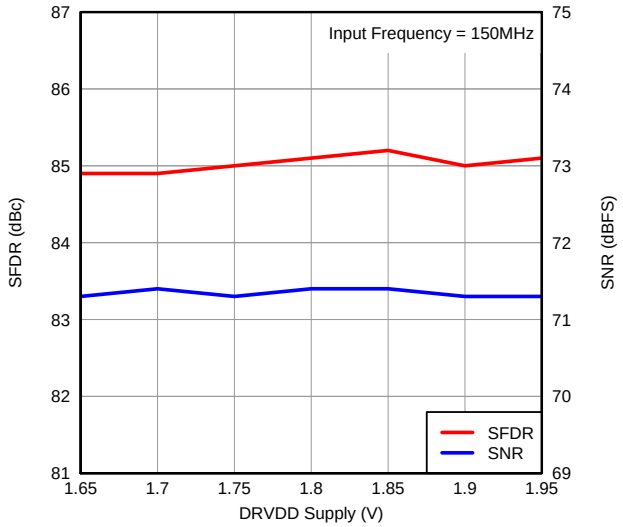



**Figure 92.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

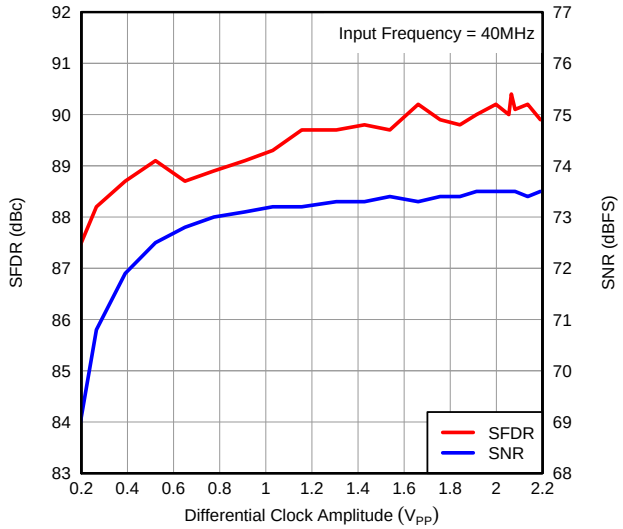



**Figure 93.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

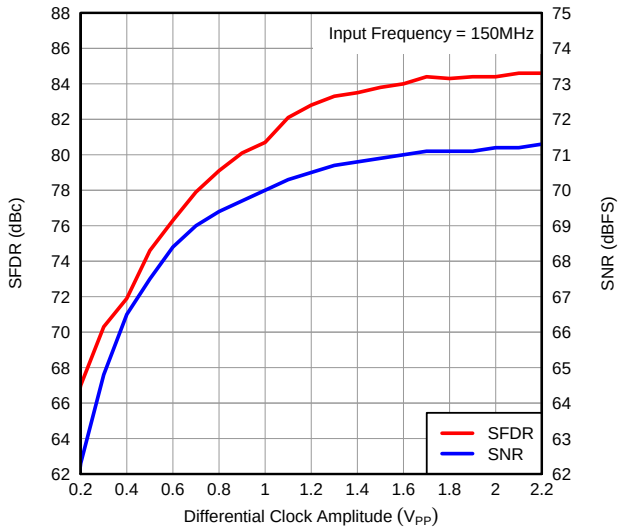



**Figure 94.**

**PERFORMANCE ACROSS INPUT CLOCK DUTY CYCLE**

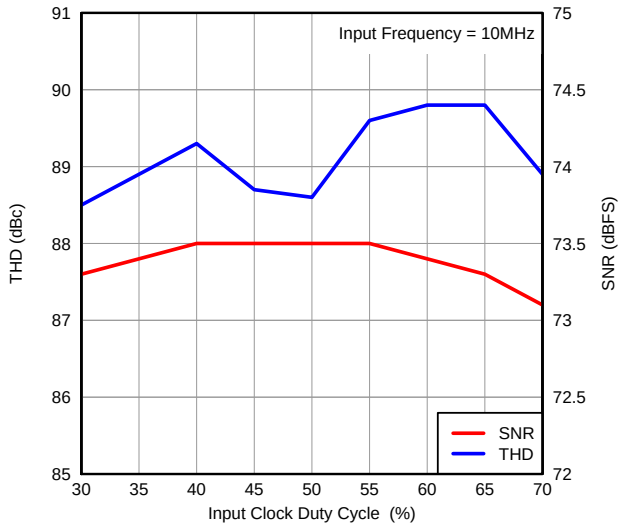



**Figure 95.**

## TYPICAL CHARACTERISTICS: ADS4242 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, $1.5V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**INTEGRATED NONLINEARITY**

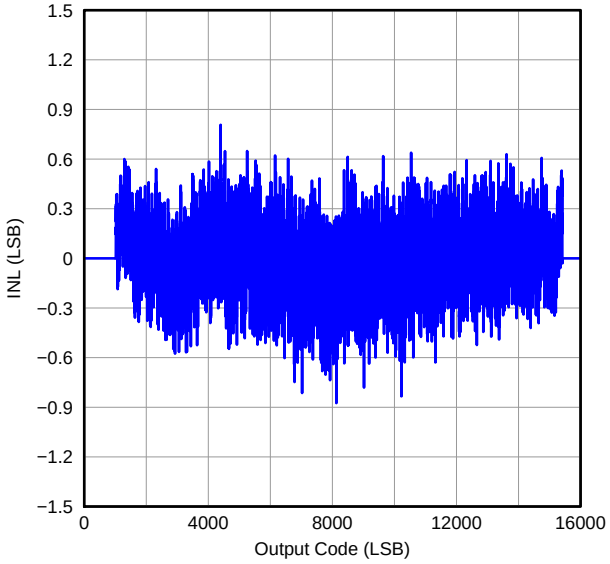



**Figure 96.**

**OUTPUT NOISE HISTOGRAM (WITH INPUTS SHORTED TO VCM)**

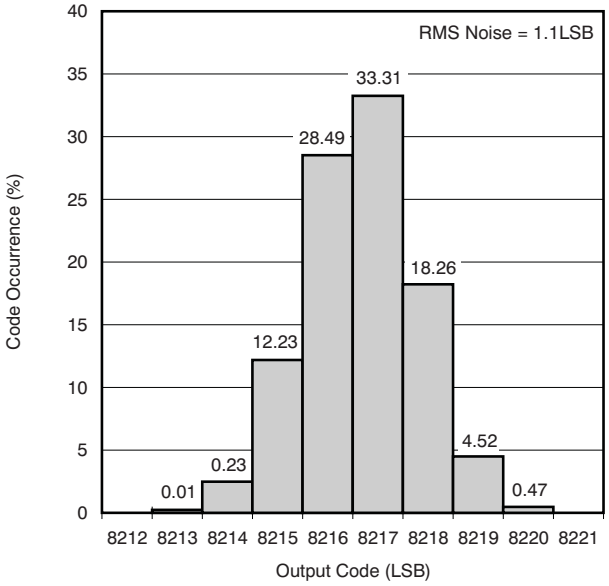



**Figure 97.**

## TYPICAL CHARACTERISTICS: ADS4245

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, $1.5V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR 20MHz INPUT SIGNAL**

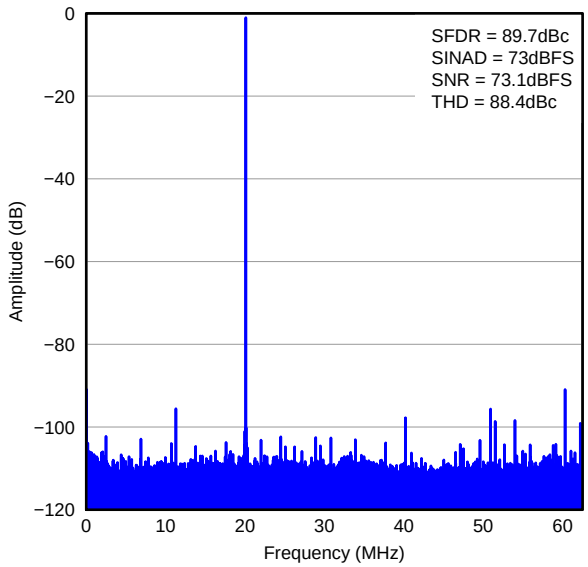



**Figure 98.**

**FFT FOR 170MHz INPUT SIGNAL**

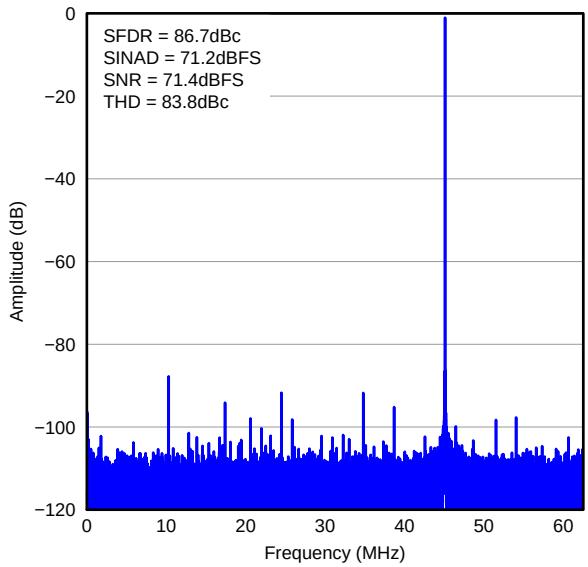



**Figure 99.**

**FFT FOR 300MHz INPUT SIGNAL**

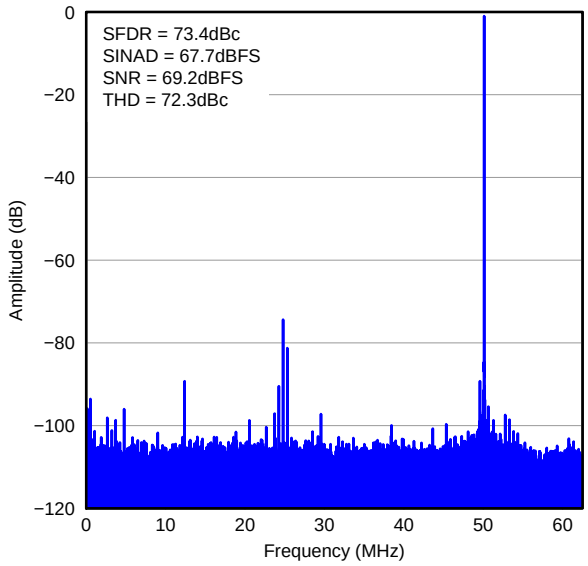



**Figure 100.**

**FFT FOR TWO-TONE INPUT SIGNAL**

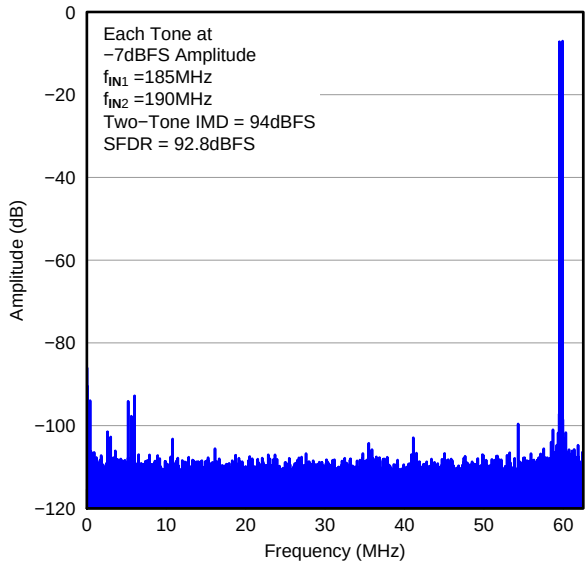



**Figure 101.**

## TYPICAL CHARACTERISTICS: ADS4245 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR TWO-TONE INPUT SIGNAL**

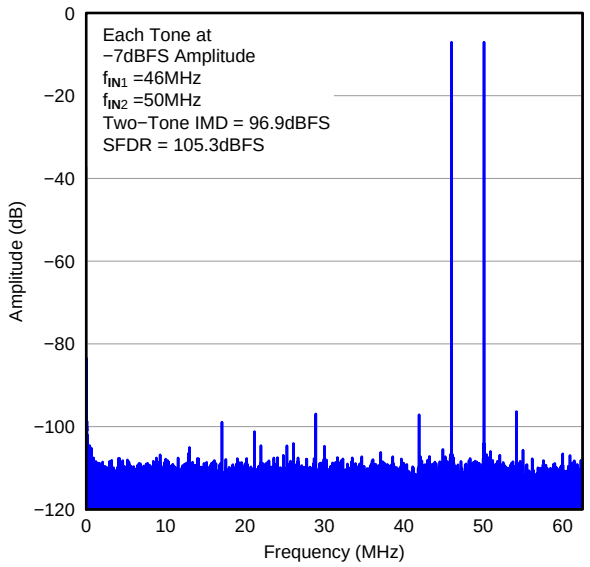



**Figure 102.**

**SFDR vs INPUT FREQUENCY**

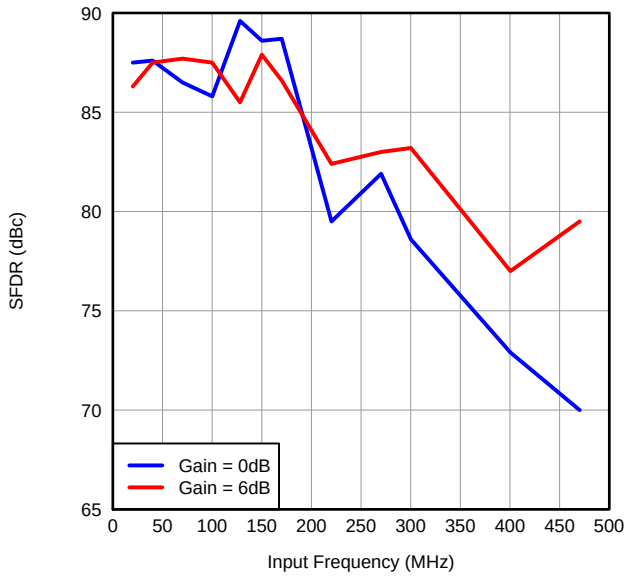



**Figure 103.**

**SNR vs INPUT FREQUENCY**

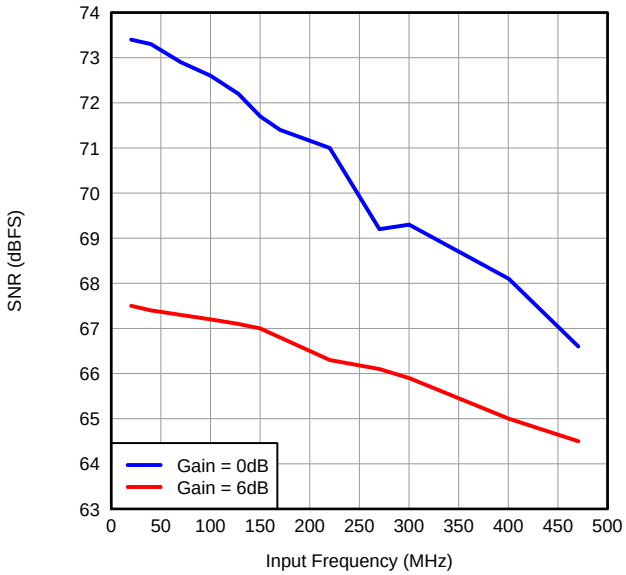



**Figure 104.**

**SNR vs INPUT FREQUENCY (CMOS)**

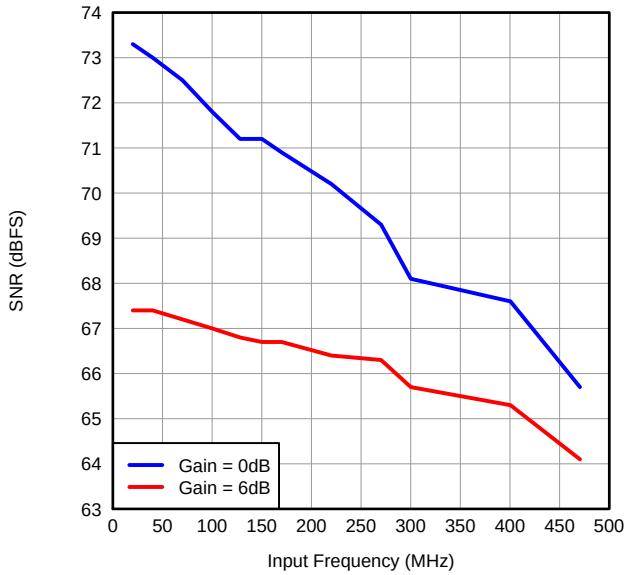



**Figure 105.**

## TYPICAL CHARACTERISTICS: ADS4245 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**SFDR vs GAIN AND INPUT FREQUENCY**

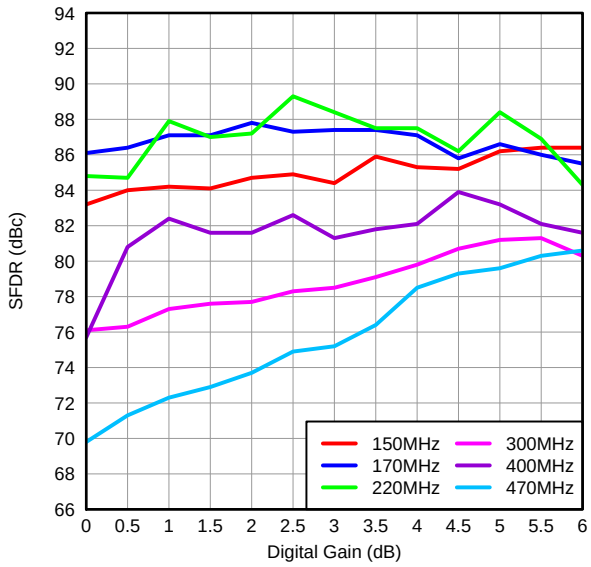



**Figure 106.**

**SINAD vs GAIN AND INPUT FREQUENCY**

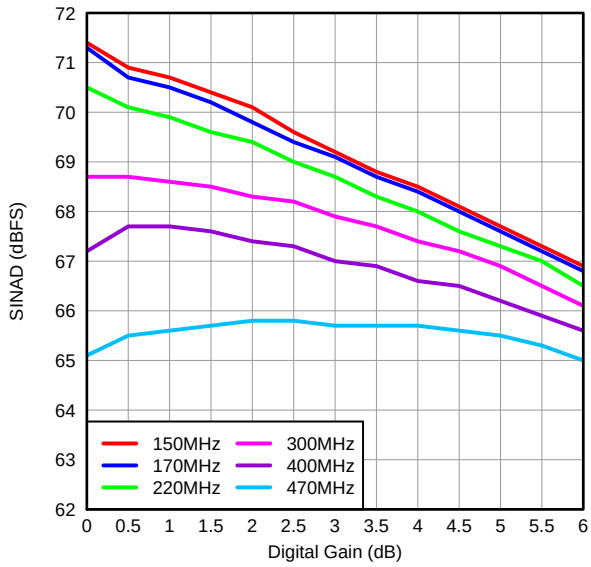



**Figure 107.**

**PERFORMANCE vs INPUT AMPLITUDE**

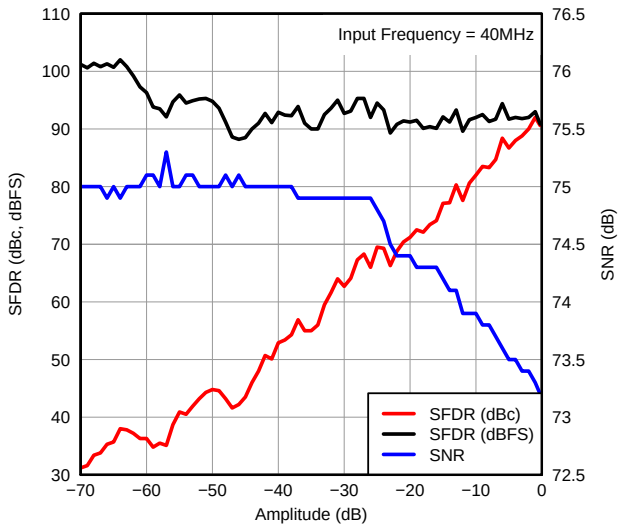



**Figure 108.**

**PERFORMANCE vs INPUT AMPLITUDE**

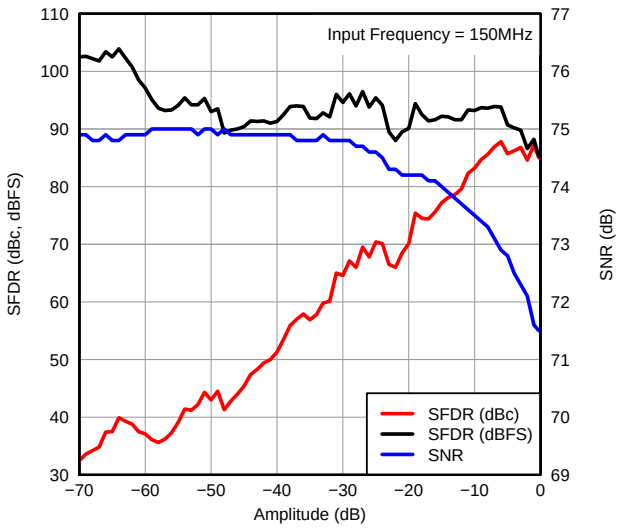



**Figure 109.**

## TYPICAL CHARACTERISTICS: ADS4245 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

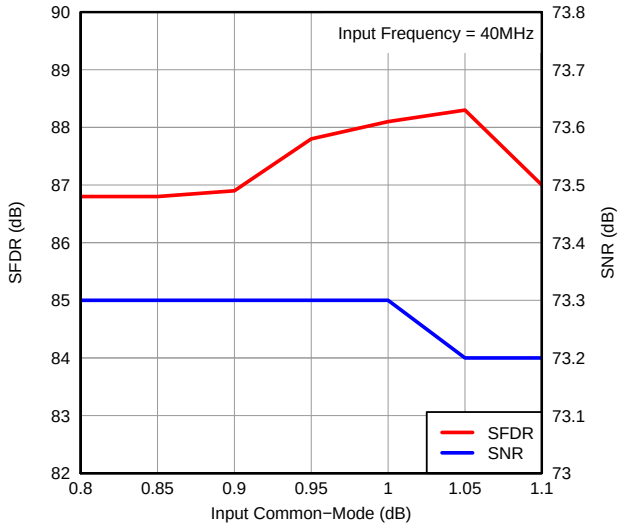



**Figure 110.**

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

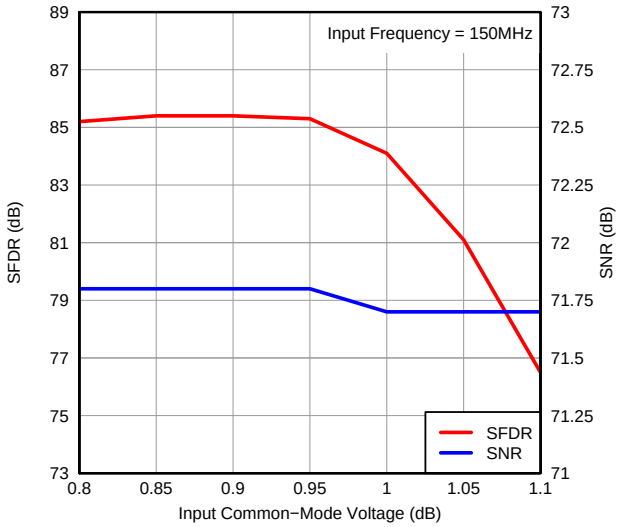



**Figure 111.**

**SFDR vs TEMPERATURE AND AVDD SUPPLY**

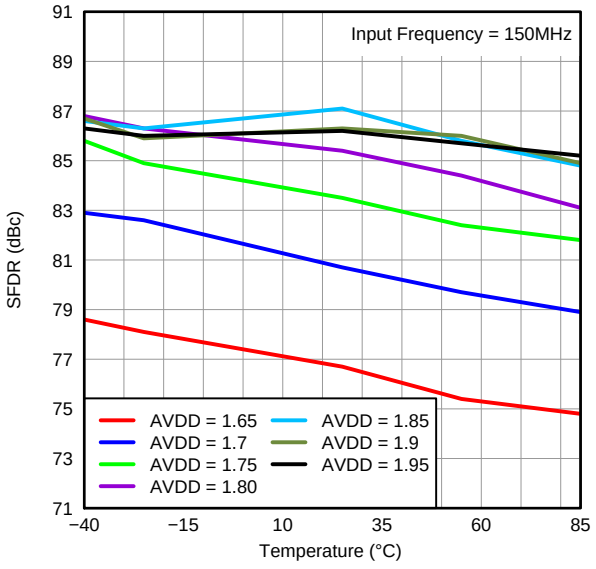



**Figure 112.**

**SNR vs TEMPERATURE AND AVDD SUPPLY**

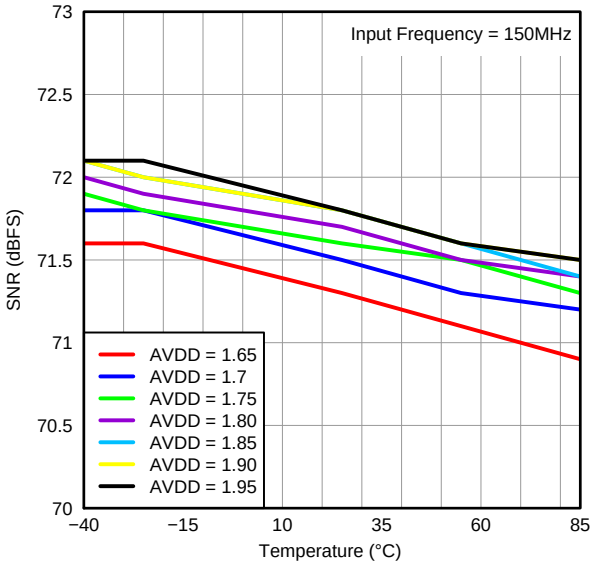



**Figure 113.**

## TYPICAL CHARACTERISTICS: ADS4245 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs DRVDD SUPPLY VOLTAGE**

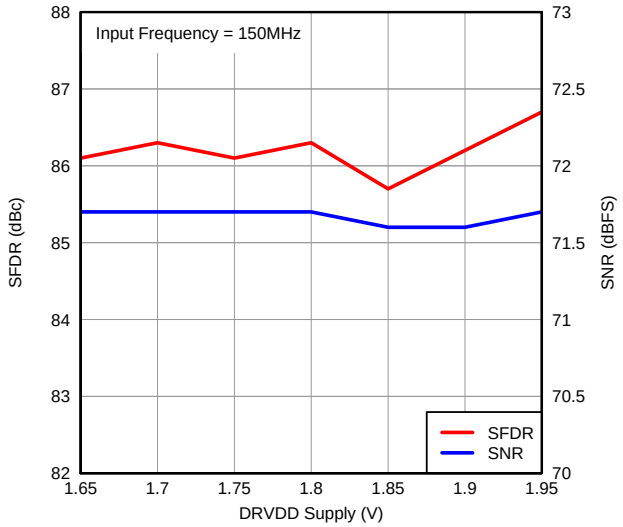



**Figure 114.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

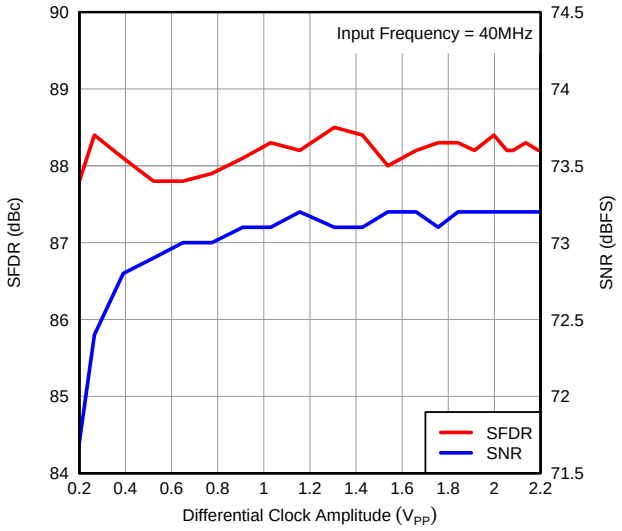



**Figure 115.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

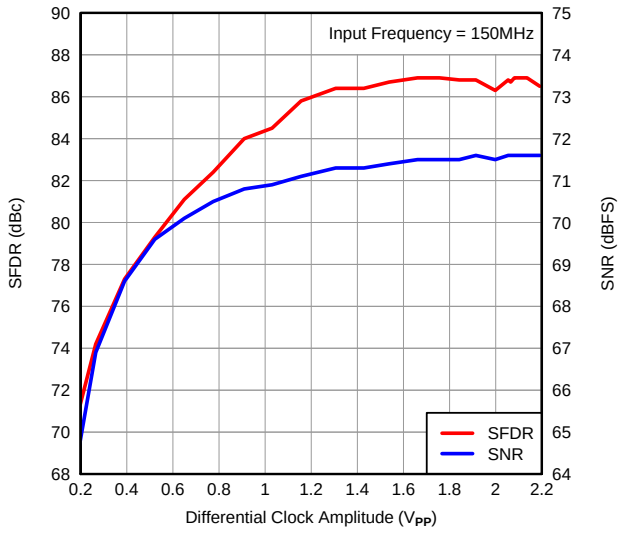



**Figure 116.**

**PERFORMANCE vs INPUT CLOCK DUTY CYCLE**

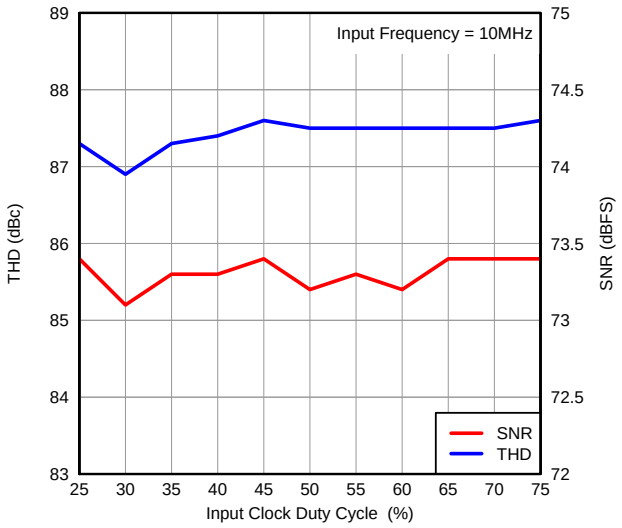



**Figure 117.**

## TYPICAL CHARACTERISTICS: ADS4245 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, $1.5V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**INTEGRATED NONLINEARITY**

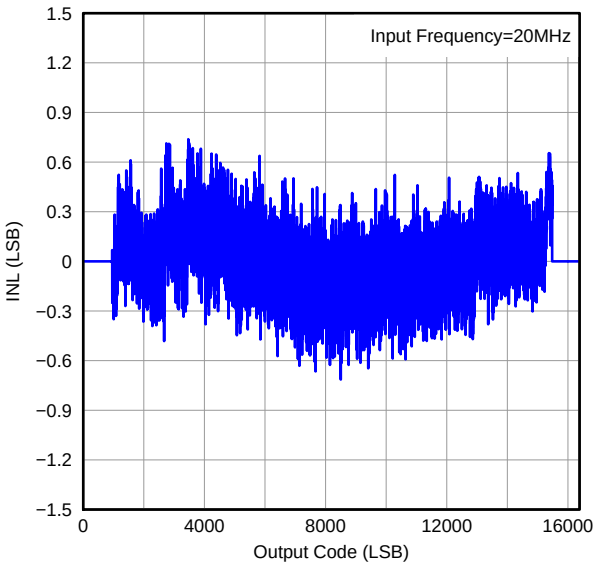



**Figure 118.**

**OUTPUT NOISE HISTOGRAM (WITH INPUTS SHORTED TO VCM)**

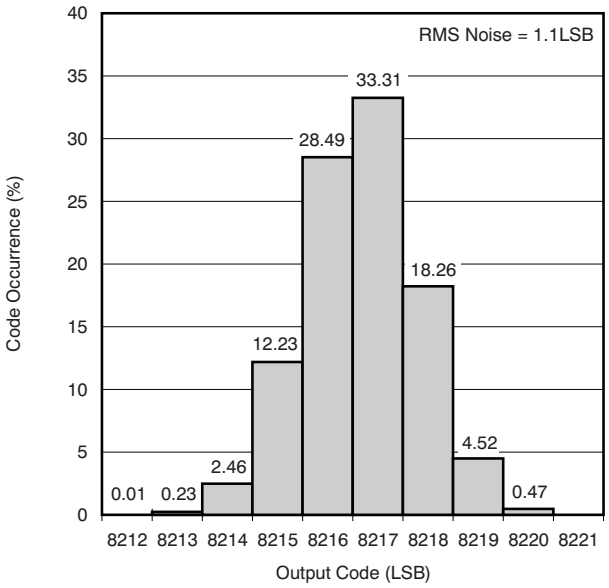



**Figure 119.**

## TYPICAL CHARACTERISTICS: ADS4246

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR 20MHz INPUT SIGNAL**

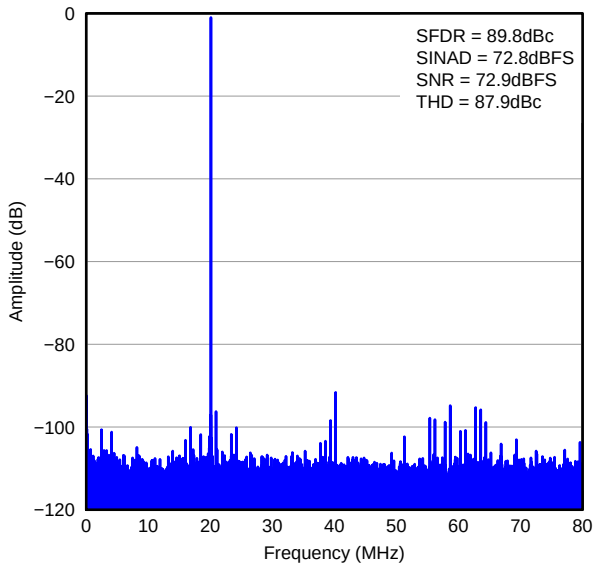



**Figure 120.**

**FFT FOR 170MHz INPUT SIGNAL**

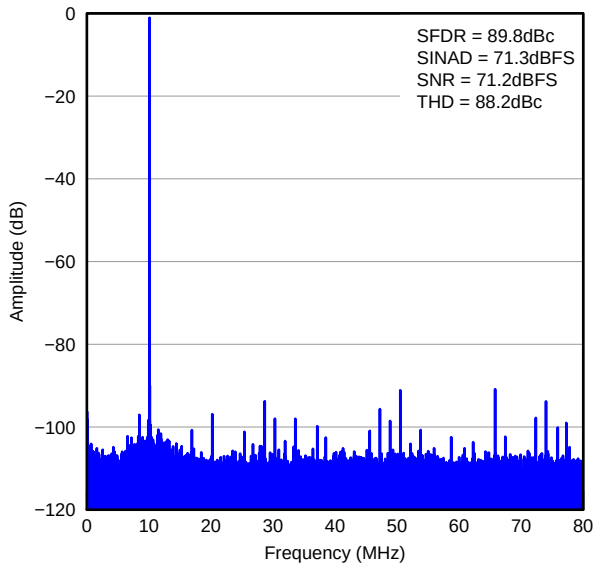



**Figure 121.**

**FFT FOR 300MHz INPUT SIGNAL**

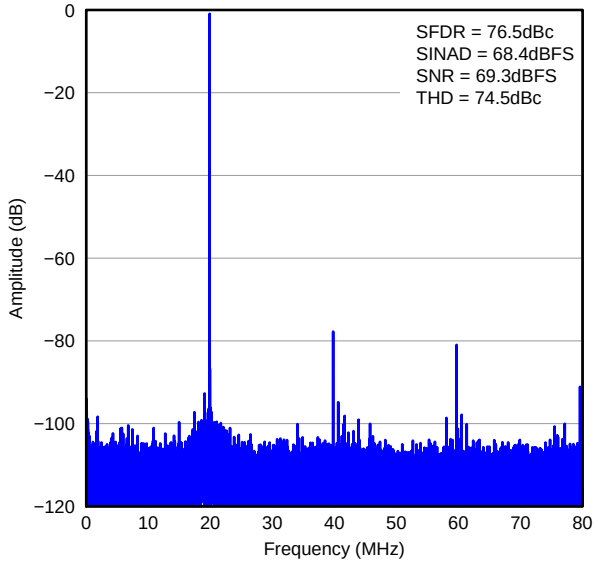



**Figure 122.**

**FFT FOR TWO-TONE INPUT SIGNAL**

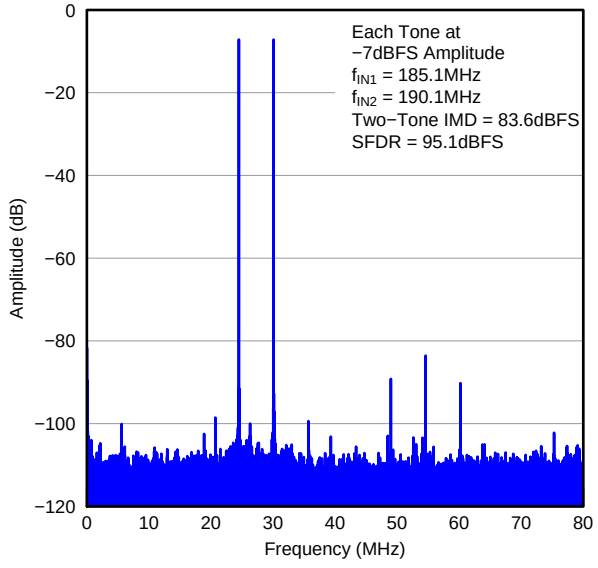



**Figure 123.**

## TYPICAL CHARACTERISTICS: ADS4246 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**FFT FOR TWO-TONE INPUT SIGNAL**

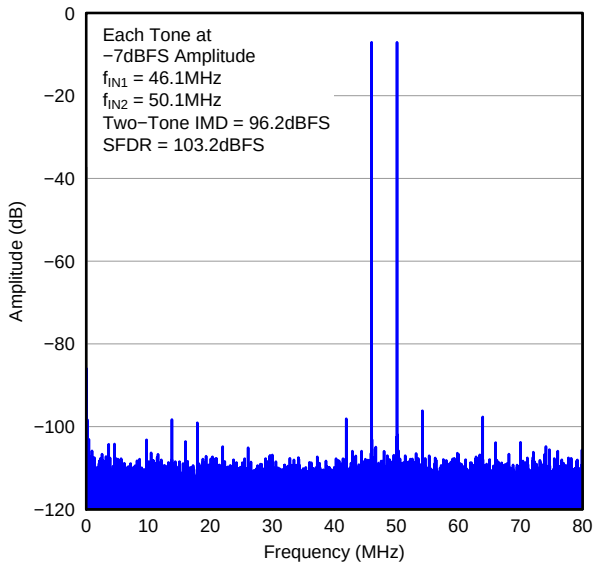



**Figure 124.**

**SFDR vs INPUT FREQUENCY**

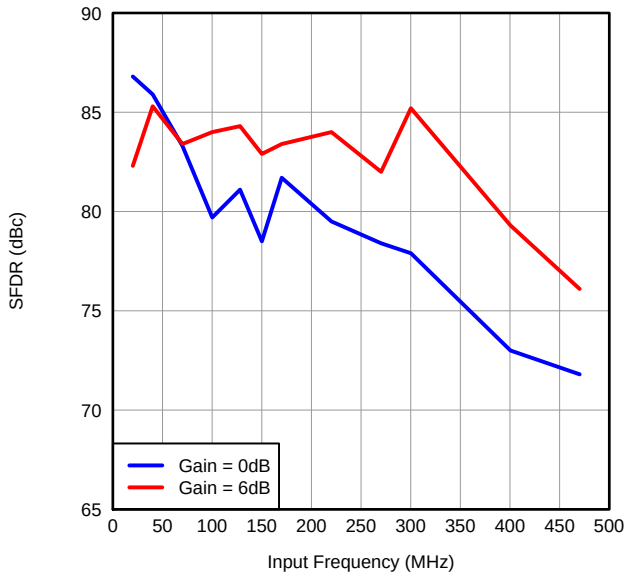



**Figure 125.**

**SNR vs INPUT FREQUENCY**

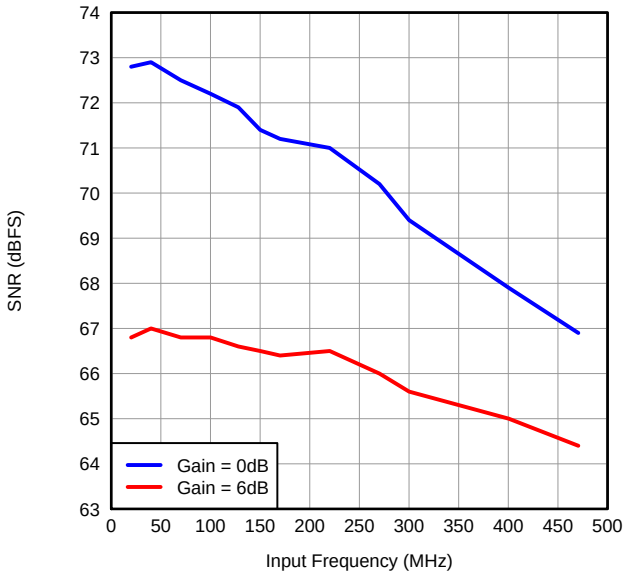



**Figure 126.**

**SNR vs INPUT FREQUENCY (CMOS)**

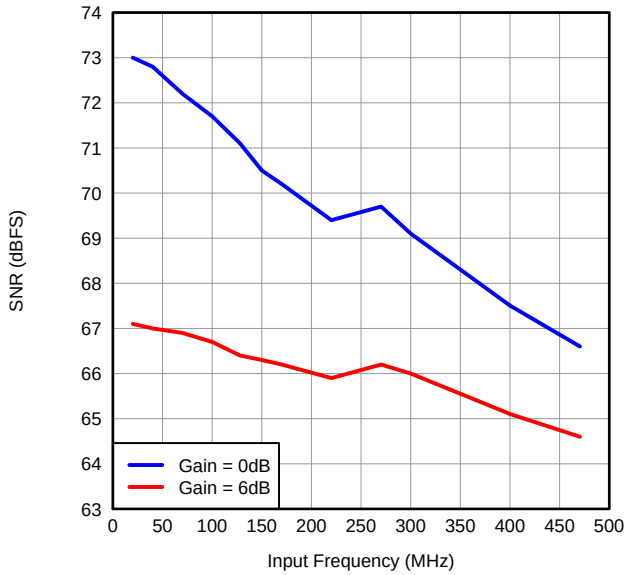



**Figure 127.**

## TYPICAL CHARACTERISTICS: ADS4246 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**SFDR vs GAIN AND INPUT FREQUENCY**

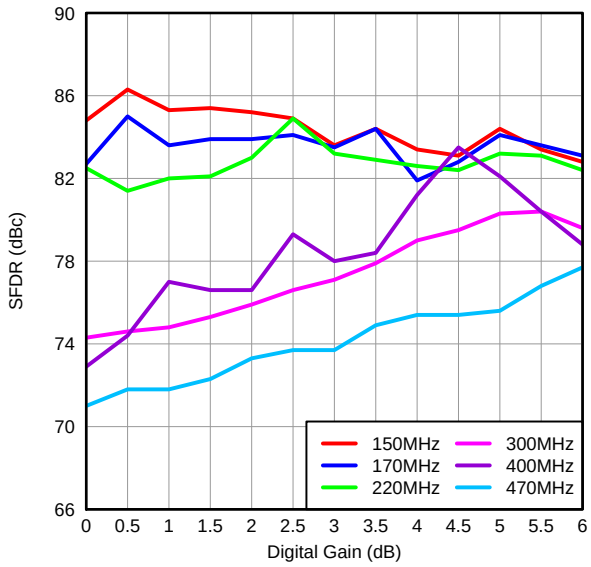



**Figure 128.**

**SINAD vs GAIN AND INPUT FREQUENCY**

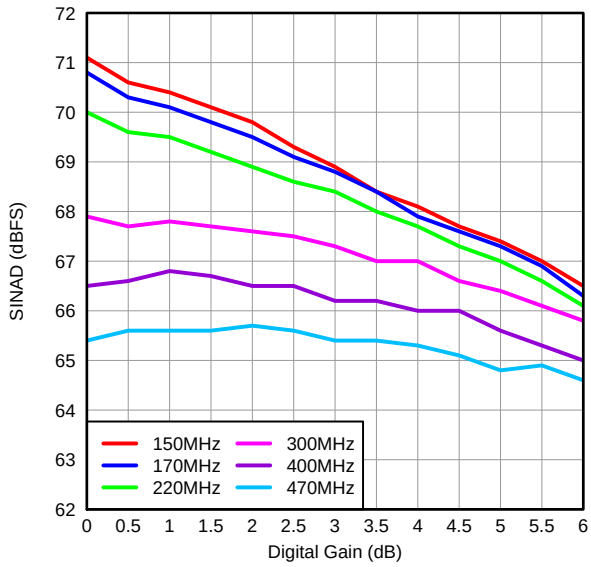



**Figure 129.**

**PERFORMANCE vs INPUT AMPLITUDE**

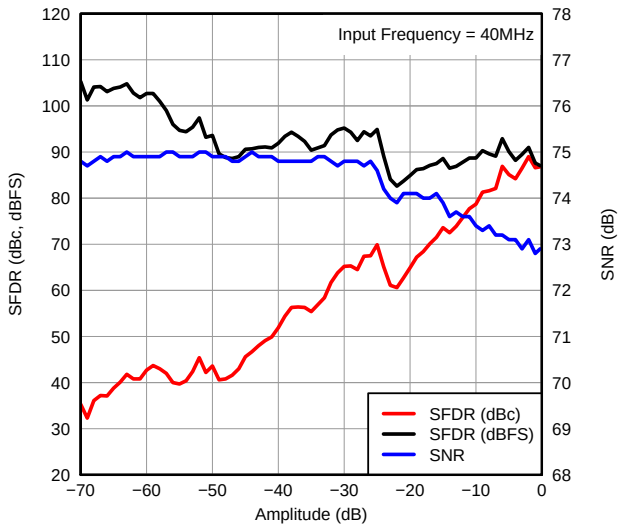



**Figure 130.**

**PERFORMANCE vs INPUT AMPLITUDE**

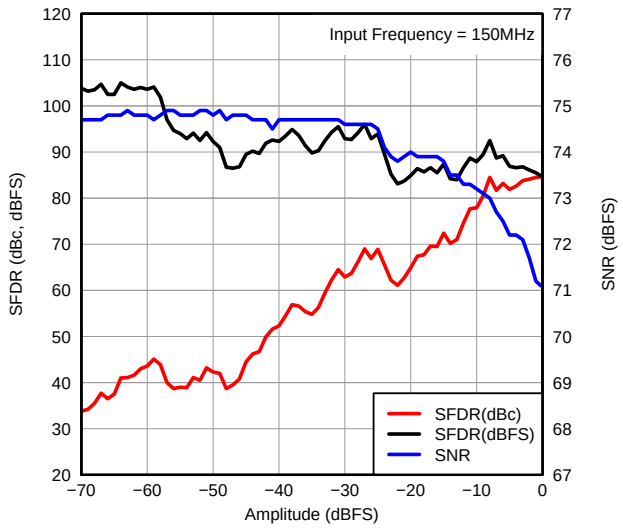



**Figure 131.**

## TYPICAL CHARACTERISTICS: ADS4246 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

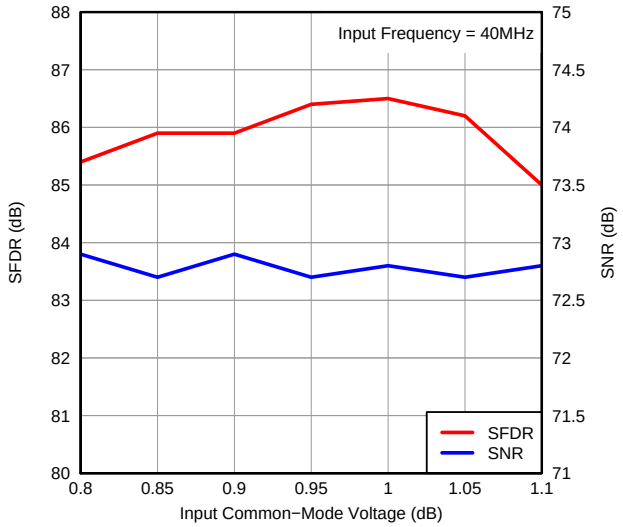



**Figure 132.**

**PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

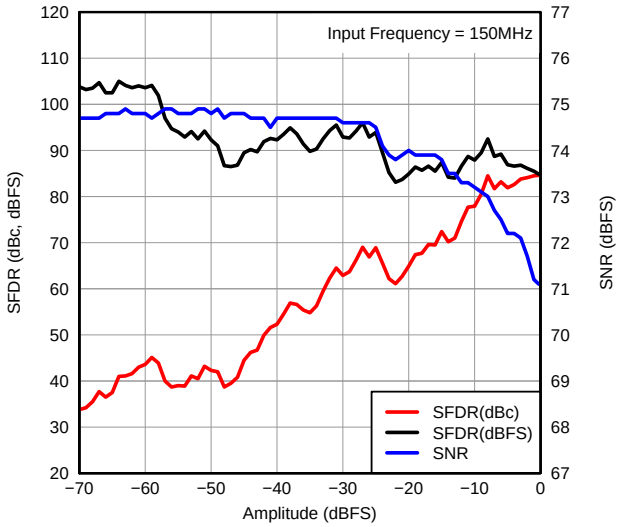



**Figure 133.**

**SFDR vs TEMPERATURE AND AVDD SUPPLY**

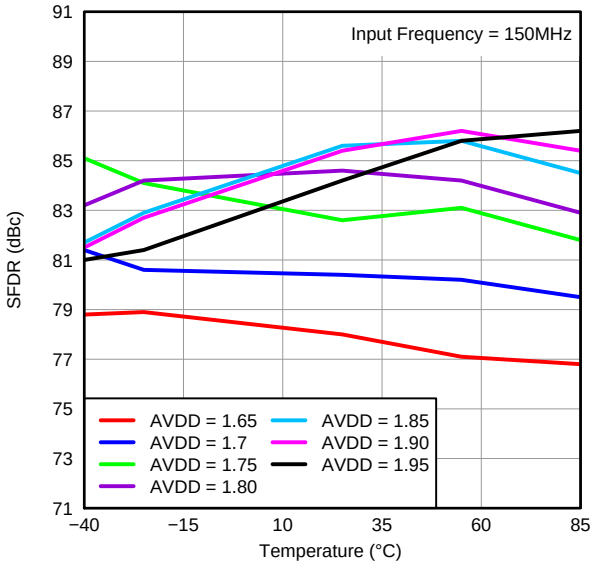



**Figure 134.**

**SNR vs TEMPERATURE AND AVDD SUPPLY**

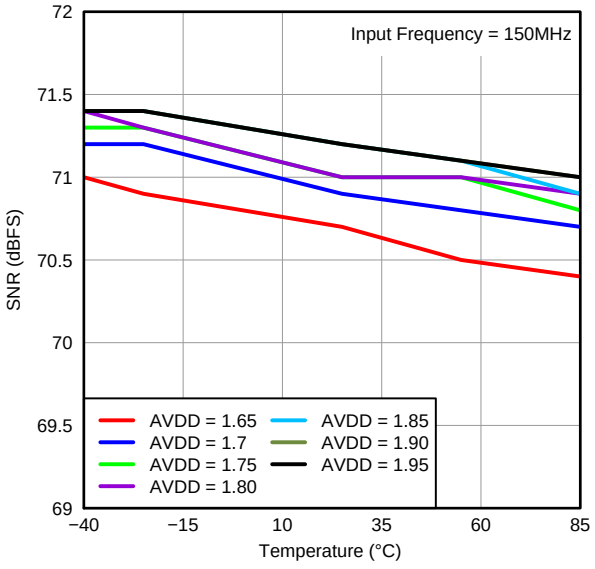



**Figure 135.**

## TYPICAL CHARACTERISTICS: ADS4246 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**PERFORMANCE vs DRVDD SUPPLY VOLTAGE**

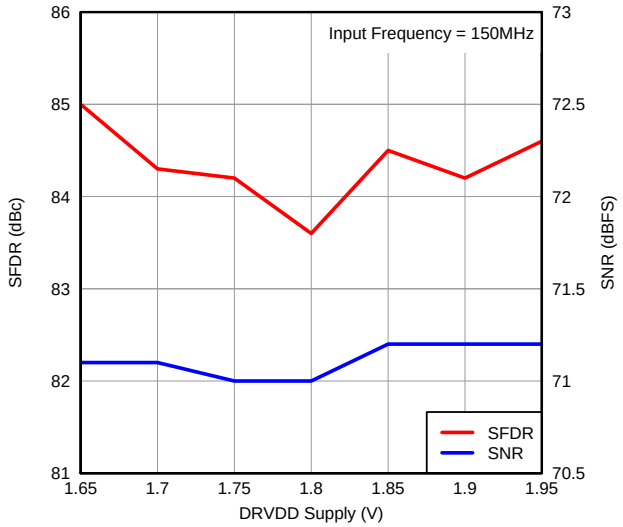



**Figure 136.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

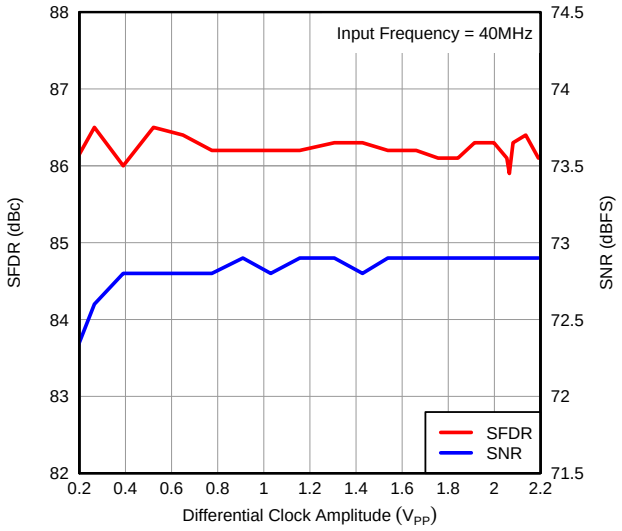



**Figure 137.**

**PERFORMANCE vs INPUT CLOCK AMPLITUDE**

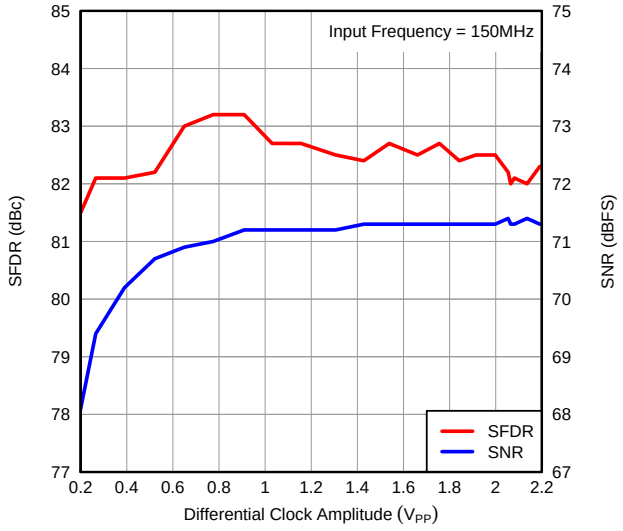



**Figure 138.**

**PERFORMANCE vs INPUT CLOCK DUTY CYCLE**

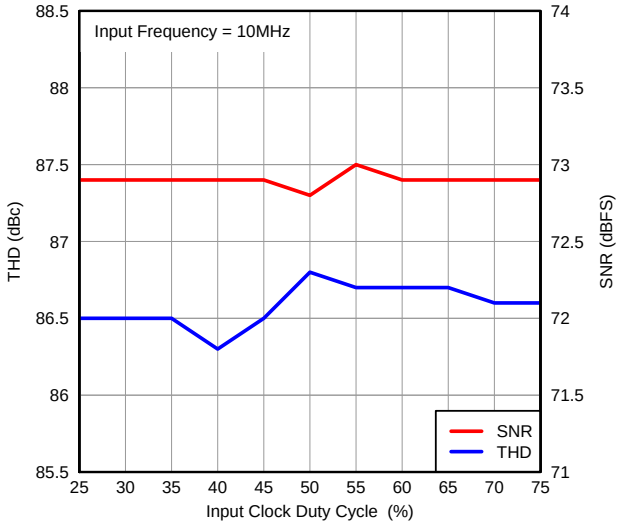



**Figure 139.**

## TYPICAL CHARACTERISTICS: ADS4246 (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, $1.5V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**INTEGRATED NONLINEARITY**

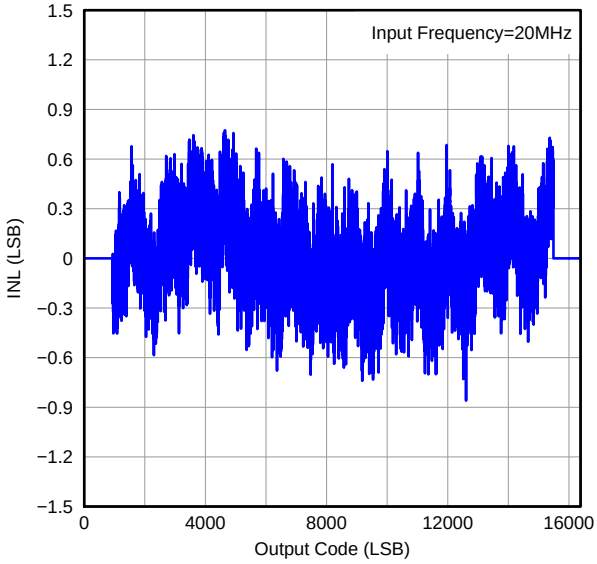



**Figure 140.**

**OUTPUT NOISE HISTOGRAM (WITH INPUTS SHORTED TO VCM)**

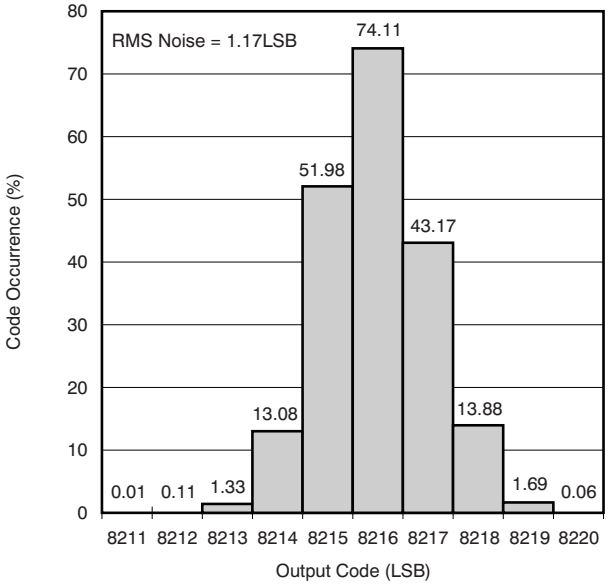



**Figure 141.**

## TYPICAL CHARACTERISTICS: General

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**CMRR vs TEST SIGNAL FREQUENCY**

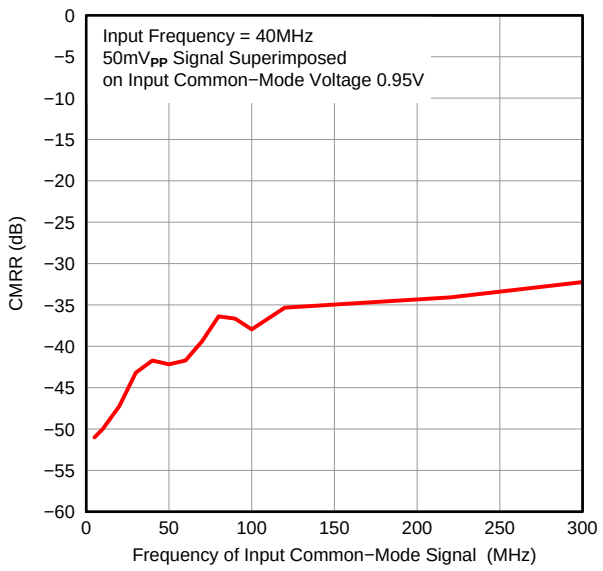



**Figure 142.**

**PSRR vs TEST SIGNAL FREQUENCY**

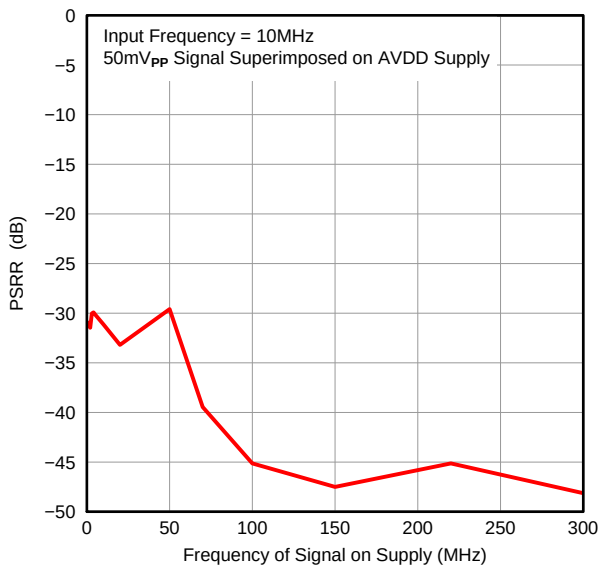



**Figure 143.**

**ANALOG POWER vs SAMPLING FREQUENCY**

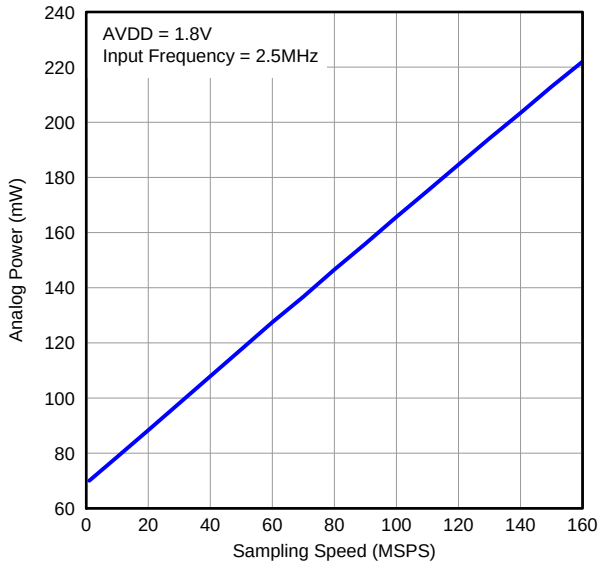



**Figure 144.**

**DIGITAL POWER LVDS CMOS**

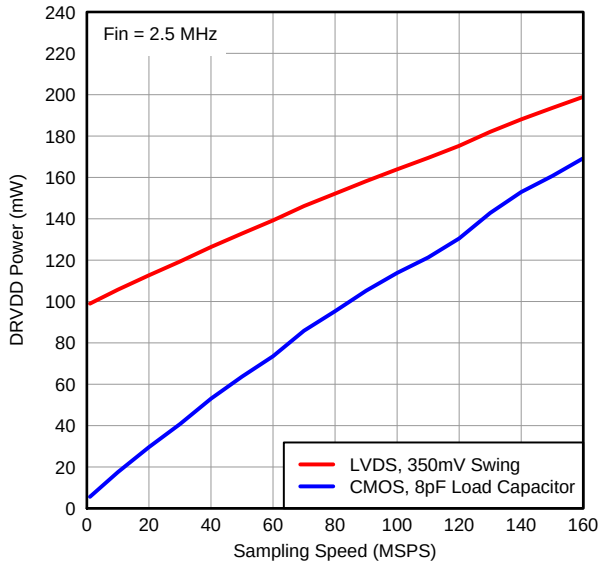



**Figure 145.**

## TYPICAL CHARACTERISTICS: General (continued)

At $T_A$ = +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**DIGITAL POWER IN VARIOUS MODES**

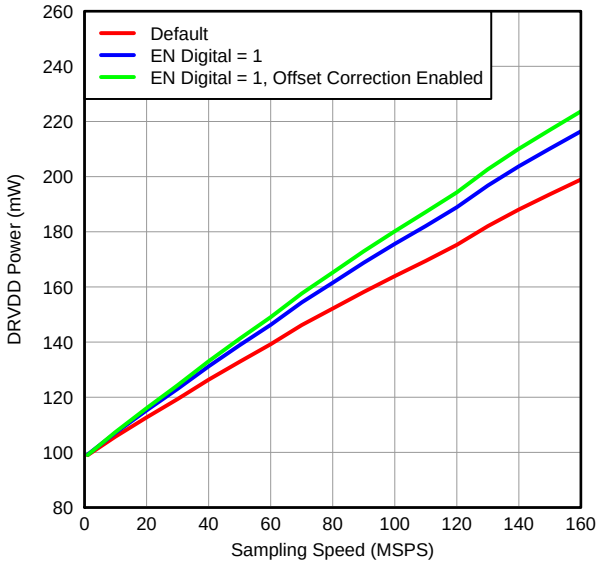



**Figure 146.**

## TYPICAL CHARACTERISTICS: Contour

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**SPURIOUS-FREE DYNAMIC RANGE (0dB Gain)**

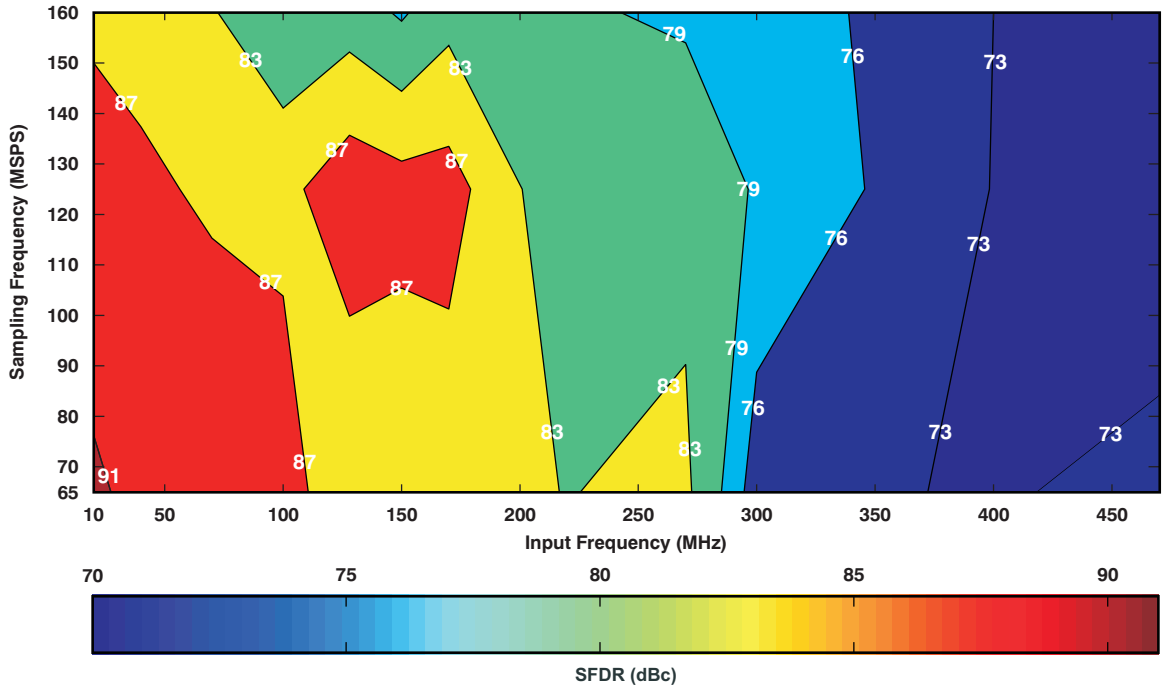



**Figure 147.**

**SPURIOUS-FREE DYNAMIC RANGE (6dB Gain)**

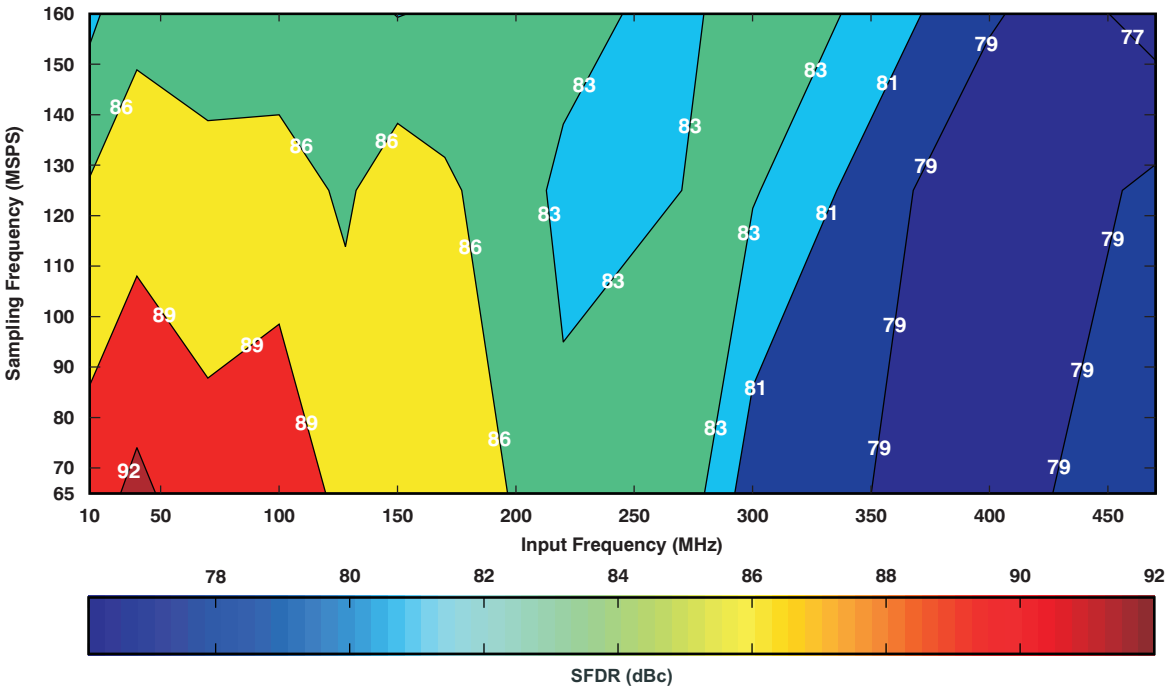



**Figure 148.**

## TYPICAL CHARACTERISTICS: Contour (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

**ADS414x SIGNAL-TO-NOISE RATIO (0dB Gain)**

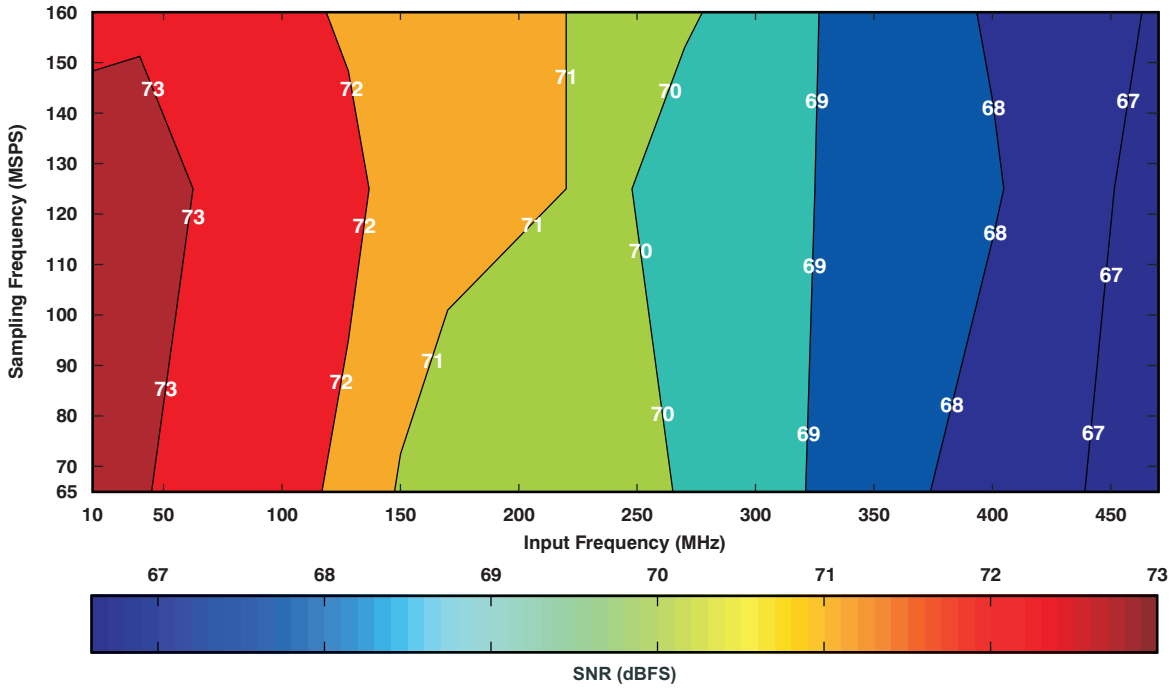



**Figure 149.**

**ADS414x SIGNAL-TO-NOISE RATIO (6dB Gain)**

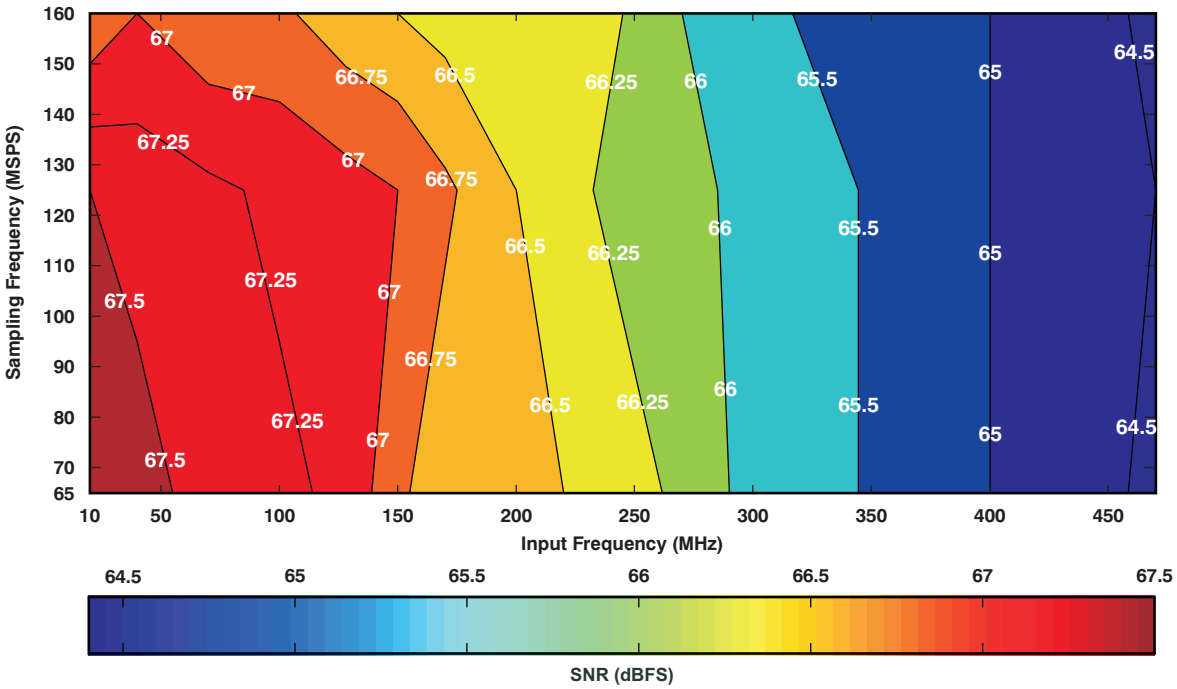



**Figure 150.**

## TYPICAL CHARACTERISTICS: Contour (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5$V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

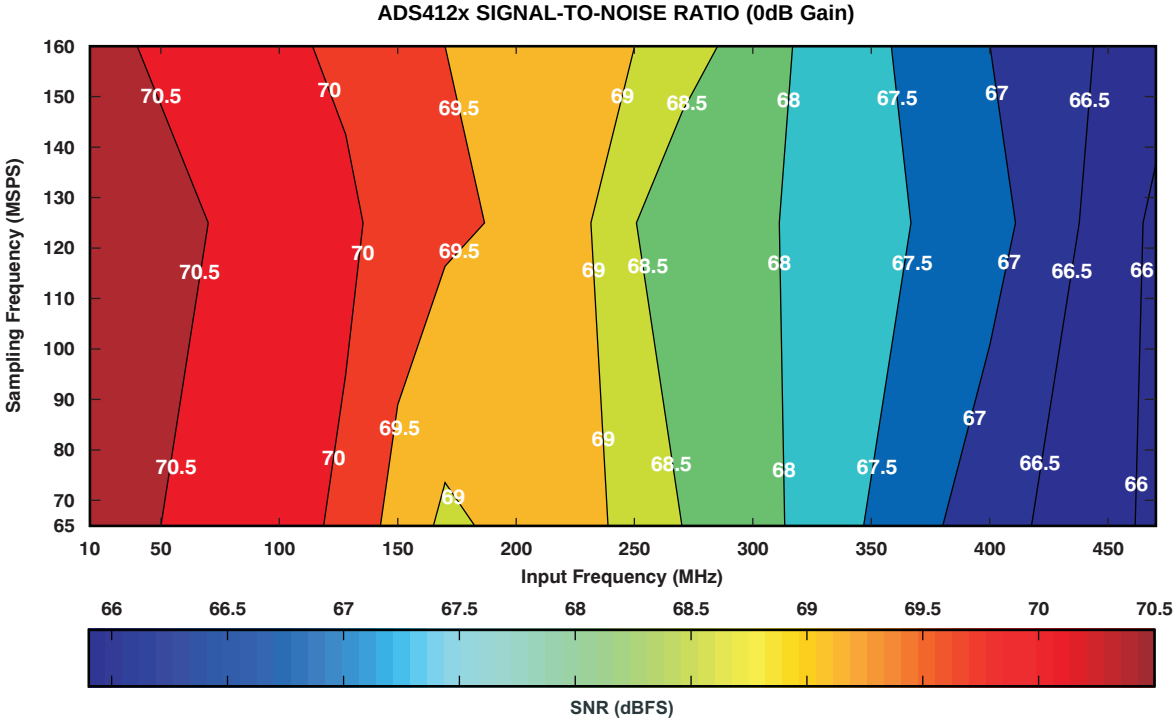



Figure 151.

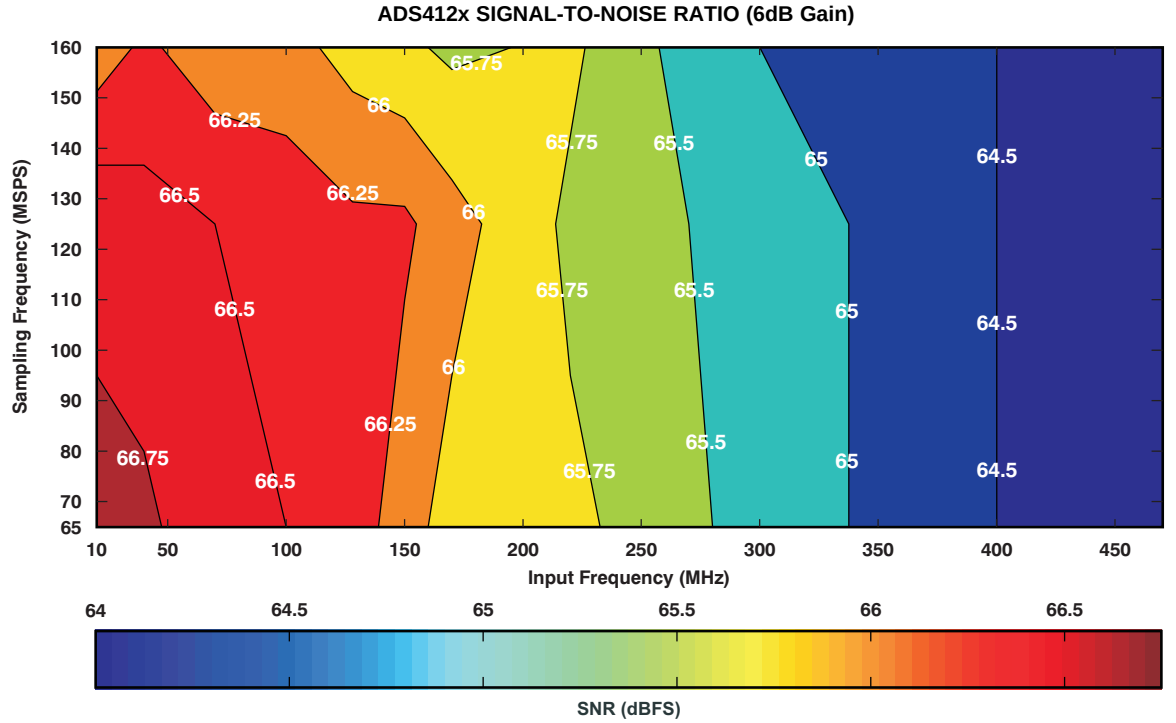



Figure 152.

# APPLICATION INFORMATION

## THEORY OF OPERATION

The ADS422x/424x belong to TI's ultralow-power family of dual-channel 12-bit and 14-bit analog-to-digital converters (ADCs). At every rising edge of the input clock, the analog input signal of each channel is simultaneously sampled. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled/held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference between the stage input and the quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and digitally processed to create the final code after a data latency of 16 clock cycles. The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary twos complement format. The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to approximately 400MHz (with $2V_{PP}$ amplitude) or approximately 600MHz (with $1V_{PP}$ amplitude).

## ANALOG INPUT

The analog input consists of a switched-capacitor based, differential sample-and-hold (S/H) architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95V, available on the VCM pin. For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between VCM + 0.5V and VCM – 0.5V, resulting in a $2V_{PP}$ differential input swing. The input sampling circuit has a high 3dB bandwidth that extends up to 550MHz (measured from the input pins to the sampled voltage). Figure 153 shows an equivalent circuit for the analog input.

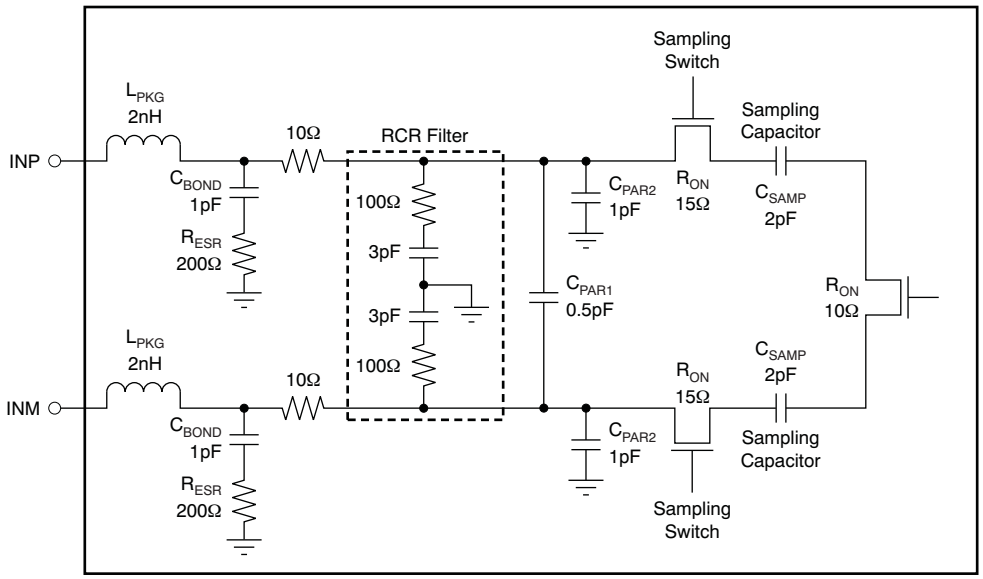



**Figure 153. Analog Input Equivalent Circuit**

### Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This operation improves the common-mode noise immunity and even-order harmonic rejection. A 5Ω to 15Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics.

SFDR performance can be limited as a result of several reasons, including the effects of sampling glitches; nonlinearity of the sampling circuit; and nonlinearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate, and input amplitude, one of these factors plays a dominant part in limiting performance. At very high input frequencies (greater than approximately 300MHz), SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, glitches could limit performance, primarily at low input frequencies (up to approximately 200MHz). It is also necessary to present low impedance (less than 50Ω) for the common-mode switching currents. This configuration can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cutoff frequency (smaller C), bandwidth support is maximized. However, the sampling glitches now must be supplied by the external drive circuit. This tradeoff has limitations as a result of the presence of the package bond-wire inductance.

In the ADS422x/424x, the R-C component values have been optimized while supporting high input bandwidth (up to 550MHz). However, in applications with input frequencies up to 200MHz to 300MHz, the filtering of the glitches can be improved further using an external R-C-R filter; see Figure 156 and Figure 157.

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. Furthermore, the ADC input impedance must be considered. Figure 154 and Figure 155 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) looking into the ADC input pins.

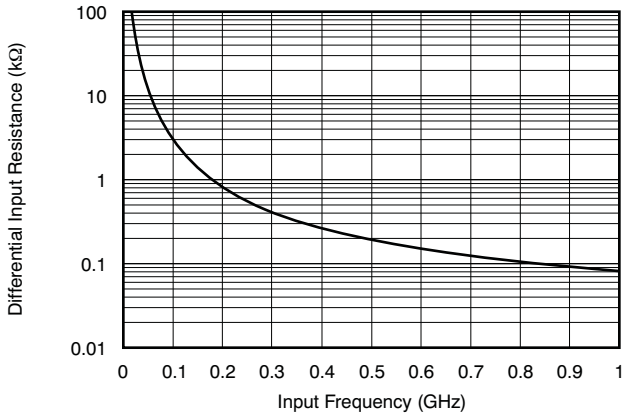



**Figure 154. ADC Analog Input Resistance ($R_{IN}$) Across Frequency**

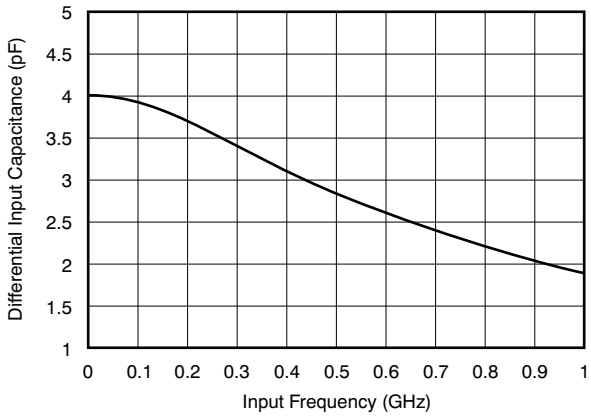



**Figure 155. ADC Analog Input Capacitance ($C_{IN}$) Across Frequency**

### Driving Circuit

Two example driving circuit configurations are shown in Figure 156 and Figure 157—one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies. Note that both of the drive circuits have been terminated by 50Ω near the ADC side. The termination is accomplished by a 25Ω resistor from each input to the 1.5V common-mode (VCM) from the device. This architecture allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch; good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 156, Figure 157, and Figure 158. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50Ω (in the case of 50Ω source impedance).

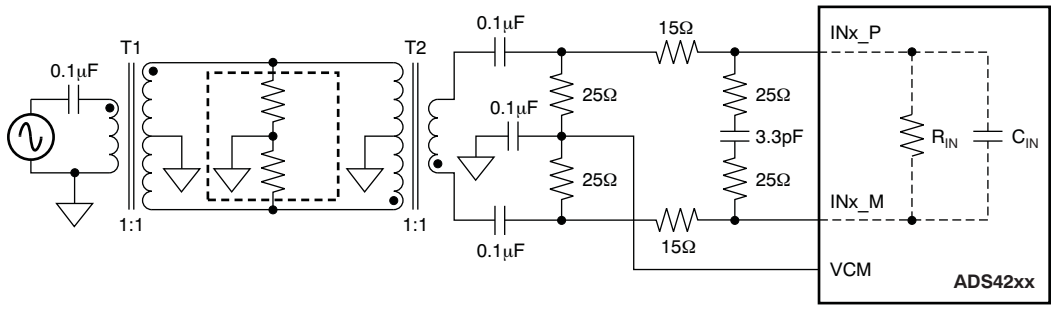



**Figure 156. Drive Circuit with Low Bandwidth (for Low Input Frequencies Less Than 150MHz)**

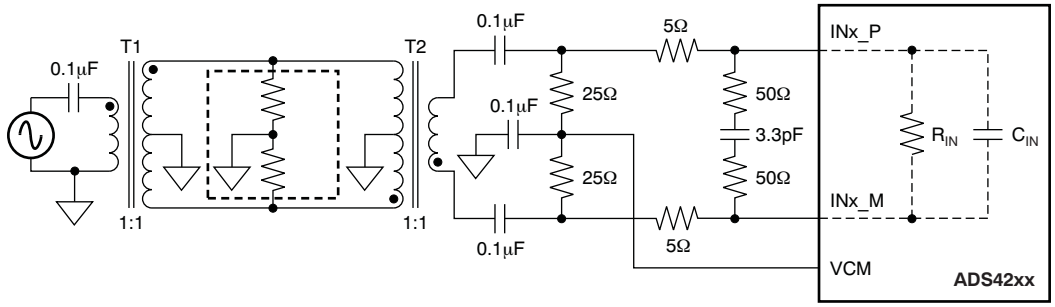



**Figure 157. Drive Circuit with High Bandwidth (for High Input Frequencies Greater Than 150MHz and Less Than 270MHz)**

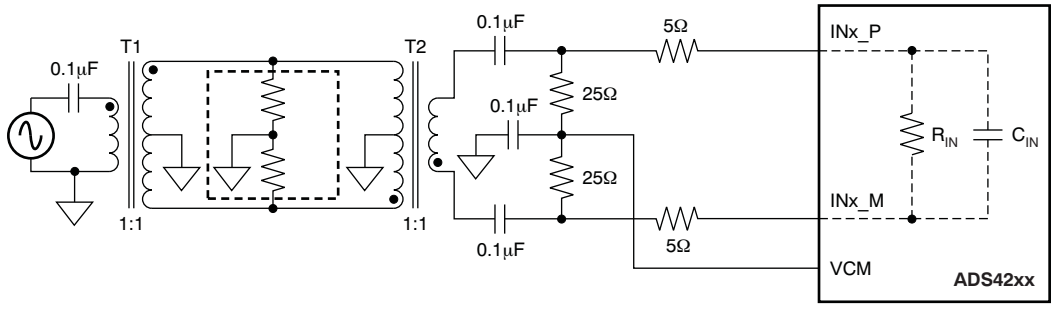



**Figure 158. Drive Circuit with Very High Bandwidth (Greater than 270MHz)**

All of these examples show 1:1 transformers being used with a 50Ω source. As explained in the *Drive Circuit Requirements* section, this configuration helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance is 200Ω. The higher source impedance is unable to absorb the sampling glitches effectively and can lead to degradation in performance (compared to using 1:1 transformers).

In almost all cases, either a band-pass or low-pass filter is required to obtain the desired dynamic performance, as shown in Figure 159. Such filters present low source impedance at the high frequencies corresponding to the sampling glitch and help avoid the performance loss with the high source impedance.

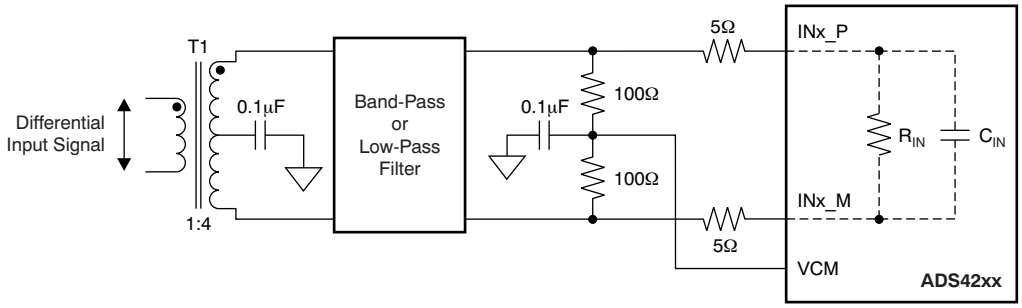



**Figure 159. Drive Circuit with a 1:4 Transformer**

## CLOCK INPUT

The ADS422x/424x clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources are shown in Figure 160, Figure 161 and Figure 162. The internal clock buffer is shown in Figure 163.

(1) $R_T$ = termination resister, if necessary.

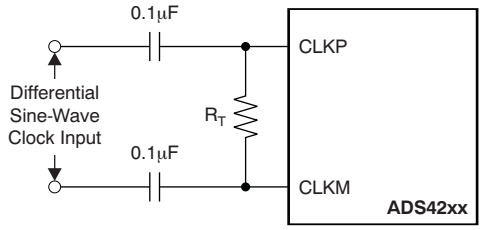



**Figure 160. Differential Sine-Wave Clock Driving Circuit**

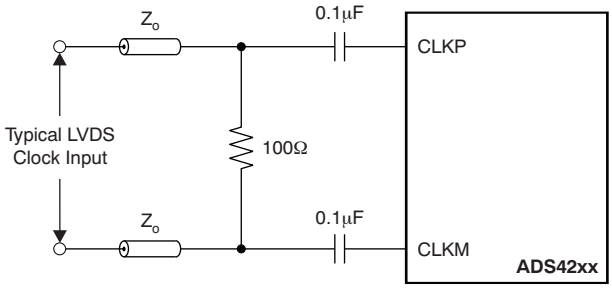



**Figure 161. LVDS Clock Driving Circuit**

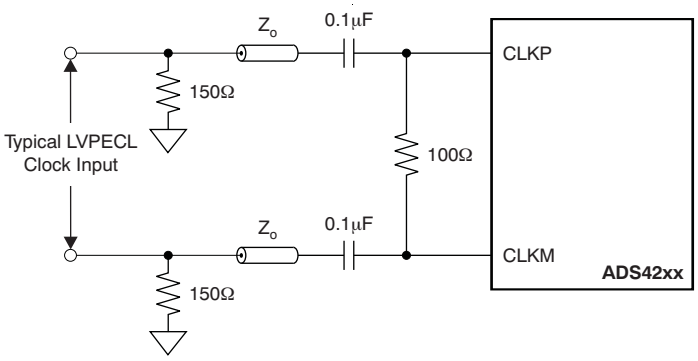
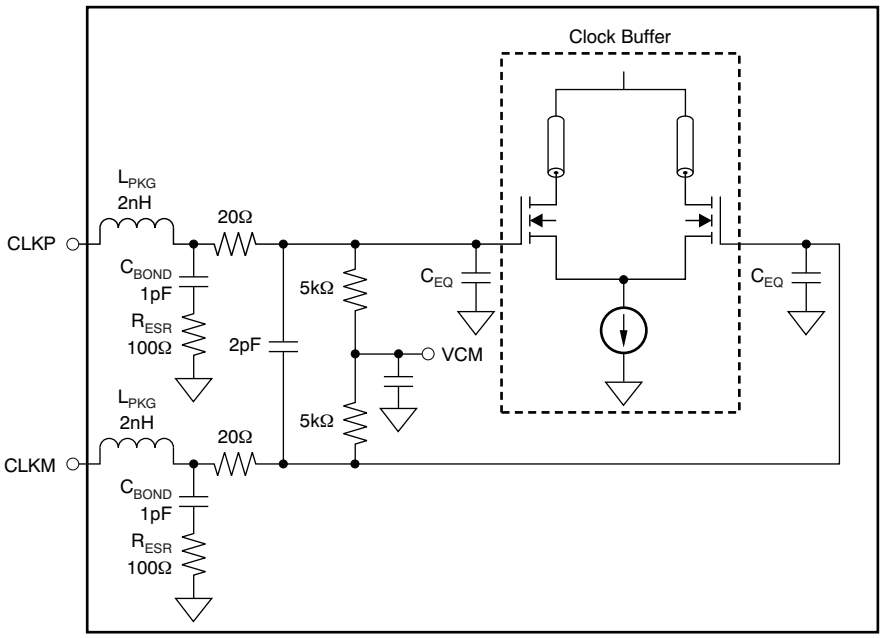



**Figure 162. LVPECL Clock Driving Circuit**




NOTE: $C_{EQ}$ is 1pF to 3pF and is the equivalent input capacitance of the clock buffer.

**Figure 163. Internal Clock Buffer**

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1µF capacitor, as shown in Figure 164. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

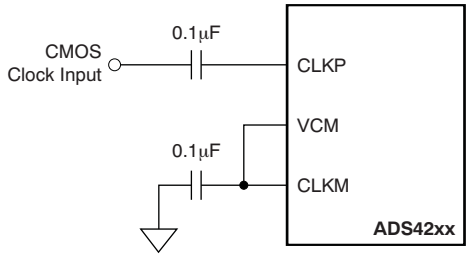



**Figure 164. Single-Ended Clock Driving Circuit**

## DIGITAL FUNCTIONS

The device has several useful digital functions (such as test patterns, gain, and offset correction). These functions require extra clock cycles for operation and increase the overall latency and power of the device. These digital functions are disabled by default after reset and the raw ADC output is routed to the output data pins with a latency of 16 clock cycles. Figure 165 shows more details of the processing after the ADC. In order to use any of the digital functions, the EN DIGITAL bit must be set to '1'. After this, the respective register bits must be programmed as described in the following sections and in the Serial Register Map section.

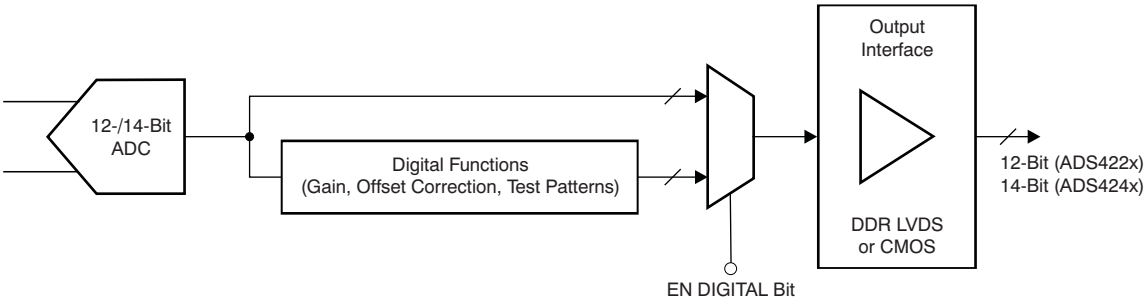



**Figure 165. Digital Processing Block**

## GAIN FOR SFDR/SNR TRADE-OFF

The ADS422x/424x include gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0dB to 6dB (in 0.5dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 11.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5dB and 1dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0dB.

**Table 11. Full-Scale Range Across Gains**

| GAIN (dB) | TYPE | FULL-SCALE ($V_{PP}$) |
|---|---|---|
| 0 | Default after reset | 2 |
| 1 | Fine, programmable | 1.78 |
| 2 | Fine, programmable | 1.59 |
| 3 | Fine, programmable | 1.42 |
| 4 | Fine, programmable | 1.26 |
| 5 | Fine, programmable | 1.12 |
| 6 | Fine, programmable | 1 |

## OFFSET CORRECTION

The ADS422x/424x have an internal offset corretion algorithm that estimates and corrects dc offset up to ±10mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 12.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 0. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

**Table 12. Time Constant of Offset Correction Algorithm**

| OFFSET CORR TIME CONSTANT | TIME CONSTANT, $TC_{CLK}$ (Number of Clock Cycles) | TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (ms)(1) |
|---|---|---|
| 0000 | 1M | 7 |
| 0001 | 2M | 13 |
| 0010 | 4M | 26 |
| 0011 | 8M | 52 |
| 0100 | 16M | 105 |
| 0101 | 32M | 210 |
| 0110 | 64M | 419 |
| 0111 | 128M | 839 |
| 1000 | 256M | 1678 |
| 1001 | 512M | 3355 |
| 1010 | 1G | 6711 |
| 1011 | 2G | 13422 |
| 1100 | Reserved | — |
| 1101 | Reserved | — |
| 1110 | Reserved | — |
| 1111 | Reserved | — |

(1) Sampling frequency, $f_S$ = 160MSPS.

## POWER-DOWN

The ADS422x/424x have two power-down modes: global power-down and channel standby. These modes can be set using either the serial register bits or using the control pins CTRL1 to CTRL3 (as shown in Table 13).

**Table 13. Power-Down Settings**

| CTRL1 | CTRL2 | CTRL3 | DESCRIPTION |
|---|---|---|---|
| Low | Low | Low | Default |
| Low | Low | High | Not available |
| Low | High | Low | Not available |
| Low | High | High | Not available |
| High | Low | Low | Global power-down |
| High | Low | High | Channel A powered down, channel B is active |
| High | High | Low | Not available |
| High | High | High | MUX mode of operation, channel A and B data is multiplexed and output on DB[10:0] pins |

### Global Power-Down

In this mode, the entire chip (including ADCs, internal reference, and output buffers) are powered down, resulting in reduced total power dissipation of approximately 20mW when the CTRL pins are used and 3mW when the PDN GLOBAL serial register bit is used. The output buffers are in high-impedance state. The wake-up time from global power-down to data becoming valid in normal mode is typically 100µs.

### Channel Standby

In this mode, each ADC channel can be powered down. The internal references are active, resulting in a quick wake-up time of 50µs. The total power dissipation in standby is approximately 200mW at 160MSPS.

### Input Clock Stop

In addition to the previous modes, the converter enters a low-power mode when the input clock frequency falls below 1MSPS. The power dissipation is approximately 160mW.

## DIGITAL OUTPUT INFORMATION

The ADS422x/424x provide 12-bit/14-bit digital data for each channel and an output clock synchronized with the data.

### Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit or by setting the proper voltage on the SEN pin in parallel configuration mode.

### DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 166.

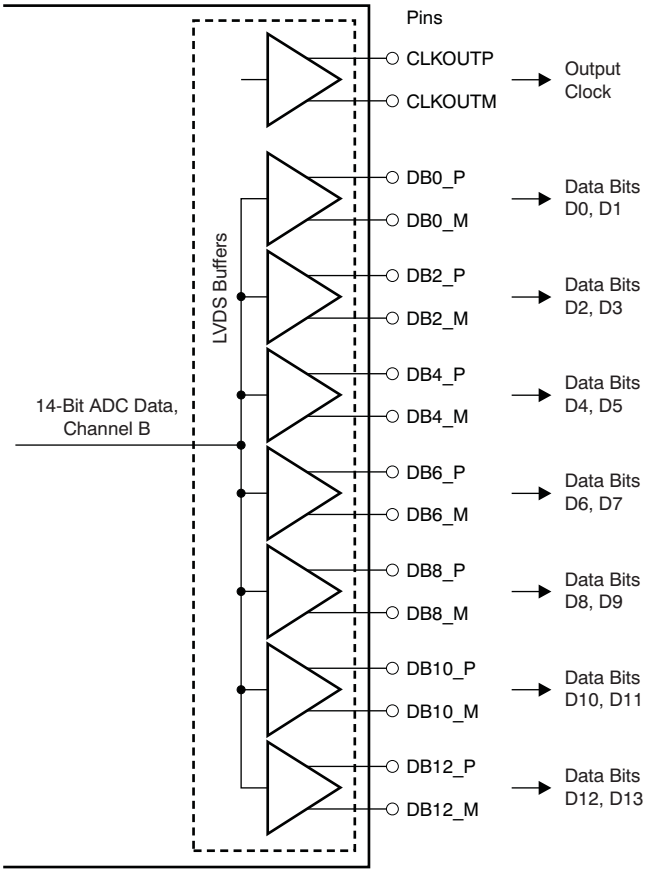



**Figure 166. LVDS Interface**

Even data bits (D0, D2, D4, etc.) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, etc.) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in Figure 167.

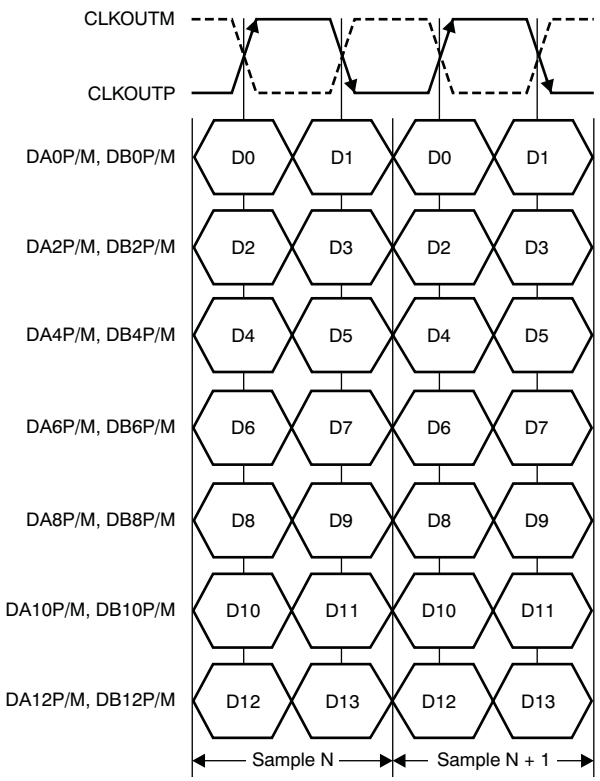
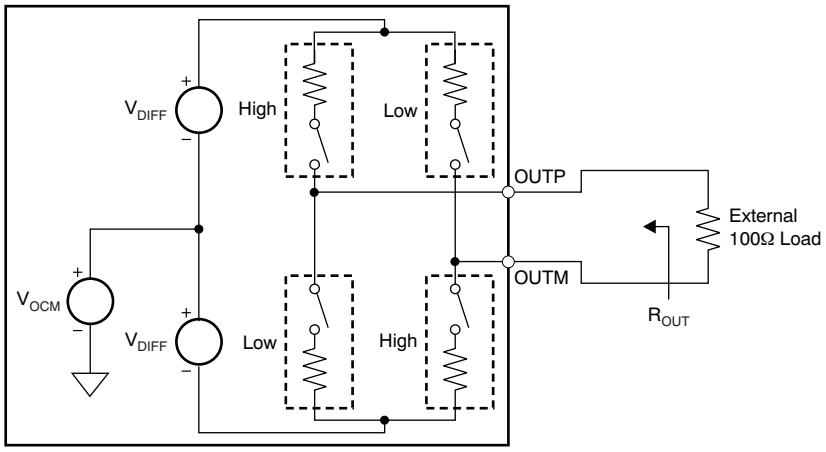



**Figure 167. DDR LVDS Interface Timing**

### LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 168. After reset, the buffer presents an output impedance of 100Ω to match with the external 100Ω termination.




NOTE: Default swing across 100Ω load is ±350mV. Use the LVDS SWING bits to change the swing.

**Figure 168. LVDS Buffer Equivalent Circuit**

The $V_{DIFF}$ voltage is nominally 350mV, resulting in an output swing of ±350mV with 100Ω external termination. The $V_{DIFF}$ voltage is programmable using the LVDS SWING register bits from ±125mV to ±570mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50Ω differential termination, as shown in Figure 169. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

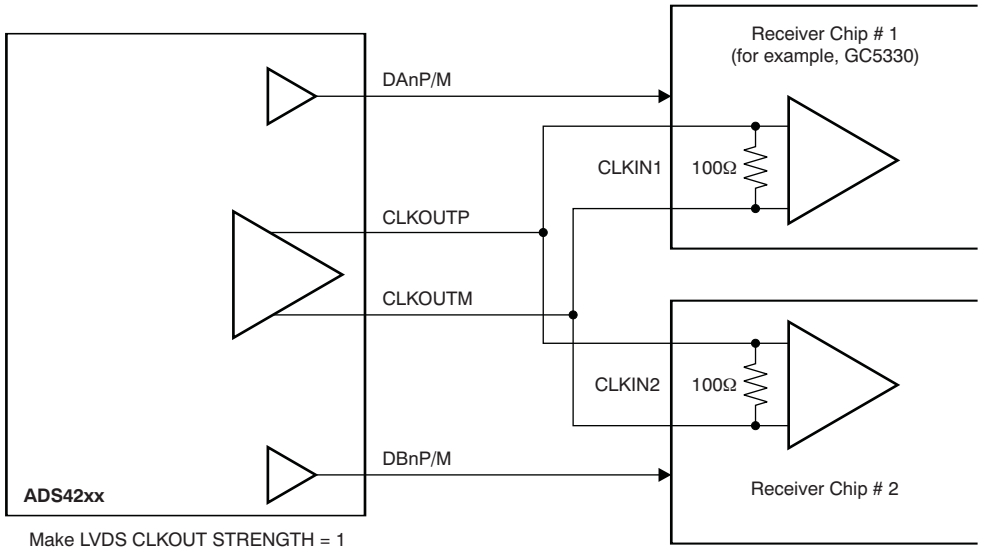



**Figure 169. LVDS Buffer Differential Termination**

### Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pins as CMOS voltage level, every clock cycle, as Figure 170 shows. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. It is recommended to minimize the load capacitance of the data and clock output pins by using short traces to the receiver. Furthermore, match the output data and clock traces to minimize the skew between them.

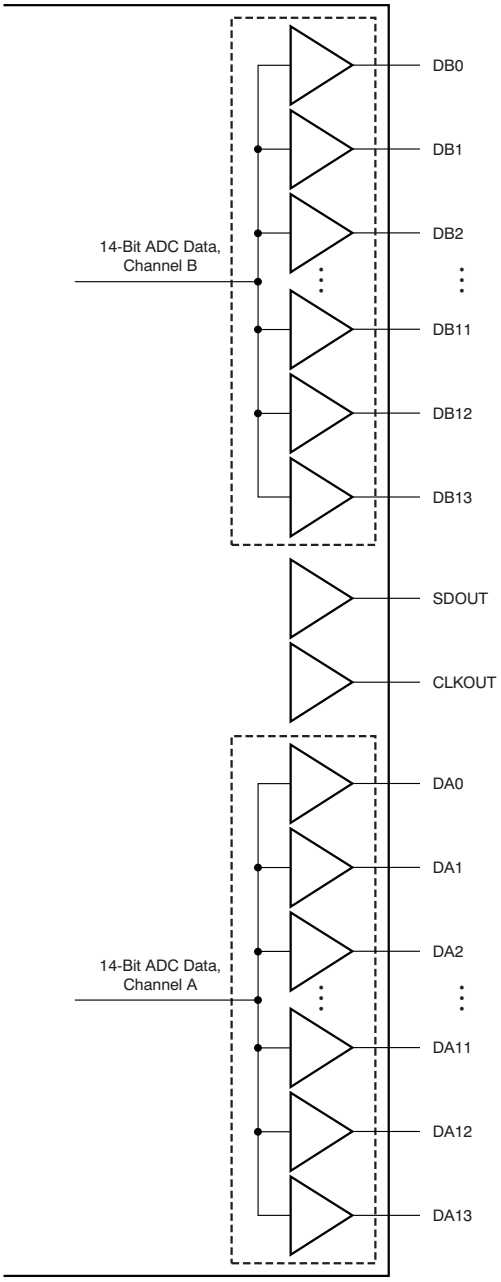



**Figure 170. CMOS Outputs**

### CMOS Interface Power Dissipation

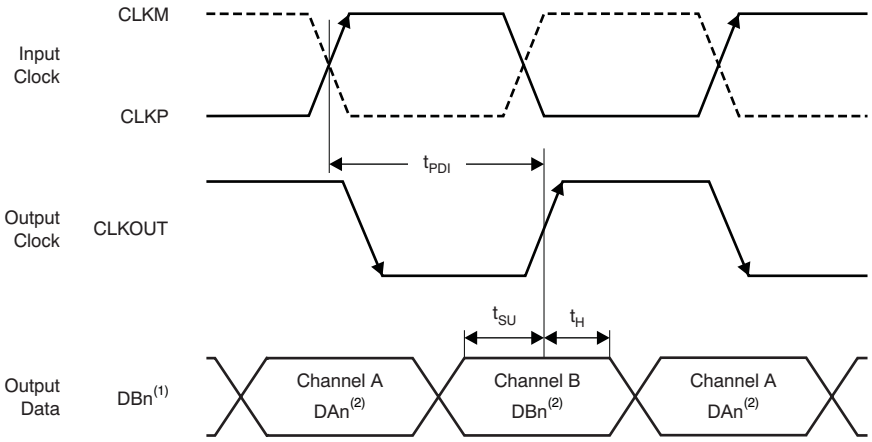
With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal. This relationship is shown by the formula:

Digital current as a result of CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$,

where $C_L$ = load capacitance, $N \times F_{AVG}$ = average number of output bits switching.

### Multiplexed Mode of Operation

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (DB[13:0] pins), as shown in Figure 171. The channel A output pins (DA[13:0]) are in 3-state. Because the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (less than 80MSPS). This mode can be enabled using the POWER-DOWN MODE register bits or using the CTRL[3:1] parallel pins.




(1) In multiplexed mode, both channels outputs come on the channel B output pins.

(2) Dn = bits D0, D1, D2, etc.

**Figure 171. Multiplexed Mode Timing Diagram**

### Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit or by controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is FFFh for the ADS422x and 3FFFh for the ADS424x in offset binary output format; the output code is 7FFh for the ADS422x and 1FFFh for the ADS424x in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 800h for the ADS422x and 2000h for the ADS424x in twos complement output format.

## DEFINITION OF SPECIFICATIONS

**Analog Bandwidth** – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

**Aperture Delay** – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

**Aperture Uncertainty (Jitter)** – The sample-to-sample variation in aperture delay.

**Clock Pulse Width/Duty Cycle** – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

**Maximum Conversion Rate** – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

**Minimum Conversion Rate** – The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL)** – An ideal ADC exhibits code transitions at analog input values spaced exactly 1LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

**Integral Nonlinearity (INL)** – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Gain Error** – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy ($E_{GREF}$) and error as a result of the channel ($E_{GCHAN}$). Both errors are specified independently as $E_{GREF}$ and $E_{GCHAN}$.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

**Offset Error** – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

**Temperature Drift** – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from $T_{MIN}$ to $T_{MAX}$. It is calculated by dividing the maximum deviation of the parameter across the $T_{MIN}$ to $T_{MAX}$ range by the difference $T_{MAX} – T_{MIN}$.

**Signal-to-Noise Ratio** – SNR is the ratio of the power of the fundamental ($P_S$) to the noise floor power ($P_N$), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**Signal-to-Noise and Distortion (SINAD)** – SINAD is the ratio of the power of the fundamental ($P_S$) to the power of all the other spectral components including noise ($P_N$) and distortion ($P_D$), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**Effective Number of Bits (ENOB)** – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{3}$$

**Total Harmonic Distortion (THD)** – THD is the ratio of the power of the fundamental ($P_S$) to the power of the first nine harmonics ($P_D$).

$$\text{THD} = 10\text{Log}^{10} \frac{P_S}{P_N} \tag{4}$$

THD is typically given in units of dBc (dB to carrier).

**Spurious-Free Dynamic Range (SFDR)** – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion** – IMD3 is the ratio of the power of the fundamental (at frequencies $f_1$ and $f_2$) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**DC Power-Supply Rejection Ratio (DC PSRR)** – DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

**AC Power-Supply Rejection Ratio (AC PSRR)** – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If $\Delta V_{SUP}$ is the change in supply voltage and $\Delta V_{OUT}$ is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \tag{5}$$

**Voltage Overload Recovery** – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

**Common-Mode Rejection Ratio (CMRR)** – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If $\Delta V_{CM\_IN}$ is the change in the common-mode voltage of the input pins and $\Delta V_{OUT}$ is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \tag{6}$$

**Crosstalk (only for multi-channel ADCs)** – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

## BOARD DESIGN CONSIDERATIONS

### Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS4226 Evaluation Module* (SLAU333) for details on layout and grounding.

### Supply Decoupling

Because the ADS422x/424x already include internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

### Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically connected internally to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271).

### Routing Analog Inputs

It is advisable to route differential analog input pairs (INP_x and INM_x) close to each other. To minimize the possibility of coupling from one channel to other, the analog input pairs of two channels should be routed perpendicular to each other; see the *ADS4226 Evaluation Module* (SLAU333) for reference routing.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/ Ball Finish | MSL Peak Temp [3] | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| ADS4222IRGCR | PREVIEW | VQFN | RGC | 64 | 2000 | TBD | Call TI | Call TI | |
| ADS4222IRGCT | PREVIEW | VQFN | RGC | 64 | 250 | TBD | Call TI | Call TI | |
| ADS4225IRGC25 | PREVIEW | VQFN | RGC | 64 | 25 | TBD | Call TI | Call TI | |
| ADS4225IRGCR | PREVIEW | VQFN | RGC | 64 | 2000 | TBD | Call TI | Call TI | |
| ADS4225IRGCT | PREVIEW | VQFN | RGC | 64 | 250 | TBD | Call TI | Call TI | |
| ADS4226IRGC25 | ACTIVE | VQFN | RGC | 64 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| ADS4226IRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| ADS4226IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| ADS4242IRGCR | PREVIEW | VQFN | RGC | 64 | 2000 | TBD | Call TI | Call TI | |
| ADS4242IRGCT | PREVIEW | VQFN | RGC | 64 | 250 | TBD | Call TI | Call TI | |
| ADS4245IRGC25 | PREVIEW | VQFN | RGC | 64 | 25 | TBD | Call TI | Call TI | |
| ADS4245IRGCR | PREVIEW | VQFN | RGC | 64 | 2000 | TBD | Call TI | Call TI | |
| ADS4245IRGCT | PREVIEW | VQFN | RGC | 64 | 250 | TBD | Call TI | Call TI | |
| ADS4246IRGC25 | PREVIEW | VQFN | RGC | 64 | 25 | TBD | Call TI | Call TI | |
| ADS4246IRGCR | PREVIEW | VQFN | RGC | 64 | 2000 | TBD | Call TI | Call TI | |
| ADS4246IRGCT | PREVIEW | VQFN | RGC | 64 | 250 | TBD | Call TI | Call TI | |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

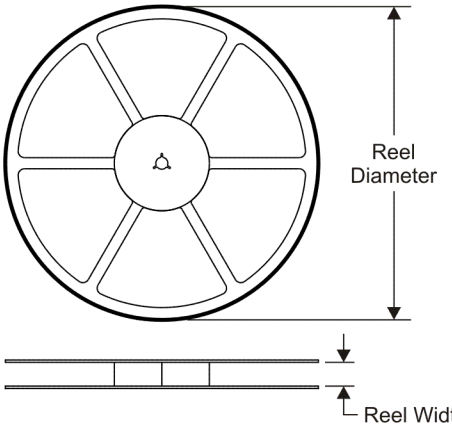
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

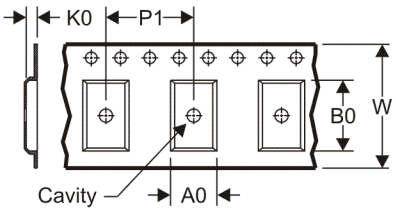
**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

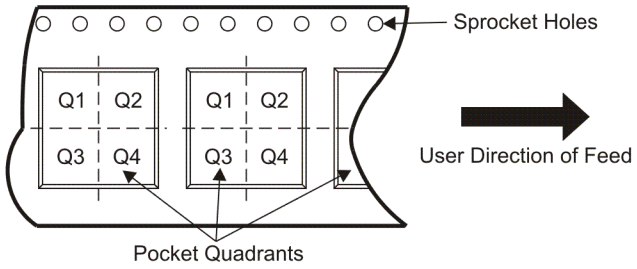



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

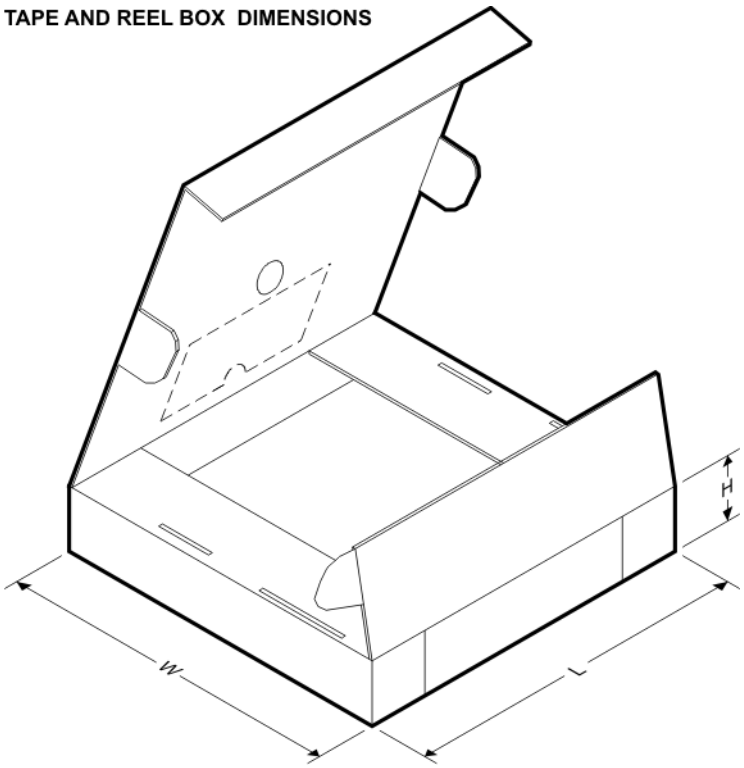
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS4226IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS4226IRGCT | VQFN | RGC | 64 | 250 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

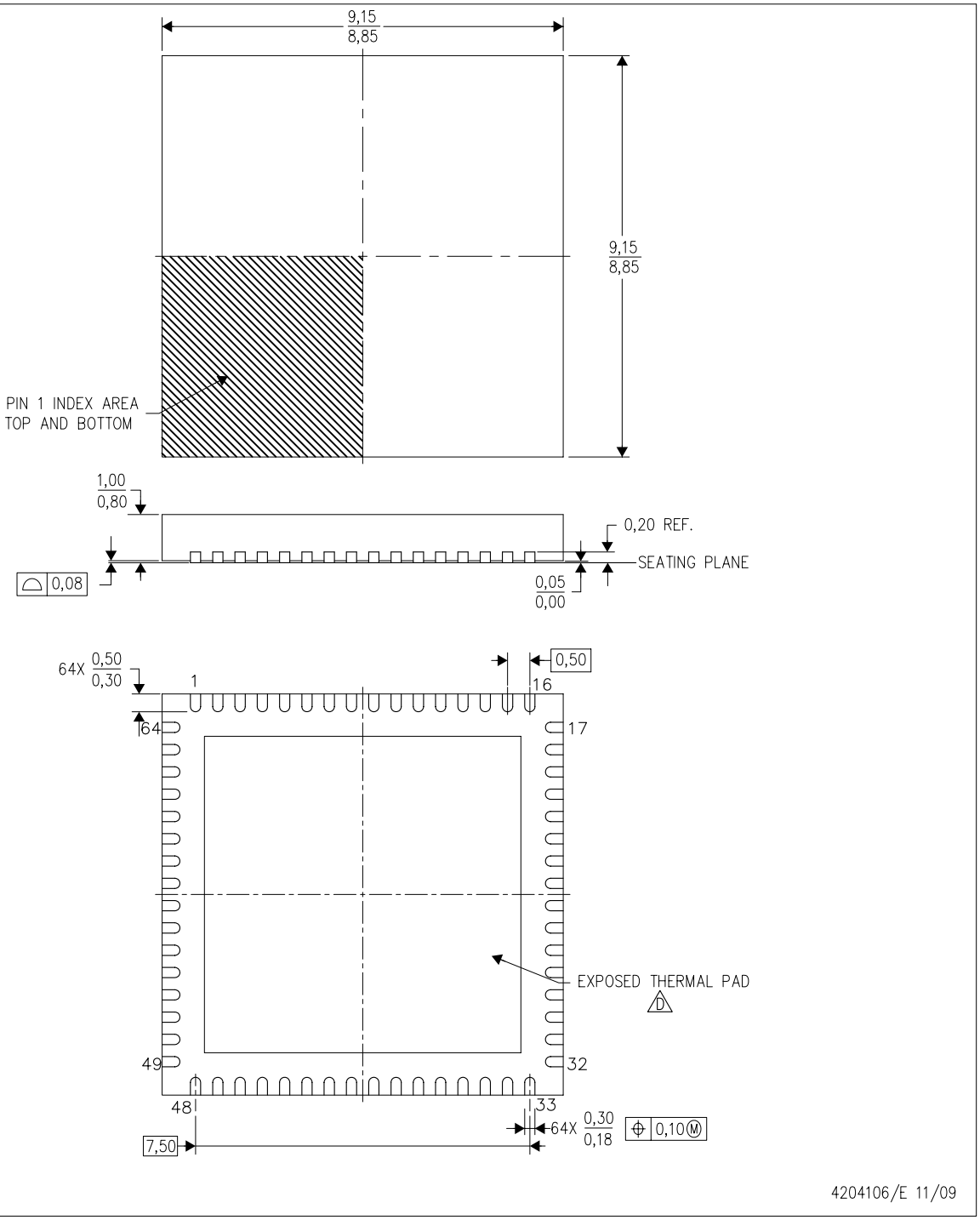
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS4226IRGCR | VQFN | RGC | 64 | 2000 | 333.2 | 345.9 | 28.6 |
| ADS4226IRGCT | VQFN | RGC | 64 | 250 | 333.2 | 345.9 | 28.6 |

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

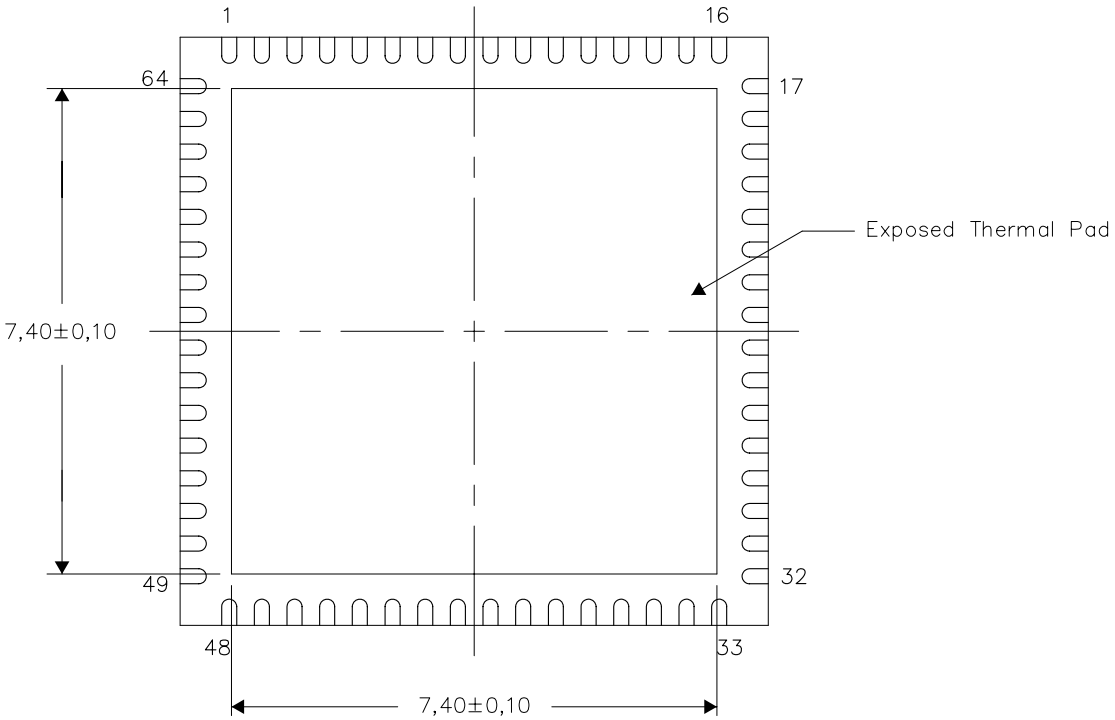
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



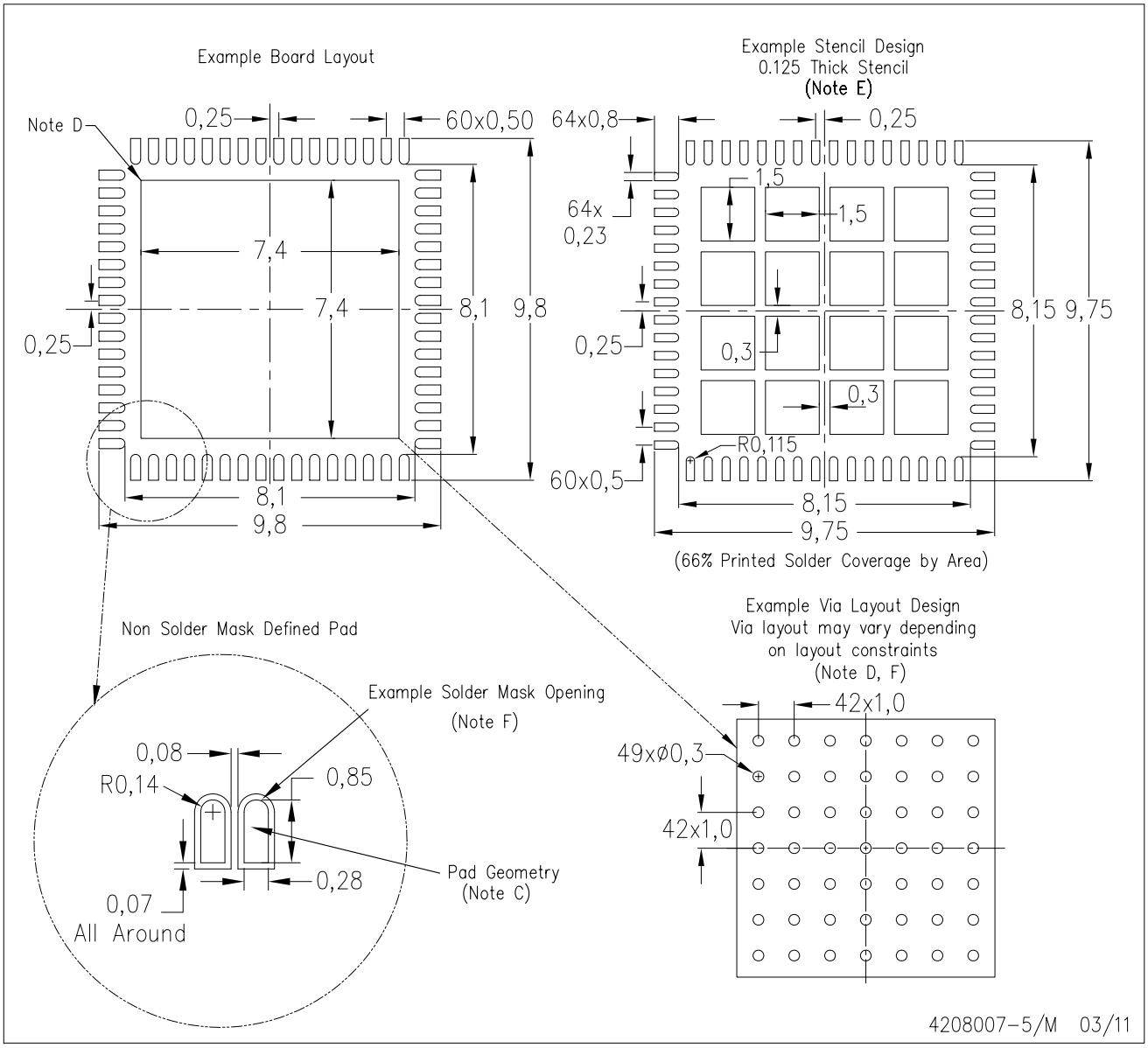

Bottom View

Exposed Thermal Pad Dimensions

4206192–4/N 02/11

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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