Digital Controller for Isolated Power Supply with PMBus Interface

Preliminary Technical Data

ADP1051

FEATURES

Versatile, digital voltage mode controller
High speed, input voltage feed-forward control
6 PWM logic outputs with 625ps resolution
Switching frequency 50 kHz to 625 kHz
Frequency synchronization master & slave
Multiple energy saving modes
Adaptive dead-time compensation for efficiency optimization
Low device power consumption - typical 100 mW
Direct Parallel operation
- **Accurate droop current share**
- **Pre-bias start-up**
- **Reverse current protection**
- **Conditional over-voltage protection**

Extensive fault detection and protections
Ultra compact package design 4*4mm 24-pin LFCSP
PMBus Compliant
Easy to use programming via Graphic User Interface (GUI)
High reliability EEPROM for programming & data storage
-40 °C ~ 125 °C operation temperature

APPLICATIONS

High density, Isolated DC/DC power supplies
- **Intermediate bus converters**
- **High availability parallel power systems**

Server, storage, industrial, networking, and communications infrastructure

GENERAL DESCRIPTION

The ADP1051 is an advanced digital controller with PMBus™ interface targeting high density, high efficiency DCDC power conversion. This controller implements voltage mode control with high speed, input line feed-forward for enhanced transient and improved noise performance. The ADP1051 has 6 programmable PWM outputs capable of controlling most high efficiency power supply topologies with added control of synchronous rectification. The device includes adaptive dead-time compensation to improve the efficiency over the load range and programmable light load mode operation combined with low device power consumption to reduce system standby power losses.

The ADP1051 implements several features to enable a robust system of parallel and redundant operation for customers that require high availability or parallel connection. The device includes master/slave synchronization, reverse current protection and pre-bias start-up, accurate current sharing between power supplies and conditional overvoltage techniques to identify and safely shutdown an erroneous power supply in parallel operation mode.

The ADP1051 is based on flexible state machine architecture and is register programmed using an intuitive, graphical-user interface. The easy–to-use interface reduces design cycle time and results in a robust, hardware coded system loaded into the built-in EEPROM. The small size 4*4 mm LFCSP package makes the ADP1051 ideal for ultra-compact, isolated DCDC power module or embedded designs.

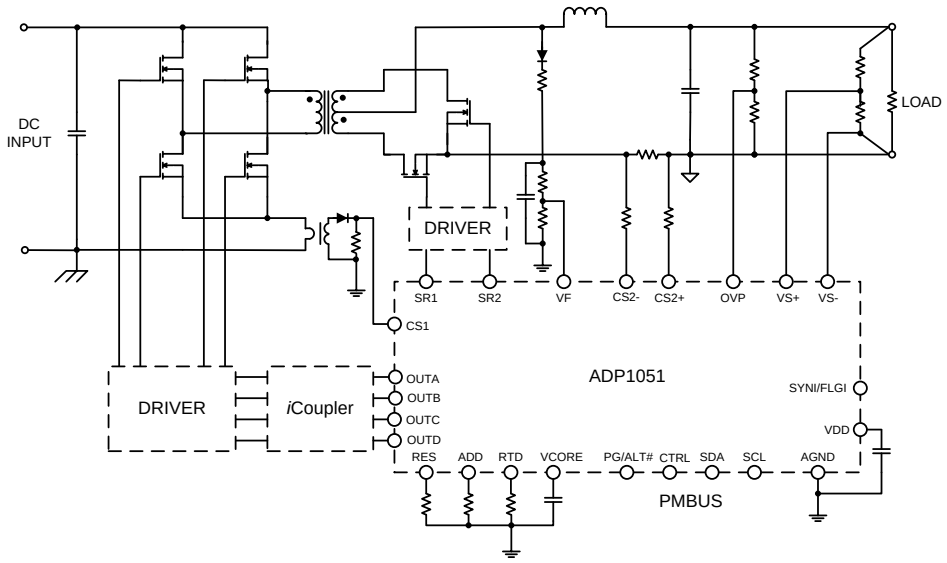

Figure 1. Typical Application Circuit

Rev. PrA

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SPECIFICATIONS

V_{DD} = 3.0V to 3.6 V, T_A = -40°C to +125°C, unless otherwise noted. FSR = Full Scale Range.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	V_{DD}		3.0	3.3	3.6	V
I_{DD}	I_{DD}	PWM pins unloaded				
		Normal operation (PSON is high or low)		29		mA
		Shut down (VDD below UVLO)		60	100	µA
		During EEPROM programming, 40 ms		I_{DD} + 6		mA
POWER-ON RESET						
Power-ON RESET		V_{DD} rising			3.0	V
UVLO Threshold		V_{DD} falling	2.750	2.850	2.975	V
UVLO Hysteresis				35		mV
OVLO Threshold			3.7	3.9	4.1	V
OVLO Debounce		When set to 2 µs		2		µs
		When set to 500 µs		500		µs
VCORE PIN						
Output Voltage		330 nF capacitor between VCORE to AGND	2.50	2.6	2.70	V
OSCILLATOR AND PLL						
PLL Frequency		Using RES = 10 kΩ (±0.1%)	190	200	210	MHz
DPWM Resolution				625		ps
OUTA, OUTB, OUTC, OUTD, SR1, SR2 PINS						
Output Low Voltage	V_{OL}	Sinking Current = 10 mA			0.4	V
Output High Voltage	V_{OH}	Sourcing Current = 10 mA	V_{DD}–0.4			V
Rise Time		C_{LOAD} = 50 pF		3.5		ns
Fall Time		C_{LOAD} = 50 pF		1.5		ns
VS VOLTAGE SENSE PIN						
Input Voltage Range		Differential voltage from VS+ to VS-	0	1	1.60	V
Input Voltage FSR				1.6		V
VS Accurate ADC						
Valid Input Voltage Range					1.6	V
ADC Clock Frequency				1.56		MHz
Register Update Rate				100		Hz
Resolution				12		Bits
Measurement Accuracy		Factory trimmed at 1.0 V				
		From 0% to 100% of Input Voltage Range	−10		+10	% FSR
			-160		+160	mV
		From 10% to 90% of Input Voltage Range	−2.5		+2.5	% FSR
			-40		+40	mV
		From 900 mV to 1.1 V	−1.0		+1.0	% FSR
			-16		+16	mV
Temperature Coeffient					65	ppm/°C
Common Mode Voltage Offset			-200		+200	mV
VS High Speed ADC						
Equivalent Sampling				f_{sw}		kHz

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Frequency Equivalent Resolution		At 390.6 kHz switching frequency		6		Bits
Dynamic Range		Regulation voltage TBD mV to TBD V		±25		mV
VS UVP		Based on VS Accurate ADC				
UVP accuracy				1	4	%
Comparator Update Speed				82		us
OVP PIN						
Usable Voltage Range			0.75		1.5	V
Threshold Accuracy				1	1.25	%
Propagation Delay (Latency)		Debounce time not included		58	110	ns
VF VOLTAGE SENSE PIN						
Input Voltage Range		Voltage from VF to AGND	0	1	1.60	V
Input Voltage FSR				1.6		V
General ADC						
Valid Input Voltage Range					1.6	V
ADC Clock Frequency				1.56		MHz
Register Update Rate				100		Hz
Resolution				12		Bits
Measurement Accuracy		From 10% to 90% of Input Voltage FSR	−3.5		+3.5	% FSR
			-56		+56	mV
		From 0% to 100% of Input Voltage FSR	−10		+10	% FSR
			-160		+160	mV
Feed Forward ADC						
Input Voltage Range			0.5	1	1.6	V
Resolution				11		Bits
Sampling Period				10		µs
CS1 CURRENT SENSE PIN						
Input Voltage Range	V_{IN}	Differential voltage from CS1 to AGND	0	1	1.60	V
Input Voltage FSR				1.6		V
CS1 ADC						
Valid Input Voltage Range					1.6	V
ADC Clock Frequency				1.56		MHz
Register Update Rate				100		Hz
Resolution				12		Bits
Measurement Accuracy		From 10% to 90% of Input Voltage Range	−3.5		+3.5	% FSR
			-56		+56	mV
		From 0% to 100% of Input Voltage Range	−10		+10	% FSR
			-160		+160	mV
CS1 Fast OCP						
Threshold Value 1			1.18	1.2	1.22	V
Threshold Value 2			0.22	0.25	0.28	V
Propagation Delay (Latency)		Debounce/blanking time not included		58	110	ns
CS2 CURRENT SENSE PINS						
Input Voltage Range		Differential voltage from CS2+ to CS2−	0		120	mV
Input Voltage FSR				120		mV
Common Mode Voltage		To achieve measurement accuracy	0.9	1.15	1.4	V
Current Sink (High Side)			1.81	1.9	1.99	mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Current Source (Low Side)		4.99 kΩ, 0.1% differential resistor	180	230	280	µA
Temperature Coefficient					70	ppm/°C
CS2 ADC						
Valid Input Voltage Range			0		120	mV
ADC Clock Frequency				1.56		MHz
Resolution				12		Bits
Measurement Accuracy			-1		+1	mV
Low Side Mode with User Trim						
		From 0 mV to 110 mV	−1.85		+2.1	% FSR
			−2.22		+2.52	mV
		From 110 mV to 120 mV	−6.1		+1.5	% FSR
			−6.36		+0.84	mV
High Side Mode with User Trim						
		From 0 mV to 110 mV	−1.6		+2.3	% FSR
			−1.92		+2.76	mV
		From 110 mV to 120 mV	−5.3		+0.7	% FSR
			−6.36		+0.84	mV
CS2 Accurate OCP						
Threshold Accuracy		Same as ADC accuracy				
Speed		When set to 7 bits averaging speed		82		us
		When set to 9 bits averaging speed		328		us
CS2 Reverse Current Comparator						
Threshold Accuracy		−3 mV setting	-8.5	−3.00	0	mV
		−6 mV setting	-12.0	−6	0	mV
		−9 mV setting	-15.5	−9	-2.9	mV
		−12 mV setting	-18.5	−12	-5.9	mV
		−15 mV setting	−22.0	−15	−8.0	mV
		−18 mV setting	−25.5	−18	−11.0	mV
		−21 mV setting	−28.5	−21	-14.0	mV
		−24 mV setting	−32	−24	−16.5	mV
Threshold Speed		Debounce = 40 ns		110	150	ns
RTD TEMPERATURE SENSE PIN						
Input Voltage		Voltage from RTD to AGND	0		1.6	V
Input Voltage FSR				1.6		V
Source Current		When set to 46 µA, factory default setting	44.3	46	47.3	µA
		When set to 40 µA	38.6	40	42	µA
		When set to 30 µA	28.8	30	31.7	µA
		When set to 20 µA	18.8	20	21.5	µA
		When set to 10 µA	9.1	10	11	µA
RTD ADC						
Valid Input Voltage Range					1.6	V
ADC Clock Frequency				1.56		MHz
Register Update Rate				100		Hz
Resolution				12		Bits
Measurement Accuracy		From 2% to 20% of valid input voltage	−0.3		+0.45	% FSR

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
			−4.8		+7.2	mV
		From 0% to 100% of valid input voltage	−2.6		+1.6	% FSR
OTP						
Threshold Accuracy		T = 85°C with 100 kΩ||16.5 kΩ	−0.9		+0.25	% FSR
			−14.4		+4	mV
		T = 100°C with 100 kΩ||16.5 kΩ	-0.5		+1.1	% FSR
			-8		+17.6	mV
Comparator Speed				10		ms
Temperature Readings According to Internal Linearization Scheme		Factory trimmed to 46 µA (set Register 0xFE2D to 0xE6); NTC R_0 = 100 kΩ, 1%; beta = 4250 1%; R_{EXT} = 16.5 kΩ 1%				
		T = 25°C to 100°C			7	°C
		T = 100°C to 125°C			5	°C
PG/ALT# (OPEN DRAIN) PIN						
Output Low Level	V_{OL}	Sinking Current = 10 mA			0.4	V
CTRL, SYNI/FLGI PINS						
Input Low Level	V_{IL}	Sinking Current = 10 mA			0.4	V
Input High Level	V_{IH}		V_{DD} − 0.8			V
SDA/SCL PINS		V_{DD} = 3.3 V				
Input Voltage Low	V_{IL}				0.8	V
Input Voltage High	V_{IH}		V_{DD} − 1.2			V
Output Voltage Low	V_{OL}				0.4	V
Leakage Current			−5		+5	µA
SERIAL BUS TIMING						
Clock Frequency				100	400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus Free Time	t_{BUF}		4.7			µs
Start Setup Time	$t_{SU;STA}$		4.7			µs
Start Hold Time	$t_{HD;STA}$		4			µs
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
SCL, SDA Rise Time	t_R				1000	ns
SCL, SDA Fall Time	t_F				300	ns
Data Setup Time	$t_{SU;DAT}$		250			ns
Data Hold Time	$t_{HD;DAT}$		300			ns
EEPROM						
EEPROM Update Time		Time from the updating command to EEPROM updating finish (T_J = 25°C)		40		ms
Reliability						
Endurance[1]		T_J = 85°C	10,000			Cycles
		T_J = 125°C	1,000			Cycles
Data Retention[2]		T_J = 85°C	20			Years
		T_J = 125°C	10			Years

[1] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.

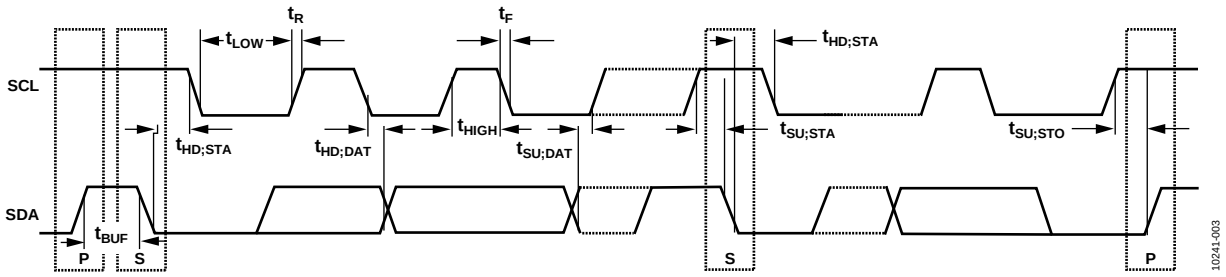

Figure 2. Serial Bus Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Rating

Parameter	Rating
Supply Voltage (Continuous) VDD	4.2 V
Digital Pins: OUTA, OUTB, OUTC, OUTD, SR1, SR2, PG/ALT#, SDA, SCL	−0.3 V to V_{DD} + 0.3 V
VS- to AGND	−0.3 V to +0.3 V
VS, VF, OVP, RTD, ADD, CS1, CS2+, CS2-	−0.3 V to V_{DD} + 0.3 V
SYNI/FLGI, CTRL	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150 °C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 to 30 secs)	240 °C
RoHS Compliant Assemblies (20 to 40 secs)	260 °C
ESD Charged Device Model	1.5 kV
ESD Human Body Model	5.0 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24 Lead LFCSP	36.26	1.51	°C/W

SOLDERING

It is important to follow the correct guidelines when laying out the PCB footprint for the ADP1051, and for soldering the part onto the PCB. For detailed information about these guidelines, see the AN-772 Application Note.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

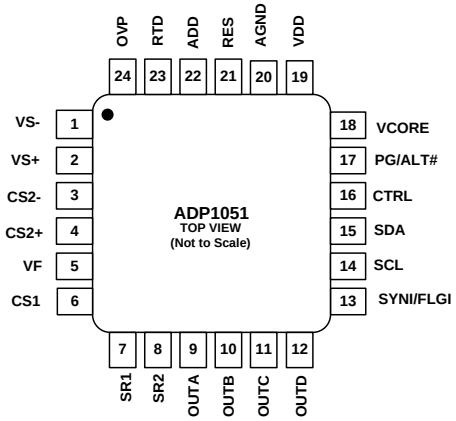

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS-	Inverting Voltage Sense Input. This is the connection for the ground line of the power rail. There should be a low ohmic connection to AGND. It is recommended that the resistor divider on this input have a tolerance specification of 0.5% or better to allow for trimming.
2	VS+	Noninverting Voltage Sense Input. This signal is referred to VS–. It is recommended that the resistor divider on this input have a tolerance specification of 0.5% or better to allow for trimming.
3	CS2-	Inverting Differential Current Sense Input. Nominal voltage at this pin should be 1.15 V for best operation. When using high-side current sensing in a 12 V application, place a 5.62 kΩ resistor between the sense resistor and this pin. When using low-side current sensing, place a 5 kΩ resistor between the sense resistor and this pin. When using high-side current sensing, use the formula R = ($V_{COMMONMODE}$ – 1.15)/1.9mA. A 0.1% resistor must be used to connect this circuit.
4	CS2+	Noninverting Differential Current Sense Input. Nominal voltage at this pin should be 1.15 V for best operation. When using high-side current sensing in a 12 V application, place a 5.62 kΩ resistor between the sense resistor and this pin. When using low-side current sensing, place a 5 kΩ resistor between the sense resistor and this pin. When using high-side current sensing, use the formula R = ($V_{COMMONMODE}$ – 1.15)/1.9 mA. A 0.1% resistor must be used to connect this circuit.
5	VF	Three optional functions can be implemented with this pin: feed forward, primary side input voltage sensing and input voltage lost detect. It is connected upstream of the output inductor through a resistor divider network. The nominal voltage at this pin should be 1V. This signal is referred to AGND
6	CS1	Primary Side Current Sense Input. This pin is connected to the primary side current sensing ADC and to the fast OCP comparator. This signal is referred to AGND. The resistors on this input must have a tolerance specification of 0.5% or better to allow for trimming.
7	SR1	PWM logic output drive. This pin can be disabled when not in use. This signal is referred to AGND.
8	SR2	PWM logic output drive. This pin can be disabled when not in use. This signal is referred to AGND.
9	OUTA	PWM logic output drive. This pin can be disabled when not in use. This signal is referred to AGND.
10	OUTB	PWM logic output drive. This pin can be disabled when not in use. This signal is referred to AGND.
11	OUTC	PWM logic output drive. This pin can be disabled when not in use. This signal is referred to AGND. This pin can also be programmed as a synchronization output.
12	OUTD	PWM logic output drive. This pin can be disabled when not in use. This signal is referred to AGND. This pin can also be programmed as a synchronization output.
13	SYNI/FLGI	Synchronization signal input. It also used as an external signal input to generate a flag condition.
14	SCL	I2C/PMBus Serial Clock Input and Output (Open Drain). This signal is referred to AGND.
15	SDA	I2C/PMBus Serial Data Input and Output (Open Drain). This signal is referred to AGND.
16	CTRL	PMBus CONTROL signal. It is recommended that a 1 nF capacitor be included from the CTRL pin to AGND for noise debounce and decoupling. This signal is referred to AGND.
17	PG/ALT#	Power Good Output (Open Drain). This signal is referred to AGND. This pin is also used PMBus ALERT# signal.
18	VCORE	Output of 2.6 V regulator. Connect a minimum 330 nF decoupling capacitor from this pin to the AGND as close as possible to the IC, minimizing the PCB trace length. It is recommended that the VCORE pin not be used as a reference or to generate other logic levels using resistive dividers.
19	VDD	Positive Supply voltage 3.0 V to 3.6 V referred to AGND. Connect a 2.2 µF decoupling capacitor from this pin to the AGND as close as possible to the IC, minimizing the PCB trace length.

Pin No.	Mnemonic	Description
20	AGND	IC Common Analog GND. The internal analog circuitry ground and digital circuitry ground is star connected to this pin through bonding wires.
21	RES	Resistor Input. This pin sets up the internal reference for internal PLL Frequency. Connect a 10 kΩ resistor (±0.1%) from RES to AGND. This signal is referred to AGND.
22	ADD	Address Select Input to program I2C/PMBus address. Connect a resistor from ADD to AGND. This signal is referred to AGND.
23	RTD	Thermistor Input. Place a thermistor 100 kΩ 1% beta = 4250 1% in parallel with a 16.5 kΩ (1%) resistor. This pin is referenced to AGND. Connect to AGND if not used.
24	OVP	Over Voltage Protection. This signal is used as redundant OVP protection. This signal is referred to VS-.
	EP	Exposed Pad. The ADP1051 has an exposed thermal pad on the underside of the package. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the PCB AGND plane.

APPLICATION CONFIGURATIONS

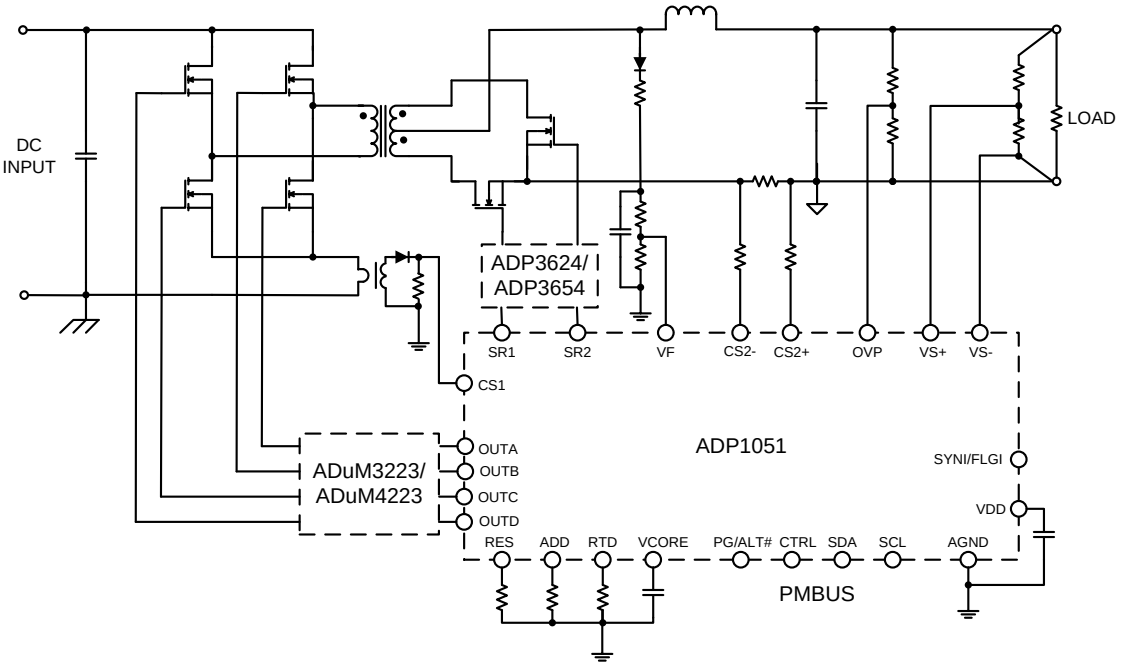

Figure 4. Full Bridge Converter

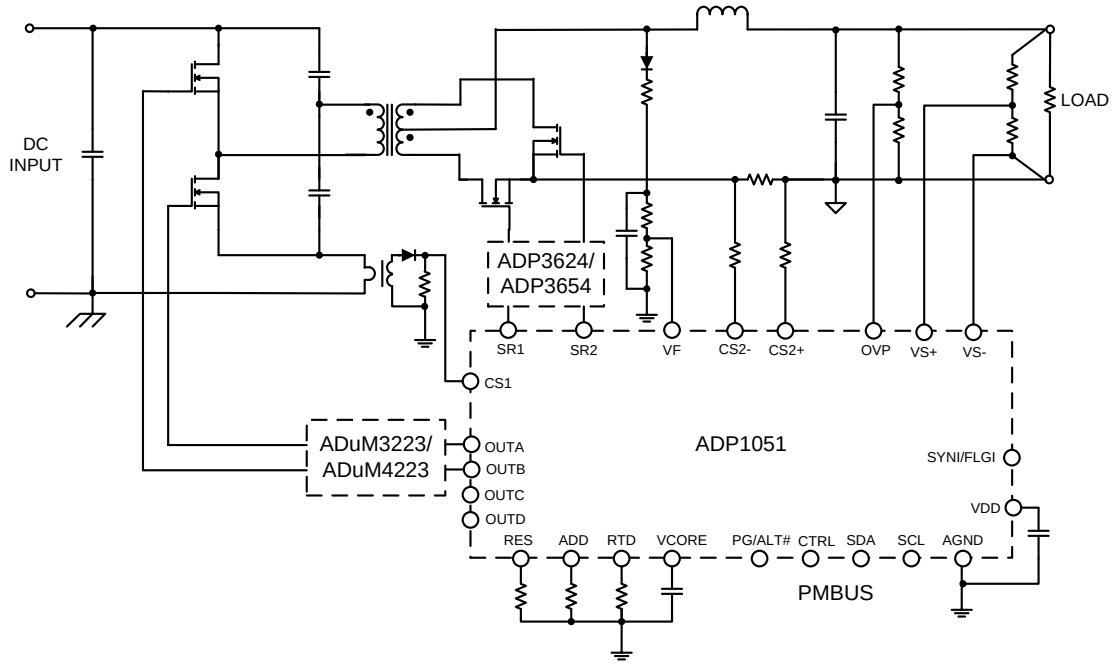

Figure 5. Half Bridge Converter

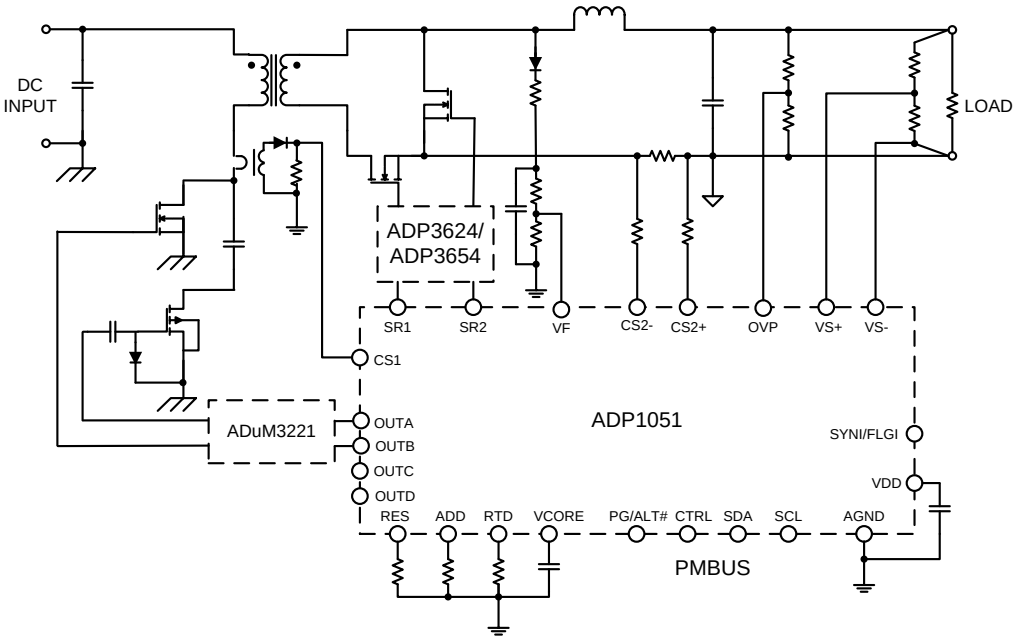

Figure 6. Active Clamp Forward Converter

TYPICAL PERFORMANCE CHARACTERISTICS

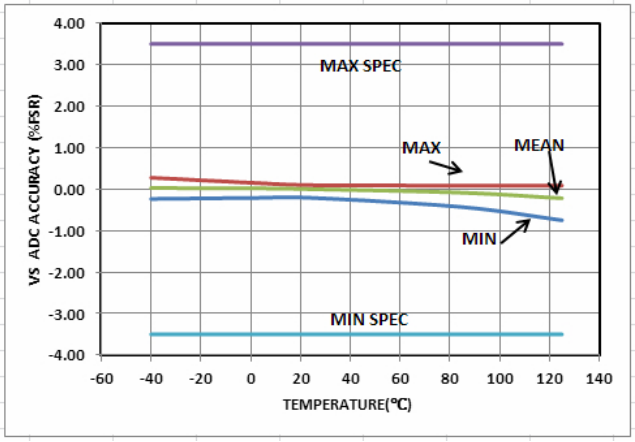

Figure 7. VS ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

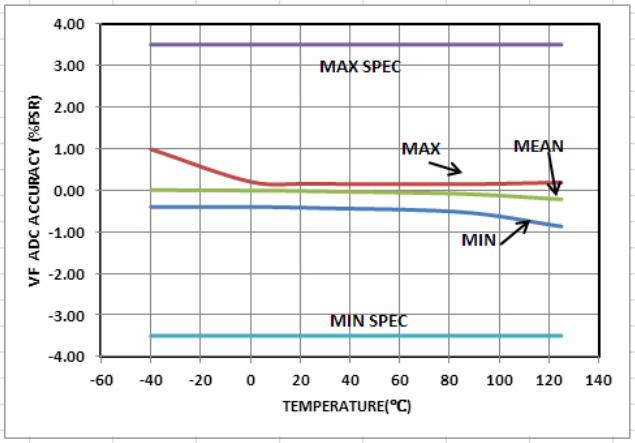

Figure 8. VF ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

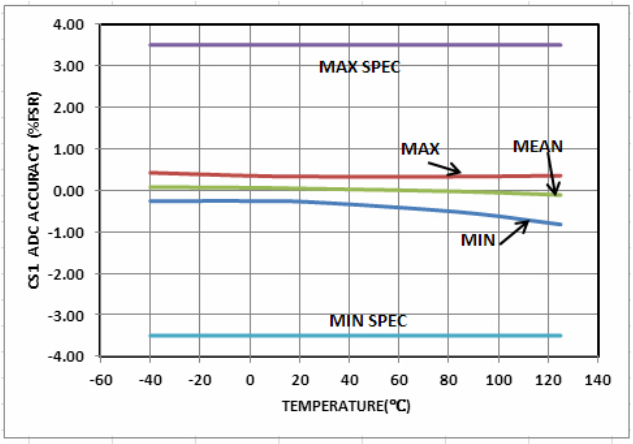

Figure 9. CS1 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

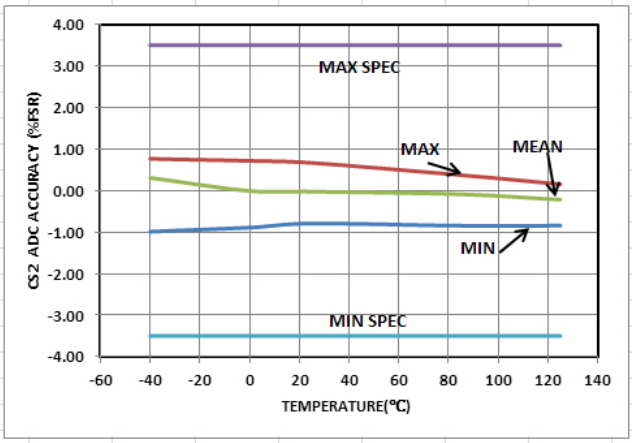

Figure 10. CS2 ADC Accuracy vs. Temperature (from 0 mV to 120 mV)

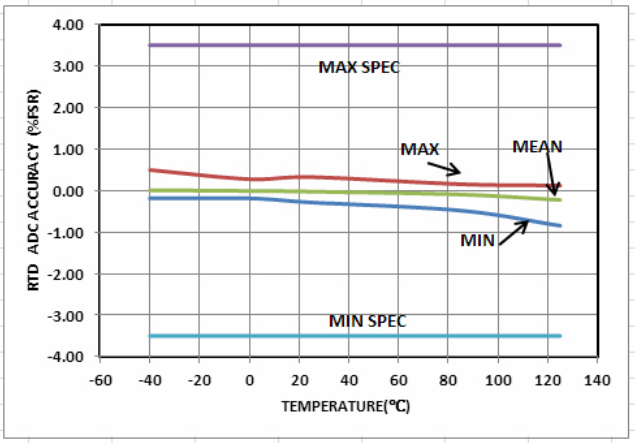

Figure 11. RTD ADC Accuracy vs. Temperature

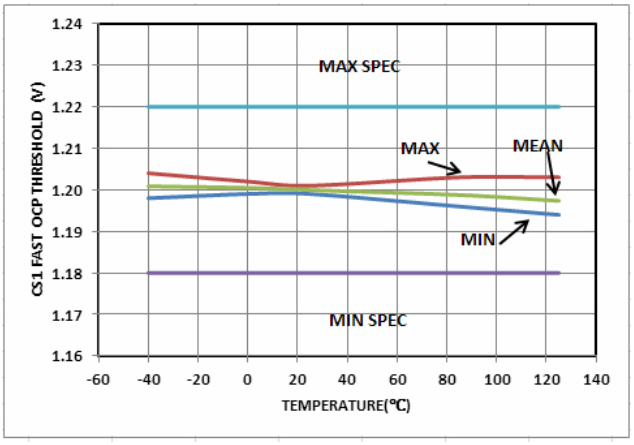

Figure 12. CS1 Fast OCP Threshold vs. Temperature

THEORY OF OPERATION

The ADP1051 is designed as a flexible, easy-to-use, digital power supply controller. The ADP1051 integrates the typical functions that are needed to control a power supply such as:

- Output voltage sense and feedback
- Voltage feed forward control
- Digital loop filter compensation
- PWM generation
- Current, voltage, and temperature sense
- Housekeeping and I²C/PMBus interface
- Calibration and trimming

The main function of controlling the output voltage is performed using the feedback ADCs, the digital loop filter, and the PWM block.

The feedback ADCs use a multipath approach. There is a combination of a high speed, low resolution (fast and coarse) ADC and a low speed, high resolution (slow and accurate) ADC. The ADC outputs combine to form a high speed and high resolution feedback path. Loop compensation is implemented using the digital filter. This PID (proportional, integral, derivative) filter is implemented in the digital domain, allowing easy programming of filter characteristics, which is of great value in customizing and debugging designs. The PWM block generates up to six programmable PWM outputs for control of FET drivers and synchronous rectification FET drivers. This programmability allows many traditional and specific switching topologies to be realized.

Conventional power supply housekeeping features, such as remote and local voltage sense and primary side current sense, are included. An extensive set of protections are offered, including overvoltage protection (OVP), over current protection (OCP), over temperature protection (OTP), under voltage protection (UVP), SR reverse current protection (RCP).

All these features are programmable through the I²C/PMBus interface. This interface is also used for calibrations. Other information, such as input current, output current, and fault flags, is also available through this digital bus interface.

The internal EEPROM can store all programmed values and allows standalone control without a microcontroller. A free, downloadable ADP1051 GUI is available that provides all the necessary software to program the ADP1051. To obtain the latest GUI software and a user guide, visit http://www.analog.com/digitalpower.

The ADP1051 operates from a single 3.3V power supply and is specified from -40°C to 125°C.

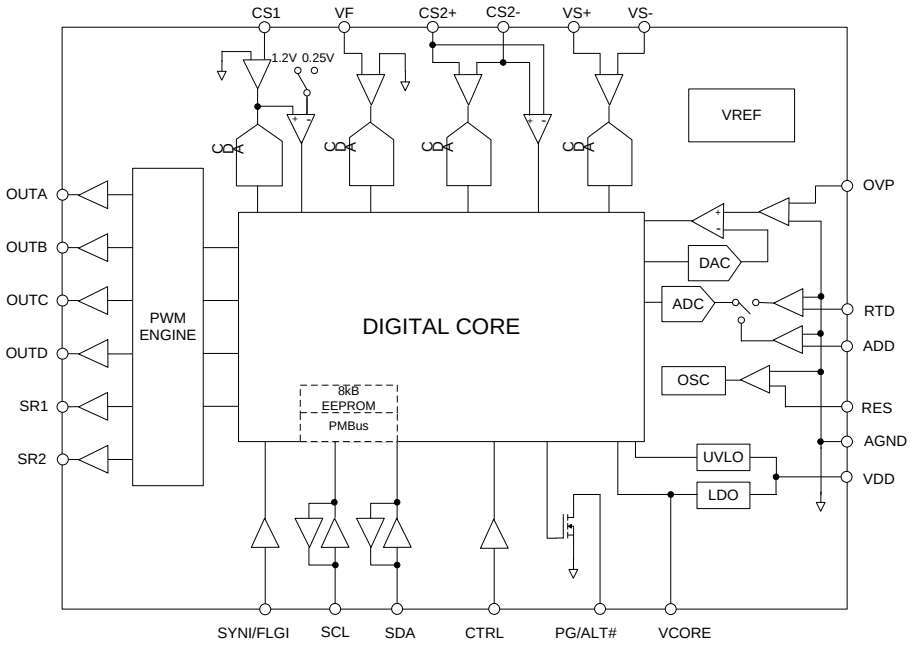

Figure 13. Functional Block Diagram

OUTLINE DIMENSIONS

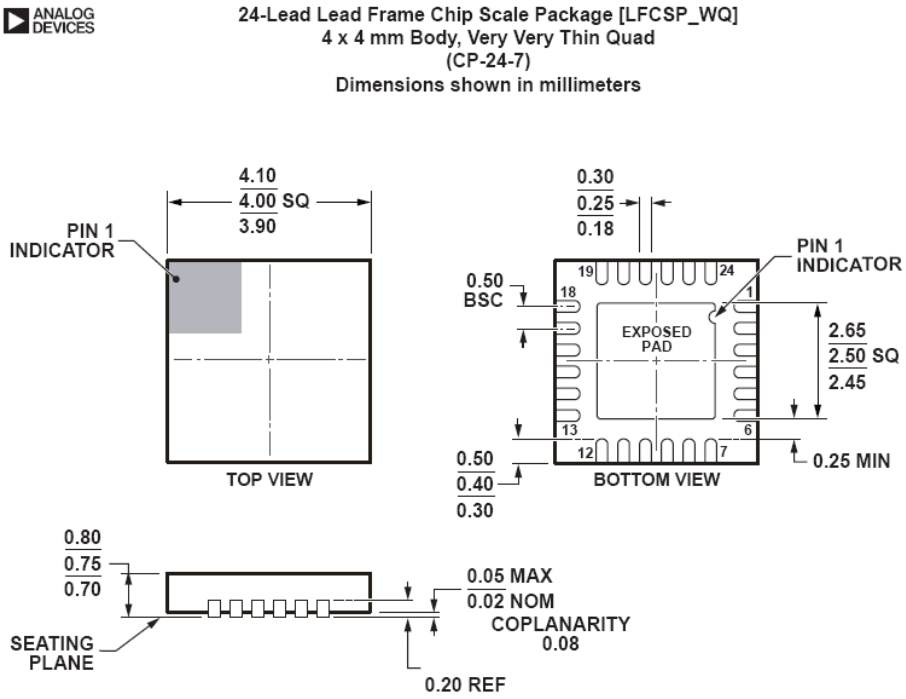

Figure 14. 24-Lead 4 x 4 mm Lead frame Chip-Scale Package [LFCSP]
Mechanical Package Dimensions

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1051ACPZ-RL	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-7
ADP1051ACPZ-R7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-7
ADP1051-240-EVALZ		ADP1051 240 W Evaluation Board	
ADP1051DC1-EVALZ		ADP1051 Daughter Card	
ADP-I2C-USB-Z		USB to I²C Adapter	

[1] Z = RoHS Compliant Part.

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