

## ADM690A/ADM692A/ADM802L/M/ADM805L/M

### FEATURES

**Precision Supply Voltage Monitor**  
 4.65 V ADM690A/ADM802L/ADM805L  
 4.40 V ADM692A/ADM802M/ADM805M  
**Reset Assertion Down to 1 V  $V_{CC}$**   
**Reset Timeout—200 ms**  
**Watchdog Timer—1.6 s**  
**100  $\mu$ A Quiescent Supply Current**  
**Automatic Battery Backup Power Switching**  
**Voltage Monitor for Power Fail**  
 $\pm 2\%$  Power Fail Accuracy on ADM802L/M  
**Space-Saving MicroSOIC Package (ADM690A)**

### APPLICATIONS

**Microprocessor Systems**  
**Computers**  
**Controllers**  
**Intelligent Instruments**

### GENERAL DESCRIPTION

The ADM690A/ADM692A/ADM802L/M/ADM805L/M family of supervisory circuits offers complete single chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include  $\mu$ P reset, backup battery switchover, watchdog timer, and power failure warning.

The ADM690A/ADM692A/ADM802L/M/ADM805L/M are available in 8-pin packages and provide:

1. Power-on reset output during power-up, power-down and brownout conditions. The  $\overline{\text{RESET}}$  output remains operational with  $V_{CC}$  as low as 1 V.
2. Battery backup switching for CMOS RAM, CMOS microprocessor or other low power devices.
3. A reset pulse if the optional watchdog timer has not been toggled within 1.6 seconds.
4. A 1.25 V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5 V.

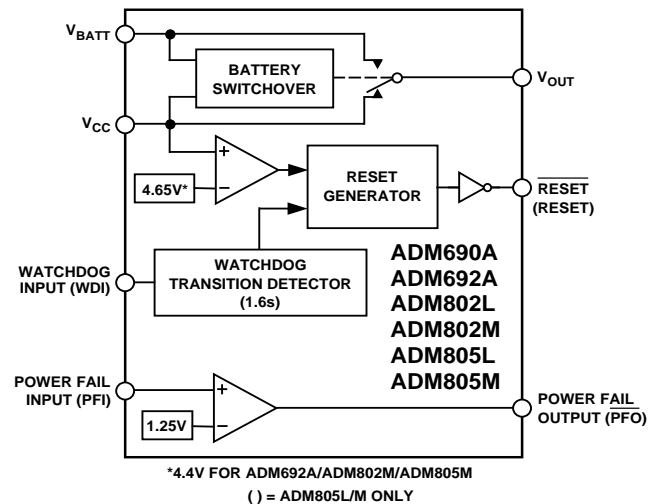
On the ADM690A/ADM802L/ADM805L the reset voltage threshold is 4.65 V. On the ADM692A/ADM802M/ADM805M, the reset voltage threshold is 4.40 V.

The ADM802L/ADM802M guarantee power fail accuracies to  $\pm 2\%$ .

### REV. 0

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### FUNCTIONAL BLOCK DIAGRAM



The ADM805L/M provides an active high reset output, RESET instead of  $\overline{\text{RESET}}$ .

The family of products is fabricated using an advanced epitaxial CMOS process combining low power consumption and high reliability.  $\overline{\text{RESET}}$  assertion is guaranteed with  $V_{CC}$  as low as 1 V.

They provide a pin-compatible upgrade for the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L.

All parts are available in 8-pin DIP and SOIC packages. The ADM690A is also available in a new space-saving microSOIC package.

# ADM690A/ADM692A/ADM802L/M/ADM805L/M—SPECIFICATIONS

( $V_{CC} = 4.75\text{ V to }5.5\text{ V}$  (ADM690A/ADM802L/ADM805L),  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , (ADM692A/ADM802M/ADM805M),  $V_{BATT} = +2.8\text{ V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
<b><math>V_{CC}/V_{BATT}</math> OPERATION<sup>1</sup></b>					
$V_{CC}$ Operating Voltage Range	1.0		5.5	V	
Supply Current (Excludes $I_{OUT}$ )		70	100	$\mu\text{A}$	
Supply Current in Battery Backup Mode		0.05	1.0	$\mu\text{A}$	$V_{CC} = 0\text{ V}$ , $V_{BATT} = 2.8\text{ V}$ $5.5\text{ V} > V_{CC} > V_{BATT} + 0.2\text{ V}$
Battery Standby Current (+ = Discharge, - = Charge)	-0.1		+0.02	$\mu\text{A}$	
$V_{OUT}$ Output Voltage	$V_{CC} - 0.02$	$V_{CC} - 0.01$		V	$I_{OUT} = 5\text{ mA}$
	$V_{CC} - 0.5$	$V_{CC} - 0.05$		V	$I_{OUT} = 50\text{ mA}$
		$V_{CC} - 0.02$		V	$I_{OUT} = 250\text{ mA}$
$V_{OUT}$ in Battery Backup Mode	$V_{BATT} - 0.05$	$V_{BATT} - 0.002$		V	$I_{OUT} = 250\text{ }\mu\text{A}$ , $V_{CC} < V_{BATT} - 0.2\text{ V}$
Battery Switchover Threshold		20		mV	Power Up
		-20		mV	Power Down
Battery Switchover Hysteresis		40		mV	
<b>RESET THRESHOLD</b>					
Reset Voltage Threshold					
ADM690A, ADM802L, ADM805L	4.5	4.65	4.75	V	
ADM692A, ADM802M, ADM805M	4.25	4.4	4.5	V	
ADM802L	4.55		4.7	V	$T_A = 25^\circ\text{C}$ , $V_{CC}$ Falling
ADM802M	4.30		4.45	V	$T_A = 25^\circ\text{C}$ , $V_{CC}$ Falling
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay	140	200	280	ms	
$\overline{\text{RESET}}$ Output Voltage	$V_{CC} - 1.5$			V	$I_{SOURCE} = 800\text{ }\mu\text{A}$ $I_{SINK} = 3.2\text{ mA}$
			0.4	V	
			0.3	V	$I_{SINK} = 100\text{ }\mu\text{A}$ , $V_{CC} = 1\text{ V}$
RESET Output Voltage	0.8			V	$I_{SOURCE} = 4\text{ }\mu\text{A}$ , $V_{CC} = 1.1\text{ V}$
	$V_{CC} - 1.5$			V	ADM805L/M, $I_{SOURCE} = 800\text{ }\mu\text{A}$
			0.4	V	ADM805L/M, $I_{SINK} = 3.2\text{ mA}$
<b>WATCHDOG TIMER</b>					
Watchdog Timeout Period	1.0	1.6	2.25	s	
WDI Input Pulse Width	50			ns	$V_{IL} = 0.4$ , $V_{IH} = 0.8 (V_{CC})$
WDI Input Threshold					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current			10	$\mu\text{A}$	$\text{WDI} = V_{CC}$
	-10			$\mu\text{A}$	$\text{WDI} = 0\text{ V}$
<b>POWER FAIL DETECTOR</b>					
PFI Input Threshold	1.20	1.25	1.30	V	ADM690A, ADM692A, ADM805L/M
	1.225	1.25	1.275	V	ADM802L/M
PFI Input Current	-25	0.01	+25	nA	
$\overline{\text{PFO}}$ Output Voltage	$V_{CC} - 1.5$			V	$I_{SOURCE} = 800\text{ }\mu\text{A}$
			0.4	V	$I_{SINK} = 3.2\text{ mA}$

## NOTES

<sup>1</sup>Either  $V_{CC}$  or  $V_{BATT}$  can be 0 V if the other  $> +2.0\text{ V}$ .

Specifications subject to change without notice.

# ADM690A/ADM692A/ADM802L/M/ADM805L/M

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = +25°C unless otherwise noted)

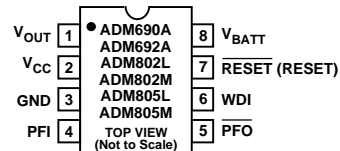
V <sub>CC</sub> .....	-0.3 V to +6 V
V <sub>BATT</sub> .....	-0.3 V to +6 V
All Other Inputs .....	-0.3 V to V <sub>CC</sub> + 0.3 V
Input Current	
V <sub>CC</sub> .....	200 mA
V <sub>BATT</sub> .....	50 mA
GND .....	20 mA
Digital Output Current .....	20 mA
Power Dissipation, N-8 DIP .....	400 mW
θ <sub>JA</sub> Thermal Impedance .....	120°C/W
Power Dissipation, SO-8 SOIC .....	500 mW
θ <sub>JA</sub> Thermal Impedance .....	110°C/W
Operating Temperature Range	
Industrial (A Version) .....	-40°C to +85°C
Lead Temperature (Soldering, 10 sec) .....	+300°C
Vapor Phase (60 sec) .....	+215°C
Infrared (15 sec) .....	+220°C
Storage Temperature Range .....	-65°C to +150°C
ESD Rating .....	>4 kV

\*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

## ORDERING GUIDE

Model	Temperature Range	Package Option
ADM690AAN	-40°C to +85°C	N-8
ADM690AARN	-40°C to +85°C	SO-8
ADM690AARM	-40°C to +85°C	RM-8
ADM692AAN	-40°C to +85°C	N-8
ADM692AARN	-40°C to +85°C	SO-8
ADM802LAN	-40°C to +85°C	N-8
ADM802LARN	-40°C to +85°C	SO-8
ADM802MAN	-40°C to +85°C	N-8
ADM802MARN	-40°C to +85°C	SO-8
ADM805LAN	-40°C to +85°C	N-8
ADM805LARN	-40°C to +85°C	SO-8
ADM805MAN	-40°C to +85°C	N-8
ADM805MARN	-40°C to +85°C	SO-8

## PIN CONFIGURATIONS



## PIN FUNCTION DESCRIPTION

Mnemonic	Function
V <sub>CC</sub>	Power Supply Input: +5 V Nominal.
V <sub>BATT</sub>	Backup Battery Input. As V <sub>CC</sub> falls below the reset threshold and below V <sub>BATT</sub> by 20 mV, V <sub>BATT</sub> will be switched to V <sub>OUT</sub> . On power-up as V <sub>CC</sub> rises to 20 mV above V <sub>BATT</sub> , V <sub>OUT</sub> will be switched back to V <sub>CC</sub> .
V <sub>OUT</sub>	Output Voltage. When V <sub>CC</sub> is above the reset threshold, V <sub>OUT</sub> is connected to V <sub>CC</sub> through an on chip switch. When V <sub>CC</sub> is below the reset threshold, the higher of V <sub>CC</sub> or V <sub>BATT</sub> is connected to V <sub>OUT</sub> .
GND	0 V. Ground reference for all signals.
PFI	Power Fail Comparator Input. If PFI is less than 1.25 V, the power fail output $\overline{\text{PFO}}$ goes low. If unused, PFI should be connected to V <sub>CC</sub> or GND.
$\overline{\text{PFO}}$	Power Fail Comparator Output. If PFI is less than 1.25 V, the power fail output $\overline{\text{PFO}}$ goes low.
$\overline{\text{RESET}}$	Logic Output. $\overline{\text{RESET}}$ goes low if 1. V <sub>CC</sub> falls below the Reset Threshold 2. The watchdog timer is not serviced within its timeout period (1.6 seconds) The reset threshold is typically 4.65 V for the ADM690A/ADM802L/ADM805L and 4.4 V for the ADM692A/ADM802M/ADM805M. $\overline{\text{RESET}}$ remains low for 200 ms after V <sub>CC</sub> returns above the threshold. $\overline{\text{RESET}}$ also goes low for 200 ms if the watchdog timer is enabled but not serviced within its timeout period.
RESET	Active high RESET output (ADM805L/M only). This is the inverse of $\overline{\text{RESET}}$ . The asserted (high) level is V <sub>CC</sub> or V <sub>BATT</sub> whichever is higher.
WDI	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than 1.6 s, (RESET) (RESET) is activated. The timer resets with each transition on the WDI line. The watchdog timer may be disabled if WDI is left floating or is connected to a high impedance three stated logic output.

# ADM690A/ADM692A/ADM802L/M/ADM805L/M

## Typical Performance Curves

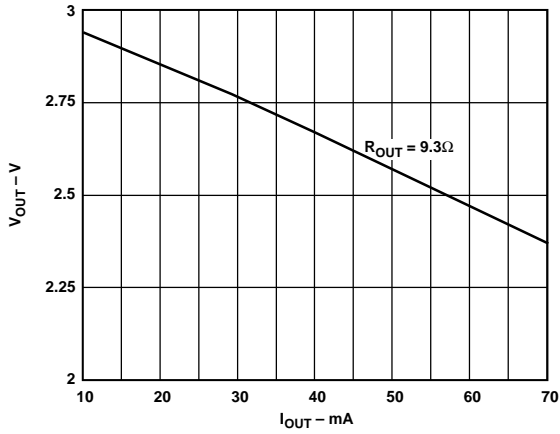


Figure 1. Output Voltage vs. Load Current in Battery Backup

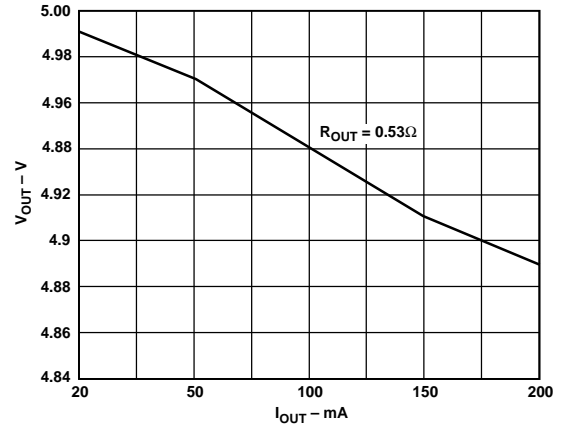


Figure 4. Output Voltage vs. Load Current in Normal Operation

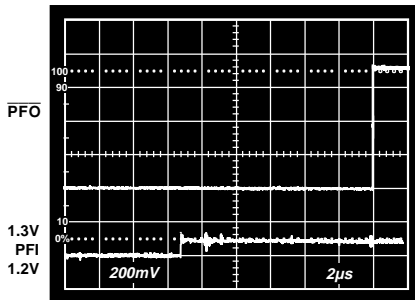


Figure 2. Power Fail Comparator Response Time L → H

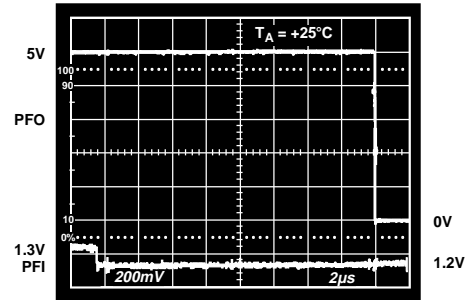


Figure 5. Power Fail Comparator Response Time H → L

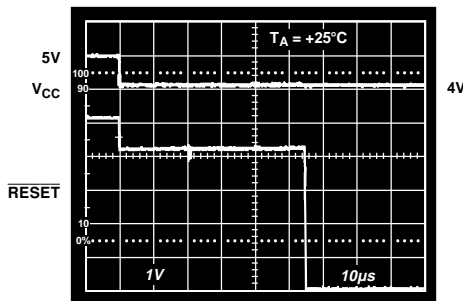


Figure 3. ADM690A  $\overline{RESET}$  Response Time

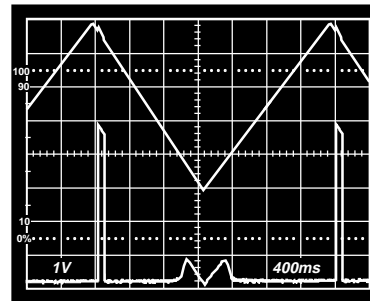


Figure 6.  $\overline{RESET}$  Output Voltage vs.  $V_{CC}$

# ADM690A/ADM692A/ADM802L/M/ADM805L/M

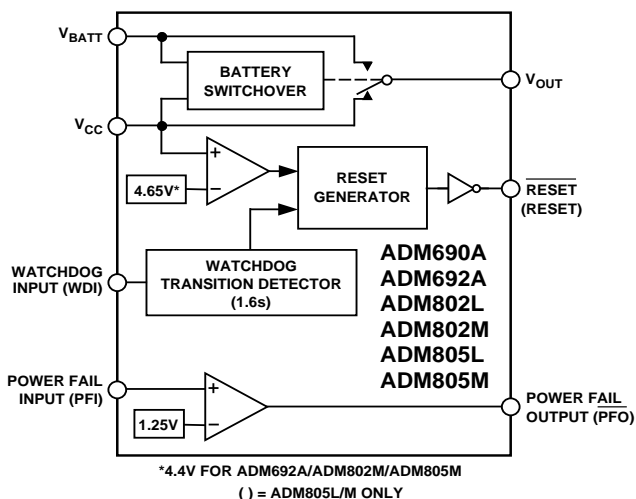


Figure 7. Functional Block Diagram

## POWER FAIL $\overline{\text{RESE}}$ , RESET

RESET is an active low output which provides a  $\overline{\text{RESE}}$  signal to the microprocessor whenever  $V_{CC}$  is at an invalid level. When  $V_{CC}$  falls below the reset threshold, the  $\overline{\text{RESE}}$  output is forced low. The nominal reset voltage threshold is 4.65 V (ADM690A/ADM802L/ADM805L or 4.4 V ADM692A/ADM802M/ADM805M).

On power-up  $\overline{\text{RESE}}$  will remain low for 200 ms after  $V_{CC}$  rises above the reset threshold. This allows time for the power supply and microprocessor to stabilize. On power-down, the  $\overline{\text{RESE}}$  output remains low with  $V_{CC}$  as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

The guaranteed minimum and maximum thresholds are as follows:  
ADM690A/ADM802L/ADM805L: 4.5 V and 4.75 V

ADM692A: 4.25 V and 4.5 V.

ADM802L: 4.55 V and 4.7 V

ADM802M: 4.3 V and 4.45 V

The ADM805L and ADM805M contain an active high reset output. This is the complement of  $\overline{\text{RESE}}$  and is intended for processors requiring an active high RESET signal.

The guaranteed minimum and maximum thresholds for the ADM805 are:

ADM805L: 4.5 V and 4.75 V

ADM805M: 4.25 V and 4.5 V.

## Watchdog Timer $\overline{\text{RESE}}$ , RESET

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within 1.6 seconds, a RESET pulse is generated. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum timeout period. If WDI remains permanently either high or low, reset pulses will be issued after each timeout period (1.6 s). The watchdog monitor can be deactivated by floating the Watchdog Input (WDI) or by connecting it to midsupply.

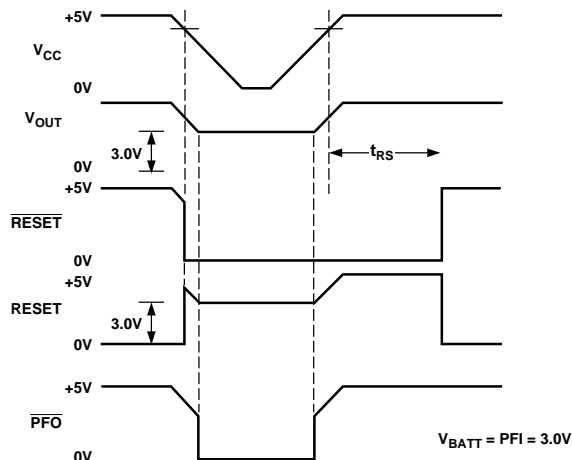


Figure 8. Timing Diagram

## BATTERY SWITCHOVER SECTION

During normal operation with  $V_{CC}$  higher than the reset threshold,  $V_{CC}$  is internally switched to  $V_{OUT}$  via an internal PMOS transistor switch. This switch has a typical on-resistance of less than 1  $\Omega$  and can supply up to 100 mA at the  $V_{OUT}$  terminal. Once  $V_{CC}$  falls below the reset threshold, the higher of  $V_{CC}$  or  $V_{BATT}$  is switched to  $V_{OUT}$ . This means that  $V_{BATT}$  connects to  $V_{OUT}$  only when  $V_{CC}$  is below the reset threshold and  $V_{BATT}$  is greater than  $V_{CC}$ .

$V_{OUT}$  is normally used to drive a RAM memory bank which may require instantaneous currents of greater than 100 mA. If this is the case, then a bypass capacitor should be connected to  $V_{OUT}$ . The capacitor will provide the peak current transients to the RAM. A capacitance value of 0.1  $\mu\text{F}$  or greater may be used.

A 9  $\Omega$  MOSFET switch connects the  $V_{BATT}$  input to  $V_{OUT}$  during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. The supply current in battery backup is typically 0.05  $\mu\text{A}$ .

Typically 3 V batteries are used as the backup supply. High value capacitors, either standard electrolytic or the farad size double layer capacitors, can also be used for short-term memory back up. A small charging current of typically 10 nA (0.1  $\mu\text{A}$  max) flows out of the  $V_{BATT}$  terminal. This current is useful for maintaining rechargeable batteries in a fully charged condition. This extends the life of the back up battery by compensating for its self discharge current. Also note that this current poses no problem when lithium batteries are used for back up since the maximum charging current (0.1  $\mu\text{A}$ ) is safe for even the smallest lithium cells.

If the battery-switchover section is not used,  $V_{BATT}$  should be connected to GND and  $V_{OUT}$  should be connected to  $V_{CC}$ .

# ADM690A/ADM692A/ADM802L/M/ADM805L/M

Table I. Input and Output Status in Battery Backup Mode

Signal	Status
V <sub>OUT</sub>	V <sub>OUT</sub> is connected to V <sub>BATT</sub> via an internal PMOS switch.
RESET	Logic low.
RESET	Logic high (ADM805L, ADM805M). The open circuit output voltage is equal to V <sub>OUT</sub> .
PFI	The power fail comparator is disabled
PFO	Logic low.
WDI	The watchdog timer is disabled

## Power Fail Comparator

The power fail comparator is an independent comparator that may be used to monitor the input power supply. The comparator's inverting input is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input may be used to monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output (PFO) goes low indicating a power failure. For early warning of power failure the comparator may be used to monitor the preregulator input simply by choosing an appropriate resistive divider network. The PFO output can be used to interrupt the processor so that a shutdown procedure is implemented before the power is lost.

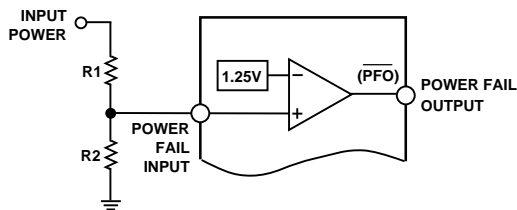
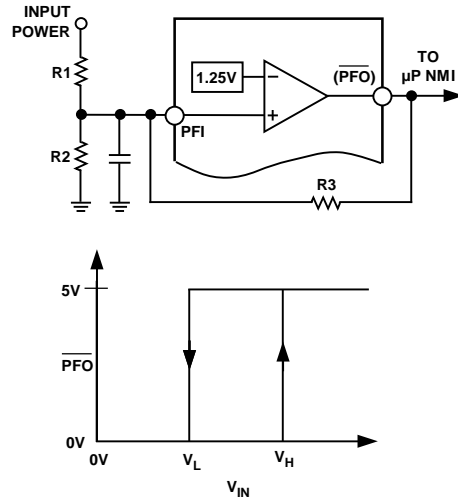


Figure 9. Power Fail Comparator

## Adding Hysteresis to the Power Fail Comparator

For increased noise immunity, hysteresis may be added to the power fail comparator. Since the comparator circuit is non-inverting, hysteresis can be added simply by connecting a resistor between the PFO output and the PFI input as shown in Figure 10. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity may be achieved by connecting a capacitor between PFI and GND.



$$V_H = 1.25 \left[ 1 + \left( \frac{R_2 + R_3}{R_2 \times R_3} \right) R_1 \right]$$

$$V_L = 1.25 + R_1 \left( \frac{1.25}{R_2} - \frac{V_{CC} - 1.25}{R_3} \right)$$

$$V_{MID} = 1.25 \left( \frac{R_1 + R_2}{R_2} \right)$$

Figure 10. Adding Hysteresis to the Power Fail Comparator

## TYPICAL APPLICATIONS

Figure 11 shows a typical power monitoring, battery backup application. V<sub>OUT</sub> powers the CMOS RAM. Under normal operating conditions with V<sub>CC</sub> present, V<sub>OUT</sub> is internally connected to V<sub>CC</sub>. If a power failure occurs, V<sub>CC</sub> will decay and V<sub>OUT</sub> will be switched to V<sub>BATT</sub> thereby maintaining power for the CMOS RAM. A RESET pulse is also generated when V<sub>CC</sub> falls below the reset threshold.

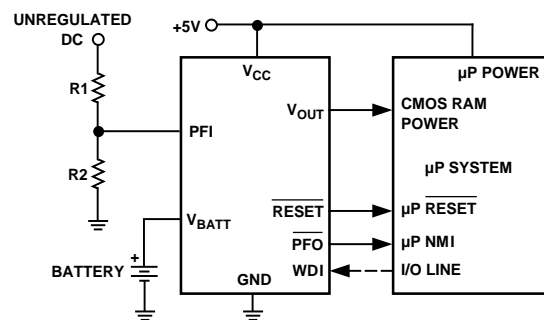


Figure 11. Typical Application Circuit

The watchdog timer input (WDI) monitors an I/O line from the μP system. This line must be toggled once every 1.6 seconds to verify correct software execution. Failure to toggle the line indicates that the μP system is not correctly executing its program and may be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the processor.

If the watchdog timer is not needed, the WDI input should be left floating.

The Power Fail Input, PFI, monitors the input power supply via a resistive divider network. The voltage on the PFI input is compared with a precision 1.25 V internal reference. If the input voltage drops below 1.25 V, a power fail output (PFO) signal is generated. This warns of an impending power failure and may be used to interrupt the processor so that the system may be shut down in an orderly fashion. The resistors in the sensing network are ratioed to give the desired power fail threshold voltage  $V_T$ .

$$V_T = (1.25 R1/R2) + 1.25 V$$

$$R1/R2 = (V_T/1.25) - 1$$

### Alternate Watchdog Input Drive Circuits

The watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer. When three-stated, the WDI input will float thereby disabling the watchdog timer.

### High Capacity Backup Capacitors

High capacity (0.1  $\mu\text{F}$  or greater) capacitors may be used as a backup power source. A typical application is shown in Figure 12.

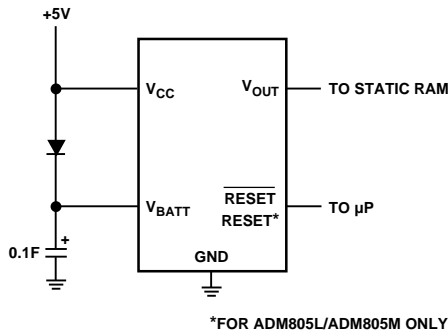


Figure 12. High Capacity Capacitor

### Operation Without a Backup Supply

If a backup power source is not used,  $V_{BATT}$  should be connected to GND and  $V_{OUT}$  should be connected to  $V_{CC}$ .

### Replacing the Backup Battery

The backup battery may be replaced without any danger of spurious resetting when  $V_{CC}$  is present. Since  $V_{CC}$  is above the reset threshold, a reset will not occur even if  $V_{BATT}$  is floating while a replacement battery is being inserted. This differs from older generation products where leakage currents flowing out  $V_{BATT}$  could cause spurious resetting during battery replacement.

### μPs With Bidirectional $\overline{\text{RESET}}$

In order to prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor should be inserted between the ADM69xA/ADM80xx  $\overline{\text{RESET}}$  output pin and the  $\mu\text{P}$  reset pin. This will limit the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 k $\Omega$ . If the reset output is required for other uses, then it should be buffered as shown in Figure 13.

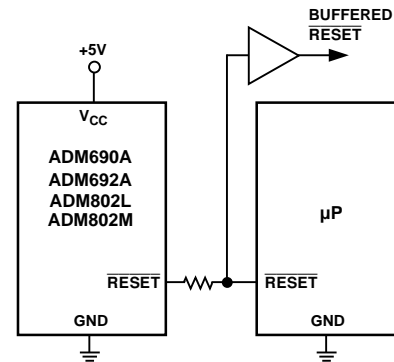


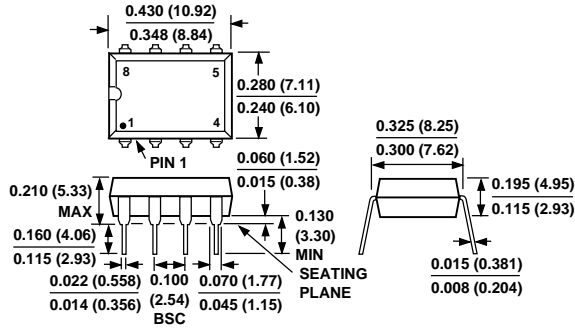
Figure 13. Bidirectional Reset

# ADM690A/ADM692A/ADM802L/M/ADM805L/M

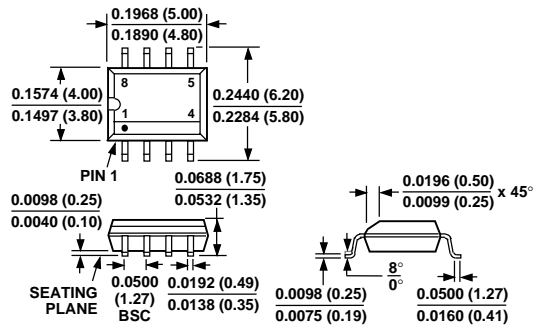
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 8-Pin Plastic DIP (N-8)



### 8-Lead SOIC (SO-8)



### 8-Lead MicroSOIC (RM-8)

