ANALOG DEVICES

Communications System Supervisory/Sequencing Circuit

| Preliminary Technical Data | ADM1060 |

ADM1060 TABLE OF CONTENTS

REV. PrJ 11/02

ADM1060

FEATURES

Faults detected on 7 independent supplies
- **1 High Voltage supply (up to 14.4V)**
- **4 Positive Voltage Only Supplies (up to 6V)**
- **2 Positive/Negative Voltage supplies (up to +6V OR down to -6V)**

Watchdog Detector Input- Timeout delay programmable from 200ms to 12.8sec

4 General Purpose Logic Inputs

Programmable Logic Block- combinatorial and sequencing logic control of all inputs and outputs

9 Programmable Output Drivers
- **Open Collector (external resistor required)**
- **Open Collector with internal pull-up to V_{DD}**
- **Fast Internal pull-up to V_{DD}**
- **Open Collector with internal pull-up to VPn**
- **Fast Internal pull-up to VPn**
- **Internally charge pumped high drive (for use with external N- channel FETS- PDO's 1 to 4 only)**

EEPROM- 512 Bytes

Industry Standard 2- Wire Bus Interface (SMBus)

Guaranteed PDO Low with VPn, VH=1V

APPLICATIONS

Central Office Systems

Servers

Infrastructure Network Boards

High density, multi- voltage system cards

GENERAL DESCRIPTION

The ADM1060 is a programmable supervisory/sequencing device which offers a single chip solution for multiple power supply fault detection and sequencing in communications systems.

In central office, servers and other infrastructure systems, a common backplane dc supply is reduced to multiple board supplies using dc/dc converters. These multiple supplies are used to power different sections of the board (eg) 3.3V Logic circuits, 5V logic circuits, DSP core and I/O circuits etc. There is usually a requirement that certain sections power up before others (eg) a DSP core to power up before the DSP I/O or vice versa. This is in order to avoid damage, miscommunication or latch- up. The ADM1060 facilitates this, providing supply fault detection and sequencing/combinatorial logic for up to 7 independent supplies. The 7 Supply Fault Detectors consist of one high voltage detector (up to +14.4V), two bipolar voltage detectors (up to +6V OR down to -6V) and 4 positive low voltage detectors (up to +6V). All of the detectors can be programmed to detect undervoltage, overvoltage or out- of window (undervoltage OR overvoltage) conditions. The inputs to these Supply Fault Detectors are via the VH pin (High Voltage), VBn pins (positive OR negative) and VPn pins (Positive only) pins respectively. Either the VH supply or one of the VPn supplies is used to power the ADM1060 (whichever is highest). This ensures that, in the event of a supply failure, the ADM1060 is kept alive for as long as possible, thus enabling a reliable fault flag to be asserted and the system to be powered down in an ordered fashion.

Other inputs to the ADM1060 include a Watchdog Detector (WDI) and 4 General Purpose Inputs (GPIn). The Watchdog Detector can be used to monitor a processor clock. If the clock does not toggle (transition from low to high or from high to low) within a programmable timeout period (up to 18 sec.), a fail flag will assert. The 4 General Purpose inputs can be configured as logic buffers or to detect positive/negative edges and to generate a logic pulse or level from those edges. Thus, the user can input control signals from other parts of their system (eg RE-SET or POWER_GOOD) to gate the sequencing of the supplies supervised by the ADM1060.

The ADM1060 features 9 Programmable Driver Outputs (PDO's). All 9 outputs can be configured to be logic outputs, which can provide multiple functions for the end user such as RESET generation, POWER_GOOD status, enabling of LDO's, Watchdog Timeout assertion etc. PDO's 1- 4 have the added feature of being able to provide an internally charge pumped high voltage for use as the gate drive of an external N- Channel FET which could be placed in the path of one of the supplies being supervised.

All of the inputs and outputs described above are controlled by the Programmable Logic Block Array. This is the logic core of the ADM1060. It is comprised of 9 macrocells, one for each PDO. These macrocells are essentially just wide AND gates. Any/all of the inputs can be used as an input to these macrocells. The output of a macrocell can also be used as an input to any macrocell other than itself (an input to itself would result in a no-terminating loop). The PLBA outputs control the PDO's of the ADM1060 via delay blocks, where a delay of between 0 and 500ms can be programmed on the rising and/or the falling edge of the data. This results in a very flexible sequencing ability. Thus, for instance, PDO1 can be programmed so that it will not assert until, say, VP2, VP3 and VP4 supplies are in tolerance, VB1 and VH have been in tolerance for 200mS, and PDO7 has already been asserted. A simple sequencing operation would be to daisy chain each PLB output into the input of the next PLB such that PDO9 doesn't assert until PDO8 asserts, which in turn doesn't assert until PDO7 asserts etc.

All of the functional capability described here is programmable through the industry standard 2 wire bus (SMBus) provided. Device settings can be written to EEPROM memory for automatic programming of the device on power-up. The EEPROM is organised in 512 bytes, half of which are used to program all of the functions on the ADM1060. The other 256 bytes of EEPROM are for general purpose system use (eg) date codes, system ID etc. Read/write access to this is also via the 2 wire interface. In addition, each output state can be directly overdriven from the serial interface, allowing a further level of control (eg) a system controlled soft powerdown.
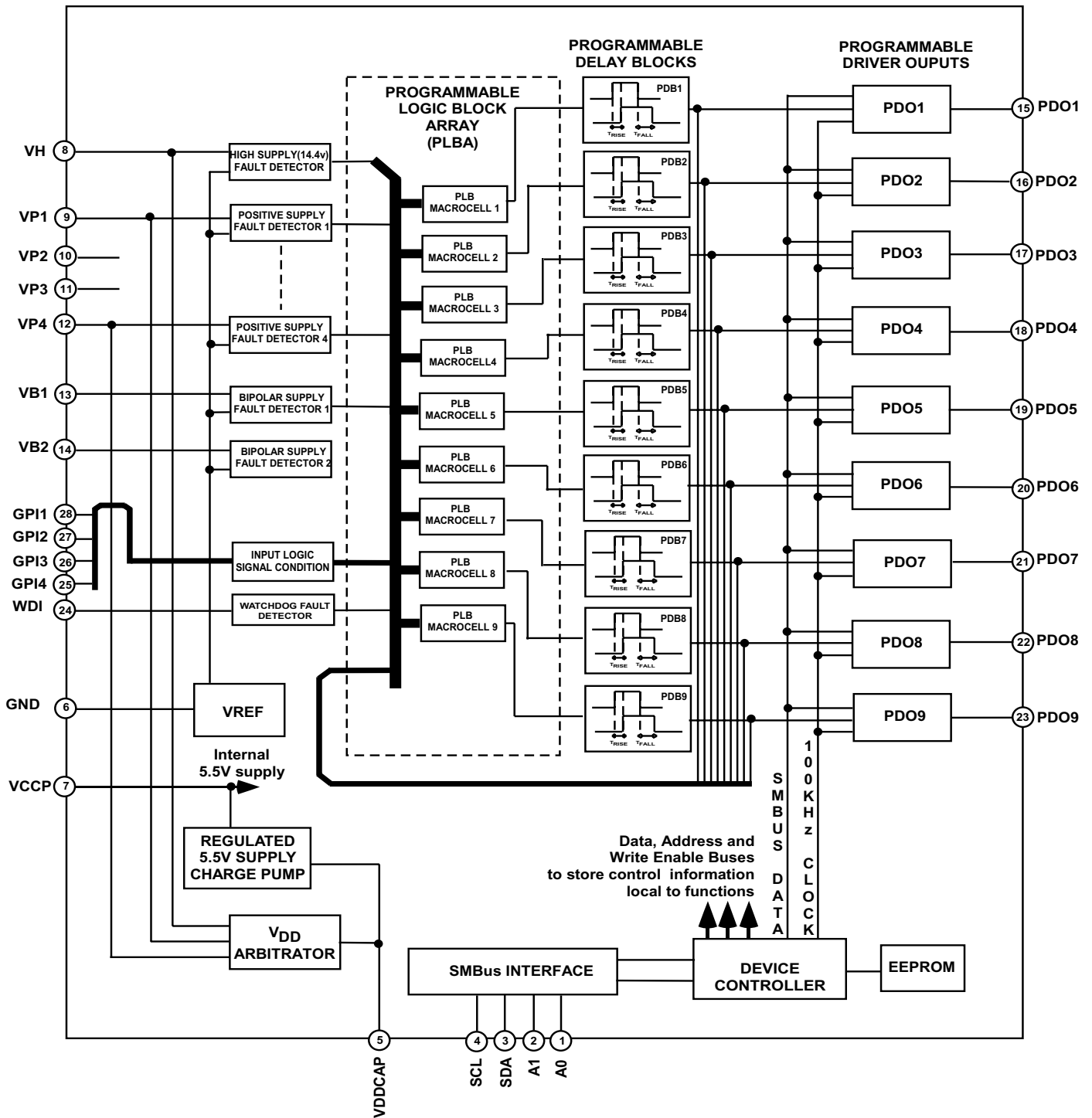
ADM1060

ADM1060 FUNCTIONAL BLOCK DIAGRAM

ADM1060–SPECIFICATIONS

(VH=4.5V to 14.4V, VPn = 3.0V to 6.0V [2], T_A = -40ºC to 85ºC, unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER SUPPLY ARBITRATION					
VDDCAP	2.7			V	Any VPn>=3.0V
	2.7				VH>=4.5V
		4.75	5.1	V	Any VPn=6.0V
		4.75	5.1	V	VH=14.4V
POWER SUPPLY					
Supply Current, I_{DD}		3		mA	VDDCAP=4.75V, no PDO FET Drivers on, no loaded PDO pullups to VDDCAP
			5	mA	VDDCAP=4.75V, all PDO FET Drivers on (loaded with 1µA), no PDO pullups to VDDCAP
Additional current available from VDDCAP			1	mA	Max. additional load that can be drawn from PDO pullups to VDDCAP
SUPPLY FAULT DETECTORS					
VH Input					
Input Impedance		52		kΩ	From VH to GND
Threshold Ranges					
Mid Range	2		6	V	
Programming Step Size		15.6		mV	
High Range	4.8		14.4	V	
Programming Step Size		37.6		mV	
VPn Inputs					
Input Impedance		52		kΩ	From VPn to GND
Threshold Ranges					
Ultra Low Range	0.6		1.8	V	
Programming Step Size		4.7		mV	
Low Range	1		3	V	
Programming Step Size		7.8		mV	
Mid Range	2		6	V	
Programming Step Size		15.6		mV	
VBn Inputs					
Input Impedance		190		kΩ	From VBn to 2.25V (Internal Ref.)
		52		kΩ	From VBn to GND (positive mode)
		30		kΩ	From VBn to GND (negative mode)
Threshold Ranges					
Negative Mode:					
Mid Range	-6		-2	V	
Programming Step Size		15.6		mV	
Positive Mode:					
Low Range	1		3	V	
Programming Step Size		7.8		mV	
Mid Range	2		6	V	
Programming Step Size		15.6		mV	
Absolute Accuracy			2.5	%	
Absolute Accuracy-					
Calibrated Voltage Thresholds[4]			1.0	%	TA=0ºC to 85ºC, Threshold Voltage>0.9V
Threshold Programming Resolution			8	Bits	
Digital Glitch Filter	0		100	µs	See figure 3. 8 timeout options between 0 and 100µs

NOTES

[1] These are target specifications and subject to change.

[2] At least one VPn must be >=3.0V if used as supply. VH must be >=4.5V if used as supply.

[3] Logic inputs will accept input high voltages up to 5.5V even when device is operating at supply voltages below 5V.

[4] Calibrated Voltage Thresholds are set at Production.

REV.PrJ11/02

ADM1060–SPECIFICATIONS[1]

(VH=4.5V to 14.4V, VPn = 3.0V to 6.0V[2], T_A = -40ºC to 85ºC, unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
PROGRAMMABLE DRIVER OUTPUTS					
High Voltage (Charge Pump) Mode (PDO's 1 to 4)					
Output Impedance, R_{OUT}		440		kΩ	
V_{OH}	10.5	12.5	14	V	I_{OH}=0
	10	12		V	I_{OH}=1µA
I_{OUTAVG}		20		µA	$2V<V_{OH}<7V$
Standard (Digital Output) Mode (PDO's 1 to 9)					
V_{OH}	2.4			V	V_{PU}(Pullup to VDDCAP or VPn)=2.7V, I_{OH}=1mA
			4.5	V	V_{PU} to VPn=6.0V, I_{OH}=0mA
	V_{PU}-0.3			V	VPU<=2.7V, I_{OH}=1mA
V_{OL}			0.4	V	I_{OL}=2mA
			1.2	V	I_{OL}=10mA
			2.0	V	I_{OL}=15mA
I_{SINK}			20	mA	Total Sink Current
$R_{PULLUP-}$ Weak Pull-up		20		kΩ	Internal pullup
$I_{SOURCE (VPn)}$			2	mA	Current Load on any VPn pull-ups (ie) total source current available through any number of PDO pull-up switches configured on to any one V_{PDO}=14.4V
Tristate Output Leakage Current			10	µA	
DIGITAL INPUTS (GPI 1-4,WDI,A0,A1)					
Input High Voltage, V_{IH}	2.0			V	Max. V_{IN}=5.5V
Input Low Voltage, V_{IL}			0.8	V	Max. V_{IN}=5.5V
Input High Current, I_{IH}	-1			µA	V_{IN} = 5.5V
Input Low Current, I_{IL}			1	µA	V_{IN} = 0
Input Capacitance		TBD		pF	
Programmable Pulldown Current, $I_{PULLDOWN}$		10		µA	If known logic state required
SERIAL BUS DIGITAL INPUTS (SDA,SCL)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.8	V	
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -3.0mA
PROGRAMMABLE DELAY BLOCK					
Timeout	0		500	ms	16 programmable options on both rising and falling edge
WATCHDOG TIMER INPUT					
Timeout	0		12.8	s	8 programmable timeout options
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}			400	KHz	See Figure 8c
Glitch Immunity, t_{SW}			50	ns	See Figure 8c
Bus Free Time, t_{BUF}	4.7			µs	See Figure 8c
Start Setup Time, $t_{SU;STA}$	4.7			µs	See Figure 8c
Start Hold Time, $t_{HD;STA}$	4			µs	See Figure 8c
SCL Low Time, t_{LOW}	4.7			µs	See Figure 8c
SCL High Time, t_{HIGH}	4			µs	See Figure 8c
SCL, SDA Rise Time, t_r			1000	ns	See Figure 8c
SCL, SDA Fall Time, t_f			300	µs	See Figure 8c
Data Setup Time, $t_{SU;DAT}$	250			ns	See Figure 8c
Data Hold Time, $t_{HD;DAT}$	300			ns	See Figure 8c

NOTES

[1] These are target specifications and subject to change.

[2] At least one supply connected to VH or VPn must be >=3.0V

[3] Logic inputs will accept input high voltages up to 5.5V even when device is operating at supply voltages below 5V.

[4] Timing specifications are tested at logic levels of V_{IL} = 0.8V for a falling edge and V_{IH} = 2.2V for a rising edge.

ADM1060

PIN FUNCTION DESCRIPTION

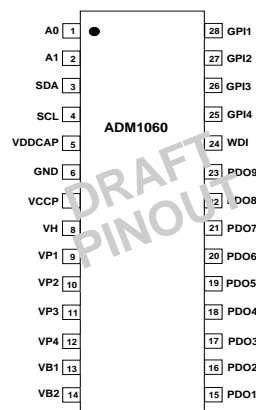| Pin	Mnemonic	Function
1	A0	Logic input. Controls the 7th bit (LSB) of the 7 bit Serial Bus Address.
2	A1	Logic input. Controls the 6th bit of the 7 bit Serial Bus Address.
3	SDA	Serial Bus data I/O pin. Open- Drain output. Requires 2.2k pullup resistor
4	SCL	Open- Drain Serial Bus Clock pin. Requires 2.2k pullup resistor
5	VDDCAP	V_{DD} bypass capacitor pin. A capacitor from this pin to GND stabilises the V_{DD} Arbitrator. 0.1μF is recommended for this function.
6	GND	Ground. Connect to common of power supplies.
7	VCCP	Reservoir Capacitor for Central Charge Pump. This charge pump powers all of the internal circuits of the ADM1060 and provides the first stage in the tripler circuits used to produce 12V of gate drive on PDO's 1- 4.
8	VH	High Voltage Supply Input. 2 input ranges. A supply of between 2V and 6V or between 4.8V and 14.4V can be applied to this pin. The V_{DD} arbitrator will select this supply to power the ADM1060 if it is the highest supply supervised.
9-12	VP1-4	Positive Only Supply Inputs. 2 input ranges. A supply of between 1V and 3V or between 2V and 6V can be applied to this pin. The V_{DD} arbitrator will select one of these supplies to power the ADM1060 if it is the highest supply supervised.
13-14	VB1-2	Bipolar Supply Inputs. 2 modes. 2 input ranges in positive mode. 1 input range in negative mode. A supply of between -6V and -2V can be applied to this pin when set in negative mode. A supply of between 1V and 3V or between 2V and 6V can be applied to this pin when set in positive mode.
15-23	PDO_1-9	Programmable Driver Output pin. All 9 can be programmed as logic outputs with multiple pull-up options to VDD or VPn. PDO's 1 to 4 can also provide a charge-pump generated gate drive for external N- Channel FET
24	WDI	Watchdog Input. Used to monitor a processor clock and asserts a fault condition if the clock fails to transition from low-to-high or high-to-low within a programmed timeout period (up to 18sec).
25-28 Reset,	GPI_4-1	General Purpose Logic Input. TTL compatible Logic. Can be used as, say, a Manual a Chip Enable pin or as an input for a control logic signal which may be critical to the power up/down sequence of the supplies under control.

ABSOLUTE MAXIMUM RATINGS*

Voltage on VH Pin . . . . +17 V
Voltage on VP Pins . . . . +7 V
Voltage on VB Pins . . . . - 7 V to +7V
Voltage on A0,A1 . . . . -0.3V to (V_{CC}+0.3V)
Voltage on Any Other Input . . . . -0.3V to 6.5V
Input Current at any pin . . . . ±5mA
Package Input Current . . . . ±20mA
Maximum Junction Temperature ($T_J$max) . . . . . . .150 °C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature, Soldering
   Vapor Phase 60 sec . . . . +215°C
ESD Rating all pins . . . . 2000 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS
28-Pin TSSOP Package:
Θ_{JA} =   98°C/Watt

```
         ┌───────────┐
   A0 ─┤1         28├─ GPI1
   A1 ─┤2         27├─ GPI2
  SDA ─┤3         26├─ GPI3
  SCL ─┤4         25├─ GPI4
VDDCAP─┤5  ADM1060 24├─ WDI
  GND ─┤6         23├─ PDO9
 VCCP ─┤7         22├─ PDO8
   VH ─┤8         21├─ PDO7
  VP1 ─┤9         20├─ PDO6
  VP2 ─┤10        19├─ PDO5
  VP3 ─┤11        18├─ PDO4
  VP4 ─┤12        17├─ PDO3
  VB1 ─┤13        16├─ PDO2
  VB2 ─┤14        15├─ PDO1
         └───────────┘
```

DRAFT PINOUT

ADM1060 PIN CONFIGURATION

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1060ARU	-40°C to +85°C	28-PinTSSOP	RU-28

REV. PrJ 11/02

ADM1060 INPUTS

POWERING THE ADM1060

The ADM1060 is powered from the highest voltage input on either the Positive Only supply inputs (VPn) or the High Voltage supply input (VH). The same pins are used for supply fault detection (discussed below) . A V_{DD} Arbitrator on the device chooses which supply to use. The arbitrator can be considered to be diode OR'ing the positive supplies together (as shown in figure 1). In addition to this, the diodes are supplemented with switches in a synchronous rectifier manner, to minimise voltage loss. This loss can be reduced to ~0.2V, resulting in the ability to power the ADM1060 from a supply as low as 3.0V. Note that the supply on the VBn pins cannot be used to power the device, even if the input on these pins is positive. Also, the minimum supply of 3.0V must appear on one of the VPn pins in order to power up the ADM1060 correctly. A supply of no less than 4.5V can be used on VH. This is because there is no synchronous rectifier circuit on the VH pin, resulting in a voltage drop of ~1.5V across the diode of the V_{DD} Arbitrator.

An external cap to GND is required to decouple the on-chip supply from noise. This cap should be connected to the VDDCAP pin, as shown in figure 1. The cap has another use during "brown outs" (momentary loss of power). Under these conditions, where the input supply, VPn, dips transiently below V_{DD}, the synchronous rectifier switch immediately turns off so that it doesn't pull V_{DD} down. The V_{DD} cap can then act like a reservoir and keep the chip active until the next highest supply takes over the powering of the device. $0.1\mu F$ is recommended for this function.

Note that in the case where there are 2 or more supplies within 100mV of each other, the supply which takes control of V_{DD} first will keep control (e.g) if VP1 is connected to a 3.3V supply, then V_{DD} will power up to approximately 3.1V through VP1. If VP2 is then connected to another 3.3V supply, VP1 will still power the device, unless VP2 goes 100mV higher than VP1.
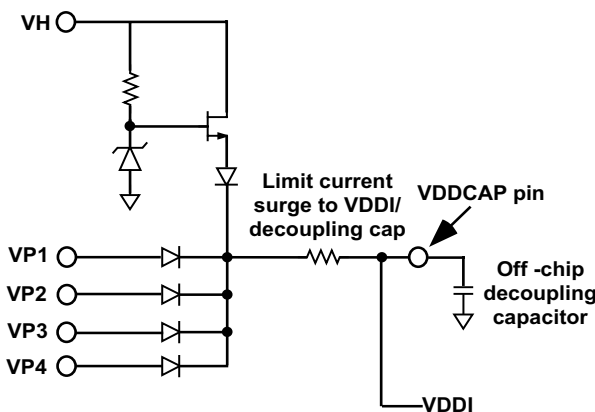

Figure 1. VDD Arbitrator Operation

PROGRAMMABLE SUPPLY FAULT DETECTORS (SFD'S)

The ADM1060 has seven programmable Supply Fault Detectors, 1 high voltage detector (2V to 14.4V), 2 bipolar detectors (2V to 6V, -2V to -6V) and 4 Positive only voltage detectors (0.6V to 6V). Inputs are applied to these detectors via the VH (High Voltage Supply input) pin, VBn (Bipolar Supply input) pins and VPn (Positive Only input) pins respectively. The SFD's detect a fault condition on any of these input supplies. A fault is defined as Undervoltage (where the supply drops below a preprogrammed level), Overvoltage (where the supply rises above a preprogrammed level) or Out-of-Window (where the supply deviates outside either the programmed overvoltage OR undervoltage threshold). Only one fault type can be selected at a time.

An Undervoltage fault is detected by comparing the input supply to a programmed reference (the undervoltage threshold). If the input voltage drops below the undervoltage threshold the output of the comparator goes high, asserting a fault. The undervoltage threshold is programmed using an 8 bit DAC. On a given range, the UV threshold can be set with a resolution of:-

$$Step\ Size\ =\ Threshold\ Range/255$$

An Overvoltage (OV) fault is detected in exactly the same way, using a second comparator and DAC to program the reference.

All thresholds are programmed using 8 bit registers, one register each for the 7 UV thresholds and 1 each for the 7 OV thresholds. The UV or OV threshold programmed by the user is given by:-

$$V_T = \frac{V_R \times N}{255} + V_B$$

where:-
V_T = Desired Threshold Voltage (UV or OV)
V_R = Threshold Voltage Range
N = Decimalized version of 8 bit code
V_B = Bottom of Threshold Range

This results in the code for a given threshold being given by:-

$$N = 255 \times (V_T - V_B)/V_R$$

Thus, for example, if the user wishes to set a 5V OV threshold on VP1, the code to be programmed in the PS1OVTH register (discussed later) would be given by:-

$$N = 255 \times (5-2)/4$$

Thus, N=192 (11000000 or C0H)

The available threshold ranges, and the resolution they are programmed to are shown in table 1. Note that the low end of the detection range is fixed to 33.33% of the top of the range. Note also, that for a given SFD, the ranges overlap (eg) VH goes from 2V to 6V then from 4.8V to 14.4V. This is to provide better threshold setting resolution as supplies decrease in value.

Input Name	Voltage Ranges	Resolution	
VH	4.8V to 14.4V	37.6mV	
	2V to 6V	15.6mV	
VBn	2V to 6V	15.6mV	(Pos. Mode)
	1V to 3V	7.8mV	"
	-6V to -2V	15.6mV	(Neg. Mode)
VPn	2V to 6V	15.6mV	
	1V to 3V	7.8mV	
	0.6V to 1.8V	4.7mV	

Table 1. Input threshold Ranges and Resolution.

Figure 2 illustrates the function of the programmable SFD (for the case of a positive supply).
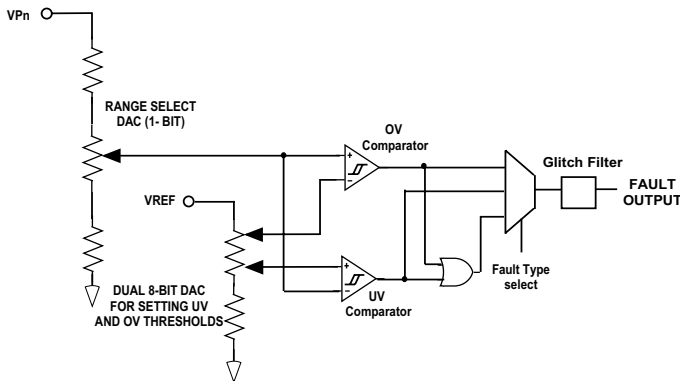

Figure 2. Positive Programmable Supply Fault Detector

SFD COMPARATOR HYSTERESIS

The OV and UV comparators, shown in figure 1, are always looking at VPn via a potential divider. In order to avoid chattering (multiple transitions when the input is very close to the threshold level set), these comparators have digitally progammable hysteresis. The UV and OV hysteresis can be programmed in two registers which are similar but separate to the UV or OV threshold registers. Only the 5 LSB's of these registers can be set. The hysteresis is added after the supply voltage goes out of tolerance. Thus, the user can determine how much above the UV threshold the input must rise again before a UV fault is de-asserted. Similarly, the user can determine how much below the OV threshold the input must fall again before an OV fault is de-asserted. The hysteresis figure is given by:-

$$V_H = V_R \; x \; N_{THRESH}/255$$

where:-

V_H = Desired Hysteresis Voltage

N_{THRESH} = Decimalized version of 5 bit hysteresis code

Therefore, if the low range threshold detector was selected (ie 1V to 3V (V_R), the max hysteresis is then defined as:-

$$(3V-1V) \; x \; 31/255 = 242mV \; (2^5-1 = 31)$$

The hysteresis programming resolution is the same as the threshold detect ranges (ie) 37.5mV on the high range, 15.6mV on the mid range, 7.8mV on the low range and 4.7mV on the ultra low range.

BIPOLAR SFD'S

The 2 bipolar SFD's also allow the detection of faults on negative supplies. A polarity bit in the setup register for this SFD (bit 7- register BSnSEL- see register map overleaf) determines if a positive or negative input should be applied to VBn. Only 1 range (-6V to -2V) is available when the SFD's are in negative mode. Note that the bipolar SFD's cannot be used to power the ADM1060, even if the voltage on VBn is positive.

SFD FAULT TYPES

3 types of faults can be asserted by the SFD- 1) An OV fault, 2) an UV fault and 3) an out-of-window fault (where the UV and OV faults are OR'ed together). The type of fault required is programmed using the Fault Type Select bits (bits 0,1- Register _SnSEL). If an application requires separate fault conditions to be detected on one supply (eg) assert PDO1 if an UV fault occurs on a 3.3V supply, assert PDO9 if an OV fault occurs on the same 3.3V supply, that supply will need to be applied to more than one input pin.

GLITCH FILTERING ON THE SFD'S

The final stage of the SFD is a glitch filter. This block provides time domain filtering on spurious transitions of the SFD fault output. These could be caused by bounce on a supply at its initial turn- on. The comparators of the SFD can have hysteresis digitally programmed into them to ensure smooth transitions but further deglitching is provided by the glitch filter stage. A fault must be asserted for greater than the programmed Glitch Filter timeout before it is seen at the output of the glitch filter. The max. programmable timeout period is 100μs. Both edges of the input are filtered by the same amount of time, so if the input pulse is longer than the glitch filter timeout and is seen at the output, the length of the output pulse is the same as the input pulse. If the input pulse is shorter than the programmed timeout, then nothing appears at the output. Figure 2 shows the implementation of glitch filtering.
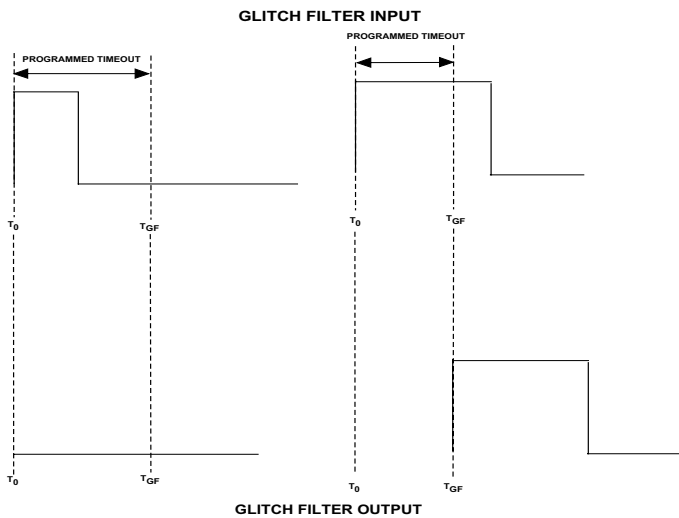
ADM1060 INPUTS — ADM1060

GLITCH FILTER INPUT

GLITCH FILTER OUTPUT

Figure 3 . Glitch Filtering on the SFD's

PROGRAMMING THE SFD'S ON THE SMBUS

The details of using the SMBus are described later, but the register names associated with the Supply Fault Detector blocks, the bitmap of those registers, and the function of each of the bits is described in the following tables. The tables show how to set up UV threshold, UV hysteresis, OV threshold, OV hysteresis, glitch filtering and fault type for each of the SFD's on the ADM1060.

SFD REGISTER NAMES

TABLE 2. LIST OF REGISTERS FOR THE SUPPLY FAULT DETECTORS

Hex Address	Table	Name	Default Power On Value	Description
A0	3	BS1OVTH	FFh	Overvoltage Threshold for Bipolar Voltage SFD1 (BS1SFD)
A1	4	BS1OVHYST	00h	Digital Hysteresis on OV threshold for BS1SFD
A2	5	BS1UVTH	00h	Undervoltage Threshold for BS1SFD
A3	6	BS1UVHYST	00h	Digital Hysteresis on UV threshold for BS1SFD
A4	7	BS1SEL	00h	Glitch filter, Range and Fault Type select for BS1SFD
A8	3	BS2OVTH	FFh	Overvoltage Threshold for Bipolar Voltage SFD2 (BS2SFD)
A9	4	BS2OVHYST	00h	Digital Hysteresis on OV threshold for BS2SFD
AA	5	BS2UVTH	00h	Undervoltage Threshold for BS2SFD
AB	6	BS2UVHYST	00h	Digital Hysteresis on UV threshold for BS2SFD
AC	7	BS2SEL	00h	Glitch filter, Range and Fault Type select for BS2SFD
B0	8	HSOVTH	FFh	Overvoltage Threshold for High Voltage SFD (HVSFD)
B1	9	HSOVHYST	00h	Digital Hysteresis on OV threshold for HVSFD
B2	10	HSUVTH	00h	Undervoltage Threshold for HVSFD
B3	11	HSUVHYST	00h	Digital Hysteresis on UV threshold for HVSFD
B4	12	HSSEL	00h	Glitch filter, Range and Fault Type select for HVSFD
B8	13	PS1OVTH	FFh	Overvoltage Threshold for Positive Voltage SFD1 (PS1SFD)
B9	14	PS1OVHYST	00h	Digital Hysteresis on OV threshold for PS1SFD
BA	15	PS1UVTH	00h	Undervoltage Threshold for PS1SFD
BB	16	PS1UVHYST	00h	Digital Hysteresis on UV threshold for PS1SFD
BC	17	PS1SEL	00h	Glitch filter, Range and Fault Type select for PS1SFD
C0	13	PS2OVTH	FFh	Overvoltage Threshold for Positive Voltage SFD2 (PS2SFD)
C1	14	PS2OVHYST	00h	Digital Hysteresis on OV threshold for PS2SFD

TABLE 2. LIST OF REGISTERS FOR THE SUPPLY FAULT DETECTORS (Contd.)

Hex Address	Table	Name	Default Power On Value	Description
C2	15	PS2UVTH	00h	Undervoltage Threshold for PS2SFD
C3	16	PS2UVHYST	00h	Digital Hysteresis on UV threshold for PS2SFD
C4	17	PS2SEL	00h	Glitch filter, Range and Fault Type select for PS2SFD
C8	13	PS3OVTH	FFh	Overvoltage Threshold for Positive Voltage SFD3 (PS3SFD)
C9	14	PS3OVHYST	00h	Digital Hysteresis on OV threshold for PS3SFD
CA	15	PS3UVTH	00h	Undervoltage Threshold for PS3SFD
CB	16	PS3UVHYST	00h	Digital Hysteresis on UV threshold for PS3SFD
CC	17	PS3SEL	00h	Glitch filter, Range and Fault Type select for PS3SFD
D0	13	PS4OVTH	FFh	Overvoltage Threshold for Positive Voltage SFD4 (PS4SFD)
D1	14	PS4OVHYST	00h	Digital Hysteresis on OV threshold for PS4SFD
D2	15	PS4UVTH	00h	Undervoltage Threshold for PS4SFD
D3	16	PS4UVHYST	00h	Digital Hysteresis on UV threshold for PS4SFD
D4	17	PS4SEL	00h	Glitch filter, Range and Fault Type select for PS4SFD

SFD REGISTER BITMAPS

BIPOLAR SUPPLY FAIL DETECT (BSnSFD) REGISTERS

TABLE 3. REGISTER A0H,A8H BSnOVTH (POWER- ON DEFAULT FFH)

Bit	Name	R/W	Description
7-0	OV7-OV0	R/W	8 bit digital value for overvoltage threshold on BSn SFD.

TABLE 4. REGISTER A1H,A9H BSnOVHYST (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	N/A	Cannot be used
4-0	HY4-HY0	R/W	5 bit digital value for hysteresis on OV threshold of BSn SFD

TABLE 5. REGISTER A2H,AAH BSnUVTH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-0	UV7-UV0	R/W	8 bit digital value for undervoltage threshold on BSn SFD

TABLE 6. REGISTER A3H,ABH BSnUVHYST (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	N/A	Cannot be used
4-0	HY4-HY0	R/W	5 bit digital value for hysteresis on UV threshold of BSn SFD

TABLE 7. REGISTER A4H,ACH BSnSEL (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	POL	R/W	Polarity of Bipolar SFDn
			POL **Sign of Detection Range**
			0 Positive
			1 Negative
6-4	GF2-GF0	R/W	**GF2** **GF1** **GF0** **Glitch Filter Delay (μs)**
			0 0 0 0
			0 0 1 5
			0 1 0 10
			0 1 1 20
			1 0 0 30
			1 0 1 50
			1 1 0 75
			1 1 1 100
3	Reserved	N/A	Cannot be used
2	RSEL	R/W	**Note:** When POL is set to 1 (ie) SFD is in negative mode, then RSEL is unused since there is only one range in this mode.
			RSEL1 **Bottom of Range** **Top of Range** **Step Size (mV)**
			0 1V 3V 7.8
			1 2V 6V 15.6
1-0	FS1-FS0	R/W	**FS1** **FS0** **Fault Select Type**
			0 0 Overvoltage
			0 1 Undervoltage
			1 0 Out-of-Window
			1 1 Not Allowed

HIGH VOLTAGE SUPPLY FAULT DETECT (HVSFD) REGISTERS

TABLE 8. REGISTER B0H HSOVTH (POWER- ON DEFAULT FFH)

Bit	Name	R/W	Description
7-0	OV7-OV0	R/W	8 bit digital value for overvoltage threshold on HV SFD.

TABLE 9. REGISTER B1H HSOVHYST (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	N/A	Cannot be used
4-0	HY4-HY0	R/W	5 bit digital value for hysteresis on OV threshold of HV SFD

TABLE 10. REGISTER B2H HSUVTH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-0	UV7-UV0	R/W	8 bit digital value for undervoltage threshold on HV SFD

TABLE 11. REGISTER B3H HSUVHYST (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	N/A	Cannot be used
4-0	HY4-HY0	R/W	5 bit digital value for hysteresis on UV threshold of HV SFD

TABLE 12. REGISTER B4H HSSEL (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description			
7	Reserved	N/A	Cannot be used			
6-4	GF2-GF0	R/W	GF2	GF1	GF0	Glitch Filter Delay (μs)
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	20
			1	0	0	30
			1	0	1	50
			1	1	0	75
			1	1	1	100
3	Reserved	N/A	Cannot be used			
2	RSEL	W	RSEL	Bottom of Range	Top of Range	Step Size (mV)
			0	2V	6V	15.6
			1	4.8V	14.4V	37.6
1-0	FS1-FS0	W	FS1	FS0	Fault Select Type	
			0	0	Overvoltage	
			0	1	Undervoltage	
			1	0	Out-of-Window	
			1	1	Not Allowed	

ADM1060 INPUTS	ADM1060

POSITIVE VOLTAGE SUPPLY FAULT DETECT (PSNSFD) REGISTERS

TABLE 13. REGISTER B8H,C0H,C8H,D0H PSNOVTH (POWER- ON DEFAULT FFH)

Bit	Name	R/W	Description
7-0	OV7-OV0	R/W	8 bit digital value for overvoltage threshold on PSn SFD.

TABLE 14. REGISTER B9H,C1H,C9H,D1H PSnOVHYST (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	N/A	Cannot be used
4-0	HY4-HY0	R/W	5 bit digital value for hysteresis on OV threshold of PSn SFD

TABLE 15. REGISTER BAH,C2H,CAH,D2H PSnUVTH (POWER- ON DEFAULT 00H)

Bit	Name	W	Description
7-0	UV7-UV0	R/W	8 bit digital value for undervoltage threshold on PSn SFD

TABLE 16. REGISTER BBH,C3H,CBH,D3H PSnUVHYST (POWER- ON DEFAULT 00H)

Bit	Name	W	Description
7-5	Reserved	N/A	Cannot be used
4-0	HY4-HY0	R/W	5 bit digital value for hysteresis on UV threshold of PSn SFD

TABLE 17. REGISTER BCH,C4H,CCH,D4H PSnSEL (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description					
7	Reserved	N/A	Cannot be used					
6-4	GF2-GF0	R/W	**GF2**	**GF1**	**GF0**	**Glitch Filter Delay (μs)**		
			0	0	0	0		
			0	0	1	5		
			0	1	0	10		
			0	1	1	20		
			1	0	0	30		
			1	0	1	50		
			1	1	0	75		
			1	1	1	100		
3-2	RSEL1-RESL0	R/W	**RSEL1**	**RSEL0**	**Bottom of Range**		**Top of Range**	**Step Size (mV)**
			0	0	2 V		6 V	15.6
			0	1	1 V		3 V	7.8
			1	X	0.6 V		1.8 V	4.7
1-0	FS1-FS0	R/W	**FS1**	**FS0**	**Fault Select Type**			
			0	0	Overvoltage			
			0	1	Undervoltage			
			1	0	Out-of-Window			
			1	1	Not Allowed			

–13–

WATCHDOG FAULT DETECTOR

The ADM1060 has a Watchdog Fault Detector. This can be used to monitor a processor clock to ensure normal operation. The detector monitors the WDI pin, expecting there to be a low-to-high or high to low transition within a preprogrammed period. The watchdog timeout period can be programmed from 200msec to a maximum of 12.8sec.

If no transition is detected, 2 signals are asserted. One is a latched high signal, indicating a fault has occurred. The other signal is a low- high- low pulse which can be used as a RESET signal for a processor core. The width of this pulse can be programmed (from $10\mu s$ to a maximum of 10ms). These two Watchdog signals can be selected as inputs to each of the PLB's (see PLBA section). They can also be inverted, if required (eg) if a high- low- high pulse was required by a processor to reset. Thus, a fault on the watchdog can be used to generate a pulsed or latched output on any or all of the 9 PDO's.

The latched signal can be cleared low by reading LATF1, then LATF2 across the SMBus interface (see Fault Registers section). The RAM register list and the bit map for the Watchdog Fault Detector are shown below.

TABLE 18. LIST OF REGISTERS FOR WATCHDOG FAULT DETECTOR

Hex Address	Table	Name	Default Power On Value	Description
9C	19	WDCFG	00h	Program length Watchdog timeout and length of pulsed output

TABLE 19. REGISTER 9CH WDCFG (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	R/W	Unused
4-3	PULS1-PULS0	R/W	Length of pulse outputted once the Watchdog Detector has timed out PULS1 PULS0 Pulse Length Selected (μs) 0 0 10 0 1 100 1 0 1000 1 1 10000
2-0	PER3-PER0	R/W	Watchdog Timeout Period PER2 PER1 PER0 Watchdog Timeout selected (ms) 0 0 0 Disabled 0 0 1 200 0 1 0 400 0 1 1 800 1 0 0 1600 1 0 1 3200 1 1 0 6400 1 1 1 12800

ADM1060 INPUTS   ADM1060

GENERAL PURPOSE INPUTS (GPI'S)

The ADM1060 has 4 General Purpose Logic Inputs (GPI's). These are TTL/CMOS logic level compatible. Standard logic signals can be applied to the pins (eg) RESET from reset generators, PWRGOOD signals, Fault flags, Manual Resets etc. These signals can be gated with the other inputs supervised by the ADM1060, and used to control the status of the PDO's. The inputs can be simply buffered, or a logic transition can be detected and a pulse output generated. The width of this pulse is programmable from 10μs to a maximum of 10ms. The configuration of the GPI's is shown in the register and bitmaps below.

The GPI's also feature a glitch filter, similar to that provided on the SFD's. This enables the user to ignore spurious transitions on the GPI's. For example, the glitch filter can be used to debounce a Manual Reset switch. The length of the glitch filter can also be programmed.

LOGIC STATE OF THE GPI'S (AND OTHER LOGIC INPUTS)

Each of the GPI's has a weak (10μA) pull-down current source. The current sources can be connected to the inputs by progamming the relevant bit in a register (PDEN). This enables the user to control the condition of these inputs, pulling them to GND, even when they are unused or left floating.

Note that the same pull-down function is provided for the SMBus address pins, A0 and A1 and for the WDI pin. A register is used to program which of the inputs is connected to the current sources.

TABLE 20. LIST OF REGISTERS FOR THE GENERAL PURPOSE INPUTS (GPIN)

Hex Address	Table	Name	Default Power On Value	Description
98		GPI4CFG	00h	Setup of the glitch filter delay, pulse width, level/edge detection etc. configuration of GPI4
99		GPI3CFG	00h	Setup of the glitch filter delay, pulse width, level/edge detection etc. configuration of GPI3
9A		GPI2CFG	00h	Setup of the glitch filter delay, pulse width, level/edge detection etc. configuration of GPI2
9B		GPI1CFG	00h	Setup of the glitch filter delay, pulse width, level/edge detection etc. configuration of GPI1

TABLE 21. BIT MAP FOR GPInCFG REGISTERS (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description
7	Reserved	N/A	Cannot be used
6	INVIN	R/W	If high, invert Input
5	INTYP	R/W	Determines whether a level or an edge is detected on the pin. If an edge is detected then positive pulse of programmable length is outputted INTYP Detect 0 Detect level 1 Detect edge
4-3	PULS1-0	R/W	Length of pulse outputted once an edge has been detected on input PULS1 PULS0 Pulse Length Selected (μs) 0 0 10 0 1 100 1 0 1000 1 1 10000
2-0	GF2-GF0	R/W	Length of time for which the input is ignored GF2 GF1 GF0 Glitch Filter Delay (μs) 0 0 0 0 0 0 1 5 0 1 0 10 0 1 1 20 1 0 0 30 1 0 1 50 1 1 0 75 1 1 1 100

–15–

TABLE 22. LIST OF REGISTERS FOR THE PULL- DOWN CURRENT SOURCES ON LOGIC INPUTS

Hex Table Address	Name	Default Power On Value	Description
91	PDEN	00h	Setup of the Pull- down current sources on all logic inputs. Pulls the selected input to GND

TABLE 23. BIT MAP FOR PDEN REGISTER- 91H (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	Reserved	N/A	Cannot be used
6	PDENA1	R/W	If high, then address pin A1 is pulled to GND using a 10uA pull- down current source.
5	PDENA0	R/W	If high, then address pin A0 is pulled to GND using a 10uA pull- down current source.
4	PDENWDI	R/W	If high, then WDI is pulled to GND using a $10\mu A$ pull- down current source.
3	PDENGPI4	R/W	If high, then GPI4 is pulled to GND using a $10\mu A$ pull- down current source.
2	PDENGPI3	R/W	If high, then GPI3 is pulled to GND using a $10\mu A$ pull- down current source.
1	PDENGPI2	R/W	If high, then GPI2 is pulled to GND using a $10\mu A$ pull- down current source.
0	PDENGPI1	R/W	If high, then GPI1 is pulled to GND using a $10\mu A$ pull- down current source.

PROGRAMMING ADM1060	ADM1060

PROGRAMMABLE LOGIC BLOCK ARRAY

The ADM1060 contains a Programmable Logic Block Array (PLBA). This block is the logical core of the device. The PLBA (and the PDBs- see next section) is what provides the sequencing function of the ADM1060. The assertion of the 9 Programmable Driver Outputs (PDO) is controlled by the PLBA. The PLBA comprises of 9 macrocells, 1 per PDO Channel. The main components of the macrocells are 2 Wide AND- OR gates, as shown in Figure 4. Each AND gate represents a function (A and B) which can be used independently to control the assertion of the PDO pin. There are 21 inputs to each of these AND gates. These are:-

• The logic outputs of all 7 of the Supply Fault Detectors

• The 4 GPI logic inputs

• The Watchdog fault detector (Latched and Pulsed)

• The delayed output of any of the other macrocells (the output of a macrocell cannot be an input to itself, since this would result in a non- terminating loop).

All 21 inputs are hardwired to both function A and function B AND gates. The user can then select which of these inputs controls the output. This is done using 2 control signals, IMK (a masking bit, setting it ignores the relevant input) and POL (a polarity bit, setting it inverts the input before it is applied to the AND gate). The effect of setting these bits can be seen in figure 4 below. The

inverting gate shown is an X-OR gate, resulting in the following truth table:-

POL	INPUT SIGNAL	X-OR OUTPUT
0	0	0
0	1	1
1	**0**	**1**
1	**1**	**0**

Table 25. Truth Table for PLB Input Inversion

The last 2 entries in the truth table show, that with the INVERT bit set, the X-OR output is always the inverse of the input.

Similarly, the ignore gate shown is an OR gate, resulting in the following truth table:-

IMK	INPUT SIGNAL	OR OUTPUT
0	0	0
0	1	1
1	0	1
1	1	1

Table 26 Truth Table for PLB Input Masking

It can be seen here that once the IMK bit is set the OR output is always 1, regardless of the input, thus ignoring it. Overleaf is a detailed diagram of the 21 inputs and the registers required to program them. Those shown are just for function A of PLB1 but function B and all of the functions in the other 8 PLB's are programmed exactly the same way. An Enable register allows the user to use function A or B or both. The output of functions A and/ or B is inputted to a Programmable Delay Block (PDB) where a delay can be programmed on both the rising and falling edge of an input (see next section). The output of this PDB block can be progammed to invert before one or any of the PDO pins is asserted.

The control bits for these macrocells are stored locally in latches which are loaded at power up. These latches can also be updated via the serial interface. The registers containing the macrocell control bits, and the function of each bit are defined in the tables overleaf.
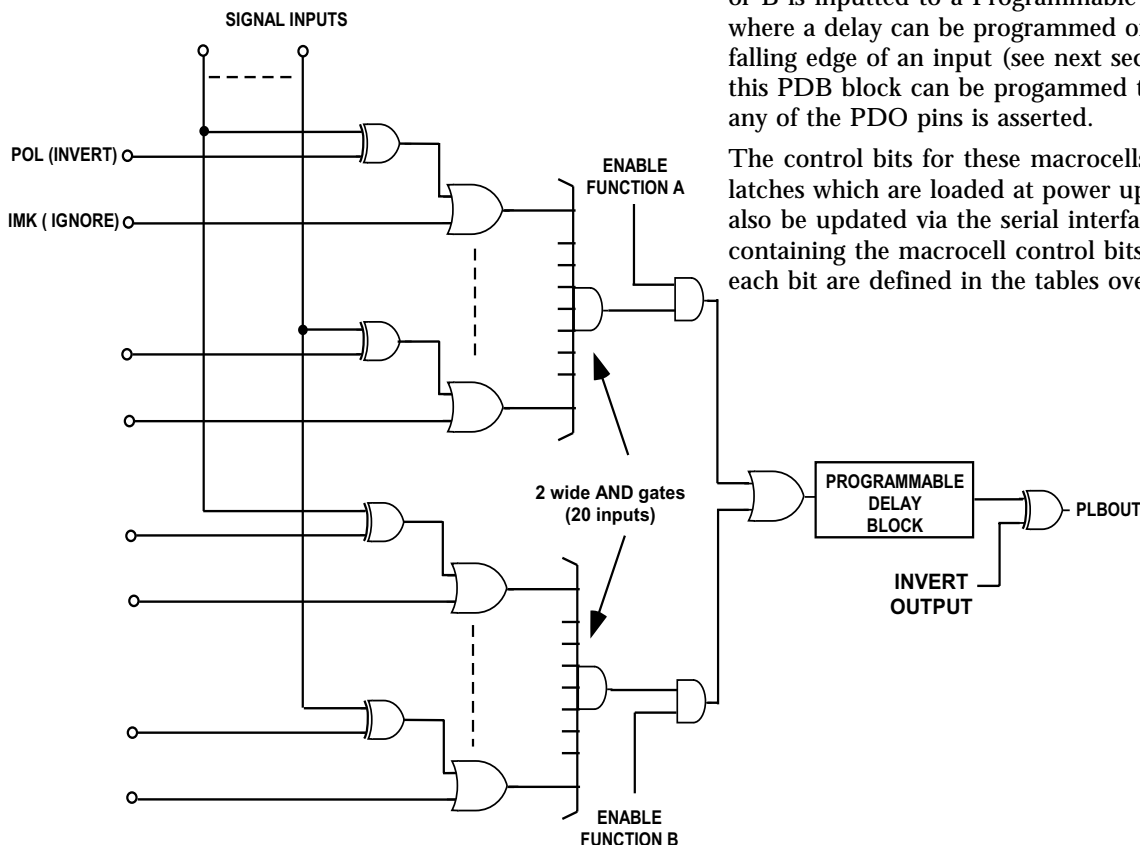

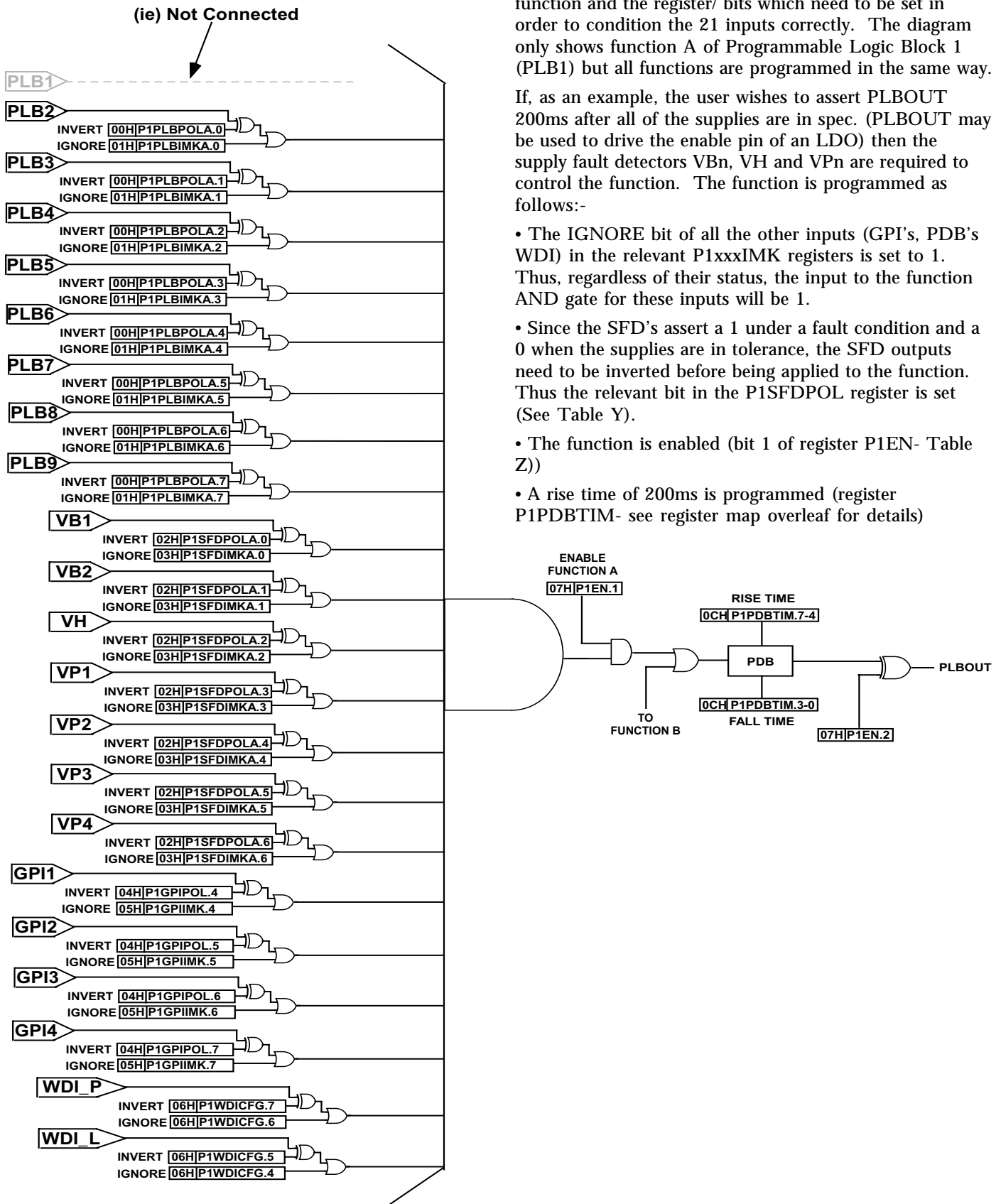*Figure 4. Simplified Programmable Logic Block Macrocell Schematic*

ADM1060

ADM1060 LOGIC

(ie) Not Connected

PLB1

PLB2
INVERT 00H P1PLBPOLA.0
IGNORE 01H P1PLBIMKA.0

PLB3
INVERT 00H P1PLBPOLA.1
IGNORE 01H P1PLBIMKA.1

PLB4
INVERT 00H P1PLBPOLA.2
IGNORE 01H P1PLBIMKA.2

PLB5
INVERT 00H P1PLBPOLA.3
IGNORE 01H P1PLBIMKA.3

PLB6
INVERT 00H P1PLBPOLA.4
IGNORE 01H P1PLBIMKA.4

PLB7
INVERT 00H P1PLBPOLA.5
IGNORE 01H P1PLBIMKA.5

PLB8
INVERT 00H P1PLBPOLA.6
IGNORE 01H P1PLBIMKA.6

PLB9
INVERT 00H P1PLBPOLA.7
IGNORE 01H P1PLBIMKA.7

VB1
INVERT 02H P1SFDPOLA.0
IGNORE 03H P1SFDIMKA.0

VB2
INVERT 02H P1SFDPOLA.1
IGNORE 03H P1SFDIMKA.1

VH
INVERT 02H P1SFDPOLA.2
IGNORE 03H P1SFDIMKA.2

VP1
INVERT 02H P1SFDPOLA.3
IGNORE 03H P1SFDIMKA.3

VP2
INVERT 02H P1SFDPOLA.4
IGNORE 03H P1SFDIMKA.4

VP3
INVERT 02H P1SFDPOLA.5
IGNORE 03H P1SFDIMKA.5

VP4
INVERT 02H P1SFDPOLA.6
IGNORE 03H P1SFDIMKA.6

GPI1
INVERT 04H P1GPIPOL.4
IGNORE 05H P1GPIIMK.4

GPI2
INVERT 04H P1GPIPOL.5
IGNORE 05H P1GPIIMK.5

GPI3
INVERT 04H P1GPIPOL.6
IGNORE 05H P1GPIIMK.6

GPI4
INVERT 04H P1GPIPOL.7
IGNORE 05H P1GPIIMK.7

WDI_P
INVERT 06H P1WDICFG.7
IGNORE 06H P1WDICFG.6

WDI_L
INVERT 06H P1WDICFG.5
IGNORE 06H P1WDICFG.4

ENABLE FUNCTION A
07H P1EN.1

RISE TIME
0CH P1PDBTIM.7-4

PDB

TO FUNCTION B

0CH P1PDBTIM.3-0
FALL TIME

07H P1EN.2

PLBOUT

The diagram shown highlights all 21 inputs to a given function and the register/ bits which need to be set in order to condition the 21 inputs correctly. The diagram only shows function A of Programmable Logic Block 1 (PLB1) but all functions are programmed in the same way.

If, as an example, the user wishes to assert PLBOUT 200ms after all of the supplies are in spec. (PLBOUT may be used to drive the enable pin of an LDO) then the supply fault detectors VBn, VH and VPn are required to control the function. The function is programmed as follows:-

• The IGNORE bit of all the other inputs (GPI's, PDB's WDI) in the relevant P1xxxIMK registers is set to 1. Thus, regardless of their status, the input to the function AND gate for these inputs will be 1.

• Since the SFD's assert a 1 under a fault condition and a 0 when the supplies are in tolerance, the SFD outputs need to be inverted before being applied to the function. Thus the relevant bit in the P1SFDPOL register is set (See Table Y).

• The function is enabled (bit 1 of register P1EN- Table Z))

• A rise time of 200ms is programmed (register P1PDBTIM- see register map overleaf for details)

Figure 5. Detailed Diagram for function A of PLB1

PLBA REGISTER NAMES
TABLE 27. LIST OF REGISTERS FOR THE PROGRAMMABLE LOGIC BLOCK ARRAY (PLBA)

Hex Address	Table	Name	Default Power On Value	Description
00	28	P1PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB1
01	29	P1PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB1
02	30	P1SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB1
03	31	P1SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB1
04	32	P1GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB1
05	33	P1GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the B function of PLB1
06	34	P1WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB1
07	35	PS1EN	00h	Enable bits for A and B functions of PLB1, polarity bit for PLB1 output
08	28	P1PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB1
09	29	P1PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB1
0A	30	P1SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB1
0B	31	P1SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB1
10	28	P2PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB2
11	29	P2PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB2
12	30	P2SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB2
13	31	P2SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB2
14	32	P2GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB2
15	33	P2GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the B function of PLB2
16	34	P2WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB2
17	35	PS2EN	00h	Enable bits for A and B functions of PLB2, polarity bit for PLB2 output
18	28	P2PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB2

TABLE 27. LIST OF REGISTERS FOR THE PROGRAMMABLE LOGIC BLOCK ARRAY (PLBA) (Contd.)

Hex Address	Table	Name	Default Power On Value	Description
19	29	P2PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB2
1A	30	P2SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB2
1B	31	P2SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB2
20	28	P3PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB3
21	29	P3PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB3
22	30	P3SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB3
23	31	P3SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB3
24	32	P3GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB3
25	33	P3GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the B function of PLB3
26	34	P3WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB3
27	35	PS3EN	00h	Enable bits for A and B functions of PLB3, polarity bit for PLB3 output
28	28	P3PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB3
29	29	P3PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB3
2A	30	P3SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB3
2B	31	P3SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB3
30	28	P4PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB1
31	29	P4PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB1
32	30	P4SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB1
33	31	P4SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB1
34	32	P4GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB1
35	33	P4GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the B function of PLB1
36	34	P4WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB4
37	35	PS4EN	00h	Enable bits for A and B functions of PLB4, polarity bit for PLB4 output

ADM1060 LOGIC   ADM1060

TABLE 27. LIST OF REGISTERS FOR THE PROGRAMMABLE LOGIC BLOCK ARRAY (PLBA) (Contd.)

Hex Address	Table	Name	Default Power On Value	Description
38	28	P4PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB4
39	29	P4PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB4
3A	30	P4SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB4
3B	31	P4SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB4
40	28	P5PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB5
41	29	P5PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB5
42	30	P5SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB5
43	31	P5SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB5
44	32	P5GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB5
45	33	P5GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the B function of PLB5
46	34	P5WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB5
47	35	PS5EN	00h	Enable bits for A and B functions of PLB5, polarity bit for PLB5 output
48	28	P5PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB5
49	29	P5PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB5
4A	30	P5SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB5
4B	31	P5SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB5
50	28	P6PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB6
51	29	P6PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB6
52	30	P6SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB6
53	31	P6SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB6
54	32	P6GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB6
55 when	33	P6GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's used as inputs to the B function of PLB6

Hex Address	Table	Name	Default Power On Value	Description

TABLE 27. LIST OF REGISTERS FOR THE PROGRAMMABLE LOGIC BLOCK ARRAY (PLBA) (Contd.)

Hex Address	Table	Name	Default Power On Value	Description
56	34	P6WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB6
57	35	PS6EN	00h	Enable bits for A and B functions of PLB6, polarity bit for PLB6 output
58	28	P6PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB6
59	29	P6PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB6
5A	30	P6SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB6
5B	31	P6SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB6
60	28	P7PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB7
61	29	P7PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB7
62	30	P7SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB7
63	31	P7SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB7
64	32	P7GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB7
65	33	P7GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the B function of PLB7
66	34	P7WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB7
67	35	PS7EN	00h	Enable bits for A and B functions of PLB7, polarity bit for PLB7 output
68	28	P7PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB7
69	29	P7PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB7
6A	30	P7SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB7
6B	31	P7SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB7
70	28	P8PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB8
71	29	P8PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB8
72	30	P8SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB8
73	31	P8SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB8
74	32	P8GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB8

ADM1060 LOGIC   ADM1060

TABLE 27. LIST OF REGISTERS FOR THE PROGRAMMABLE LOGIC BLOCK ARRAY (PLBA) (Contd.)

Hex Address	Table	Name	Default Power On Value	Description
75	33	P8GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the B function of PLB8
76	34	P8WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB8
77	35	PS8EN	00h	Enable bits for A and B functions of PLB8, polarity bit for PLB8 output
78	28	P8PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB8
79	29	P8PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB8
7A	30	P8SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB8
7B	31	P8SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB8
80	28	P9PLBPOLA	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the A function of PLB9
81	29	P9PLBIMKA	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the A function of PLB9
82	30	P9SFDPOLA	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB9
83	31	P9SFDIMKA	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the A function of PLB9
84	32	P9GPIPOL	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the A function of PLB9
85	33	P9GPIIMK	00h	Polarity Sense and Ignore Mask bits for all 4 GPI's when used as inputs to the B function of PLB9
86	34	P9WDICFG	00h	Polarity Sense and Ignore Mask bits for the pulsed and latched outputs of the watchdog detector when used as inputs to both A and B functions of PLB9
87	35	PS9EN	00h	Enable bits for A and B functions of PLB9, polarity bit for PLB9 output
88	28	P9PLBPOLB	00h	Polarity Sense for all 8 other PLB outputs when used as inputs to the B function of PLB9
89	29	P9PLBIMKB	00h	Ignore Mask for all 8 other PLB outputs when used as inputs to the B function of PLB9
8A	30	P9SFDPOLB	00h	Polarity Sense for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB9
8B	31	P9SFDIMKB	00h	Ignore Mask for all 7 SFD inputs (VH, 2 VB, 4 VP's) to the B function of PLB9

PLBA REGISTER BITMAPS

TABLE 28. BIT MAP FOR PnPLBPOLA/PnPLBPOLB REGISTERS (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description								
7-0	POL9-POL1	R/W	If high, **invert** the **PLBn** input before it is used in function A or B								
			PLB1	**PLB2**	**PLB3**	**PLB4**	**PLB5**	**PLB6**	**PLB7**	**PLB8**	**PLB9**
	Function A		00H	10H	20H	30H	40H	50H	60H	70H	80H
	Function B		08H	18H	28H	38H	48H	58H	68H	78H	88H
7			PLB9	PLB9	PLB9	PLB9	PLB9	PLB9	PLB9	PLB9	PLB8
6			PLB8	PLB8	PLB8	PLB8	PLB8	PLB8	PLB8	PLB7	PLB7
5			PLB7	PLB7	PLB7	PLB7	PLB7	PLB7	PLB6	PLB6	PLB6
4			PLB6	PLB6	PLB6	PLB6	PLB6	PLB5	PLB5	PLB5	PLB5
3			PLB5	PLB5	PLB5	PLB5	PLB4	PLB4	PLB4	PLB4	PLB4
2			PLB4	PLB4	PLB4	PLB3	PLB3	PLB3	PLB3	PLB3	PLB3
1			PLB3	PLB3	PLB2	PLB2	PLB2	PLB2	PLB2	PLB2	PLB2
0			PLB2	PLB1	PLB1	PLB1	PLB1	PLB1	PLB1	PLB1	PLB1

TABLE 29. BIT MAP FOR PnPLBIMKA/PnPLBIMKB REGISTERS (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description								
7-0	IGN9-IGN1	R/W	If high, **mask** the **PLBn** input before it is used in function A or B								
			PLB1	**PLB2**	**PLB3**	**PLB4**	**PLB5**	**PLB6**	**PLB7**	**PLB8**	**PLB9**
	Function A		01H	11H	21H	31H	41H	51H	61H	71H	81H
	Function B		09H	19H	29H	39H	49H	59H	69H	79H	89H
7			PLB9	PLB9	PLB9	PLB9	PLB9	PLB9	PLB9	PLB9	PLB8
6			PLB8	PLB8	PLB8	PLB8	PLB8	PLB8	PLB8	PLB7	PLB7
5			PLB7	PLB7	PLB7	PLB7	PLB7	PLB7	PLB6	PLB6	PLB6
4			PLB6	PLB6	PLB6	PLB6	PLB6	PLB5	PLB5	PLB5	PLB5
3			PLB5	PLB5	PLB5	PLB5	PLB4	PLB4	PLB4	PLB4	PLB4
2			PLB4	PLB4	PLB4	PLB3	PLB3	PLB3	PLB3	PLB3	PLB3
1			PLB3	PLB3	PLB2	PLB2	PLB2	PLB2	PLB2	PLB2	PLB2
0			PLB2	PLB1	PLB1	PLB1	PLB1	PLB1	PLB1	PLB1	PLB1

TABLE 30. BIT MAP FOR PnSFDPOLA/PnSFDPOLB REGISTERS (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description								
7	Reserved	N/A	Cannot be used								
6-0	POL7-POL1	R/W	If high, **invert** the **SFDn** input before it is used in function A or B								
			PLB1	**PLB2**	**PLB3**	**PLB4**	**PLB5**	**PLB6**	**PLB7**	**PLB8**	**PLB9**
	Function A		02H	12H	22H	32H	42H	52H	62H	72H	82H
	Function B		0AH	1AH	2AH	3AH	4AH	5AH	6AH	7AH	8AH
6			VP4	VP4	VP4	VP4	VP4	VP4	VP4	VP4	VP4
5			VP3	VP3	VP3	VP3	VP3	VP3	VP3	VP3	VP3
4			VP2	VP2	VP2	VP2	VP2	VP2	VP2	VP2	VP2
3			VP1	VP1	VP1	VP1	VP1	VP1	VP1	VP1	VP1

ADM1060 LOGIC   ADM1060

2	VH	VH	VH	VH	VH	VH	VH	VH	VH
1	VB2	VB2	VB2	VB2	VB2	VB2	VB2	VB2	VB2
0	VB1	VB1	VB1	VB1	VB1	VB1	VB1	VB1	VB1

TABLE 31. BIT MAP FOR PnSFDIMKA/PnSFDIMKB REGISTERS (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description								
7	Reserved	N/A	Cannot be used								
6-0	IGN7-IGN1	R/W	If high, **mask** the **SFDn** input before it is used in function A or B								
			PLB1	**PLB2**	**PLB3**	**PLB4**	**PLB5**	**PLB6**	**PLB7**	**PLB8**	**PLB9**
	Function A		**03H**	**13H**	**23H**	**33H**	**43H**	**53H**	**63H**	**73H**	**83H**
	Function B		**0BH**	**1BH**	**2BH**	**3BH**	**4BH**	**5BH**	**6BH**	**7BH**	**8BH**
6			VP4	VP4	VP4	VP4	VP4	VP4	VP4	VP4	VP4
5			VP3	VP3	VP3	VP3	VP3	VP3	VP3	VP3	VP3
4			VP2	VP2	VP2	VP2	VP2	VP2	VP2	VP2	VP2
3			VP1	VP1	VP1	VP1	VP1	VP1	VP1	VP1	VP1
2			VH	VH	VH	VH	VH	VH	VH	VH	VH
1			VB2	VB2	VB2	VB2	VB2	VB2	VB2	VB2	VB2
0			VB1	VB1	VB1	VB1	VB1	VB1	VB1	VB1	VB1

TABLE 32. BIT MAP FOR PnGPIPOL REGISTERS (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description								
7-4	APOL4-APOL1	R/W	If high, **invert** the **GPIn** input before it is used in function A								
3-0	BPOL4-BPOL1	R/W	If high, **invert** the **GPIn** input before it is used in function B								
			PLB1	**PLB2**	**PLB3**	**PLB4**	**PLB5**	**PLB6**	**PLB7**	**PLB8**	**PLB9**
			04H	**14H**	**24H**	**34H**	**44H**	**54H**	**64H**	**74H**	**84H**
7	**Function A**		GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1
6			GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2
5			GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3
4			GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4
3	**Function B**		GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1
2			GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2
1			GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3
0			GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4

TABLE 33. BIT MAP FOR PNGPIIMK REGISTERS (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description								
7-4	AIMK4-AIMK1	R/W	If high, **mask** the **GPIn** input before it is used in function A								
3-0	BIMK4-BIMK1	R/W	If high, **mask** the **GPIn** input before it is used in function B								
			PLB1	**PLB2**	**PLB3**	**PLB4**	**PLB5**	**PLB6**	**PLB7**	**PLB8**	**PLB9**
			05H	**15H**	**25H**	**35H**	**45H**	**55H**	**65H**	**75H**	**85H**
7	**Function A**		GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1
6			GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2
5			GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3
4			GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4
3	**Function B**		GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1	GPI1
2			GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2	GPI2
1			GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3	GPI3
0			GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4	GPI4

TABLE 34. PnWDICFG REGISTERS 06H,16H,26H,36H,46H,56H,66H,76H,86H (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	APOLP	R/W	If high, invert the pulsed WDI input before it is used in function A
6	AIMKP	R/W	If high, mask the pulsed WDI input before it is used in function A
5	APOLL	R/W	If high, invert the latched WDI input before it is used in function A
4	AIMKL	R/W	If high, mask the latched WDI input before it is used in function A
3	BPOLP	R/W	If high, invert the pulsed WDI input before it is used in function B
2	BIMKP	R/W	If high, mask the pulsed WDI input before it is used in function B
1	BPOLL	R/W	If high, invert the latched WDI input before it is used in function B
0	BIMKL	R/W	If high, mask the latched WDI input before it is used in function B

TABLE 35. PnEN REGISTERS 07H,17H,27H,37H,47H,57H,67H,77H,87H (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-3	Reserved	N/A	Cannot be used
2	INVOP	R/W	If high, invert the PLB output
1	ENA	R/W	If high, enable function A
0	ENB	R/W	If high, enable function B

ADM1060 LOGIC   ADM1060

PROGRAMMABLE DELAY BLOCK

Each output of the PLBA is fed into a separate Programmable Delay Block (PDB). The PDB enables the user to add a delay to the logic block output before it is applied to either a PDO or one of the other PLB's (the output of a PLB can be the input to any of the other PLB's- not itself). The PDB operation is similar to that of the glitch filter (discussed in the SFD section). There is an important difference between the 2 functions, however. The delay on the falling edge of an input to the PDB can be programmed independently of the rising edge. This allows the user to program the length of the pulse outputted from the PDB. Thus, for instance, the width of the pulse from the Watchdog Fault Detector can be adjusted, or the user can ensure that a supply supervised by one of the SFD's is within its UV/OV range for a programmed period of time before asserting a PDO. A delay of between 0ms and 500ms can be programmed in the PnPDBTIM registers. 4 bits each are used to program the rising edge and falling edge. Once programmed, the PDB operates as follows. If the user programs a delay on the rising edge of, say, 200ms, the PDB looks for a rising edge on the input. Once it sees the edge it starts a timer. If the input remains high and the timer reaches 200ms, then the PDB immediately outputs a rising edge. If the input falls low before the timer has reached 200ms then no edge is outputted from the PDB and the timer is reset. Because there is separate control over the falling edge, if no delay is programmed on the falling edge, the delay defaults to 0 and a falling edge on the input will immediately appear on the output. If a falling edge delay is programmed, then the PDB operates exactly the opposite to the way it does for a rising edge. Again, if a delay of, say, 200ms is programmed on the falling edge, the PDB looks for a falling edge on the input. Once it sees the edge, it again starts a timer. If the input remains low and the timer reaches 200ms, then the output transitions from high to low. A valid rising edge must appear at the output before a falling edge delay can be activated. The function of the PDB is illustrated in figure 6 below.

Aside from the extra timing flexibility offered, the programmable delay also provides a crude form of filtering. In much the same way as the Glitch Filter operates, an input must be high (or low) for a programmed period of time before being seen on the output. Transients which are shorter that the programmed timeouts will not appear on the output. The bitmap for the register which controls both the rising and falling edges is shown overleaf:-
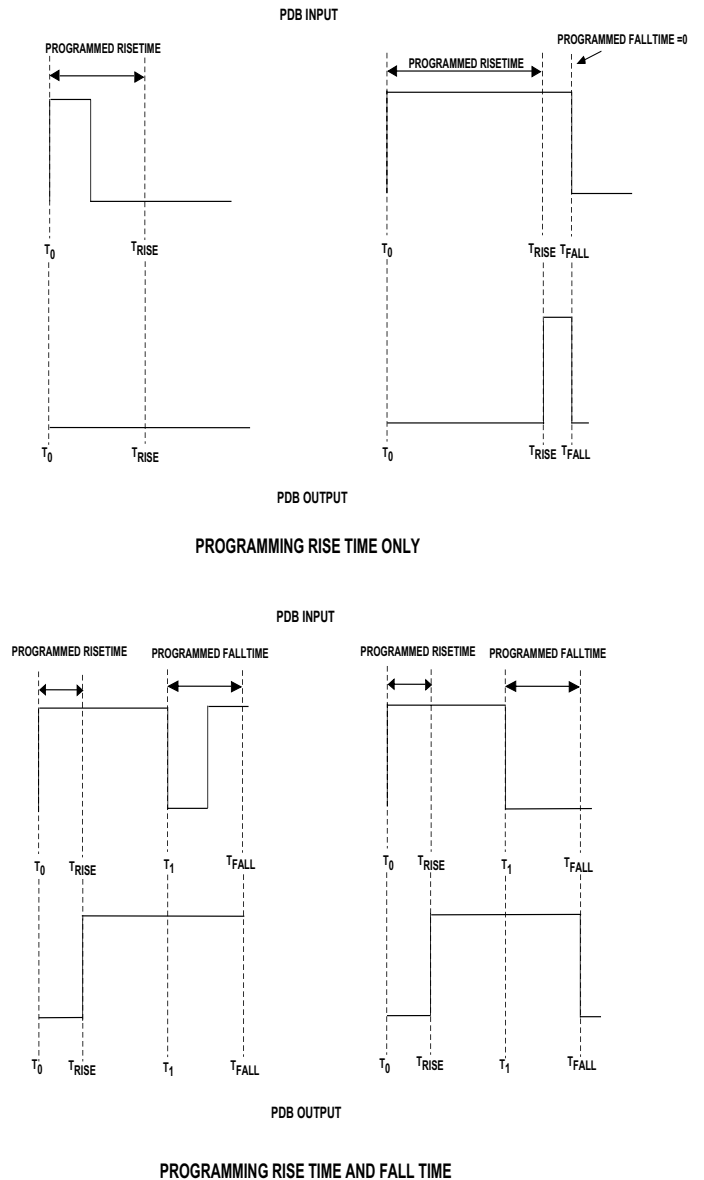
Figure 6. Functionality of the Programmable Delay Block (PDB)

TABLE 36. LIST OF REGISTERS FOR PROGRAMMABLE DELAY BLOCK (PDB)

Hex Addr.	Table	Name	Default Power On Value	Description
0 C	37	P1PDBTIM	00h	Delay for PDB1. Delay for rising edge and falling edge programmed separately.
1 C	37	P2PDBTIM	00h	Delay for PDB2. Delay for rising edge and falling edge programmed separately.
2 C	37	P3PDBTIM	00h	Delay for PDB3. Delay for rising edge and falling edge programmed separately.
3 C	37	P4PDBTIM	00h	Delay for PDB4. Delay for rising edge and falling edge programmed separately.
4 C	37	P5PDBTIM	00h	Delay for PDB5. Delay for rising edge and falling edge programmed separately.
5 C	37	P6PDBTIM	00h	Delay for PDB6. Delay for rising edge and falling edge programmed separately.
6 C	37	P7PDBTIM	00h	Delay for PDB7. Delay for rising edge and falling edge programmed separately.
7 C	37	P8PDBTIM	00h	Delay for PDB8. Delay for rising edge and falling edge programmed separately.
8 C	37	P9PDBTIM	00h	Delay for PDB9. Delay for rising edge and falling edge programmed separately.

TABLE 37. PnPDBTIM REGISTERS 0Ch,1CH,2CH,3CH,4CH,5CH,6CH,7CH,8CH

Bit	Name	R/W	Description
7-4	TR3-TR0	W	Programmed Rise Time
3-0	TF3-TF0	W	Programmed Fall Time

TR3	TR2	TR1	TR0	Delay(ms)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	5
0	1	0	0	10
0	1	0	1	20
0	1	1	0	40
0	1	1	1	60
1	0	0	0	80
1	0	0	1	100
1	0	1	0	150
1	0	1	1	200
1	1	0	0	250
1	1	0	1	300
1	1	1	0	400
1	1	1	1	500

TF3	TF2	TF1	TF0	Delay(ms)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	5
0	1	0	0	10
0	1	0	1	20
0	1	1	0	40
0	1	1	1	60
1	0	0	0	80
1	0	0	1	100
1	0	1	0	150
1	0	1	1	200
1	1	0	0	250
1	1	0	1	300
1	1	1	0	400
1	1	1	1	500

ADM1060 OUTPUTS   ADM1060

PROGRAMMABLE DRIVER OUTPUTS

The ADM1060 has 9 Programmable Driver Outputs (PDO's). These are the logic outputs of the device. Each PDO is normally controlled by a PDB. Thus, the PDO's can be set up assert when the conditions on the PDB are met (eg) the SFD's are in tolerance, the levels on the GPI are correct, the Watchdog timer has not timed out etc. The PDO's can be used for a number of functions (eg) provide a POWER_GOOD signal when all the SFD's are in tolerance, provide a reset generator output if one of the SFD's goes out of spec. (which can be used as a status signal for a DSP or other microprocessor), provide enable signals for LDO's on the supplies that the ADM1060 is supervising etc.

There are a number of pull up options on the PDO's to enable the user to program the output level.

The outputs can be programmed to be:-
• Open Drain (allows the user to connect an external pull- up resistor)
• Open Drain with weak internal pull-up to V_{DD}
• Open Drain with strong internal pull-up to V_{DD}
• Open Drain with weak internal pull-up to VP_n
• Open Drain with strong internal pull-up to VP_n
• Internally charge-pumped high drive (+12V)

The last option is only available on PDO1- 4. This allows the user to directly drive the gate of an N- Channel FET in the path of a power supply. The required pull- up is selected by programming bits 0 to 3 in PnPDOCFG appropriately (see table overleaf).

The data driving each of the PDO's can come from one of 3 inputs. These inputs are enabled by a bit each in the PnPDOCFG registers. The inputs are:-

• The (delayed) output from the associated PLB (enabled by setting bit CFG4 to 1)

• Data which is driven directly over the SMBus interface (enabled by setting bit CFG5 to1). When set in this mode, the data from the PDB is disabled and the data on the PDO is the data on CFG4. Thus the PDO can be software controlled (eg) to initiate a software power up/ powerdown.

• An On- Chip Clock (enabled by setting bit CFG6 to1). A 100KHz clock is available to clock an external device (eg) a LED.

More detail of these data modes is given in the register map overleaf.

The default setup of each of the PDO's is to be pulled low by a weak (20kΩ) pulldown resistor. This is also the setup of the PDO's on power- up until the registers are loaded and the programmed conditions are latched. The outputs are actively pulled low once 1V or greater is seen at any of VPn or VH. Until there is a 1V supply on the chip the outputs are high impedance. This provides a known condition for the PDO's during power- up. The pulldown can be overdriven if required (eg) tie an external pull- up resistor to the PDO to ensure that the gate of a PMOS device was not turned on.

The register list and the bit map for the PDO's is shown below.
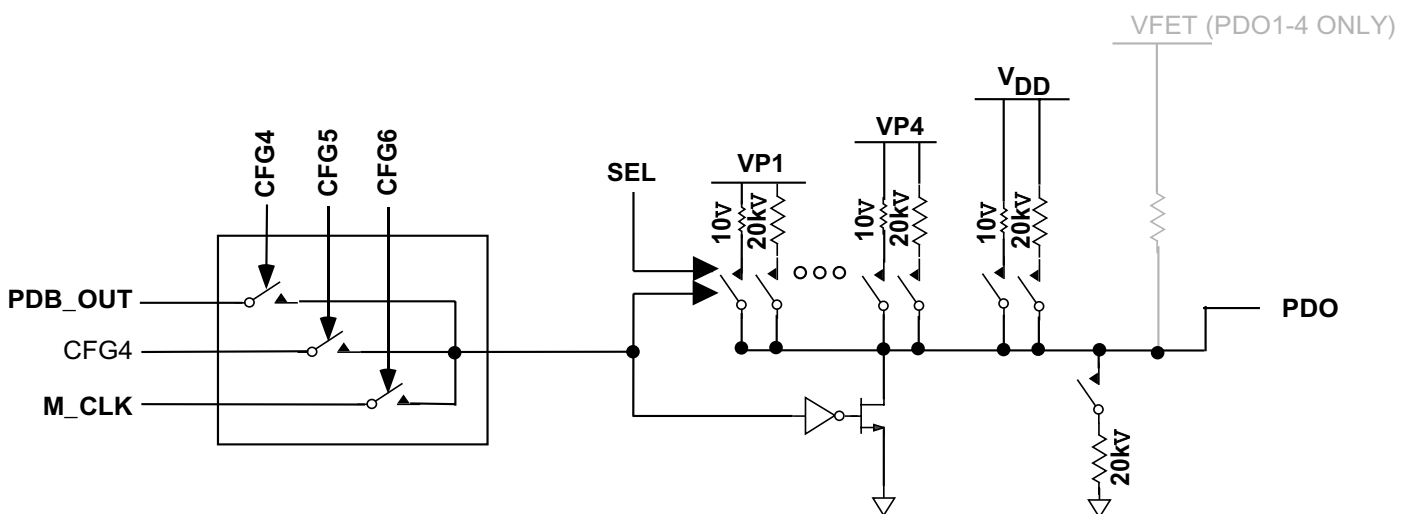
Figure 7. Programmable Driver Output

TABLE 38. LIST OF REGISTERS FOR THE PROGRAMMABLE DRIVER OUTPUTS

Hex Address	Table	Name	Default Power On Value	Description
0D	39	P1PDOCFG	00h	Selects the format of the PDO1 output (open drain, open drain with internal pull-up, charge pumped etc.)
1D	39	P2PDOCFG	00h	Selects the format of the PDO2 output (open drain, open drain with internal pull-up, charge pumped etc.)
2D	39	P3PDOCFG	00h	Selects the format of the PDO3 output (open drain, open drain with internal pull-up, charge pumped etc.)
3D	39	P4PDOCFG	00h	Selects the format of the PDO4 output (open drain, open drain with internal pull-up, charge pumped etc.)
4D	39	P5PDOCFG	00h	Selects the format of the PDO5 output (open drain, open drain with internal pull-up etc.). **Note: Charge Pumped output is not available on this driver**
5D	39	P6PDOCFG	00h	Selects the format of the PDO6 output (open drain, open drain with internal pull-up etc.). **Note: Charge Pumped output is not available on this driver**
6D	39	P7PDOCFG	00h	Selects the format of the PDO7 output (open drain, open drain with internal pull-up etc.). **Note: Charge Pumped output is not available on this driver**
7D	39	P8PDOCFG	00h	Selects the format of the PDO8 output (open drain, open drain with internal pull-up etc.). **Note: Charge Pumped output is not available on this driver**
8D	39	P9PDOCFG	00h	Selects the format of the PDO9 output (open drain, open drain with internal pull-up etc.). **Note: Charge Pumped output is not available on this driver**

TABLE 39. REGISTER 0DH,1DH,2DH,3DH,4DH,5DH,6DH,7DH,8DH PnPDOCFG (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	Reserved	N/A	Cannot be used
6-4	CFG6-CFG4	R/W	Control the logical state of the PDO. These three bits deter mine what effect, if any, the logical input to the PDO has on its output

CFG6	CFG5	CFG4	PDO	State
0	0	0	0	Disabled, with weak pull-down
0	0	1	PLB_OUT	Enabled, follows PLB Logic Output
0	1	0	0	Enable SMBus Data, Drive Low
0	1	1	1	Enable SMBus Data, Drive High
1	X	X	MCLK	Enable MCLK out onto pin

Bit	Name	R/W	CFG3	CFG2	CFG1	CFG0	Pull-Up Supply	Pull-Up Strength
3-0	CFG3-CFG0	R/W	0	0	0	X	none	N/A
			0	0	1	X	VCP	(1/fC)
			0	1	0	0	VP1	Low
			0	1	0	1	VP1	High
			0	1	1	0	VP2	Low
			0	1	1	1	VP2	High
			1	0	0	0	VP3	Low
			1	0	0	1	VP3	High
			1	0	1	0	VP4	Low
			1	0	1	1	VP4	High
			1	1	1	0	VDD	Low
			1	1	1	1	VDD	High

ADM1060 STATUS/FAULTS   ADM1060

FAULT/STATUS REPORTING ON THE ADM1060

As discussed in the last section, any one, a number or all of the PDO's can be programmed to assert under a set of pre- programmed conditons. These conditions could be a fault on a SFD, a change in status on a GPI, a timeout on the watchdog detector etc. Because of the flexibility and the choice of combinations available on the ADM1060, the assertion of the PDO will tell the user nothing about what caused it to assert (unless it is programmed to assert with only one input).

To enable the user to debug the cause of the PDO assertion, a number of registers are provided on the ADM1060 which provide status and fault information on the various individual functions supervised by the device.

STATUS REGISTERS

A number of Status Registers are provided which indicate the logic state of all of the functions controlled by the ADM1060. These logics states include the output of both the UV and OV comparators of each of the 7 SFD's, the logic output of the SFD's themselves, the logic state of the GPI's, the error condition on the WDI, and the logic state of each of the 9 PDO's. The contents of these registers can be read at any time via the SMBus interface. The content of these registers is read- only. The register and bitmap for each of these status registers is described in the table overleaf.

FAULT REGISTERS

Fault reporting is also provided on the ADM1060. If a fault occurs, causing, say, a PDO to change its status, the user can determine what function actually faulted. This is achieved by providing a "fault plane", consisting of 2 registers, LATF1 and LATF2, which the system controller can read out of the ADM1060 via the SMBus. Each bit in the 2 registers (with one important exception, see below) is assigned to one of the inputs of the devices as shown in the table below:-

REGISTER	BIT	ASSIGNED FUNCTION
LATF1	7	ANYFLT
	6	Logic Output of VP4's SFD
	5	Logic Output of VP3's SFD
	4	Logic Output of VP2's SFD
	3	Logic Output of VP1's SFD
	2	Logic Output of VH's SFD
	1	Logic Output of VB2's SFD
	0	Logic Output of VB1's SFD
LATF2	7	-
	6	-
	5	-
	4	Logic Output of WDI
	3	Logic Input on GPI4
	2	Logic Input on GPI3
	1	Logic Input on GPI2
	0	Logic Input on GPI1

Table 25. Fault Plane of ADM1060

Each bit represents the logical status of its assigned function (ie) the logical output of the SFD's and WDI and the logic level on the GPI inputs.

The important exception is the MSB of the LATF1 register. This is the ANYFLT bit. This bit goes high if one of the other bits in the 2 registers "faults". A "fault" is defined as a change in polarity from the last time the fault registers were read. Once ANYFLT goes high the contents of the 2 registers are latched, thus preventing more than 1 of the other bits from changing polarity before the contents of the registers are read. The first faulting input can, therefore, be determined.

The sequence in which the registers are read is determined by ANYFLT. As long as ANYFLT remains at 0, only the contents of LATF1 are read. There are 2 reasons for this. The first is that ANYFLT=0 implies that no fault has occurred and, therefore, there is no need to read the contents of LATF2. Secondly, and more importantly, reading register LATF2 actually resets the ANYFLT bit to 0. Thus, if a fault occurred on an SFD after LATF1 had been read but before LATF2 had been read, ANYFLT would change to 1, indicating that a fault had occurred, but would be reset to 0 once LATF2 was read, thus erasing the log of the fault. In summary then, LATF2 should only ever be read if ANYFLT=1. Reading the registers in this sequence ensures that the contents are never reset before a fault has been logged over the SMBus, thus ensuring that the supervising processor or CPLD knows what function supervised by the ADM1060 caused the fault. The "faulting" function is determined by comparing the contents of the fault plane (ie) the contents of the 2 registers, with the values read previously, and determining which bit changed polarity.

The functionality of the Fault Plane is best illustrated with an example. Take, for instance, VP1 to have an input supply of 5.0V. A UV/OV window of 4.5V to 5.5V is set up on VP1. The supply is ramped in and out of this window, each time reading the contents of LATF1 and LATF2. The values recorded are as follows:-

1. VP1 at 5V- LATF1=LATF2=00000000. This is expected. The supply is in tolerance, SFD output is 0, therefore no fault.

2. VP1 at 4.2V- LATF1=10001000, LATF2=00000000. SFD output has changed status to 1, therefore ANYFLT goes high.

3. VP1 at 5.0V- LATF1=10000000, LATF2=00000000. SFD output has changed status to 0, therefore ANYFLT goes high again.

4. VP1 at 5.8V- LATF1=10001000, LATF2=00000000. SFD output again changed status from 0 to 1, so ANYFLT goes high.

5. VP1 at 4.2V- LATF1=10000000, LATF2=00000000. At first glance, this would appear to be incorrect, since SFD output should be at 1 (4.2V is an undervoltage fault). However, in ramping down from 5.8V to 4.2V, the supply passed into the UV/OV window, the SFD output changed status from 1 to 0, ANYFLT was set high and the register contents were latched. It is these values which were read before being reset by reading LATF2.

There are also two mask registers provided, which enable the user to ignore a fault on a given function. The bits of the error mask registers are mapped in the same way as

ADM1060	ADM1060 STATUS/FAULTS

those of the fault registers with the exception that the ANYFLT bit cannot be masked. Setting a 1 in the error mask register results in the equivalent bit in the fault register always remaining at 0, regardless of whether there is a fault on that function or not. The register and bit maps for both the fault and error mask registers are shown below.

STATUS REGISTERS

TABLE 40. LIST OF STATUS REGISTERS

Hex Addr.	Table	Name	Default Power On Value	Description
D8	41	UVSTAT	00h	Logic output of the UV comparator on each of the 7 SFD's
D9	42	OVSTAT	00h	Logic output of the OV comparator on each of the 7 SFD's
DA	43	SFDSTAT	00h	Logic output (post Fault Type block) on each of the 7 SFD's
DB	44	GWSTAT	00h	Logic state of the 4 GPI's and the Watchdog Fault Detector
DE	45	PDOSTAT1	00h	Logic output of PDO's 1 to 8
DF	46	PDOSTAT2	00h	Logic output of PDO 9

TABLE 41. BIT MAP FOR UVSTAT REGISTER D8H (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	Reserved	N/A	Cannot be used
6	VP4UV	R	If high, then voltage on VP4 input is lower than the UV threshold
5	VP3UV	R	If high, then voltage on VP3 input is lower than the UV threshold
4	VP2UV	R	If high, then voltage on VP2 input is lower than the UV threshold
3	VP1UV	R	If high, then voltage on VP1 input is lower than the UV threshold
2	VHUV	R	If high, then voltage on VH input is lower than the UV threshold
1	VB2UV	R	If high, then voltage on VB2 input is lower than the UV threshold
0	VB1UV	R	If high, then voltage on VB1 input is lower than the UV threshold

TABLE 42. BIT MAP FOR OVSTAT REGISTER D9H (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	Reserved	N/A	Cannot be used
6	VP4OV	R	If high, then voltage on VP4 input is higher than the OV threshold
5	VP3OV	R	If high, then voltage on VP3 input is higher than the OV threshold
4	VP2OV	R	If high, then voltage on VP2 input is higher than the OV threshold
3	VP1OV	R	If high, then voltage on VP1 input is higher than the OV threshold
2	VHOV	R	If high, then voltage on VH input is higher than the OV threshold
1	VB2OV	R	If high, then voltage on VB2 input is higher than the OV threshold
0	VB1OV	R	If high, then voltage on VB1 input is higher than the OV threshold

ADM1060 STATUS/FAULTS | ADM1060

TABLE 43. BIT MAP FOR SFDSTAT REGISTER DAH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	Reserved	N/A	Cannot be used
6	VP4FLT	R	If high, then fault (UV, OV or Out- of- Window) has occurred on VP4 input
5	VP3FLT	R	If high, then fault (UV, OV or Out- of- Window) has occurred on VP3 input
4	VP2FLT	R	If high, then fault (UV, OV or Out- of- Window) has occurred on VP2 input
3	VP1FLT	R	If high, then fault (UV, OV or Out- of- Window) has occurred on VP1 input
2	VHFLT	R	If high, then fault (UV, OV or Out- of- Window) has occurred on VH input
1	VB2FLT	R	If high, then fault (UV, OV or Out- of- Window) has occurred on VB2 input
0	VB1FLT	R	If high, then fault (UV, OV or Out- of- Window) has occurred on VB1 input

TABLE 44. BIT MAP FOR GWSTAT REGISTER DBH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	N/A	Cannot be used
4	WDISTAT	R	If high, then timeout has elapsed on the Watchdog Detector
3	GPI4STAT	R	Logic level currently being driven on GPI4 input
2	GPI3STAT	R	Logic level currently being driven on GPI3 input
1	GPI2STAT	R	Logic level currently being driven on GPI2 input
0	GPI1STAT	R	Logic level currently being driven on GPI1 input

TABLE 45. BIT MAP FOR PDOSTAT1 REGISTER DEH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	PDO8STAT	R	Logic level currently being driven on PDO8 output
6	PDO7STAT	R	Logic level currently being driven on PDO7 output
5	PDO6STAT	R	Logic level currently being driven on PDO6 output
4	PDO5STAT	R	Logic level currently being driven on PDO5 output
3	PDO4STAT	R	Logic level currently being driven on PDO4 output
2	PDO3STAT	R	Logic level currently being driven on PDO3 output
1	PDO2STAT	R	Logic level currently being driven on PDO2 output
0	PDO1STAT	R	Logic level currently being driven on PDO1 output

TABLE 46. BIT MAP FOR PDOSTAT2 REGISTER DFH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-1	Reserved	N/A	Cannot be used
0	PDO9STAT	R	Logic level currently being driven on PDO9 output

ADM1060	ADM1060 STATUS/FAULTS

FAULT REGISTERS

TABLE 47. LIST OF FAULT REGISTERS

Hex Addr.	Table	Name	Default Power On Value	Description
DC	48	LATF1	00h	Fault Status Register for the 7 SFD's
DD	49	LATF2	00h	Fault Status Register for the 4 GPI's and the Watchdog Detector

TABLE 48. BIT MAP FOR LATF1 REGISTER DCH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	ANYFLT	R	If high, then a change in logic status (fault) has been logged on one of the 12 func-tions monitored since the last time the Fault Registers were read.
6	VP4FLT	R	If high, then a fault has occurred on supply at input VP4
5	VP3FLT	R	If high, then a fault has occurred on supply at input VP3
4	VP2FLT	R	If high, then a fault has occurred on supply at input VP2
3	VP1FLT	R	If high, then a fault has occurred on supply at input VP1
2	VHFLT	R	If high, then a fault has occurred on supply at input VH
1	VB2FLT	R	If high, then a fault has occurred on supply at input VB2
0	VB1FLT	R	If high, then a fault has occurred on supply at input VB1

TABLE 49. BIT MAP FOR LATF2 REGISTER DDH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	N/A	Cannot be used
4	WDFLT	R	If high, then the logic level on the WDI output has changed since the last time that the fault registers were read
3	GPI4FLT	R	If high, then the logic level on GPI4 input has changed since the last time that the fault registers were read
2	GPI3FLT	R	If high, then the logic level on GPI3 input has changed since the last time that the fault registers were read
1	GPI2FLT	R	If high, then the logic level on GPI2 input has changed since the last time that the fault registers were read
0	GPI1FLT	R	If high, then the logic level on GPI1 input has changed since the last time that the fault registers were read

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MASK REGISTERS

TABLE 50. LIST OF MASK REGISTERS

Hex Addr.	Table	Name	Default Power On Value	Description
9D	51	ERRMASK1	00h	Error Mask Register for the 7 SFD's
9E	52	ERRMASK2	00h	Error Mask Register for the 4 GPI's and the Watchdog Detector

TABLE 51. BIT MAP FOR ERRMASK1 REGISTER 9DH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7	Reserved	X	Unused
6	VP4MASK	R/W	If high, then a fault occurring on the supply at input VP4 is ignored, and not logged in LATF1
5	VP3MASK	R/W	If high, then a fault occurring on the supply at input VP3 is ignored, and not logged in LATF1
4	VP2MASK	R/W	If high, then a fault occurring on the supply at input VP2 is ignored, and not logged in LATF1
3	VP1MASK	R/W	If high, then a fault occurring on the supply at input VP1 is ignored, and not logged in LATF1
2	VHMASK	R/W	If high, then a fault occurring on the supply at input VH is ignored, and not logged in LATF1
1	VB2MASK	R/W	If high, then a fault occurring on the supply at input VB2 is ignored, and not logged in LATF1
0	VB1MASK	R/W	If high, then a fault occurring on the supply at input VB1 is ignored, and not logged in LATF1

TABLE 52. BIT MAP FOR ERRMASK2 REGISTER 9EH (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-5	Reserved	X	Unused
4	WDIMASK	R/W	If high, then a change in the logic level on the WDI output is ignored, and not logged in LATF2
3	GPI4MASK	R/W	If high, then a change in the logic level on the GPI4 input is ignored, and not logged in LATF2
2	GPI3MASK	R/W	If high, then a change in the logic level on the GPI3 input is ignored, and not logged in LATF2
1	GPI2MASK	R/W	If high, then a change in the logic level on the GPI2 input is ignored, and not logged in LATF2
0	GPI1MASK	R/W	If high, then a change in the logic level on the GPI1 input is ignored, and not logged in LATF2

CONFIGURATION DOWNLOAD AT POWER- UP

The configuration of the ADM1060- the UV/OV thresholds, glitch filter timeouts, PLB combinations, PDO pullups etc, is dictated by the contents of the RAM. The RAM is comprised of local latches which set the configuration. These latches are double buffered and are actually comprised of 2 identical latches (Latch A and Latch B). An update of the double- buffered latch updates Latch A first then Latch B. The advantage of this architecture is explained below. These latches are volatile memory and lose their contents at power- down. Therefore, at power-up the configuration in the RAM must be restored. This is achieved by downoading the contents of the EEPROM (non- volatile memory) to the local latches. This download occurs in a number of steps.

1. With no power applied to the device, the PDO's are all high impedance.

2. Once 1V appears on any of the inputs connected to the VDD Arbitrator (VH or VPn), the PDO's are all (weakly) pulled to GND.

3. Once the supply rises above the Undervoltage Lockout of the device (UVLO is 2.5V), the EEPROM starts to download to the RAM.

4. The EEPROM downloads its contents to all Latch A's.

5. Once the contents of the EEPROM are completely downloaded, the device controller outputs a control pulse enabling all Latch A's to download to all Latch B's, thus completing the configuration download. Any attempt to communicate with the device prior to this download completion will result in a NACK being issued from the ADM1060.

UPDATING THE CONFIGURATION OF THE ADM1060

Once powered up, with all of the configuration settings loaded from EEPROM into the RAM registers, the user may wish to alter the configuration of functions on the ADM1060 (eg) change the UV or OV limit of an SFD, change the fault output of an SFD, change the timeout of the Watchdog Detector, change the rise time delay of one of the PDO's etc.

The ADM1060 provides a number of options which allow the user to update the configuration differently over the SMBus interface. All of these options are controlled in the register UPDCFG. The options are:-

1. Update the configuration in real time. The user writes to RAM across the SMBus and the configuration is updated immediately.

2. Update A Latches "offline" and then update all B Latches at the same time. With this method, the configuration of the ADM1060 will remain unchanged and continue to operate in the original setup until the instruction is given to update the B Latches.

3. Change EEPROM register contents "offline" and then download the revised EEPROM contents to the RAM registers. Again, with this method, the configuration of the ADM1060 will remain unchanged and continue to operate

in the original setup until the instruction is given to change.

The instruction to download from the EEPROM in option 3 above is also a useful way to restore the original EEPROM contents if revisions to the configuration are unsatisfactory to the user and they wish the ADM1060 to return to a known operating mode.

This type of operation is possible because of the topology of the ADM1060. The Local (volatile) registers, or RAM, are all double buffered latches. Setting bit 0 of the UPDCFG register to 1 leaves the double buffered latches open at all times. If bit 0 is set to 0, then when RAM write occurs across the SMBus only the first side of the double buffered latch is written to. The user must then write a 1 to bit 1 of the UPDCFG register. This generates a pulse to update all of the second latches at once. Similarly with EEPROM writes.

A final bit in this register is used to enable EEPROM page erasure. If this bit is set high, then the contents of an EEPROM page can all be set to 0. If low, then the contents of a page cannot be erased, even if the command code for page erasure is programmed across the SMBus.

The bitmap for register UPDCFG is shown below. A flow chart for download at power up and subsequent configuration updates is shown overleaf:-

PROGRAMMING ADM1060   ADM1060

TABLE 52. LIST OF CONFIGURATION UPDATE REGISTERS

Hex Addr.	Table	Name	Default Power On Value	Description
90	53	UPDCFG	00h	Configuration Update Control register for changing configuration of the ADM1060 after power- up

TABLE 53. BIT MAP FOR UPDCFG REGISTER 90H (POWER- ON DEFAULT 00H)

Bit	Name	R/W	Description
7-4	Reserved	N/A	Cannot be used
3	EE_ERASE	R/W	If set high, then EEPROM page erasure can be programmed.
2	EEPROMLD	W	If set high, the ADM1060 will download the contents of its EEPROM to the RAM registers. This bit self clears (returns to 0) after the download
1	RAMLD	W	If set high, the ADM1060 will download the buffered RAM register data into the local latches. This bit self clears (returns to 0) after the download
0	UPD	R/W	If set high, the ADM1060 will update its configuration in real time as a word is written to a local RAM register via the SMBus
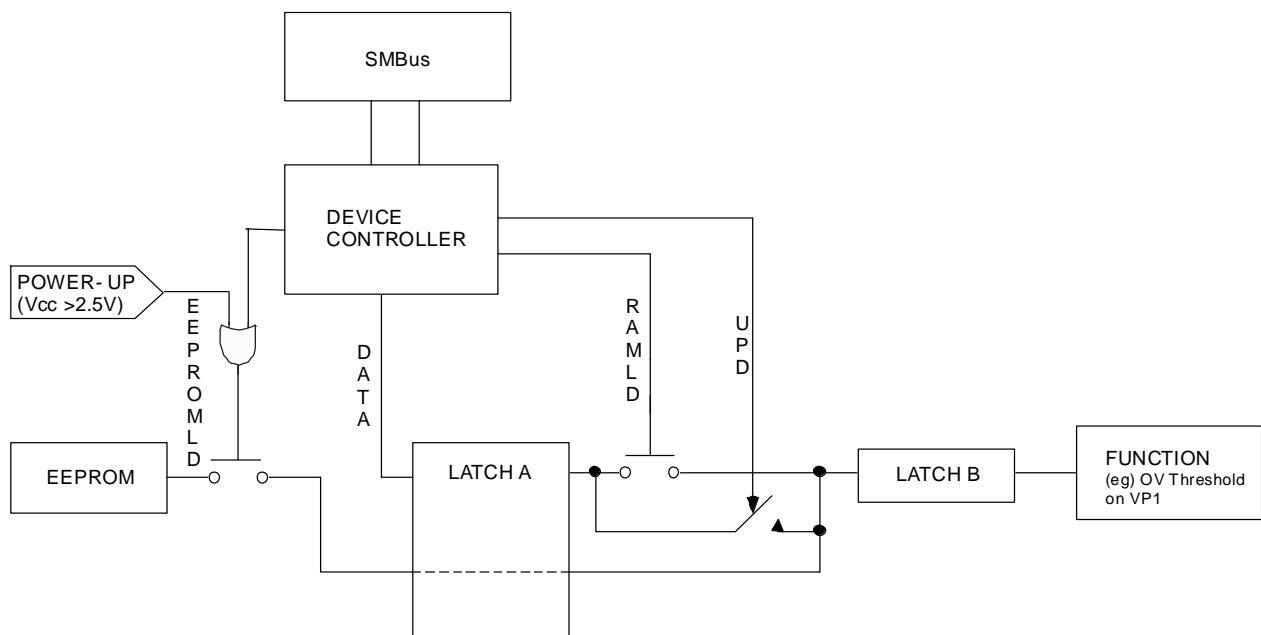
Figure 8. Configuration Update Flow Diagram

INTERNAL REGISTERS OF THE ADM1060

The ADM1060 contains a large number of data registers. A brief description of the principal registers is given below. More detailed descriptions are given in the relevant sections of the data sheet.

Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM1060, the first byte of data is always a register address, which is written to the Address Pointer Register.

Configuration Registers: Provide control and configuration for various operating parameters of the ADM1060.

Polarity Registers: These registers define the polarity of inputs to the PLBA

Mask Registers: Allow masking of individual inputs to the PLBA and also masking of faults in the fault reporting registers.

EEPROM

The ADM1060 has 512 bytes of non-volatile, Electrically-Erasable Programmable Read-Only Memory (EEPROM), from register addresses F800h to F9FFh. This may be used for permanent storage of data that will not be lost when the ADM1060 is powered down, unlike the data in the volatile registers. Although referred to as Read Only Memory, the EEPROM can be written to (as well as read from) via the serial bus in exactly the same way as the other registers. The only major differences between the E²PROM and other registers are:

1. An EEPROM location must be blank before it can be written to. If it contains data, it must first be erased.

2. Writing to EEPROM is slower than writing to RAM.

3. Writing to the EEPROM should be restricted because it has a limited write/cycle life of typically 10,000 write operations, due to the usual EEPROM wear-out mechanisms.

The EEPROM is split into 16 (0 to 15) pages of 32 Bytes each. Pages 0 to 6, starting at address F800, hold the configuration data for the applications on the ADM1060 (the PLB, SFD's, GPI's, WDI, PDO's etc.). These EEPROM addresses are the same as the RAM register addresses, prefixed by F8. Page 7 is reserved. Pages 8 to 15 are for customer use. Data can be downloaded from EEPROM to RAM in one of 2 ways:-

1. At Power- up, pages 0 to 6 are downloaded.

2. Setting bit 2 of the UPDCFG Register (90h) performs a user download of pages 0 to 6.

SERIAL BUS INTERFACE

Control of the ADM1060 is carried out via the serial System Management Bus (SMBus). The ADM1060 is connected to this bus as a slave device, under the control of a master device. It takes approximately 2ms after power up for the ADM1060 to download from it's EEPROM. Therefore access is restricted to the ADM1060 until the download is completed.

IDENTIFYING THE ADM1060 ON THE SMBUS

The ADM1060 has a 7-bit serial bus slave address. When the device is powered up, it will do so with a default serial bus address. The five MSB's of the address are set to 10101, the two LSB's are determined by the logical states of pin A1 and A0. This allows the connection of 4 ADM1060's to the one SMBus. The device also has a number of identification registers (read only) which can be read across the SMBus.   These are:-

Name	Address	Value	Function
MANID	93h	41h	Manufacturer ID for Analog Devices
DEVID	94h	3Eh	Device ID
REVID	95h	--h	Silicon Revision
MARK1	96h	--h	S/w brand
MARK2	97h	--h	S/w brand

GENERAL SMBUS TIMING

Figures 8a and 8b show timing diagrams for general read and write operations using the SMBus. The SMBus specification defines specific conditions for different types of read and write operation, which are discussed later.

The general SMBus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line SCL remains high. This indicates that a data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device (0 = write, 1 = read).

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0 then the master will write to the slave device. If the R/$\overline{W}$ bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.

PROGRAMMING ADM1060   ADM1060

If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction such as telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written.

Since data can flow in only one direction as defined by the $R/\overline{W}$ bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will release the SDA line during the low period before the 9th clock pulse, but the slave device will not pull it low. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.
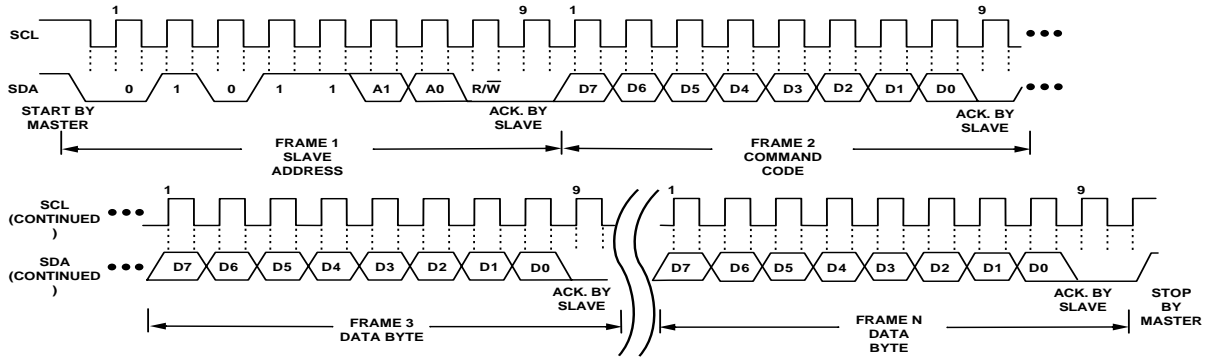
Figure 8a. General SMBus Write Timing Diagram
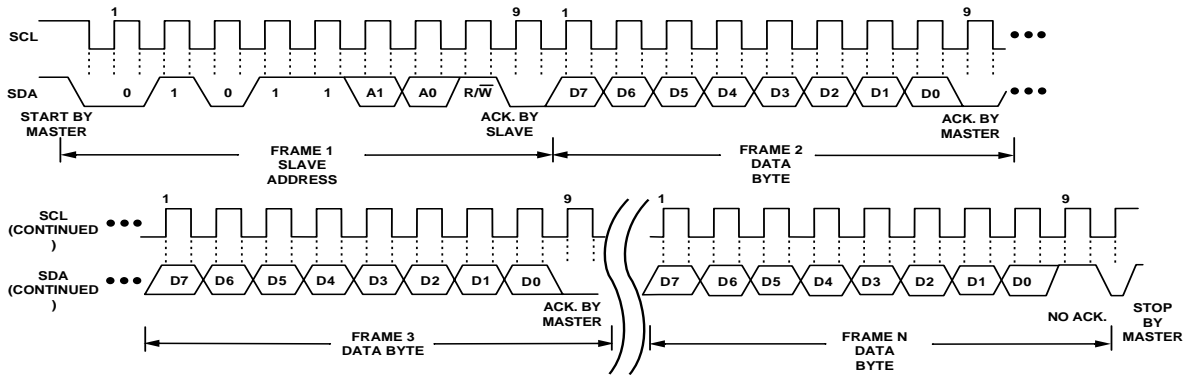
Figure 8b. General SMBus Read Timing Diagram
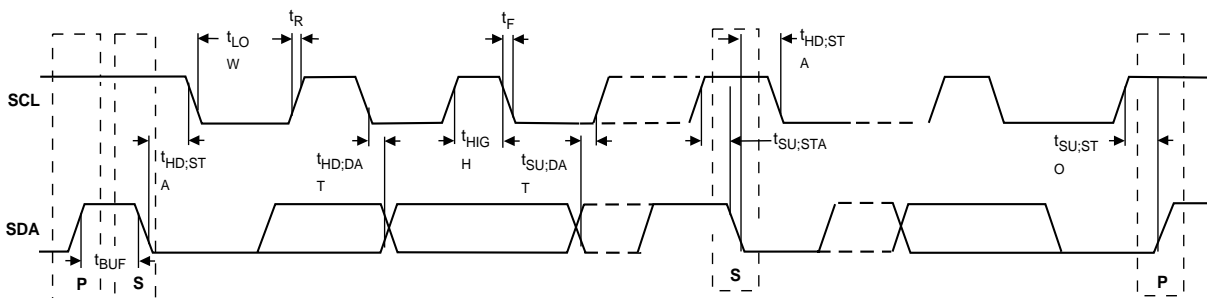
Figure 8c. Diagram for Serial Bus Timing

ADM1060   PROGRAMMING ADM1060

SMBUS PROTOCOLS FOR RAM AND EEPROM

The ADM1060 contains volatile registers (RAM) and non-volatile EEPROM. User RAM occupies address locations from 00h to DFh, whilst EEPROM occupies addresses from F800h to F9FFh.

Data can be written to and read from both RAM and EEPROM as single data bytes.

Data can only be written to unprogrammed EEPROM locations. To write new data to a programmed location it is first necessary to erase it. EEPROM erasure cannot be done at the byte level, the EEPROM is arranged as 16 pages of 32 bytes, and an entire page must be erased.

Page erasure is enabled by setting bit 3 in register UPDCFG (address 90h) to 1. If this is not set then page erasure cannot occur, even if the command byte (FEh) is programmed across the SMBus.

ADM1060 WRITE OPERATIONS

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADM1060 are discussed below. The following abbreviations are used in the diagrams:

S - START

P - STOP

R - READ

W - WRITE

A - ACKNOWLEDGE

$\overline{A}$ - NO ACKNOWLEDGE

The ADM1060 uses the following SMBus write protocols:

Send Byte

In this operation the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the ADM1060, the send byte protocol is used for two purposes.

1. To write a register address to RAM for a subsequent single byte read from the same address or block read or write starting at that address. This is illustrated in Figure 9a.
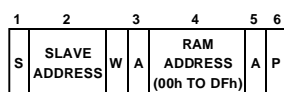

Figure 9a. Setting A RAM Address For Subsequent Read

3. Erase a page of EEPROM memory. EEPROM memory can be written to only if it is unprogrammed. Before writing to one or more EEPROM memory locations that are already programmed, the page or pages containing those locations must first be erased. EEPROM memory is erased by writing a command byte.

The master sends a command code that tells the slave device to erase the page. The ADM1060 command code for a pages(s) erasure is FEh (11111110). Note that, in order for page erasure to take place, the page address has to be given in the previous write word transaction (see write byte below). Also, bit 3 in register UPDCFG (address 90h) must be set to 1.
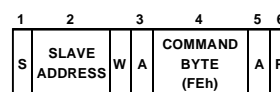

Figure 9b. EEPROM Page Erasure

As soon as the ADM1060 receives the command byte, page erasure begins. The master device can send a STOP command as soon as it sends the command byte. Page erasure takes approximately 20ms. If the ADM1060 is accessed before erasure is complete, it will respond with No Acknowledge.

Write Byte/Word

In this operation the master device sends a command byte and one or two data bytes to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master sends a data byte (or may assert STOP at this point).
9. The slave asserts ACK on SDA.
10. The master asserts a STOP condition on SDA to end the transaction.

In the ADM1060, the write byte/word protocol is used for three purposes.

1. Write a single byte of data to RAM. In this case the command byte is the RAM address from 00h to DFh and the (only) data byte is the actual data. This is illustrated in Figure 9c.
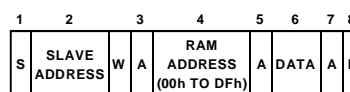

Figure 9c. Single Byte Write To RAM

2. Set up a two byte EEPROM address for a subsequent read, write, block read, block write or page erase. In

PROGRAMMING ADM1060 ADM1060

this case the command byte is the high byte of the EEPROM address from F8h to F9h. The (only) data byte is the low byte of the EEPROM address. This is illustrated in Figure 9c.
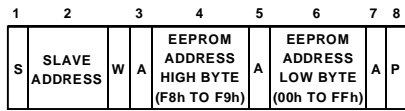

Figure 9d. Setting An EEPROM Address

Note for page erasure that as a page consists of 32 bytes only the three MSB's of the address low byte are important. The lower 5 bits of the EEPROM address low byte only specify addresses within a page and are ignored during an erase operation.

3. Write a single byte of data to EEPROM. In this case the command byte is the high byte of the EEPROM address from F8h to F9h. The first data byte is the low byte of the EEPROM address and the second data byte is the actual data. This is illustrated in Figure 9e.
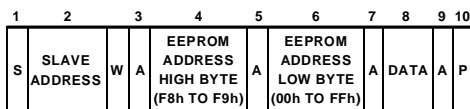

Figure 9e. Single Byte Write To EEPROM

Block Write

In this operation the master device writes a block of data to a slave device. The start address for a block write must previously have been set. In the case of the ADM1060 this is done by a Send Byte operation to set a RAM address or a Write Byte/Word operation to set an EEPROM address.

1. The master device asserts a start condition on SDA.

2. The master sends the 7-bit slave address followed by the write bit (low).

3. The addressed slave device asserts ACK on SDA.

4. The master sends a command code that tells the slave device to expect a block write. The ADM1060 command code for a block write is FCh (11111100).

5. The slave asserts ACK on SDA.

6. The master sends a data byte that tells the slave device how many data bytes will be sent. The SMBus specification allows a maximum of 32 data bytes to be sent in a block write.

7. The slave asserts ACK on SDA.

8. The master sends N data bytes.

9. The slave asserts ACK on SDA after each data byte.

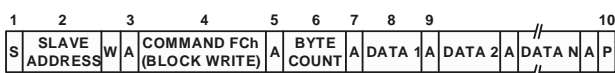10. The master asserts a STOP condition on SDA to end the transaction.

Figure 9f. Block Write To EEPROM Or RAM

Unlike some EEPROM devices which limit block writes to within a page boundary, there is no limitation on the start address when performing a block write to EEPROM, except:

1. There must be at least N locations from the start address to the highest EEPROM address (F9FFh), to avoiding writing to invalid addresses.

2. If the addresses cross a page boundary, both pages must be erased before programming.

Note that the ADM1060 features a clock extend function for writes to EEPROM. Programming an EEPROM byte takes approximately 250μs, which would limit the SMBus clock for repeated or block write operations. The ADM1060 pulls SCL low and extends the clock pulse when it cannot accept any more data.

ADM1060 READ OPERATIONS

The ADM1060 uses the following SMBus read protocols:

RECEIVE BYTE

In this operation the master device receives a single byte from a slave device, as follows:

1. The master device asserts a START condition on SDA.

2. The master sends the 7-bit slave address followed by the read bit (high).

3. The addressed slave device asserts ACK on SDA.

4. The master receives a data byte.

5. The master asserts NO ACK on SDA.

6. The master asserts a STOP condition on SDA and the transaction ends.

In the ADM1060, the receive byte protocol is used to read a single byte of data from a RAM or EEPROM location whose address has previously been set by a send byte or write byte/word operation. This is illustrated in Figure 9g.
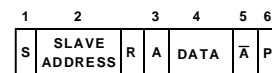

Figure 9g. Single Byte Read From EEPROM Or RAM

Block Read

In this operation the master device reads a block of data from a slave device. The start address for a block read must previously have been set. In the case of the ADM1060 this is done by a Send Byte operation to set a RAM address, or a Write Byte/Word operation to set an EEPROM address. The block read operation itself consists of a Send Byte operation that sends a block read command to the slave, immediately followed by a repeated start and a read operation that reads out multiple data bytes, as follows:

1. The master device asserts a START condition on SDA.

2. The master sends the 7-bit slave address followed by the write bit (low).

3. The addressed slave device asserts ACK on SDA.

4. The master sends a command code that tells the slave device to expect a block read. The ADM1060 command code for a block read is FDh (11111101).

5. The slave asserts ACK on SDA.

6. The master asserts a repeat start condition on SDA.

7. The master sends the 7-bit slave address followed by the read bit (high).

8. The slave asserts ACK on SDA.

9. The ADM1060 sends a byte count data byte that tells the master how many data bytes to expect. The ADM1060 will always return 32 data bytes (20h), which is the maximum allowed by the SMBus 1.1 specification.

10. The master asserts ACK on SDA.

11. The master receives 32 data bytes.

12. The master asserts ACK on SDA after each data byte.

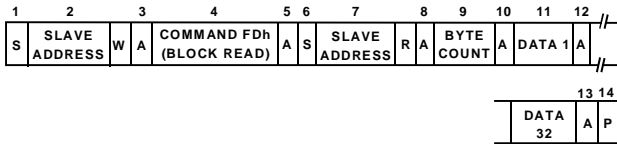13. The master asserts a STOP condition on SDA to end the transaction.

Figure 9h. Block Read From EEPROM or RAM

ERROR CORRECTION

The ADM1060 provides the option of issuing a PEC (Packet Error Correction) byte after a write to RAM, a write to EEPROM, a block write to RAM/EEPROM or a block read from RAM/EEPROM. This enables the user to verify that the data received by or sent from the ADM1060 is correct. The PEC byte is an optional byte sent after that last data byte has been written to or read from the ADM1060. The protocol is as follows:-

1. The ADM1060 issues a PEC byte to the master. The master should check the PEC byte and issue another block read if the PEC byte is incorrect.

2. A NACK is generated after the PEC byte to signal the end of the read.

Note: The PEC byte is calculated using CRC-8. The Frame Check Sequence (FCS) conforms to CRC-8 by the polynomial:-

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult SMBus 1.1 specification for more information. An example of a block read with the optional PEC byte is shown in figure 9i below.
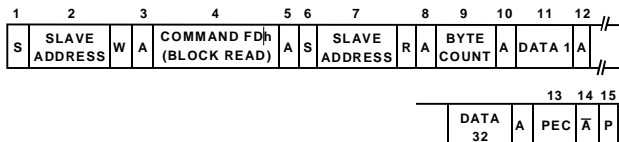

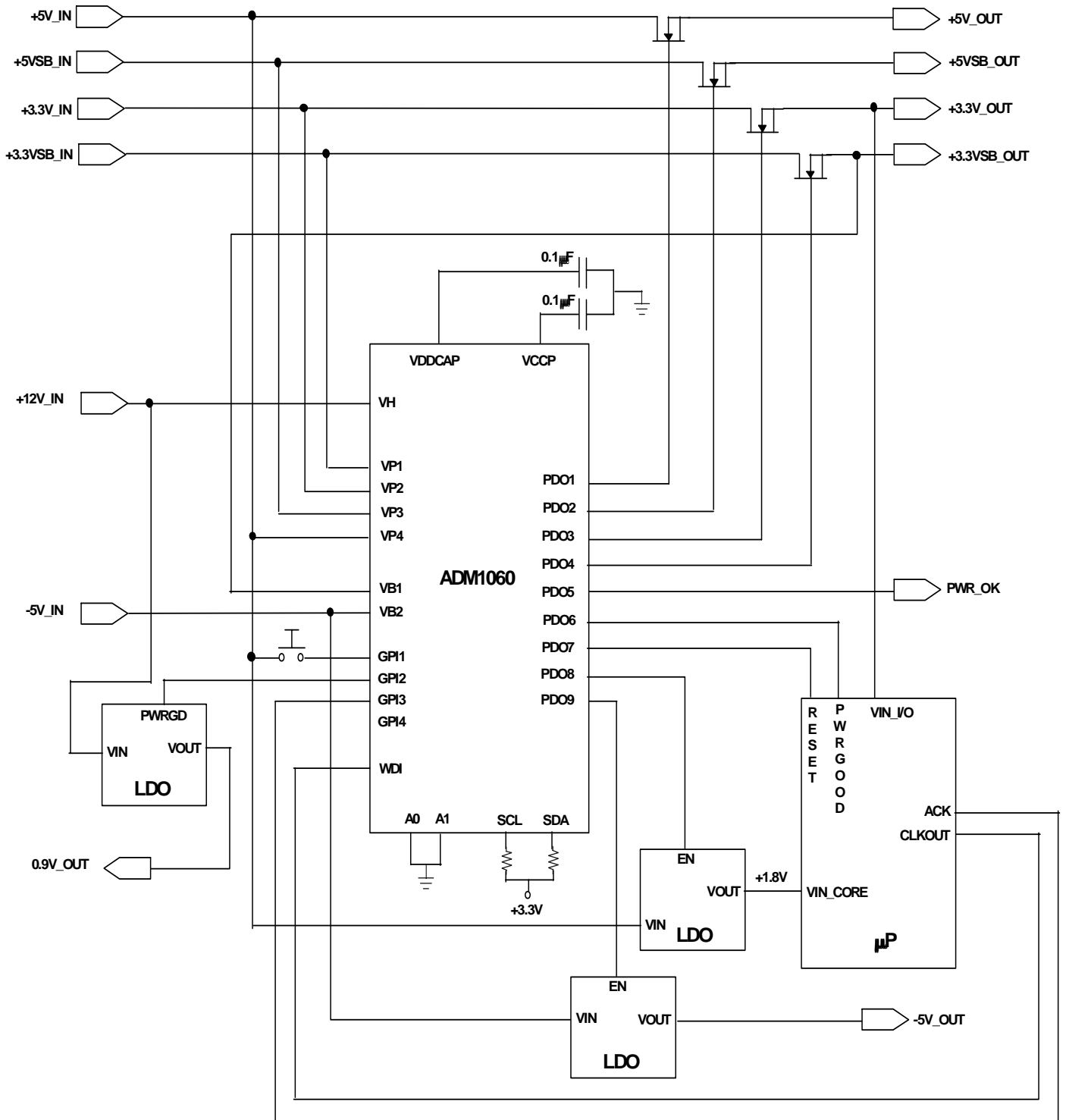*Figure 9i. Block Read From EEPROM or RAM with PEC*

ADM1060

Figure 10. ADM1060 Application Diagram

ADM1060 Register Map

BLOCK		0	1	2	3	4	5	6	7	8	9	A	B	C	D
PLB1	0	P1PLBPOLA	P1PLBIMKA	P1SFDPOLA	P1SFDIMKA	P1GPIPOL	P1GPIIMK	P1WDICFG	P1EN	P1PLBPOLB	P1PLBIMKB	P1SFDPOLB	P1SFDIMKB	P1PDBTIM	P1PDOCFG
PLB2	1	P2PLBPOLA	P2PLBIMKA	P2SFDPOLA	P2SFDIMKA	P2GPIPOL	P2GPIIMK	P2WDICFG	P2EN	P2PLBPOLB	P2PLBIMKB	P2SFDPOLB	P2SFDIMKB	P2PDBTIM	P2PDOCFG
PLB3	2	P3PLBPOLA	P3PLBIMKA	P3SFDPOLA	P3SFDIMKA	P3GPIPOL	P3GPIIMK	P3WDICFG	P3EN	P3PLBPOLB	P3PLBIMKB	P3SFDPOLB	P3SFDIMKB	P3PDBTIM	P3PDOCFG
PLB4	3	P4PLBPOLA	P4PLBIMKA	P4SFDPOLA	P4SFDIMKA	P4GPIPOL	P4GPIIMK	P4WDICFG	P4EN	P4PLBPOLB	P4PLBIMKB	P4SFDPOLB	P4SFDIMKB	P4PDBTIM	P4PDOCFG
PLB5	4	P5PLBPOLA	P5PLBIMKA	P5SFDPOLA	P5SFDIMKA	P5GPIPOL	P5GPIIMK	P5WDICFG	P5EN	P5PLBPOLB	P5PLBIMKB	P5SFDPOLB	P5SFDIMKB	P5PDBTIM	P5PDOCFG
PLB6	5	P6PLBPOLA	P6PLBIMKA	P6SFDPOLA	P6SFDIMKA	P6GPIPOL	P6GPIIMK	P6WDICFG	P6EN	P6PLBPOLB	P6PLBIMKB	P6SFDPOLB	P6SFDIMKB	P6PDBTIM	P6PDOCFG
PLB7	6	P7PLBPOLA	P7PLBIMKA	P7SFDPOLA	P7SFDIMKA	P7GPIPOL	P7GPIIMK	P7WDICFG	P7EN	P7PLBPOLB	P7PLBIMKB	P7SFDPOLB	P7SFDIMKB	P7PDBTIM	P7PDOCFG
PLB8	7	P8PLBPOLA	P8PLBIMKA	P8SFDPOLA	P8SFDIMKA	P8GPIPOL	P8GPIIMK	P8WDICFG	P8EN	P8PLBPOLB	P8PLBIMKB	P8SFDPOLB	P8SFDIMKB	P8PDBTIM	P8PDOCFG
PLB9	8	P9PLBPOLA	P9PLBIMKA	P9SFDPOLA	P9SFDIMKA	P9GPIPOL	P9GPIIMK	P9WDICFG	P9EN	P9PLBPOLB	P9PLBIMKB	P9SFDPOLB	P9SFDIMKB	P9PDBTIM	P9PDOCFG
FLT/STS GPI/WDI	9	UPDCFG	PDEN		MANID	DEVID	REVID	MARK1	MARK2	GPI1CFG	GPI2CFG	GPI3CFG	GPI4CFG	WDICFG	ERRMASK1 **E** ERRMASK2
BSFD1/2	A	BS1OVTH	BS1OVHYST	BS1UVTH	BS1UVHYST	BS1SEL				BS2OVTH	BS2OVHYST	BS2UVTH	BS2UVHYST	BS2SEL	
H/PSFD1	B	HSOVTH	HSOVHYST	HSUVTH	HSUVHYST	HSSEL				PS1OVTH	PS1OVHYST	PS1UVTH	PS1UVHYST	PS1SEL	
PSFD2/3	C	PS2OVTH	PS2OVHYST	PS2UVTH	PS2UVHYST	PS2SEL				PS3OVTH	PS3OVHYST	PS3UVTH	PS3UVHYST	PS3SEL	
PSFD4/ FLT/STS	D	PS4OVTH	PS4OVHYST	PS4UVTH	PS4UVHYST	PS4SEL				UVSTAT	OVSTAT	SFDSTAT	GWSTAT	LATF1	LATF2 **E** PDOSTAT1 **F** PDOSTAT2

ADM1060

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm)

28- Lead TSSOP (RU-28)
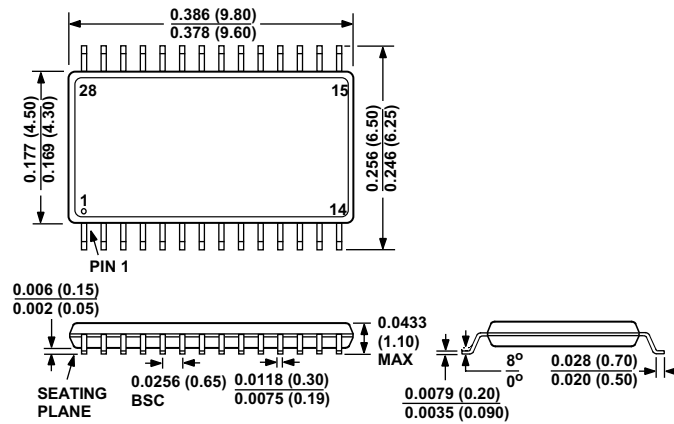
Revision History
Rev. H
1. Update of specs. pages
2. Inclusion of Table of Contents
3. Inclusion of EEPROM download at Power- Up (p.38)
2**Rev. G**
1. Update of specs. pages (better definition of supply conditions, inclusion of input impedance, better definition of PDO output conditions).
2. Removal of PUEN (pull-up current source on logic inputs) function (See Rev. F-7).
Rev. F
1. Update of specs. to reflect 14V drive capability of charge pumped outputs.
2. Correction of features on bipolar SFD's- only 1 range available in negative mode.
3. Better definition of SFD Glitch Filter
4. Completion of register map- addition of table numbers for each register, addition of register map matrix (p.43)
5. Improved definition of all ADM1060 blocks.
6. Definition of fault/status reporting on the ADM1060
7. Addition of Pull- Up/Down current source on logic inputs
8. Corrected version of how SMBus protocol is implemented on the ADM1060.
9. Inclusion of device ID registers (p.37)