10-Channel Gamma Buffer with V_{COM} Driver

ADD8710

FEATURES

Single-supply operation: 4.5 V to 16.5 V
Upper/lower buffers swing to V_S/GND
Gamma continuous output current: >10 mA
V_{COM} peak output current: 250 mA
Offset voltage: 12 mV
Slew rate: 8 V/µs
Unity gain stable with large capacitive loads
Supply current: 700 µA per amplifier
Compact 28-lead TSSOP
Pb-free package
Drop-in replacement for BUF11702

APPLICATIONS

TFT LCD monitor panels
TFT LCD notebook panels

GENERAL DESCRIPTION

The ADD8710 is a low cost, 10-channel gamma buffer with a V_{COM} driver that operates from a single supply. The part is designed for high resolution TFT LCD panels, and is built on an advanced, high voltage CBCMOS process.

The gamma buffers have a high slew rate, minimum 10 mA output current, and a high capacitive load drive capability. The V_{COM} buffer is capable of delivering 250 mA of peak current, and can also drive large capacitive loads. The ADD8710 offers wide supply range and offset voltages below 12 mV.

The ADD8710 is specified over the −40°C to +85°C temperature range and is available in a Pb-free 28-lead TSSOP package.

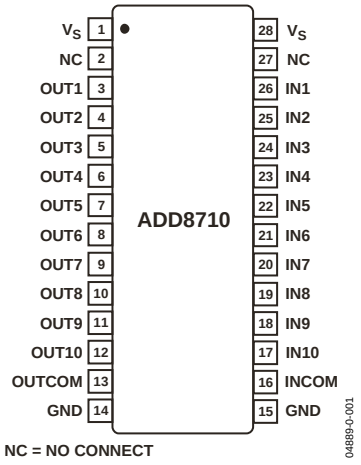

Figure 1. 28-Lead TSSOP (RU Suffix)

FUNCTIONAL BLOCK DIAGRAM

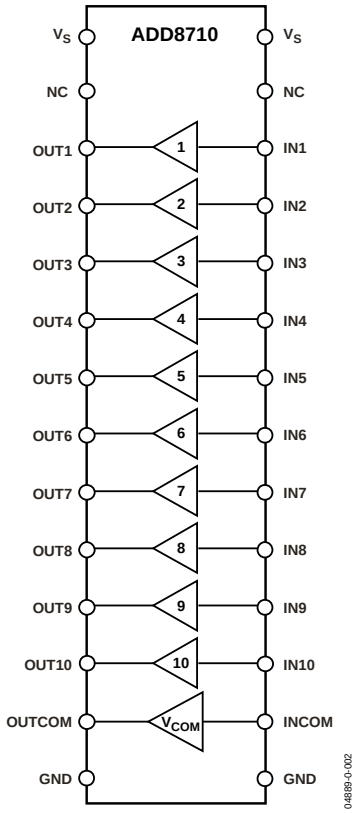

Figure 2.

Rev. 0

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REVISION HISTORY

6/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

V_S = 16 V, V_{CM} = V_S/2, T_A @ 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS		Applies to all channels				
Offset Voltage	V_{OS}			4	12	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta_T$	–40°C ≤ T_A ≤ +85°C		5		µV/°C
Input Bias Current	I_B			0.5	1.1	µA
		–40°C ≤ T_A ≤ +85°C			1.5	µA
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
BUFFER CHARACTERISTICS						
Output Voltage High (V1)	V_{OH}	V_S = 16 V, V_I = 16 V, I_L = 10 mA	15.82	15.9		V
		V_S = 10 V, V_I = 9.8 V, I_L = 10 mA	9.75	9.8		V
		–40°C ≤ T_A ≤ +85°C	9.7			V
Output Voltage High (V2 to V5)	V_{OH}	V_S = 10 V, V_I = 8.5 V, I_L = 10 mA	8.45	8.5		V
		–40°C ≤ T_A≤ +85°C	8.4			V
Output Voltage High (V6 to V10)	V_{OH}	V_S = 10 V, V_I= 8 V, I_L= 10 mA	7.95	8		V
		–40°C ≤ T_A≤ +85°C	7.9			V
Output Voltage Low (V1 to V5)	V_{OL}	V_S = 10 V, V_I = 2 V, I_L = 10 mA		2	2.05	V
		–40°C ≤ T_A≤ +85°C			2.10	V
Output Voltage Low (V6 to V9)	V_{OL}	V_S = 10 V, V_I = 1.5 V, I_L = 10 mA		1.5	1.55	V
		–40°C ≤ T_A ≤ +85°C			1.60	V
Output Voltage Low (V10)	V_{OL}	V_S = 16 V, V_I = 0 V, I_L = 10 mA		0.1	0.175	V
		V_S = 10 V, V_I = 0.2 V, I_L = 10 mA		0.2	0.25	V
		–40°C ≤ T_A ≤ +85°C		0.3		V
Continuous Output Current	I_{OUT}			10		mA
Peak Output Current	I_{PK}	V_S = 16 V		100		mA
V_{COM} CHARACTERISTICS						
Output Voltage High	V_{OH}	V_S = 10 V, V_I = 8 V, I_L = 30 mA	7.95	8		
		–40°C ≤ T_A≤ +85°C	7.9			
Output Voltage Low	V_{OL}	V_S = 10 V, V_I = 2 V, I_L = 30 mA		2	2.05	
		–40°C ≤ T_A ≤ +85°C			2.10	
Continuous Output Current	I_{OUT}			35		mA
Peak Output Current	I_{PK}	V_S = 16 V		250		mA
SUPPLY CHARACTERISTICS						
Supply Voltage	V_S		4.5		16.5	V
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 16.5 V, –40°C ≤ T_A ≤ +85°C	70	90		dB
Total Supply Current	I_{SY}	V_O = V_S/2, No Load		7.7	10	mA
		–40°C ≤ T_A ≤ +85°C			11.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 200 pF	4	8		V/µs
Bandwidth	BW	–3 dB, R_L= 10 kΩ, C_L = 200 pF		5		MHz
Settling Time to 0.1% (Buffers)	t_S	1 V step, R_L = 10 kΩ, C_L = 200 pF		1.1		µs
Settling Time to 0.1% (V_{COM})	t_S	1 V step, R_L = 10 kΩ, C_L = 200 pF		0.7		µs
Phase Margin	Øo	R_L = 10 kΩ, C_L = 200 pF		45		Degree
Channel Separation				75		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_S)	18 V
Input Voltage	−0.5 V to V_S + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range	300°C
ESD Tolerance (HBM)	±2500 V
ESD Tolerance (MM)	±200 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Package Characteristics

Package Type	θ_{JA}[1]	Unit
28-Lead TSSOP (RU)	67.7	°C/W

[1] θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for devices soldered on to a circuit board for surface mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

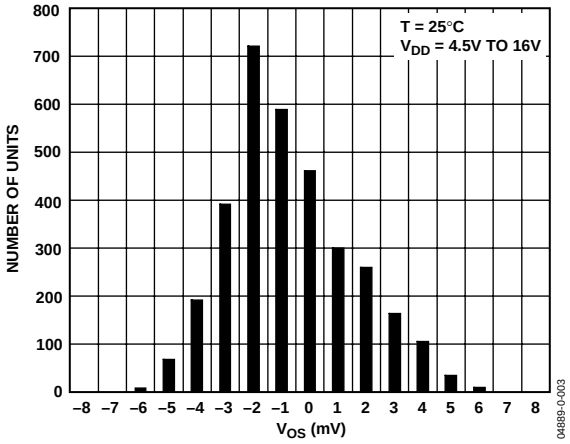

Figure 3. Input Offset Voltage

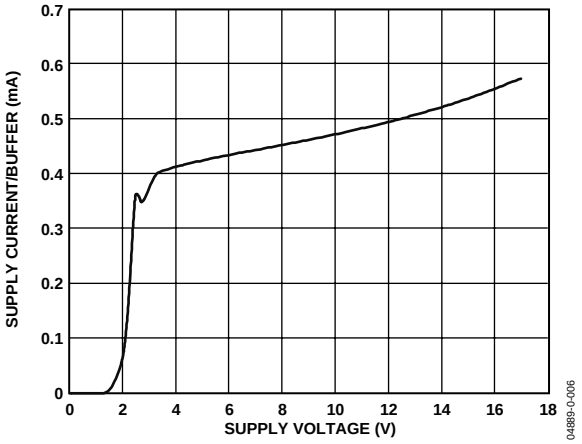

Figure 6. Supply Current/Buffer v. Supply Voltage

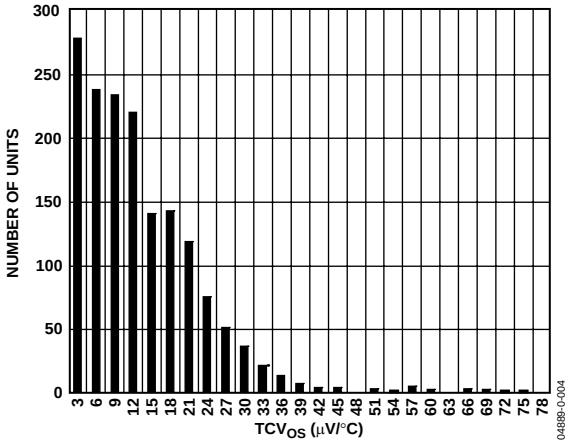

Figure 4. Input Offset Voltage Drift Distribution

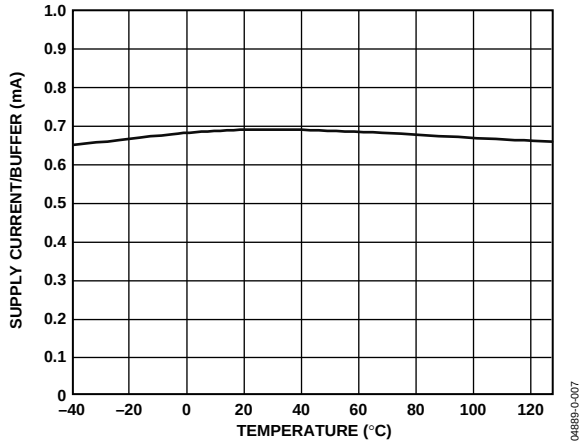

Figure 7. Supply Current/Buffer vs. Temperature

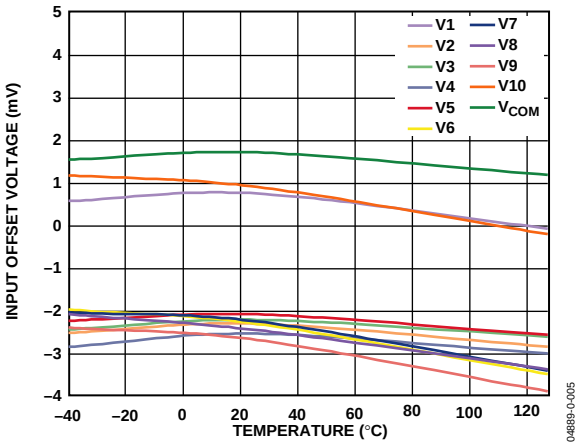

Figure 5. Input Offset Voltage vs. Temperature

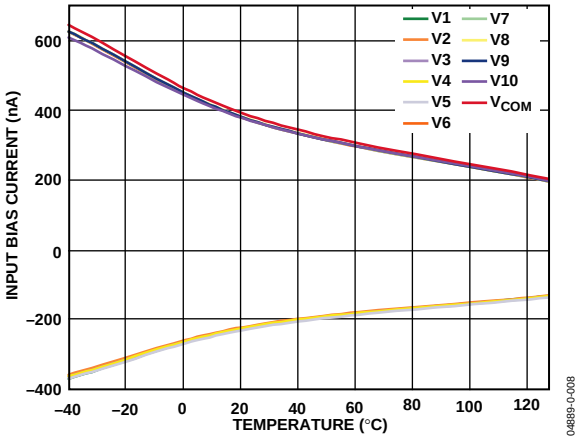

Figure 8. Input Bias Current vs. Temperature

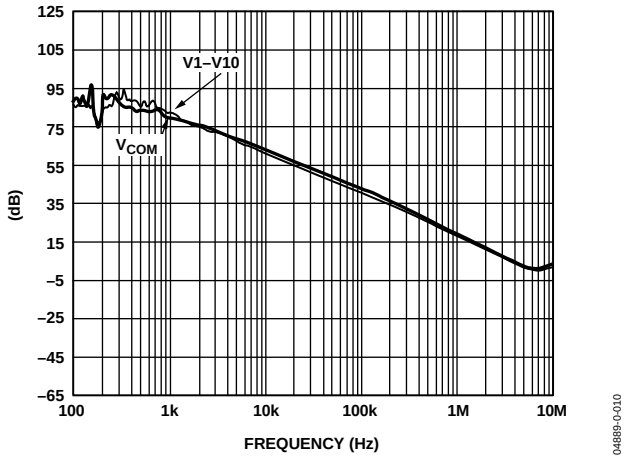

Figure 9. Power Supply Rejection Ratio vs. Frequency

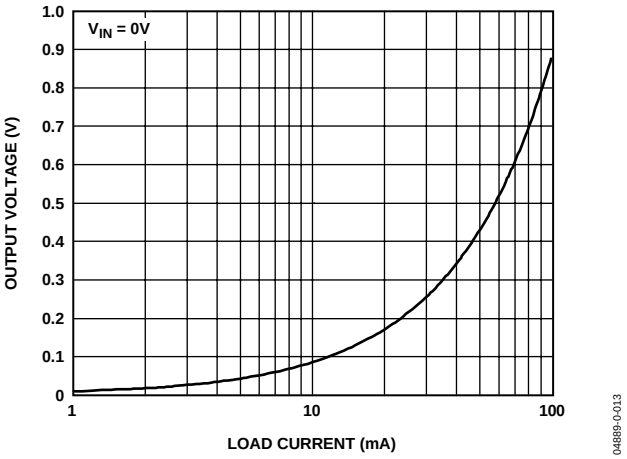

Figure 12. Chan V_{COM} Output Voltage Low vs. I Load

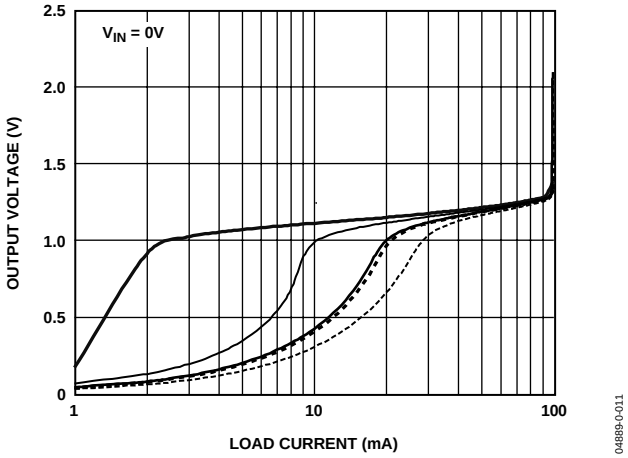

Figure 10. Chan 1-5 Output Voltage Low vs. I Load

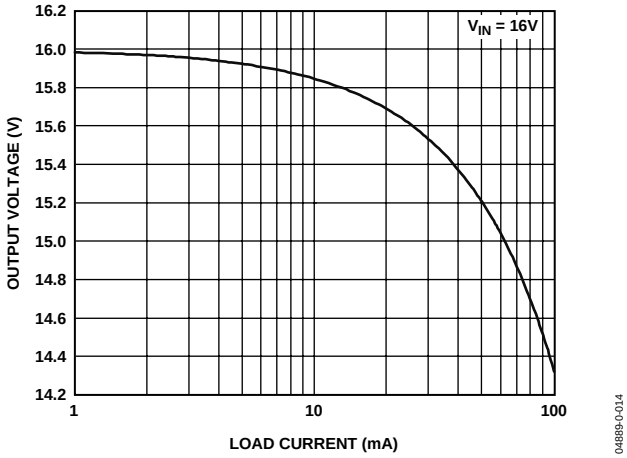

Figure 13. Chan 1 Output Voltage High vs. I Load

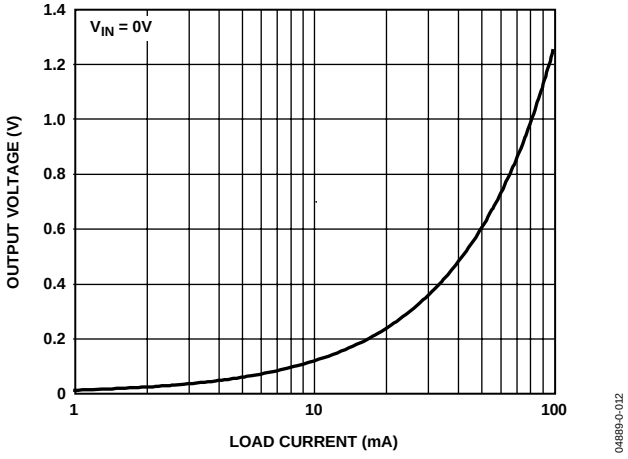

Figure 11. Chan 6-10 Output Voltage Low vs. I Load

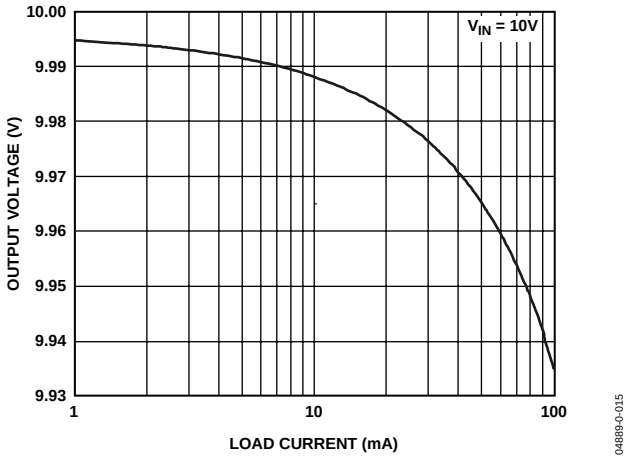

Figure 14. Chan 2-5 Output Voltage High vs. I Load

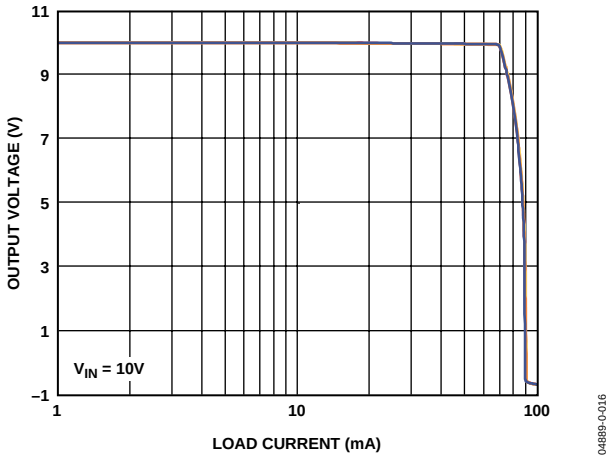

Figure 15. Chan 6-10 Output Voltage High vs. I Load

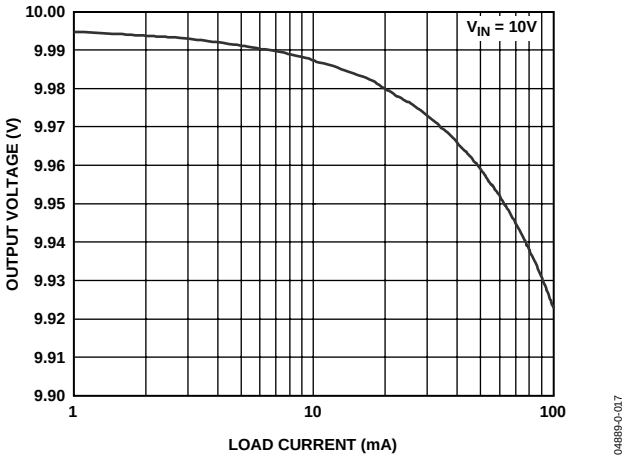

Figure 16. Chan V_{COM} Output Voltage High vs. I Load

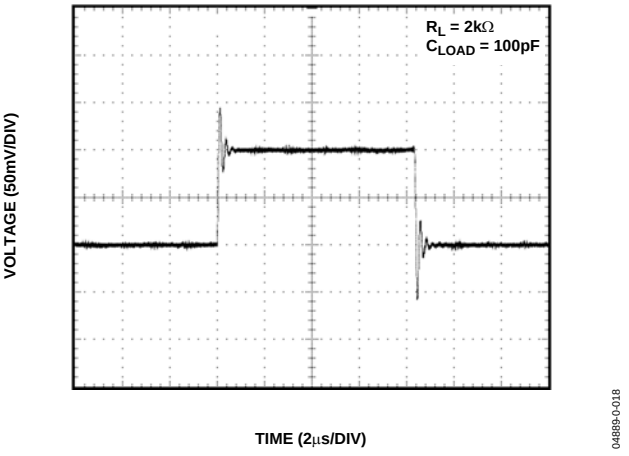

Figure 17. Small-Signal Transient Response

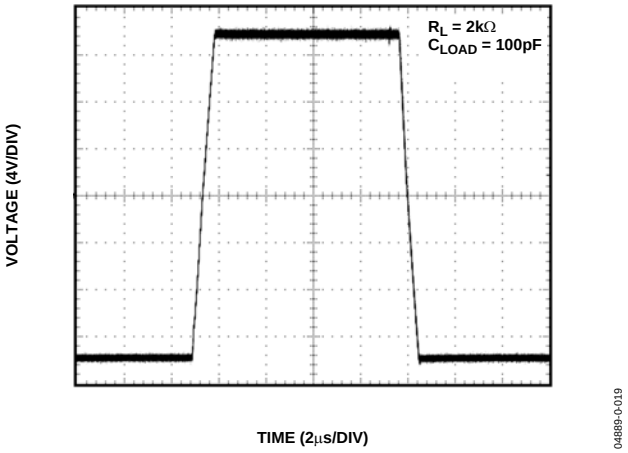

Figure 18. Large-Signal Transient Response

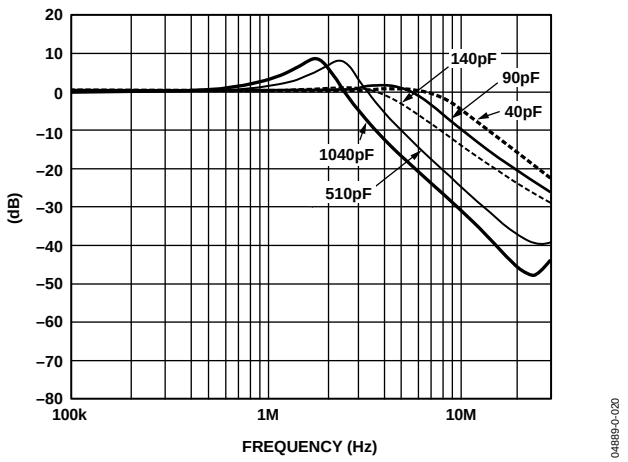

Figure 19. Chan 1-5 Frequency Response vs. Capacitive Loading

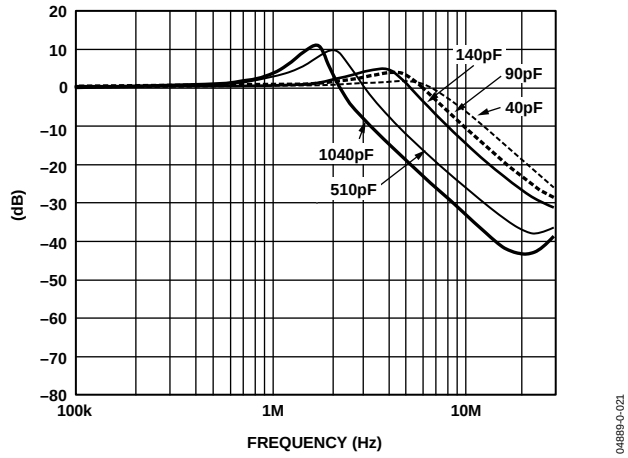

Figure 20. Chan 6-10 Frequency Response vs. Capacitive Loading

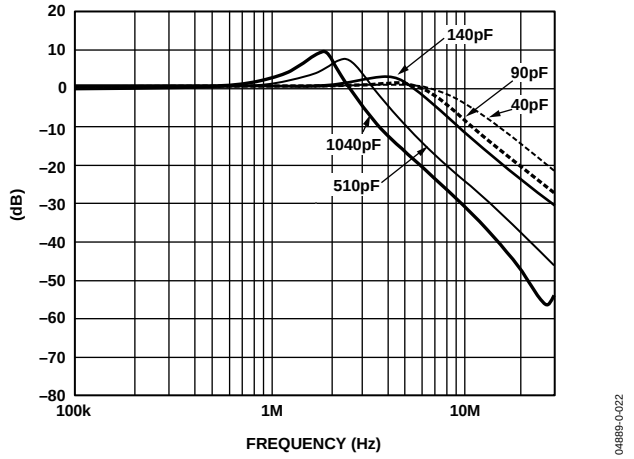

Figure 21. Chan V_{COM} Frequency Response vs. Capacitive Loading

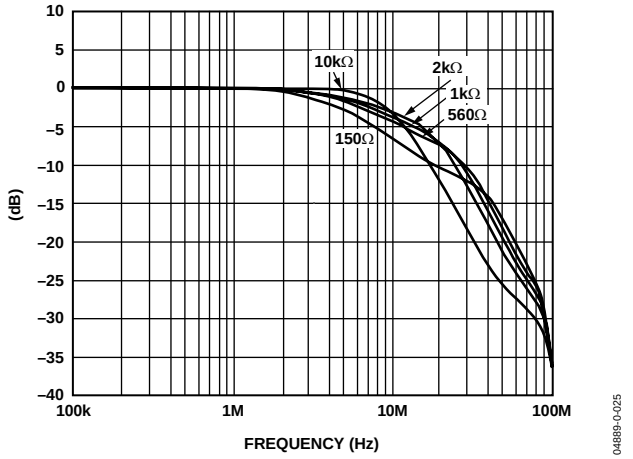

Figure 24. Chan V_{COM} Frequency Response vs. Resistive Loading

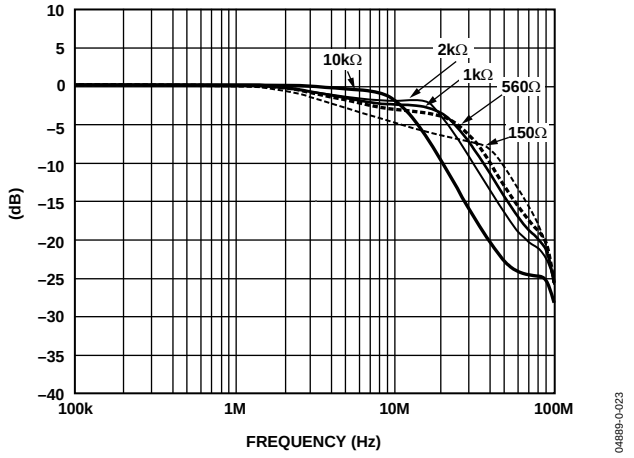

Figure 22. Chan 1-5 Frequency Response vs. Resistive Loading

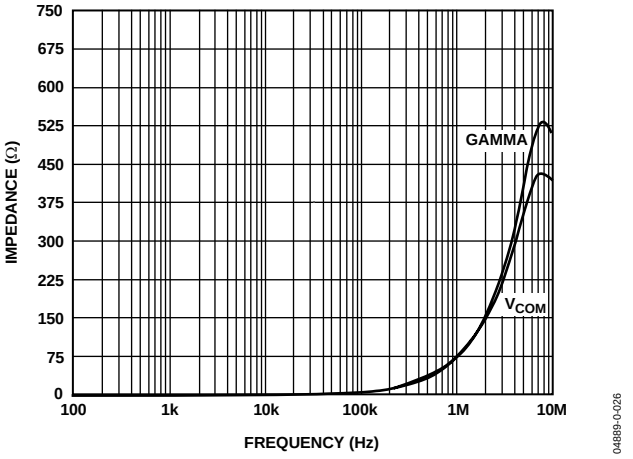

Figure 25. Closed-Loop Output Impedance vs. Frequency

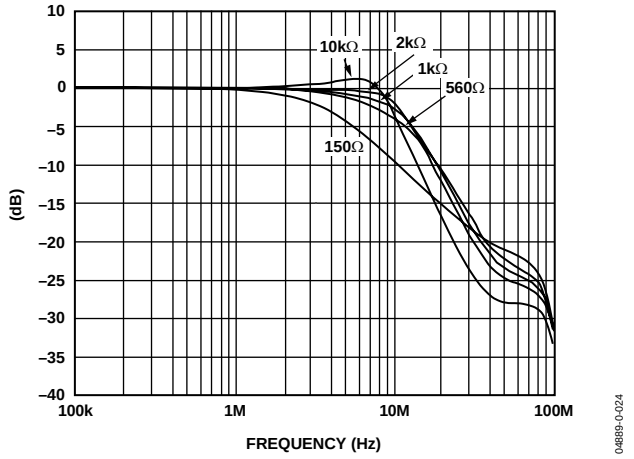

Figure 23. Chan 6-10 Frequency Response vs. Resistive Loading

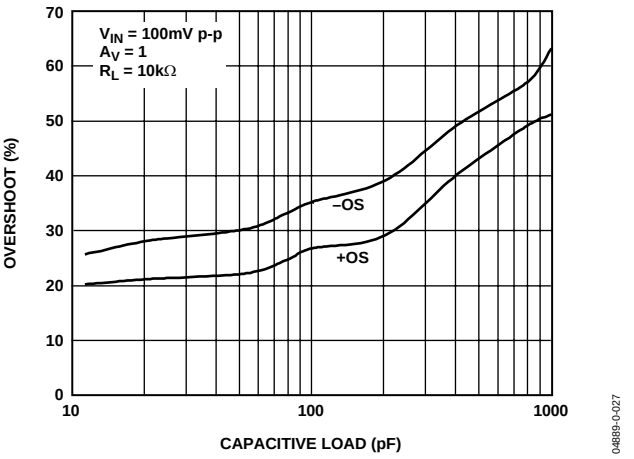

Figure 26. Chan 1-5 Small Signal Overshoot vs. Load Capacitance

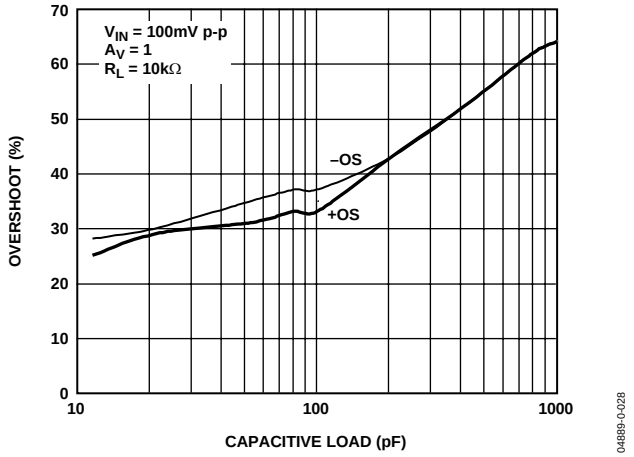

Figure 27. Chan 6-10 Small Signal Overshoot vs. Load Capacitance

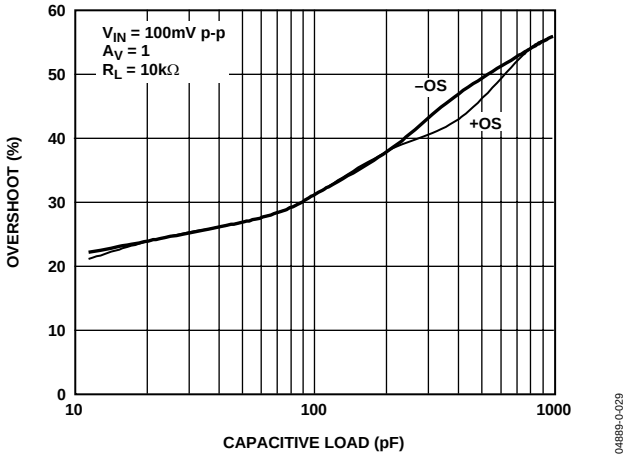

Figure 28. Chan V_{COM} Small Signal Overshoot vs. Load Capacitance

OUTLINE DIMENSIONS

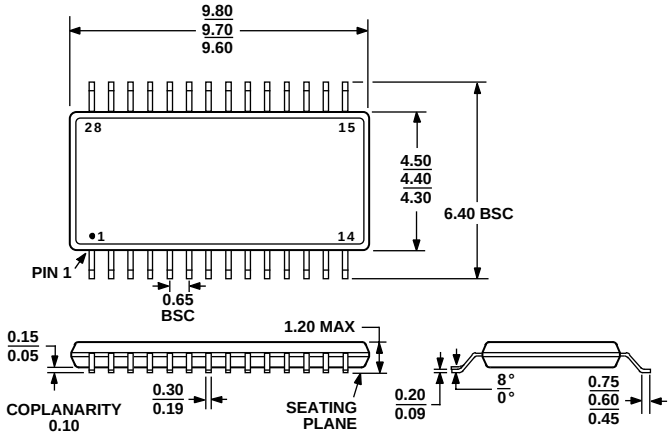

Figure 29. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADD8710ARUZ[1]	−40°C to +85°C	28-Lead TSSOP	RU-28
ADD8710ARUZ-REEL[1]	−40°C to +85°C	28-Lead TSSOP	RU-28

[1] Z = Pb-free part.

NOTES

NOTES

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