ADC101C021/ADC101C027 I²C-Compatible, 10-Bit Analog-to-Digital Converter (ADC) with Alert Function

Check for Samples: ADC101C021, ADC101C027

FEATURES

- **I²C-Compatible 2-wire Interface which supports standard (100kHz), fast (400kHz), and high speed (3.4MHz) modes**
- **Extended power supply range (+2.7V to +5.5V)**
- **Up to nine pin-selectable chip addresses (VSSOP-8 only)**
- **Out-of-range Alert Function**
- **Automatic Power-down mode while not converting**
- **Very small SOT-6 and VSSOP-8 packages**
- **±8kV HBM ESD protection (SDA, SCL)**

APPLICATIONS

- **System Monitoring**
- **Peak Detection**
- **Portable Instruments**
- **Medical Instruments**
- **Test Equipment**

KEY SPECIFICATIONS

- **Resolution 10 bits; no missing codes**
- **Conversion Time 1µs (typ)**
- **INL & DNL ±0.5 LSB (max)**
- **Throughput Rate 188.9 kSPS (max)**
- **Power Consumption (at 22kSPS)**
  - **3V Supply 0.26 mW (typ)**
  - **5V Supply 0.78 mW (typ)**

DESCRIPTION

The ADC101C021 is a low-power, monolithic, 10-bit, analog-to-digital converter (ADC) that operates from a +2.7 to 5.5V supply. The converter is based on a successive approximation register architecture with an internal track-and-hold circuit that can handle input frequencies up to 11MHz. The ADC101C021 operates from a single supply which also serves as the reference. The device features an I²C-compatible serial interface that operates in all three speed modes, including high speed mode (3.4MHz).

The ADC's Alert feature provides an interrupt that is activated when the analog input violates a programmable upper or lower limit value. The device features an automatic conversion mode, which frees up the controller and I²C interface. In this mode, the ADC continuously monitors the analog input for an "out-of-range" condition and provides an interrupt if the measured voltage goes out-of-range.

The ADC101C021 comes in two packages: a small SOT-6 package with an alert output, and an VSSOP-8 package with an alert output and two address selection inputs. The ADC101C027 comes in a small SOT-6 package with an address selection input. The ADC101C027 provides three pin-selectable addresses while the VSSOP-8 version of the ADC101C021 provides nine pin-selectable addresses. Pin-compatible alternatives to the SOT-6 options are available with additional address options.

Normal power consumption using a +3V or +5V supply is 0.26mW or 0.78mW, respectively. The automatic power-down feature reduces the power consumption to less than 1µW while not converting. Operation over the industrial temperature range of −40°C to +105°C is guaranteed. Their low power consumption and small packages make this family of ADCs an excellent choice for use in battery operated equipment.

The ADC101C021 and ADC101C027 are part of a family of pin-compatible ADCs that also provide 12 and 8 bit resolution. For 12-bit ADCs see the ADC121C021 and ADC121C027. For 8-bit ADCs see the ADC081C021 and ADC081C027.

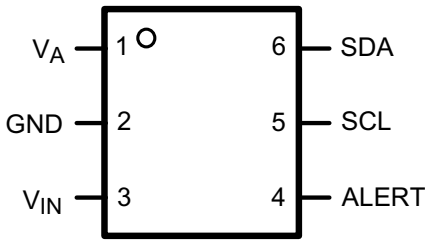
Table 1. Pin-Compatible Alternatives[1]

Resolution	SOT-6 (Alert only) and VSSOP-8	SOT-6 (Addr only)
12-bit	ADC121C021	ADC121C027
10-bit	**ADC101C021**	**ADC101C027**
8-bit	ADC081C021	ADC081C027

(1) All devices are fully pin and function compatible.

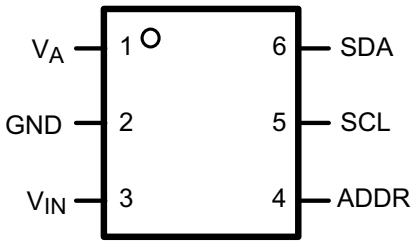
Connection Diagrams

SOT PACKAGE



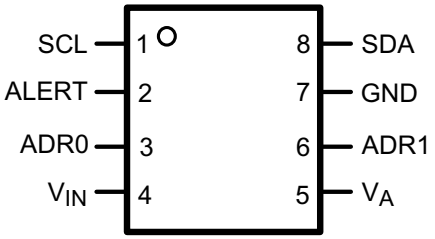
ADC101C021

SOT PACKAGE



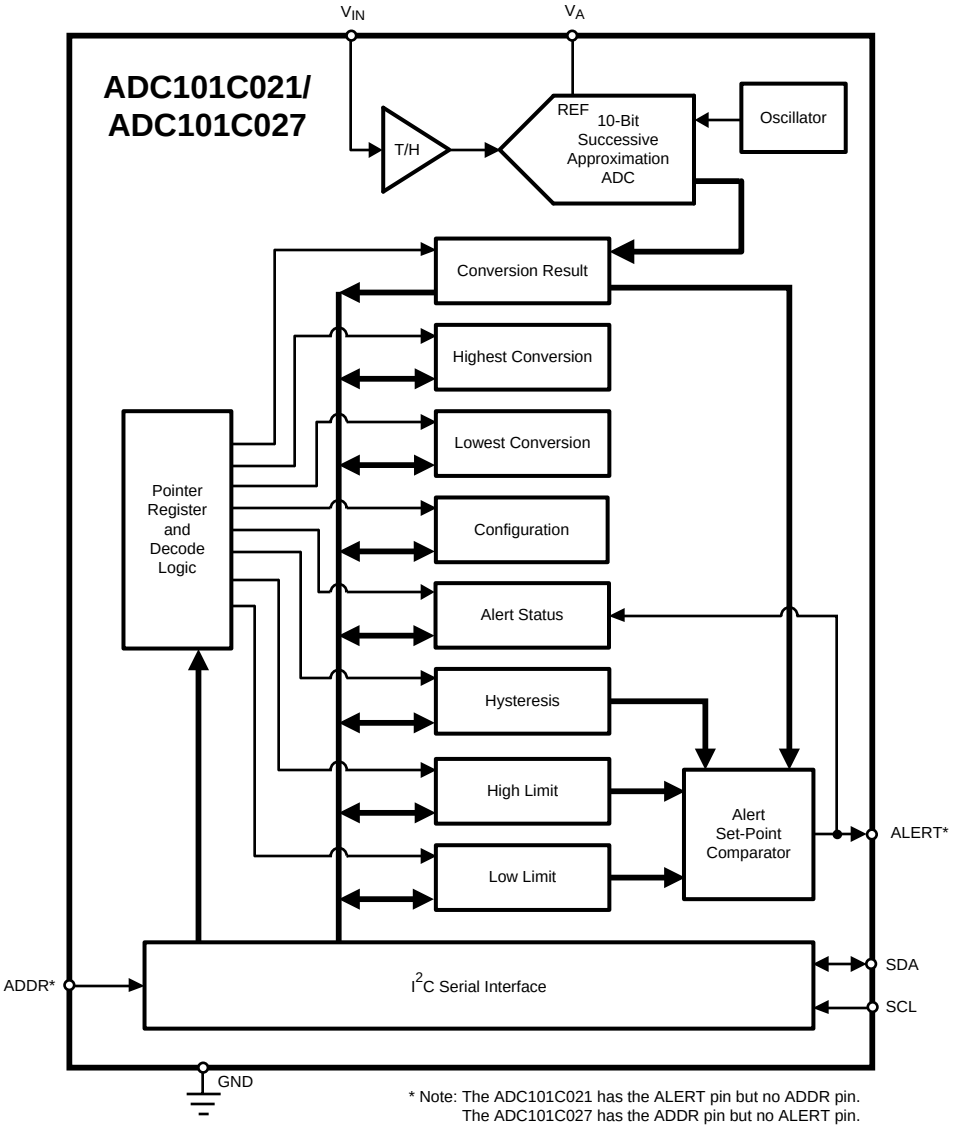
ADC101C027

VSSOP PACKAGE



ADC101C021

Block Diagram



* Note: The ADC101C021 has the ALERT pin but no ADDR pin.
The ADC101C027 has the ADDR pin but no ALERT pin.

PIN DESCRIPTIONS

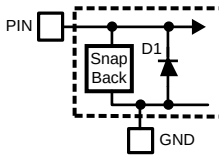
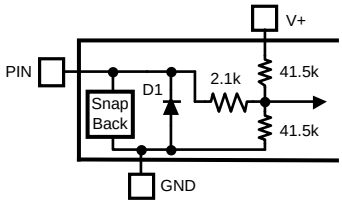
Symbol	Type	Equivalent Circuit	Description
V_A	Supply		Power and unbufferred reference voltage. V_A must be free of noise and decoupled to GND.
GND	Ground		Ground for all on-chip circuitry.
V_{IN}	Analog Input	See Figure 19	Analog input. This signal can range from GND to V_A.
ALERT	Digital Output		Alert output. Can be configured as active high or active low. This is an open drain data line that must be pulled to the supply (V_A) with an external pull-up resistor.
SCL	Digital Input		Serial Clock Input. SCL is used together with SDA to control the transfer of data in and out of the device. This is an open drain data line that must be pulled to the supply (V_A) with an external pull-up resistor. This pin's extended ESD tolerance(8kV HBM) allows extension of the I^2C bus across multiple boards without extra ESD protection.
SDA	Digital Input/Output		Serial Data bi-directional connection. Data is clocked into or out of the internal 16-bit register with SCL. This is an open drain data line that must be pulled to the supply (V_A) with an external pull-up resistor. This pin's extended ESD tolerance(8kV HBM) allows extension of the I^2C bus across multiple boards without extra ESD protection.
ADR0	Digital Input, three levels		Tri-level Address Selection Input. Sets Bits A0 & A1 of the 7-bit slave address. (see Table 3)
ADR1			Tri-level Address Selection Input. Sets Bits A2 & A3 of the 7-bit slave address. (see Table 3)

Table 2. Package Pinouts

	V_A	GND	V_{IN}	ALERT	SCL	SDA	ADR0	ADR1
ADC101C021 SOT-6	1	2	3	4	5	6	N/A	N/A
ADC101C027 SOT-6	1	2	3	N/A	5	6	4	N/A
ADC101C021 VSSOP-8	5	7	4	2	1	8	3	6

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

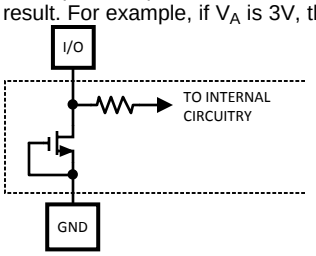
Supply Voltage, V_A			-0.3V to +6.5V
Voltage on any Analog Input Pin to GND			−0.3V to (V_A +0.3V)
Voltage on any Digital Input Pin to GND			−0.3V to 6.5V
Input Current at Any Pin[4]			±15 mA
Package Input Current[4]			±20 mA
Power Dissipation at T_A = 25°C			See [5]
ESD Susceptibility	V_A, GND, V_{IN}, ALERT, ADR pins:	Human Body Model	2500 V
		Machine Model	250 V
		Charged Device Model (CDM)	1250 V
	SDA, SCL pins:	Human Body Model	8000 V
		Machine Model	400 V
Junction Temperature			+150°C
Storage Temperature			−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds 5.5V or is less than GND, the current at that pin should be limited per the Absolute Maximum Ratings. The maximum package input current rating limits the number of pins that can safely exceed the power supplies.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed).

Operating Ratings[1] [2]

Operating Temperature Range	−40°C ≤ T_A ≤ +105°C
Supply Voltage, V_A	+2.7V to 5.5V
Analog Input Voltage, V_{IN}	0V to V_A
Digital Input Voltage[3]	0V to 5.5V
Sample Rate	up to 188.9 ksps

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) The inputs are protected as shown below. Input voltage magnitudes up to 5.5V, regardless of V_A, will not cause errors in the conversion result. For example, if V_A is 3V, the digital input pins can be driven with a 5V logic device.



Package Thermal Resistances

Package	θ_{JA}
6-Lead SOT	250°C/W
8-Lead VSSOP	200°C/W

Electrical Characteristics

The following specifications apply for V_A = +2.7V to +5.5V, GND = 0V, f_{SCL} up to 3.4MHz, f_{IN} = 1kHz for f_{SCL} up to 400kHz, f_{IN} = 10kHz for f_{SCL} = 3.4MHz unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Typical (1)	Limits (1)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10**	Bits
INL	Integral Non-Linearity (End Point Method)	V_A = +2.7V to +3.6V	±0.1	**±0.5**	LSB (max)
		V_A = +2.7V to +5.5V. f_{SCL} up to 400 kHz (2)	+0.21	**+0.7**	LSB (max)
			−0.16	**−0.7**	LSB (min)
DNL	Differential Non-Linearity	V_A = +2.7V to +3.6V	±0.1	**±0.5**	LSB (max)
		V_A = +2.7V to +5.5V. f_{SCL} up to 400 kHz (2)	+0.25	**+0.7**	LSB (max)
			−0.16	**−0.7**	LSB (min)
V_{OFF}	Offset Error	V_A = +2.7V to +3.6V f_{SCL} up to 3.4 MHz	+0.25	**±0.8**	LSB (max)
		V_A = +2.7V to +5.5V. f_{SCL} up to 400kHz (2)	+0.27	**±0.8**	LSB (max)
GE	Gain Error		-0.13	**±1**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
ENOB	Effective Number of Bits	V_A = +2.7V to +3.6V	9.97	**9.87**	Bits (min)
		V_A = +3.6V to +5.5V	9.94		Bits
SNR	Signal-to-Noise Ratio	V_A = +2.7V to +3.6V	61.8	**61.2**	dB (min)
		V_A = +3.6V to +5.5V	61.6		dB
THD	Total Harmonic Distortion	V_A = +2.7V to +3.6V	−88.9	**−74**	dB (max)
		V_A = +3.6V to +5.5V	−85.7		dB
SINAD	Signal-to-Noise Plus Distortion Ratio	V_A = +2.7V to +3.6V	61.8	**61.2**	dB (min)
		V_A = +3.6V to +5.5V	61.6		dB
SFDR	Spurious-Free Dynamic Range	V_A = +2.7V to +3.6V	84	**76**	dB (min)
		V_A = +3.6V to +5.5V	84.3		dB
IMD	Intermodulation Distortion, Second Order Terms (IMD_2)	f_a = 1.035 kHz, f_b = 1.135 kHz	−83.9		dB
	Intermodulation Distortion, Third Order Terms (IMD_3)	f_a = 1.035 kHz, f_b = 1.135 kHz	−82.4		dB
FPBW	Full Power Bandwidth (−3dB)	V_A = +3.0V	8		MHz
		V_A = +5.0V	11		MHz
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to V_A		V
I_{DCL}	DC Leakage Current (3)			**±1**	µA (max)
C_{INA}	Input Capacitance	Track Mode	30		pF
		Hold Mode	3		pF

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) The ADC will meet Minimum/Maximum specifications for f_{SCL} up to 3.4MHz when operating in the Quiet Interface Mode (Section 1.11).
(3) This parameter is guaranteed by design and/or characterization and is not tested in production.

Electrical Characteristics (continued)

The following specifications apply for V_A = +2.7V to +5.5V, GND = 0V, f_{SCL} up to 3.4MHz, f_{IN} = 1kHz for f_{SCL} up to 400kHz, f_{IN} = 10kHz for f_{SCL} = 3.4MHz unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		Typical (1)	Limits (1)	Units (Limits)
SERIAL INTERFACE INPUT CHARACTERISTICS (SCL, SDA)						
V_{IH}	Input High Voltage				**0.7 x V_A**	V (min)
V_{IL}	Input Low Voltage				**0.3 x V_A**	V (max)
I_{IN}	Input Current (4)				**±1**	µA (max)
C_{IN}	Input Pin Capacitance			3		pF
V_{HYST}	Input Hysteresis				**0.1 x V_A**	V (min)
ADDRESS SELECTION INPUT CHARACTERISTICS (ADDR)						
V_{IH}	Input High Voltage				**V_A - 0.5V**	V (min)
V_{IL}	Input Low Voltage				**0.5**	V (max)
I_{IN}	Input Current (4)				**±1**	µA (max)
LOGIC OUTPUT CHARACTERISTICS, OPEN-DRAIN (SDA, ALERT)						
V_{OL}	Output Low Voltage	I_{SINK} = 3 mA			**0.4**	V (max)
		I_{SINK} = 6 mA			**0.6**	V (max)
I_{OZ}	High-Impedence Output Leakage Current (4)				**±1**	µA (max)
	Output Coding			Straight (Natural) Binary		
POWER REQUIREMENTS						
V_A	Supply Voltage Minimum				**2.7**	V (min)
	Supply Voltage Maximum				**5.5**	V (max)
Continuous Operation Mode -- 2-wire interface active.						
I_N	Supply Current	f_{SCL}=400kHz	V_A = 2.7V to 3.6V	0.08	**0.14**	mA (max)
			V_A = 4.5V to 5.5V	0.16	**0.30**	mA (max)
		f_{SCL}=3.4MHz	V_A = 2.7V to 3.6V	0.37	**0.55**	mA (max)
			V_A = 4.5V to 5.5V	0.74	**0.99**	mA (max)
P_N	Power Consumption	f_{SCL}=400kHz	V_A = 3.0V	0.26		mW
			V_A = 5.0V	0.78		mW
		f_{SCL}=3.4MHz	V_A = 3.0V	1.22		mW
			V_A = 5.0V	3.67		mW
Automatic Conversion Mode -- 2-wire interface stopped and quiet (SCL = SDA = V_A). $f_{SAMPLE} = T_{CONVERT} * 32$						
I_A	Supply Current		V_A = 2.7V to 3.6V	0.41	**0.59**	mA (max)
			V_A = 4.5V to 5.5V	0.78	**1.2**	mA (max)
P_A	Power Consumption		V_A = 3.0V	1.35		mW
			V_A = 5.0V	3.91		mW
Power Down Mode (PD_1) -- 2-wire interface stopped and quiet. (SCL = SDA = V_A). (4)						
I_{PD1}	Supply Current			0.1	**0.2**	µA (max)
P_{PD1}	Power Consumption			0.5	**0.9**	µW (max)
Power Down Mode (PD_2) -- 2-wire interface active. Master communicating with a different device on the bus.						
I_{PD2}	Supply Current	f_{SCL}=400kHz	V_A = 2.7V to 3.6V	13	**45**	µA (max)
			V_A = 4.5V to 5.5V	27	**80**	µA (max)
		f_{SCL}=3.4MHz	V_A = 2.7V to 3.6V	89	**150**	µA (max)
			V_A = 4.5V to 5.5V	168	**250**	µA (max)

(4) This parameter is guaranteed by design and/or characterization and is not tested in production.

Electrical Characteristics (continued)

The following specifications apply for V_A = +2.7V to +5.5V, GND = 0V, f_{SCL} up to 3.4MHz, f_{IN} = 1kHz for f_{SCL} up to 400kHz, f_{IN} = 10kHz for f_{SCL} = 3.4MHz unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		Typical (1)	Limits (1)	Units (Limits)
P_{PD2}	Power Consumption	f_{SCL}=400kHz	V_A = 3.0V	0.04		mW
			V_A = 5.0V	0.14		mW
		f_{SCL}=3.4MHz	V_A = 3.0V	0.29		mW
			V_A = 5.0V	0.84		mW

A.C. and Timing Characteristics

The following specifications apply for V_A = +2.7V to +5.5V. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions (1)	Typical (2)	Limits (2) (1)	Units (Limits)
CONVERSION RATE					
	Conversion Time		1		µs
f_{CONV}	Conversion Rate	f_{SCL} = 100kHz	5.56		ksps
		f_{SCL} = 400kHz	22.2		ksps
		f_{SCL} = 1.7MHz	94.4		ksps
		f_{SCL} = 3.4MHz	188.9		ksps
DIGITAL TIMING SPECS (SCL, SDA)					
f_{SCL}	Serial Clock Frequency	Standard Mode Fast Mode High Speed Mode, C_b = 100pF High Speed Mode, C_b = 400pF		**100** **400** **3.4** **1.7**	kHz (max) kHz (max) MHz (max) MHz (max)
t_{LOW}	SCL Low Time	Standard Mode Fast Mode High Speed Mode, C_b = 100pF High Speed Mode, C_b = 400pF		**4.7** **1.3** **160** **320**	us (min) us (min) ns (min) ns (min)
t_{HIGH}	SCL High Time	Standard Mode Fast Mode High Speed Mode, C_b = 100pF High Speed Mode, C_b = 400pF		**4.0** **0.6** **60** **120**	us (min) us (min) ns (min) ns (min)
$t_{SU;DAT}$	Data Setup Time	Standard Mode Fast Mode High Speed Mode		**250** **100** **10**	ns (min) ns (min) ns (min)
$t_{HD;DAT}$	Data Hold Time	Standard Mode (3)		**0** **3.45**	us (min) us (max)
		Fast Mode (3)		**0** **0.9**	us (min) us (max)
		High Speed Mode, C_b = 100pF		**0** **70**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**0** **150**	ns (min) ns (max)
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard Mode Fast Mode High Speed Mode		**4.7** **0.6** **160**	us (min) us (min) ns (min)
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard Mode Fast Mode High Speed Mode		**4.0** **0.6** **160**	us (min) us (min) ns (min)
t_{BUF}	Bus free time between a stop and start condition	Standard Mode Fast Mode		**4.7** **1.3**	us (min) us (min)

(1) C_b refers to the capacitance of one bus line. C_b is expressed in pF units.
(2) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) The ADC101C021 will provide a minimum data hold time of 300ns to comply with the I^2C Specification.

A.C. and Timing Characteristics (continued)

The following specifications apply for V_A = +2.7V to +5.5V. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions (1)	Typical (2)	Limits (2) (1)	Units (Limits)
$t_{SU;STO}$	Setup time for a stop condition	Standard Mode Fast Mode High Speed Mode		**4.0** **0.6** **160**	us (min) us (min) ns (min)
t_{rDA}	Rise time of SDA signal	Standard Mode		**1000**	ns (max)
		Fast Mode		**20+0.1C_b** **300**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **80**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **160**	ns (min) ns (max)
t_{fDA}	Fall time of SDA signal	Standard Mode		**250**	ns (max)
		Fast Mode		**20+0.1C_b** **250**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **80**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **160**	ns (min) ns (max)
t_{rCL}	Rise time of SCL signal	Standard Mode		**1000**	ns (max)
		Fast Mode		**20+0.1C_b** **300**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **40**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **80**	ns (min) ns (max)
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit.	Standard Mode		**1000**	ns (max)
		Fast Mode		**20+0.1C_b** **300**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **80**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **160**	ns (min) ns (max)
t_{fCL}	Fall time of a SCL signal	Standard Mode		**300**	ns (max)
		Fast Mode		**20+0.1C_b** **300**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **40**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **80**	ns (min) ns (max)
C_b	Capacitive load for each bus line (SCL and SDA)			**400**	pF (max)
t_{SP}	Pulse Width of spike suppressed (4)	Fast Mode High Speed Mode		**50** **10**	ns (max) ns (max)

(4) Spike suppression filtering on SCL and SDA will suppress spikes that are less than 50ns for standard and fast modes, and less than 10ns for hs-mode.

Timing Diagrams

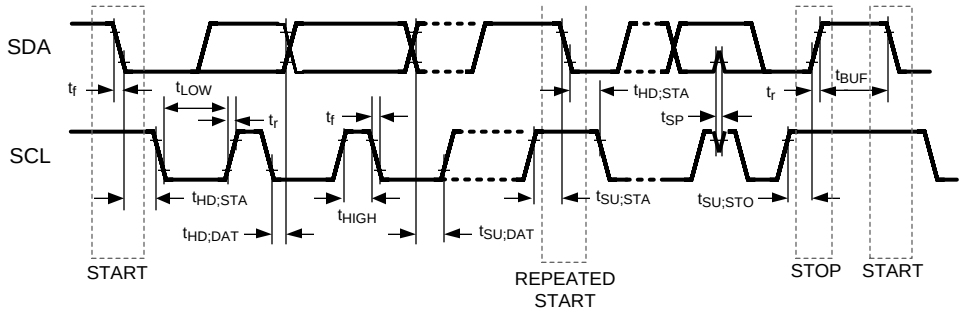


Figure 1. Serial Timing Diagram

Specification Definitions

ACQUISITION TIME is the time required for the ADC to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage.

APERTURE DELAY is the time between the start of a conversion and the time when the input signal is internally acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} - 1.5 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to an individual ADC input at the same time. It is defined as the ratio of the power in both the second and third order intermodulation products to the power in one of the original frequencies. Second order products are $f_a \pm f_b$, where f_a and f_b are the two sine wave input frequencies. Third order products are ($2f_a \pm f_b$) and ($f_a \pm 2f_b$). IMD is usually expressed in dB.

MISSING CODES are those output codes that will never appear at the ADC output. The ADC101C021 is guaranteed not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first n harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \times \log_{10} \sqrt{\frac{A_{f2}^2 + \Lambda + A_{Fn}^2}{A_{f1}^2}} \quad (1)$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{fn} are the RMS power in the first n harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion time.

LEAST SIGNIFICANT BIT (LSB) is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_A / 2^n \quad (2)$$

where V_A is the supply voltage for this product, and "n" is the resolution in bits, which is 10 for the ADC101C021.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_A.

Typical Performance Characteristics

f_{SCL} = 400kHz, f_{SAMPLE} = 22kSPS, f_{IN} = 1kHz, V_A = 5.0V, T_A = +25°C, unless otherwise stated.

INL vs. Code - V_A=3V

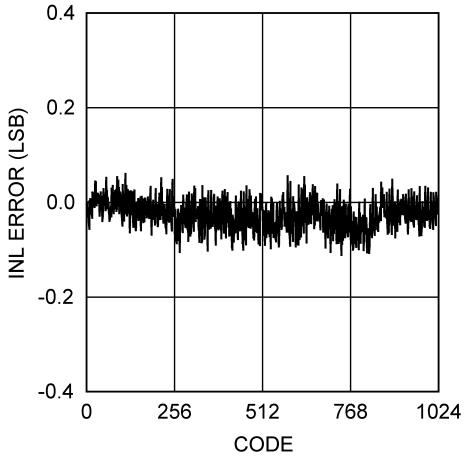


Figure 2.

DNL vs. Code - V_A=3V

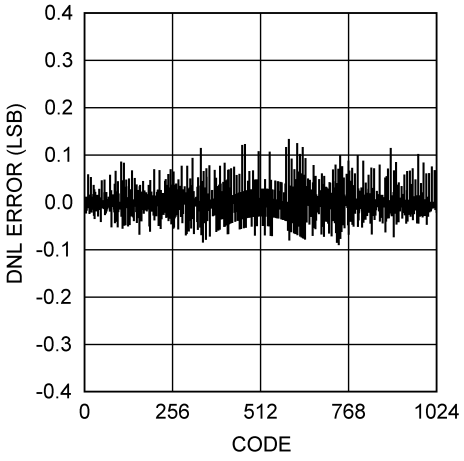


Figure 3.

INL vs. Code - V_A=5V

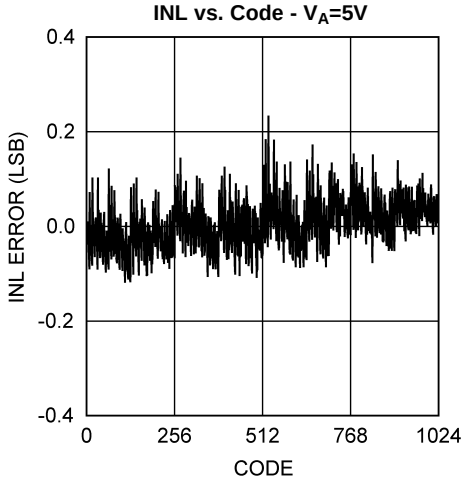


Figure 4.

DNL vs. Code - V_A=5V

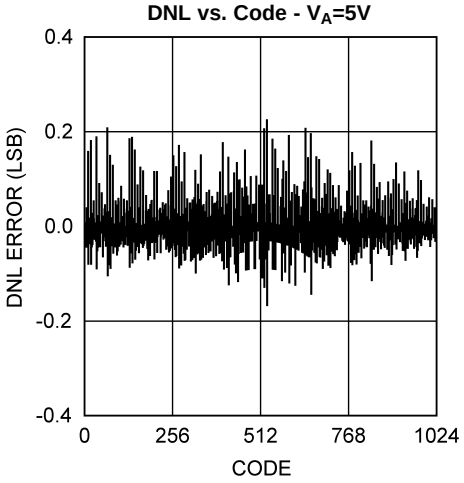


Figure 5.

INL vs. Supply

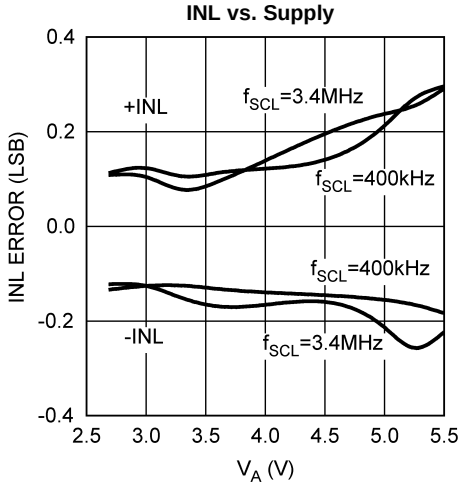


Figure 6.

DNL vs. Supply

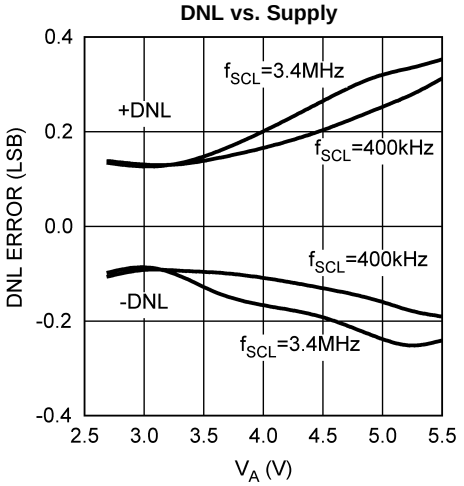


Figure 7.

Typical Performance Characteristics (continued)

f_{SCL} = 400kHz, f_{SAMPLE} = 22kSPS, f_{IN} = 1kHz, V_A = 5.0V, T_A = +25°C, unless otherwise stated.

ENOB vs. Supply

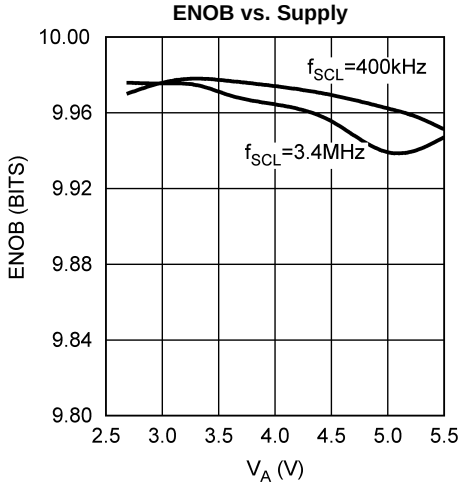


Figure 8.

SINAD vs. Supply

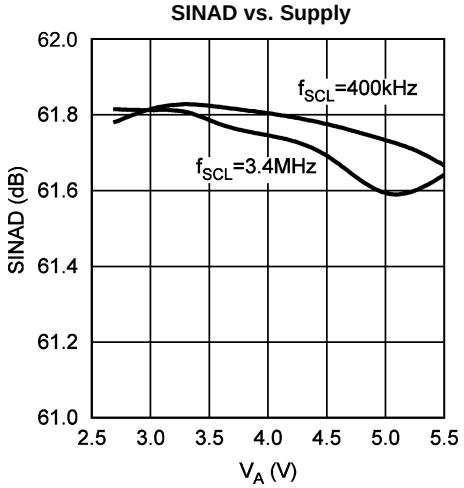


Figure 9.

FFT Plot - V_A=3V

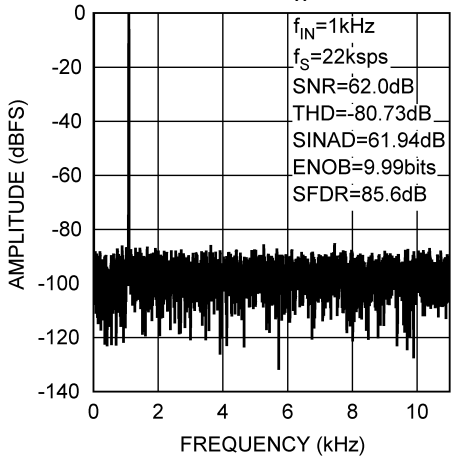


Figure 10.

FFT Plot - V_A=3V

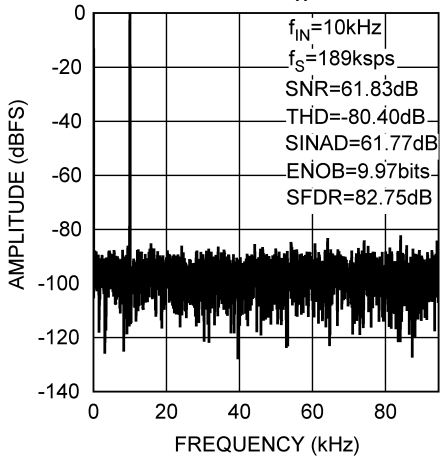


Figure 11.

Offset Error vs. Temperature

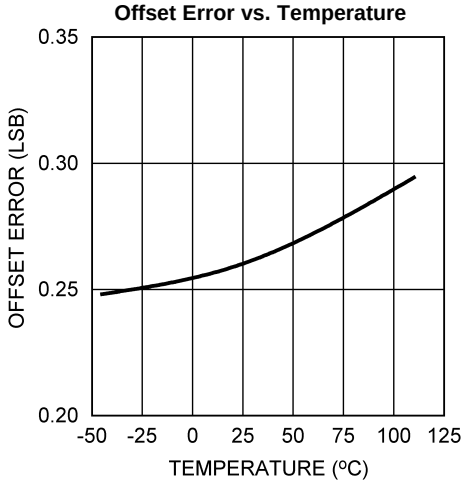


Figure 12.

Gain Error vs. Temperature

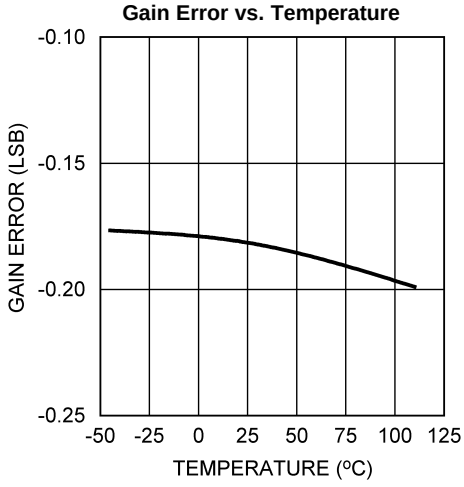


Figure 13.

Typical Performance Characteristics (continued)

f_{SCL} = 400kHz, f_{SAMPLE} = 22kSPS, f_{IN} = 1kHz, V_A = 5.0V, T_A = +25°C, unless otherwise stated.

Continuous Operation Supply Current vs. V_A

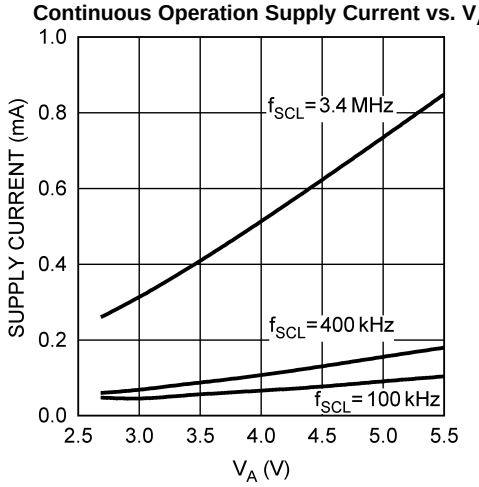


Figure 14.

Automatic Conversion Supply Current vs. V_A

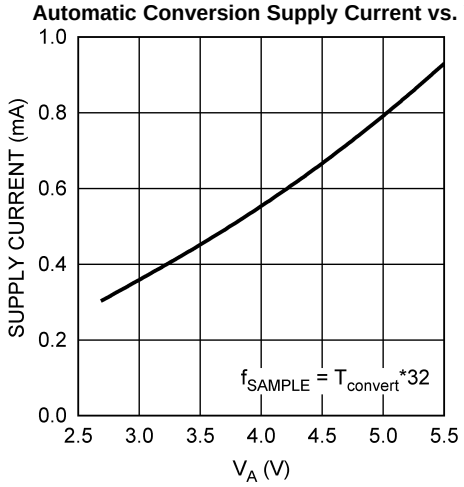


Figure 15.

Power Down (PD_1) Supply Current vs. V_A

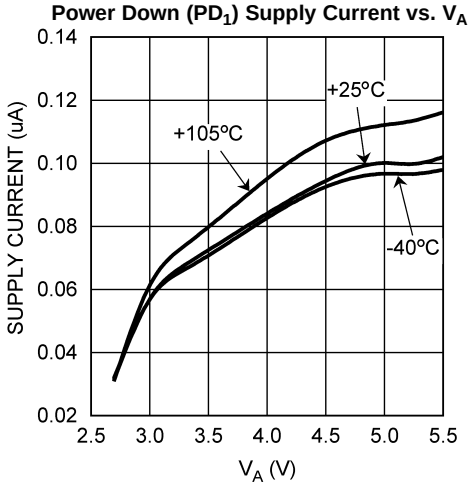


Figure 16.

FUNCTIONAL DESCRIPTION

The ADC101C021 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter. Unless otherwise stated, references to the ADC101C021 in this section will apply to both the ADC101C021 and the ADC101C027.

CONVERTER OPERATION

Simplified schematics of the ADC101C021 in both track and hold modes are shown in Figure 17 and Figure 18, respectively. In Figure 17, the ADC101C021 is in track mode. SW1 connects the sampling capacitor to the analog input channel and SW2 equalizes the comparator inputs. The ADC is in this state for approximately 0.4µs at the beginning of every conversion cycle, which begins at the ACK fall of SDA. Conversions occur when the conversion result register is read and when the ADC is in automatic conversion mode. (see *Section* AUTOMATIC CONVERSION MODE).

Figure 18 shows the ADC101C021 in hold mode. SW1 connects the sampling capacitor to ground and SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is also the digital representation of the analog input voltage. This digital word is stored in the conversion result register and read via the 2-wire interface.

In the Normal (non-Automatic) Conversion mode, a new conversion is started after the previous conversion result is read. In the Automatic Mode, conversions are started at set intervals, as determined by bits D7 through D5 of the Configuration Register. The intent of the Automatic mode is to provide a "watchdog" function to ensure that the input voltage remains within the limits set in the Alert Limit Registers. The minimum and maximum conversion results can then be read from the Lowest Conversion Register and the Highest Conversion Register, as described in *Section* INTERNAL REGISTERS.

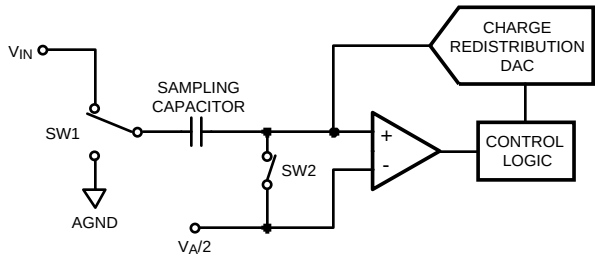


Figure 17. ADC101C021 in Track Mode

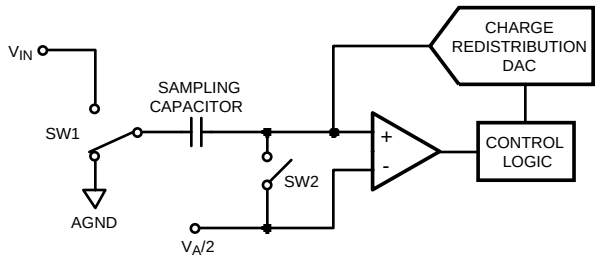


Figure 18. ADC101C021 in Hold Mode

ANALOG INPUT

An equivalent circuit for the input of the ADC101C021 is shown in Figure 19. The diodes provide ESD protection for the analog input. The operating range for the analog input is 0 V to V_A. Going beyond this range will cause the ESD diodes to conduct and may result in erratic operation. For this reason, these diodes should NOT be used to clamp the input signal.

The capacitor C1 in Figure 19 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance (R_{ON}) of the multiplexer and track / hold switch and is typically 500Ω. Capacitor C2 is the ADC101C021 sampling capacitor and is typically 30 pF. The ADC101C021 will deliver best performance when driven by a low-impedance source (less than 100Ω). This is especially important when using the ADC101C021 to sample dynamic signals. A buffer amplifier may be necessary to limit source impedance. Use a precision op-amp to maximize circuit performance. Also important when sampling dynamic signals is a band-pass or low-pass filter to reduce noise at the input.

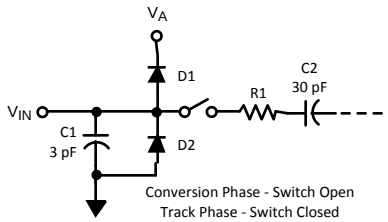


Figure 19. Equivalent Input Circuit

The analog input is sampled for eight internal clock cycles, or for typically 400 ns, after the fall of SDA for acknowledgement. This time could be as long as about 530 ns. The sampling switch opens and the conversion begins this time after the fall of ACK. This time are typical at room temperature and may vary with temperature.

ADC TRANSFER FUNCTION

The output format of the ADC101C021 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC101C021 is V_A / 1024. The ideal transfer characteristic is shown in Figure 20. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of V_A / 2048. Other code transitions occur at intervals of 1 LSB.

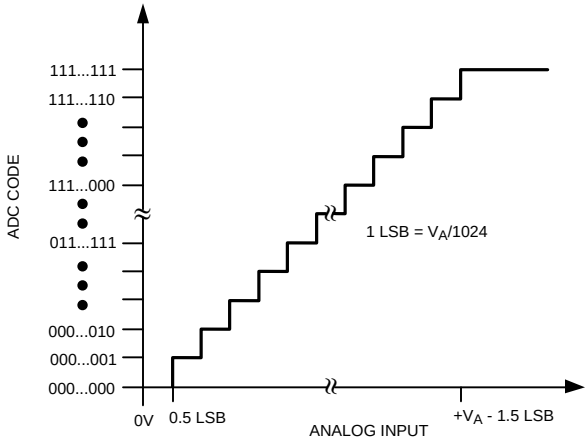


Figure 20. Ideal Transfer Characteristic

REFERENCE VOLTAGE

The ADC101C021 uses the supply (V_A) as the reference, so V_A must be treated as a reference. The analog-to-digital conversion will only be as precise as the reference (V_A), so the supply voltage should be free of noise. The reference should be driven by a low output impedance voltage source.

The Applications section provides recommended ways to provide the supply voltage appropriately. Refer to *Section* TYPICAL APPLICATION CIRCUIT for details.

POWER-ON RESET

An internal power-on reset (POR) occurs when the supply voltage transitions above the power-on reset threshold. Each of the registers contains a defined value upon POR and this data remains there until any of the following occurs:

- The first conversion is completed, causing the Conversion Result and Status registers to be updated.
- A different data word is written to a writable register.
- The ADC is powered down.

The internal registers will lose their contents if the supply voltage goes below 2.4V. Should this happen, it is important that the V_A supply be lowered to a maximum of 200mV before the supply is raised again to properly reset the device and ensure that the ADC performs as specified.

INTERNAL REGISTERS

The ADC101C021 has 8 internal data registers and one address pointer. The registers provide additional ADC functions such as storing minimum and maximum conversion results, setting alert threshold levels, and storing data to configure the operation of the device. Figure 21 shows all of the registers and their corresponding address pointer values. All of the registers are read/write capable except the conversion result register, which is read-only.

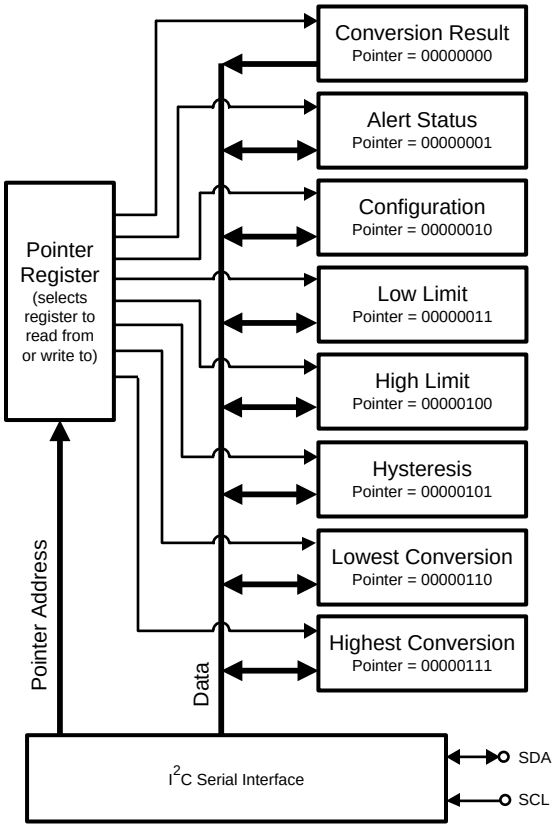


Figure 21. Register Structure

Address Pointer Register

The address pointer determines which of the data registers is accessed by the I^2C interface. The first data byte of every write operation is stored in the address pointer register. This value selects the register that the following data bytes will be written to or read from. Only the three LSBs of this register are variable. The other bits must always be written to as zeros. After a power-on reset, the pointer register defaults to all zeros (conversion result register).

Default Value: 00h

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	Register Select		

P2	P1	P0	REGISTER
0	0	0	Conversion Result (read only)
0	0	1	Alert Status (read/write)
0	1	0	Configuration (read/write)
0	1	1	Low Limit (read/write)
1	0	0	High Limit (read/write)
1	0	1	Hysteresis (read/write)
1	1	0	Lowest Conversion (read/write)
1	1	1	Highest Conversion (read/write)

Conversion Result Register

This register holds the result of the most recent conversion. In the normal mode, a new conversion is started whenever this register is read. The conversion result data is in straight binary format with the MSB at D11.

Pointer Address 00h (Read Only)

Default Value: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
Alert Flag	Reserved			Conversion Result [9:6]			

D7	D6	D5	D4	D3	D2	D1	D0
Conversion Result [5:0]						Reserved	

Bits	Name	Description
15	Alert Flag	This bit indicates when an alert condition has occurred. When the Alert Bit Enable is set in the Configuration Register, this bit will be high if either alert flag is set in the Alert Status Register. Otherwise, this bit is a zero. The I^2C controller will typically read the Alert Status register and other data registers to determine the source of the alert.
14:12	Reserved	Always reads zeros.
11:2	Conversion Result	The Analog-to-Digital conversion result. The Conversion result data is a 10-bit data word in straight binary format. The MSB is D11.
1:0	Reserved	Always reads zeros.

Alert Status Register

This register indicates if a high or a low threshold has been violated. The bits of this register are active high. That is, a high indicates that the respective limit has been violated.

Pointer Address 01h (Read/Write)

Default Value: 00h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						Over Range Alert	Under Range Alert

Bits	Name	Description
7:2	Reserved	Always reads zeros. Zeros must be written to these bits.
1	Over Range Alert Flag	Bit is set to 1 when the measured voltage exceeds the V_{HIGH} limit stored in the programmable V_{HIGH} limit register. Flag is reset to 0 when one of the following two conditions is met: (1) The controller writes a one to this bit. (2) The measured voltage decreases below the programmed V_{HIGH} limit minus the programmed V_{HYST} value (See Figure 24) . The alert will only self-clear if the Alert Hold bit is cleared in the Configuration register. If the Alert Hold bit is set, the only way to clear an over range alert is to write a one to this bit.
0	Under Range Alert Flag	Bit is set to 1 when the measured voltage falls below the V_{LOW} limit stored in the programmable V_{LOW} limit register. Flag is reset to 0 when one of the following two conditions is met: (1) The controller writes a one to this bit. (2) The measured voltage increases above the programmed V_{LOW} limit plus the programmed V_{HYST} value. The alert will only self-clear if the Alert Hold bit is cleared in the Configuration register. If the Alert Hold bit is set, the only way to clear an under range alert is to write a one to this bit.

Configuration Register

Pointer Address 02h (Read/Write)

Default Value: 00h

D7	D6	D5	D4	D3	D2	D1	D0
Cycle Time [2:0]			Alert Hold	Alert Flag Enable	Alert Pin Enable	0	Polarity

Cycle Time[2:0]			Conversion Interval	Typical $f_{convert}$ (ksps)
D7	D6	D5		
0	0	0	Mode Disabled	0
0	0	1	$T_{convert}$ x 32	27
0	1	0	$T_{convert}$ x 64	13.5
0	1	1	$T_{convert}$ x 128	6.7
1	0	0	$T_{convert}$ x 256	3.4
1	0	1	$T_{convert}$ x 512	1.7
1	1	0	$T_{convert}$ x 1024	0.9
1	1	1	$T_{convert}$ x 2048	0.4

Bits	Name	Description
7:5	Cycle Time	Configures Automatic Conversion mode. When these bits are set to zeros, the automatic conversion mode is disabled. This is the case at power-up. When these bits are set to a non-zero value, the ADC will begin operating in automatic conversion mode. (See AUTOMATIC CONVERSION MODE). The Cycle Time table shows how different values provide various conversion intervals.
4	Alert Hold	0: Alerts will self-clear when the measured voltage moves within the limits by more than the hysteresis register value. 1: Alerts will not self-clear and are only cleared when a one is written to the alert high flag or the alert low flag in the Alert Status register.
3	Alert Flag Enable	0: Disables alert status bit [D15] in the Conversion Result register. 1: Enables alert status bit [D15] in the Conversion Result register.
2	Alert Pin Enable	0: Disables the ALERT output pin. The ALERT output will TRI-STATE when the pin is disabled. 1: Enables the ALERT output pin. *This bit does not apply to the ADC101C027.
1	Reserved	Always reads zeros. Zeros must be written to these bits.
0	Polarity	This bit configures the active level polarity of the ALERT output pin. 0: Sets the ALERT pin to active low. 1: Sets the ALERT pin to active high. *This bit does not apply to the ADC101C027.

V_{LOW} -- Alert Limit Register - Under Range

This register holds the lower limit threshold used to determine the alert condition. If the conversion moves lower than this limit, a V_{LOW} alert is generated.

Pointer Address 03h (Read/Write)

Default Value: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				V_{LOW} Limit [9:6]			

D7	D6	D5	D4	D3	D2	D1	D0
V_{LOW} Limit [5:0]						Reserved	

Bits	Name	Description
15:12	Reserved	Always reads zeros. Zeros must be written to these bits.
11:2	V_{LOW} Limit	Sets the lower limit threshold used to determine the alert condition. If the conversion moves lower than this limit, a V_{LOW} alert is generated.
1:0	Reserved	Always reads zeros. Zeros must be written to these bits.

V_{HIGH} -- Alert Limit Register - Over Range

This register holds the upper limit threshold used to determine the alert condition. If the conversion moves higher than this limit, a V_{HIGH} alert is generated.

Pointer Address 04h (Read/Write)

Default Value: 0FFFh

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				V_{HIGH} Limit [9:6]			

D7	D6	D5	D4	D3	D2	D1	D0
V_{HIGH} Limit [5:0]						Reserved	

Bits	Name	Description
15:12	Reserved	Always reads zeros. Zeros must be written to these bits.
11:2	V_{HIGH} Limit	Sets the upper limit threshold used to determine the alert condition. If the conversion moves higher than this limit, a V_{HIGH} alert is generated.
1:0	Reserved	Always reads zeros. Zeros must be written to these bits.

V_{HYST} -- Alert Hysteresis Register

This register holds the hysteresis value used to determine the alert condition. After a V_{HIGH} or V_{LOW} alert occurs, the conversion result must move within the V_{HIGH} or V_{LOW} limit by more than this value to clear the alert condition. **Note:** If the Alert Hold bit is set in the configuration register, alert conditions will not self-clear.

Pointer Address 05h (Read/Write)

Default Value: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				Hysteresis [9:6]			

D7	D6	D5	D4	D3	D2	D1	D0
Hysteresis [5:0]						Reserved	

Bits	Name	Description
15:12	Reserved	Always reads zeros. Zeros must be written to these bits.
11:2	Hysteresis	Sets the hysteresis value used to determine the alert condition. D11 is MSB. After a V_{HIGH} or V_{LOW} alert occurs, the conversion result must move within the V_{HIGH} or V_{LOW} limit by more than this value to clear the alert condition. Note: If the Alert Hold bit is set in the configuration register, alert conditions will not self-clear.
1:0	Reserved	Always reads zeros. Zeros must be written to these bits.

V_{MIN} -- Lowest Conversion Register

This register holds the Lowest Conversion result when in the automatic conversion mode. Each conversion result is compared against the contents of this register. If the value is lower, it becomes the lowest conversion and replaces the current value. If the value is higher, the register contents remain unchanged. The lowest conversion value can be cleared at any time by writing 0FFFh to this register. The value of this register will update automatically when the automatic conversion mode is enabled, but is NOT updated in the normal mode.

Pointer Address 06h (Read/Write)

Default Value: 0FFFh

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				Lowest Conversion [9:6]			

D7	D6	D5	D4	D3	D2	D1	D0
Lowest Conversion [5:0]						Reserved	

Bits	Name	Description
15:12	Reserved	Always reads zeros. Zeros must be written to these bits.
11:2	Lowest Conversion	Contains the Lowest Conversion result. D11 is MSB.
1:0	Reserved	Always reads zeros. Zeros must be written to these bits.

V_{MAX} -- Highest Conversion Register

This register holds the Highest Conversion result when in the Automatic mode. Each conversion result is compared against the contents of this register. If the value is higher, it replaces the previous value. If the value is lower, the register contents remain unchanged. The highest conversion value can be cleared at any time by writing 0000h to this register. The value of this register will update automatically when the automatic conversion mode is enabled, but is NOT updated in the normal mode.

Pointer Address 07h (Read/Write)

Default Value: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				Highest Conversion [9:6]			

D7	D6	D5	D4	D3	D2	D1	D0
Highest Conversion [5:0]						Reserved	

Bits	Name	Description
15:12	Reserved	Always reads zeros. Zeros must be written to these bits.
11:2	Highest Conversion	Highest conversion result. D11 is MSB.
1:0	Reserved	Always reads zeros. Zeros must be written to these bits.

SERIAL INTERFACE

The I^2C-compatible interface operates in all three speed modes. Standard mode (100kHz) and Fast mode (400kHz) are functionally the same and will be referred to as Standard-Fast mode in this document. High-Speed mode (3.4MHz) is an extension of Standard-Fast mode and will be referred to as Hs-mode in this document.

The following diagrams describe the timing relationships of the clock (SCL) and data (SDA) signals. Pull-up resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The ADC101C021 offers extended ESD tolerance (8kV HBM) for the I^2C bus pins (SCL & SDA) allowing extension of the bus across multiple boards without extra ESD protection.

Basic I^2C Protocol

The I^2C interface is bi-directional and allows multiple devices to operate on the same bus. The bus consists of master devices and slave devices which can communicate back and forth over the I^2C interface. Master devices control the bus and are typically microcontrollers, FPGAs, DSPs, or other digital controllers. Slave devices are controlled by a master and are typically peripheral devices such as the ADC101C021. To support multiple devices on the same bus, each slave has a unique hardware address which is referred to as the "slave address." To communicate with a particular device on the bus, the controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit. If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled high. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus.

All communication on the bus begins with either a Start condition or a Repeated Start condition. The protocol for starting the bus varies between Standard-Fast mode and Hs-mode. In Standard-Fast mode, the master generates a Start condition by driving SDA from high to low while SCL is high. In Hs-mode, starting the bus is more complicated. Please refer to *Section* High-Speed (Hs) Mode for the full details of a Hs-mode Start condition.

A Repeated Start is generated to address a different device or register, or to switch between read and write modes. The master generates a Repeated Start condition by driving SDA low while SCL is high. Following the Repeated Start, the master sends out the slave address and a read/write bit as shown in Figure 22. The bus continues to operate in the same speed mode as before the Repeated Start condition.

All communication on the bus ends with a Stop condition. In either Standard-Fast mode or Hs-Mode, a Stop condition occurs when SDA is pulled high while SCL is high. After a Stop condition, the bus remains idle until a master generates another Start condition.

Please refer to the Philips $I^2C^®$ Specification (Version 2.1 Jan, 2000) for a detailed description of the serial interface.

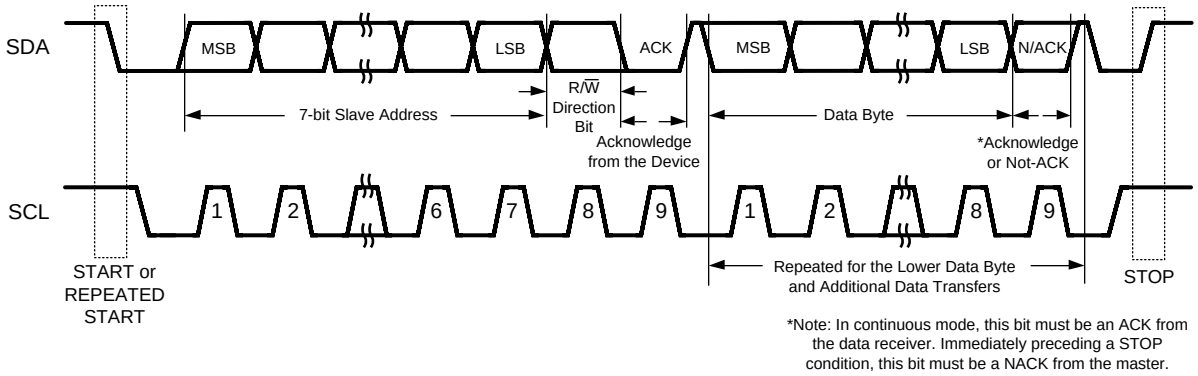


Figure 22. Basic Operation.

Standard-Fast Mode

In Standard-Fast mode, the master generates a start condition by driving SDA from high to low while SCL is high. The start condition is always followed by a 7-bit slave address and a Read/Write bit. After these 8 bits have been transmitted by the master, SDA is released by the master and the ADC101C021 either ACKs or NACKs the address. If the slave address matches, the ADC101C021 ACKs the master. If the address doesn't match, the ADC101C021 NACKs the master.

For a **write** operation, the master follows the ACK by sending the 8-bit register address pointer to the ADC. Then the ADC101C021 ACKs the transfer by driving SDA low. Next, the master sends the upper 8-bits to the ADC101C021. Then the ADC101C021 ACKs the transfer by driving SDA low. For a single byte transfer, the master should generate a stop condition at this point. For a 2-byte write operation, the lower 8-bits are sent by the master. The ADC101C021 then ACKs the transfer, and the master either sends another pair of data bytes, generates a Repeated Start condition to read or write another register, or generates a Stop condition to end communication.

A **read** operation can take place either of two ways:

If the address pointer is pre-set before the read operation, the desired register can be read immediately following the slave address. In this case, the upper 8-bits of the register, set by the pre-set address pointer, are sent out by the ADC. For a single byte read operation, the Master sends a NACK to the ADC and generates a Stop condition to end communication after receiving 8-bits of data. For a 2-byte read operation, the Master continues the transmission by sending an ACK to the ADC. Then the ADC sends out the lower 8-bits of the ADC register. At this point, the master either sends an ACK to receive more data or, a NACK followed by a Stop or Repeated Start. If the master sends an ACK, the ADC sends the next upper data byte, and the read cycle repeats.

If the ADC101C021 address pointer needs to be set, the master needs to write to the device and set the address pointer before reading from the desired register. This type of read requires a start, the slave address, a write bit, the address pointer, a Repeated Start (if appropriate), the slave address, and a read bit (refer to Figure 27). Following this sequence, the ADC sends out the upper 8-bits of the register. For a single byte read operation, the Master must then send a NACK to the ADC and generate a Stop condition to end communication. For a 2-Byte write operation, the Master sends an ACK to the ADC. Then, the ADC sends out the lower 8-bits of the ADC register. At this point, the master sends either an ACK to receive more data, or a NACK followed by a Stop or Repeated Start. If the master sends an ACK, the ADC sends another pair of data bytes, and the read cycle will repeat. The number of data words that can be read is unlimited.

High-Speed (Hs) Mode

For Hs-mode, the sequence of events to begin communication differs slightly from Standard-Fast mode. Figure 23 describes this in further detail. Initially, the bus begins running in Standard-Fast mode. The master generates a Start condition and sends the 8-bit Hs master code (00001XXX) to the ADC101C021. Next, the ADC101C021 responds with a NACK. Once the SCL line has been pulled to a high level, the master switches to Hs-mode by increasing the bus speed and generating a second Repeated Start condition (driving SDA low while SCL is pulled high). At this point, the master sends the slave address to the ADC101C021, and communication continues as shown above in the "Basic Operation" Diagram (see Figure 22).

When the master generates a Repeated Start condition while in Hs-mode, the bus stays in Hs-mode awaiting the slave address from the master. The bus continues to run in Hs-mode until a Stop condition is generated by the master. When the master generates a Stop condition on the bus, the bus must be started in Standard-Fast mode again before increasing the bus speed and switching to Hs-mode.

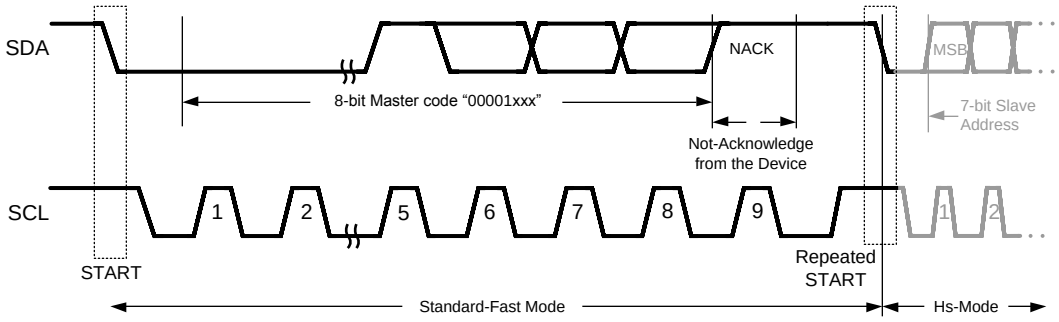


Figure 23. Beginning Hs-Mode Communication

I^2C Slave (Hardware) Address

The ADC has a seven-bit hardware address which is also referred to as a slave address. For the VSSOP-8 version of the ADC101C021, this address is configured by the ADR0 and ADR1 addres selection inputs. For the ADC101C027, the address is configured by the ADR0 address selection input. ADR0 and ADR1 can be grounded, left floating, or tied to V_A. If desired, ADR0 can be set to $V_A/2$ rather than left floating. The state of these inputs sets the hardware address that the ADC responds to on the I^2C bus (see Table 3). For the SOT-6 version of the ADC101C021, the hardware address is not pin-configurable and is set to 1010100. The diagrams in COMMUNICATING WITH THE ADC101C021 describe how the I^2C controller should address the ADC via the I^2C interface.

Pin compatible alternatives that provide additional address options to the SOT-6 version of the ADC101C021 and the ADC101C027 are available.

Table 3. Slave Addresses

Slave Address [A6 - A0]	ADC101C027 (SOT-6)	ADC101C021 (SOT-6)	ADC101C021 (VSSOP-8)	
	ADR0	ALERT	ADR1	ADR0
1010000	Floating	----------	Floating	Floating
1010001	GND	----------	Floating	GND
1010010	V_A	----------	Floating	V_A
1010100	----------	Single Address	GND	Floating
1010101	----------	----------	GND	GND
1010110	----------	----------	GND	V_A
1011000	----------	----------	V_A	Floating
1011001	----------	----------	V_A	GND
1011010	----------	----------	V_A	V_A

ALERT FUNCTION

The ALERT function is an "out-of-range" indicator. At the end of every conversion, the measured voltage is compared to the values in the V_{HIGH} and V_{LOW} registers. If the measured voltage exceeds the value stored in V_{HIGH} or falls below the value stored in V_{LOW}, an alert condition occurs. The Alert condition is indicated in up to three places. First, the alert condition always causes either or both of the alert flags in the Alert Status register to go high. If the measured voltage exceeds the V_{HIGH} limit, the Over Range Alert Flag is set. If the measured voltage falls below the V_{LOW} limit, the Under Range Alert Flag is set. Second, if the Alert Flag Enable bit is set in the Configuration register, the alert condition also sets the MSB of the Conversion Result register. Third, if the Alert Pin Enable bit is set in the Configuration register, the ALERT output becomes active (see Figure 24). The ALERT output (ADC101S021 only) can be configured as an active high or active low output via the Polarity bit in the Configuration register. If the Polarity bit is cleared, the ALERT output is configured as active low. If the Polarity bit is set, the ALERT output is configured as active high.

The Over Range Alert condition is cleared when one of the following two conditions is met:

1. The controller writes a one to the Over Range Alert Flag bit.
2. The measured voltage goes below the programmed V_{HIGH} limit minus the programmed V_{HYST} value and the Alert Hold bit is cleared in the Configuration register. (see Figure 24). If the Alert Hold bit is set, the alert condition persists and only clears when a one is written to the Over Range Alert Flag bit.

The Under Range Alert condition is cleared when one of the following two conditions is met:

1. The controller writes a one to the Under Range Alert Flag bit.
2. The measured voltage goes above the programmed V_{LOW} limit plus the programmed V_{HYST} value and the Alert Hold bit is cleared in the Configuration register. If the Alert Hold bit is set, the alert condition persists and only clears when a one is written to the Under Range Alert Flag bit.

If the alert condition has been cleared by writing a one to the alert flag while the measured voltage still violates the V_{HIGH} or V_{LOW} limits, an alert condition will occur again after the completion of the next conversion (see Figure 25).

Alert conditions only occur if the input voltage exceeds the V_{HIGH} limit or falls below the V_{LOW} limit at the sample-hold instant. The input voltage can exceed the V_{HIGH} limit or fall below the V_{LOW} limit briefly between conversions without causing an alert condition.

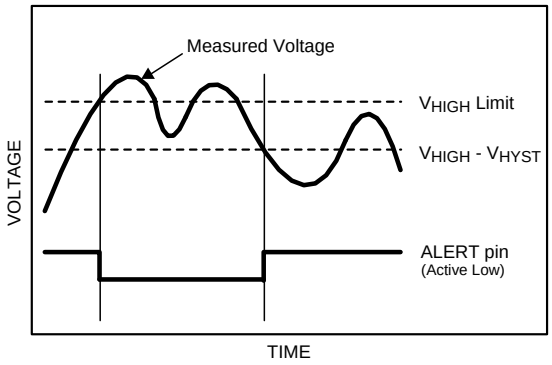


Figure 24. Alert condition cleared when measured voltage crosses V_{HIGH} - V_{HYST}

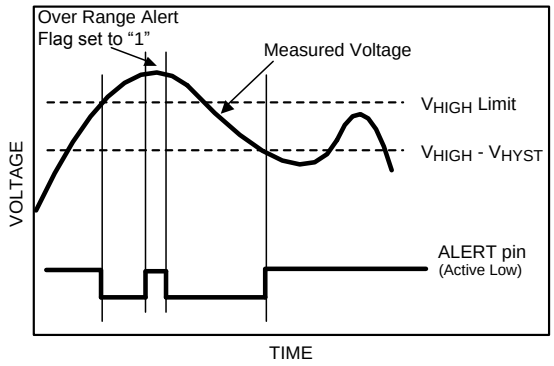


Figure 25. Alert condition cleared by writing a "1" to the Alert Flag.

AUTOMATIC CONVERSION MODE

The automatic conversion mode configures the ADC to continually perform conversions without receiving "read" instructions from the controller over the I^2C interface. The mode is activated by writing a non-zero value into the Cycle Time bits - D[7:5] - of the Configuration register (see Configuration Register). Once the ADC101C021 enters this mode, the internal oscillator is always enabled. The ADC's control logic samples the input at the sample rate set by the cycle time bits. Although the conversion result is not transmitted by the 2-wire interface, it is stored in the conversion result register and updates the various status registers of the device.

In automatic conversion mode, the out-of-range alert function is active and updates after every conversion. The ADC can operate independently of the controller in automatic conversion mode. When the input signal goes "out-of-range", an alert signal is sent to the controller. The controller can then read the status registers and determine the source of the alert condition. Also, comparison and updating of the V_{MIN} and V_{MAX} registers occur after every conversion in automatic conversion mode. The controller can occasionally read the V_{MIN} and/or V_{MAX} registers to determine the sampled input extremes. These register values persist until the user resets the V_{MIN} and V_{MAX} registers. These two features are useful in system monitoring, peak detection, and sensing applications.

COMMUNICATING WITH THE ADC101C021

The ADC101C021's data registers are selected by the address pointer (see Address Pointer Register). To read/write a specific data register, the pointer must be set to that register's address. The pointer is always written at the beginning of a write operation. When the pointer needs to be updated for a read cycle, a write operation must precede the read operation to set the pointer address correctly. On the other hand, if the pointer is preset correctly, a read operation can occur without writing the address pointer register. The following timing diagrams describe the various read and write operations supported by the ADC.

Reading from a 2-Byte ADC Register

The following diagrams indicate the sequence of actions required for a 2-Byte read from an ADC101C021 Register.

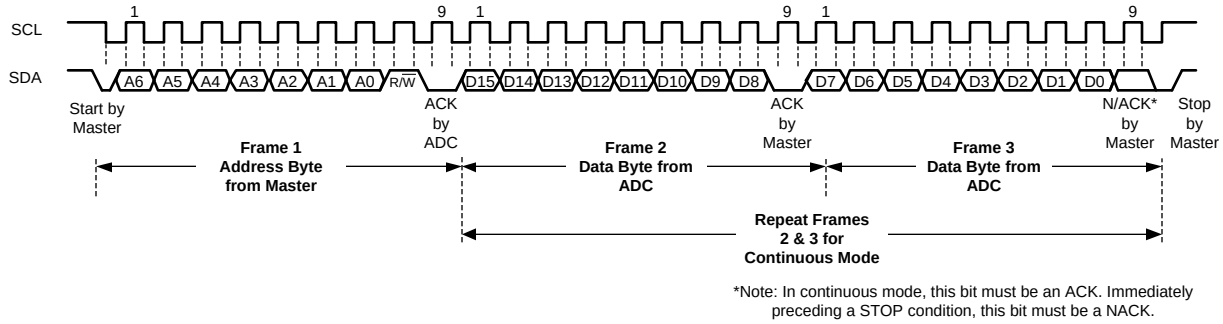


Figure 26. Typical Read from a 2-Byte ADC Register with Preset Pointer

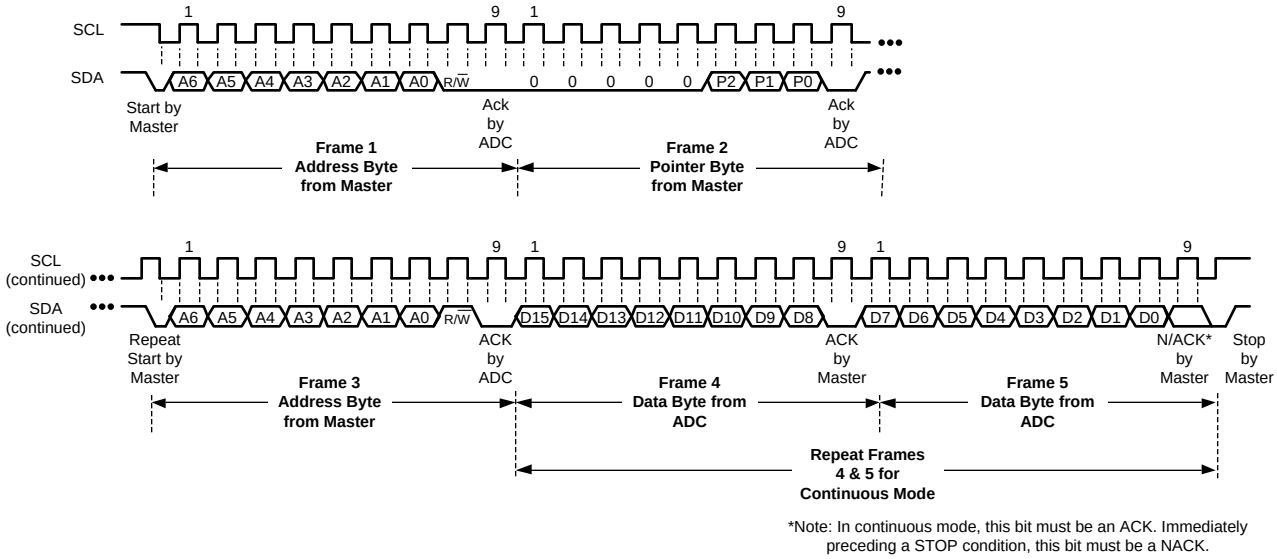


Figure 27. Typical Pointer Set Followed by Immediate Read of a 2-Byte ADC Register

Reading from a 1-Byte ADC Register

The following diagrams indicate the sequence of actions required for a single Byte read from an ADC101C021 Register.

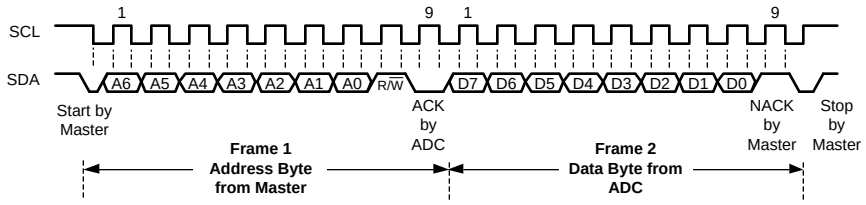


Figure 28. Typical Read from a 1-Byte ADC Register with Preset Pointer

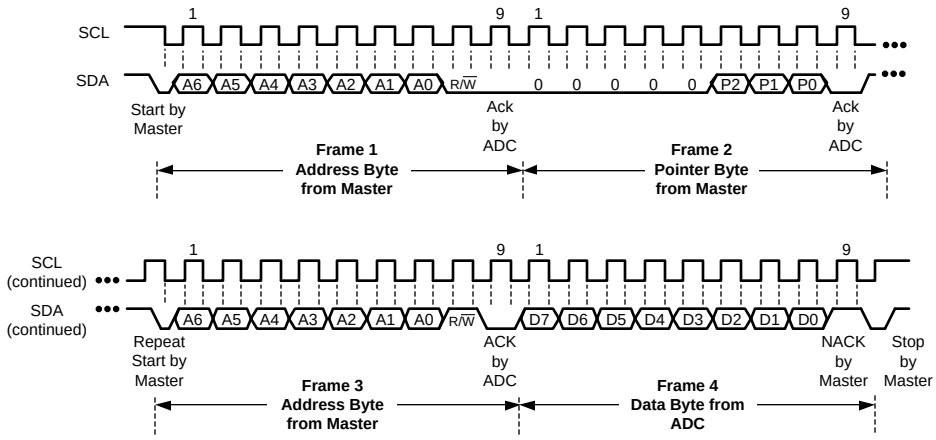


Figure 29. Typical Pointer Set Followed by Immediate Read of a 1-Byte ADC Register

Writing to an ADC Register

The following diagrams indicate the sequence of actions required for writing to an ADC101C021 Register.

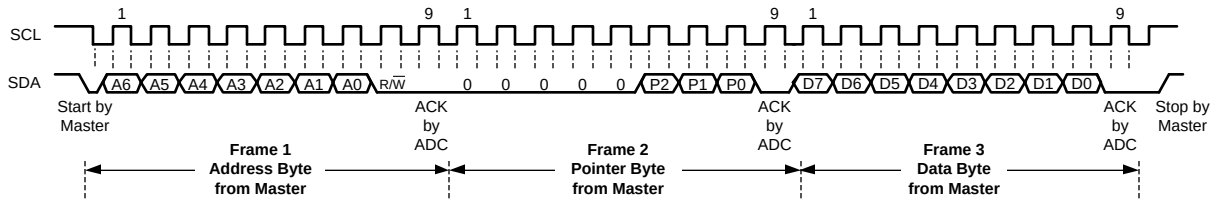


Figure 30. Typical Write to a 1-Byte ADC Register

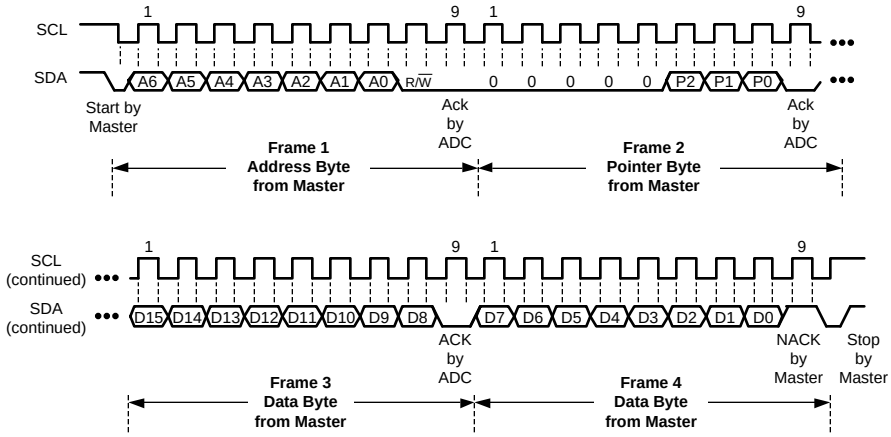


Figure 31. Typical Write to a 2-Byte ADC Register

QUIET INTERFACE MODE

To improve performance at High Speed, operate the ADC in Quiet Interface Mode. This mode provides improved INL and DNL performance in I^2C Hs-Mode (3.4MHz). The Quiet Interface mode provides a maximum throughput rate of 162ksps. Figure 32 describes how to read the conversion result register in this mode. Basically, the Master needs to release SCL for at least 1µs before the MSB of every upper data byte. The diagram assumes that the address pointer register is set to its default value.

Quiet Interface mode will only improve INL and DNL performance in Hs-Mode. Standard and Fast mode performance is unaffected by the Quiet Interface mode.

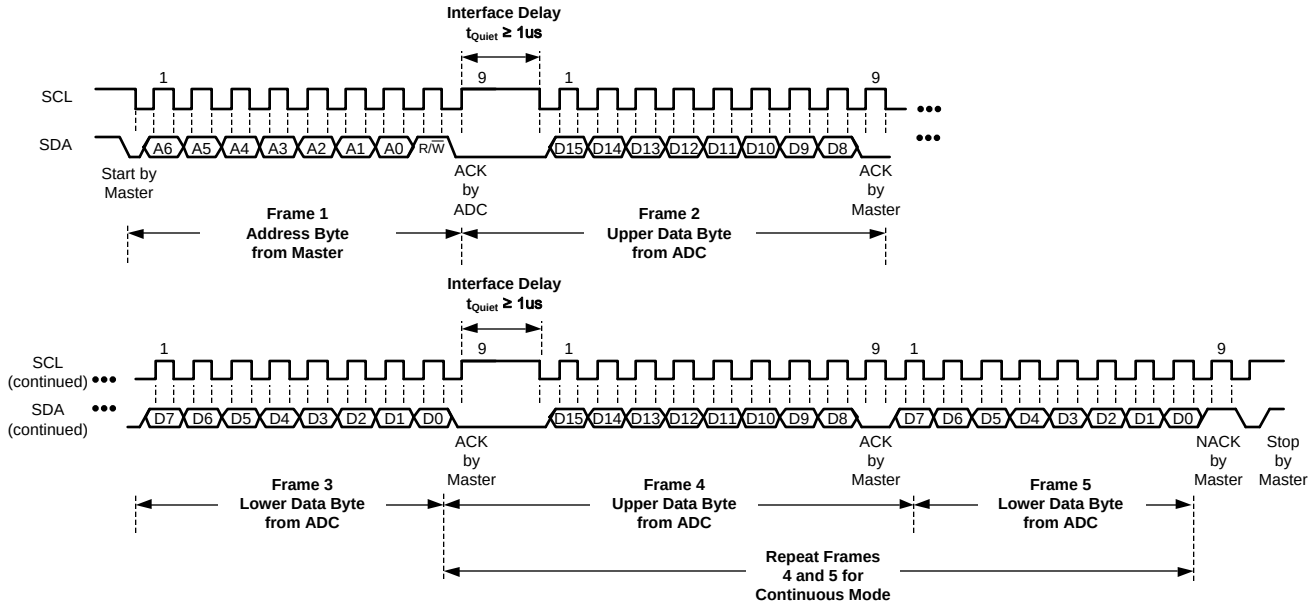


Figure 32. Reading in Quiet Interface Mode

TYPICAL APPLICATION CIRCUIT

A typical application circuit is shown in Figure 33. The analog supply is bypassed with a capacitor network located close to the ADC101C021. The ADC uses the analog supply (V_A) as its reference voltage, so it is very important that V_A be kept as clean as possible. Due to the low power requirements of the ADC101C021, it is possible to use a precision reference as a power supply.

The bus pull-up resistors (R_P) should be powered by the controller's supply. It is important that the pull-up resistors are pulled to the same voltage potential as V_A. This will ensure that the logic levels of all devices on the bus are compatible. If the controller's supply is noisy, an appropriate bypass capacitor should be added between the controller's supply pin and the pull-up resistors. For Hs-mode applications, this bypass capacitance will improve the accuracy of the ADC.

The value of the pull-up resistors (R_P) depends upon the characteristics of each particular I^2C bus. The I^2C specification describes how to choose an appropriate value. As a general rule-of-thumb, we suggest using a 1kΩ resistor for Hs-mode bus configurations and a 5kΩ resistor for Standard or Fast Mode bus configurations. Depending upon the bus capacitance, these values may or may not be sufficient to meet the timing requirements of the I^2C bus specification. Please see the I^2C specification for further information.

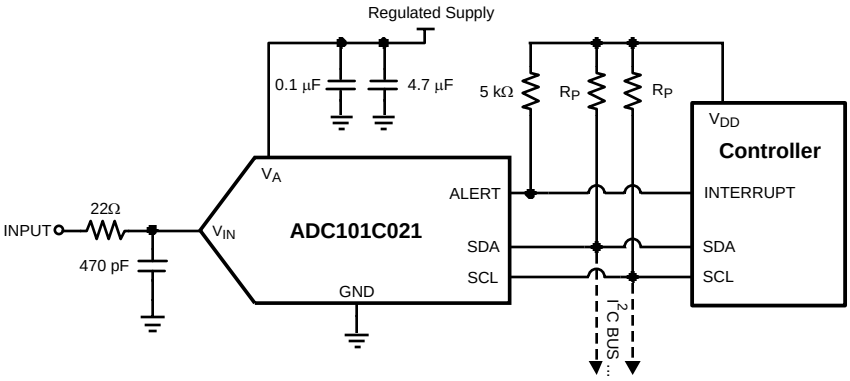


Figure 33. Typical Application Circuit

BUFFERED INPUT

A buffered input application circuit is shown in Figure 34. The analog input is buffered by a National Semiconductor LMP7731. The non-inverting amplifier configuration provides a buffered gain stage for a single ended source. This application circuit is good for single-ended sensor interface. The input must have a DC bias level that keeps the ADC input signal from swinging below GND or above the supply (+5V in this case).

The LM4132, with its 0.05% accuracy over temperature, is an excellent choice as a reference source for the ADC101C021.

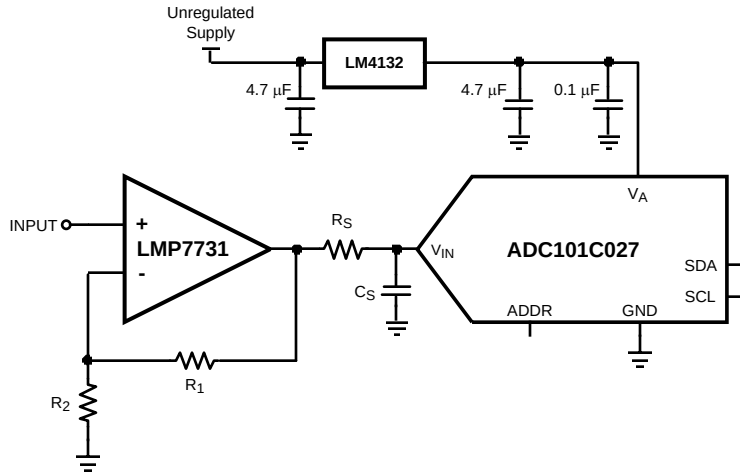


Figure 34. Buffered Input Circuit

INTELLIGENT BATTERY MONITOR

The ADC101C021 is easily used as an intelligent battery monitor. The simple circuit shown in Figure 35, uses the ADC101C021, the LP2980 fixed reference, and a resistor divider to implement an intelligent battery monitor with a window supervisory feature. The window supervisory feature is implemented by the "out of range" alert function. When the battery is recharging, the Over Range Alert will indicate that the charging cycle is complete (see Figure 36). When the battery is nearing depletion, the Under Range Alert will indicate that the battery is low (see Figure 37).

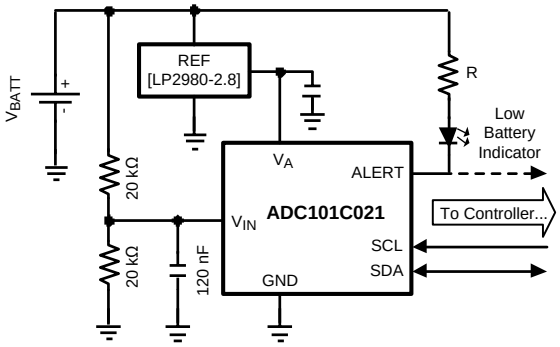


Figure 35. Intelligent Battery Monitor Circuit

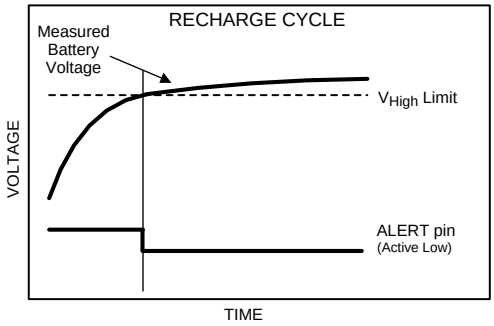


Figure 36. Recharge Cycle

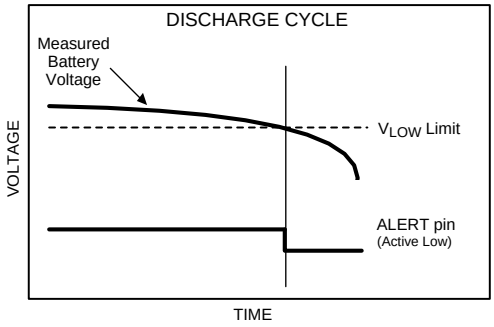


Figure 37. Discharge Cycle

In addition to the window supervisory feature, the ADC101C021 will allow the controller to read the battery voltage at any time during operation.

The accurate voltage reading and the alert feature will allow a controller to improve the efficiency of a battery-powered device. During the discharge cycle, the controller can switch to a low-battery mode, safely suspend operation, or report a precise battery level to the user. During the recharge cycle, the controller can implement an intelligent recharge cycle, decreasing the charge rate when the battery charge nears capacity.

Trickle Charge Controller

While a battery is discharging, the ADC101C021 can be used to control a trickle charge to keep the battery near full capacity (see Figure 38). When the alert output is active, the battery will recharge. An intelligent recharge cycle will prevent over-charging and damaging the battery. With a trickle charge, the battery powered device can be disconnected from the charger at any time with a full charge.

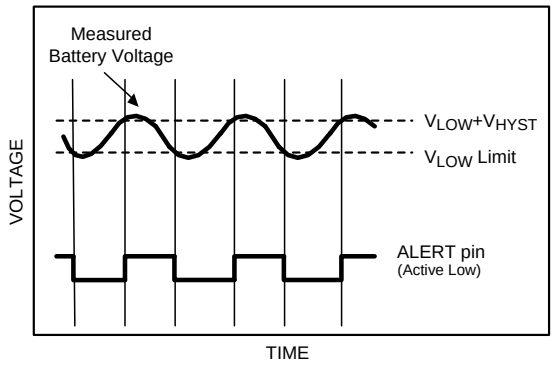


Figure 38. Trickle Charge

LAYOUT, GROUNDING, AND BYPASSING

For best accuracy and minimum noise, the printed circuit board containing the ADC101C021 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located on the same board layer. A single, solid ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will utilize a "fencing" technique to prevent the mixing of analog and digital ground currents. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the ADC121C021. Special care is required to guarantee that signals do not pass over power plane boundaries. Return currents must always have a continuous return path below their traces.

The ADC101C021 power supply should be bypassed with a 4.7µF and a 0.1µF capacitor as close as possible to the device with the 0.1µF right at the device supply pin. The 4.7µF capacitor should be a tantalum type and the 0.1µF capacitor should be a low ESL type. The power supply for the ADC101C021 should only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines should have controlled impedances.

REVISION HISTORY

Changes from Revision C (February 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	34

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC101C021CIMK/NOPB	ACTIVE	SOT	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	X33C	Samples
ADC101C021CIMKX/NOPB	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	X33C	Samples
ADC101C021CIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		X38C	Samples
ADC101C021CIMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		X38C	Samples
ADC101C027CIMK/NOPB	ACTIVE	SOT	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	X32C	Samples
ADC101C027CIMKX/NOPB	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	X32C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

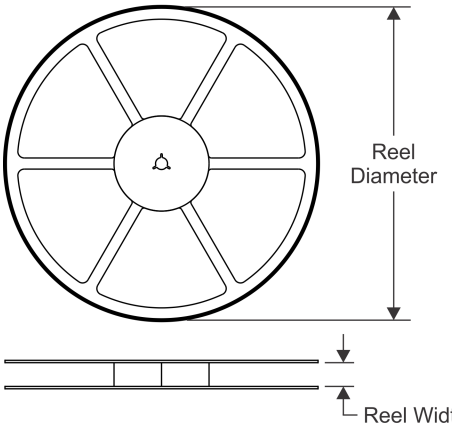
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

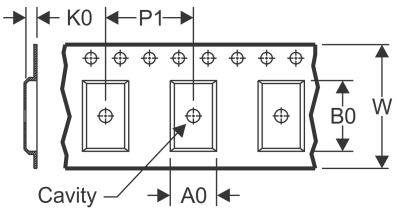
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

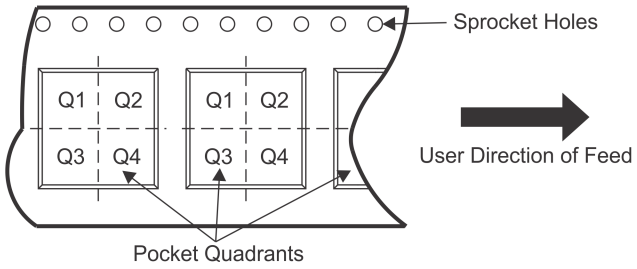


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

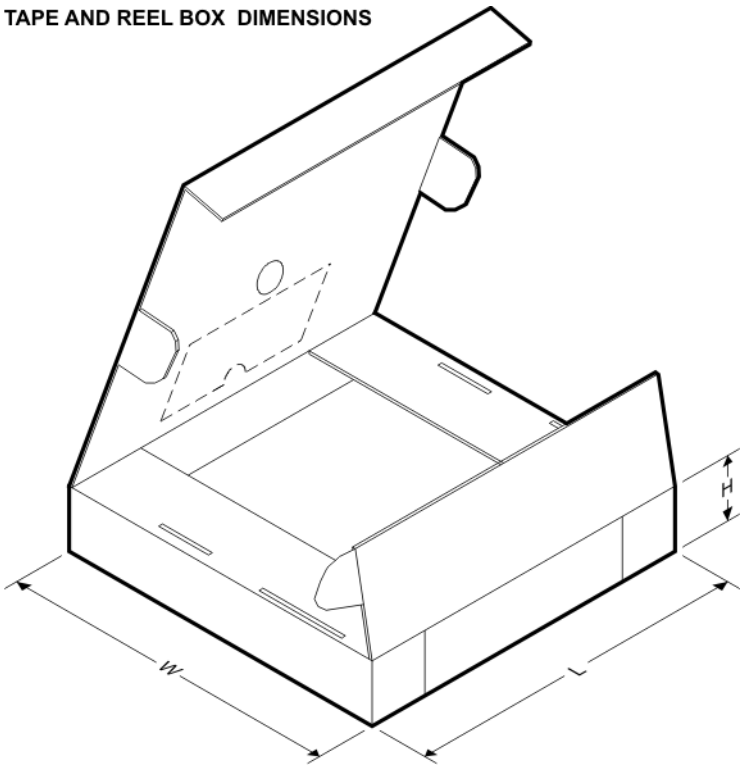
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC101C021CIMK/NOPB	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADC101C021CIMKX/NOPB	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADC101C021CIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC101C021CIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC101C027CIMK/NOPB	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADC101C027CIMKX/NOPB	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

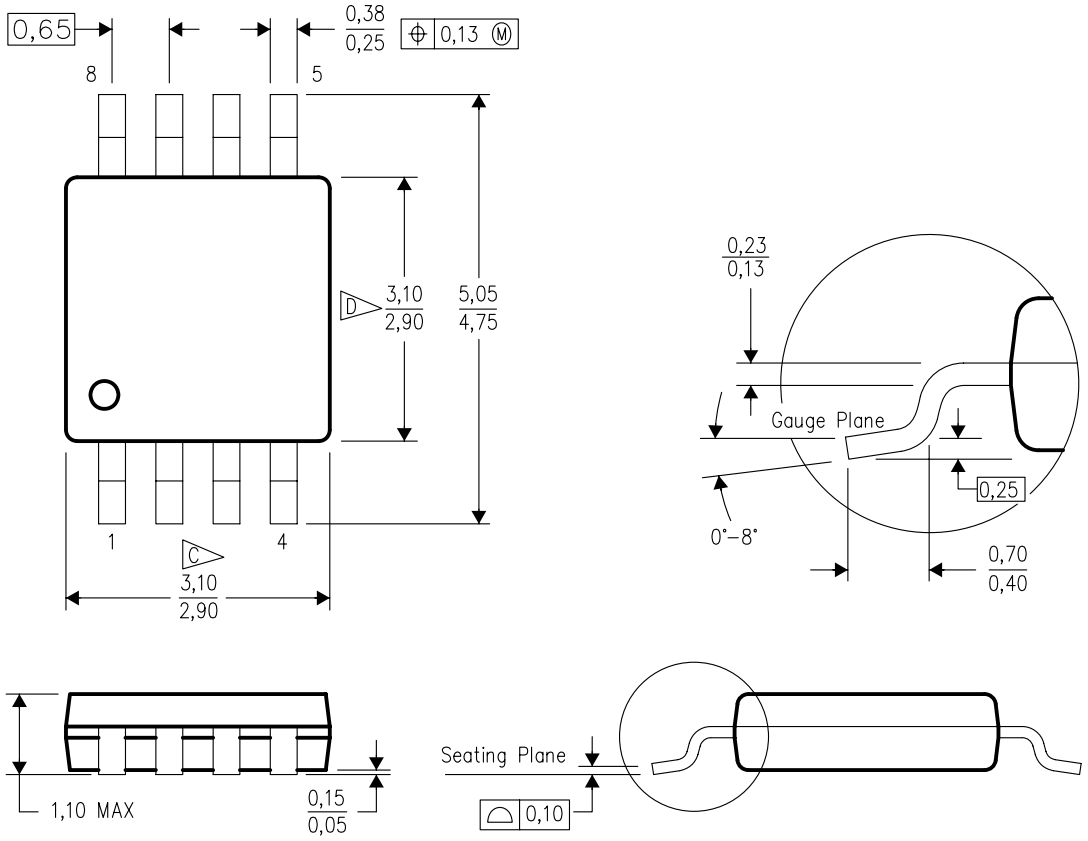
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC101C021CIMK/NOPB	SOT	DDC	6	1000	210.0	185.0	35.0
ADC101C021CIMKX/NOPB	SOT	DDC	6	3000	210.0	185.0	35.0
ADC101C021CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
ADC101C021CIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
ADC101C027CIMK/NOPB	SOT	DDC	6	1000	210.0	185.0	35.0
ADC101C027CIMKX/NOPB	SOT	DDC	6	3000	210.0	185.0	35.0

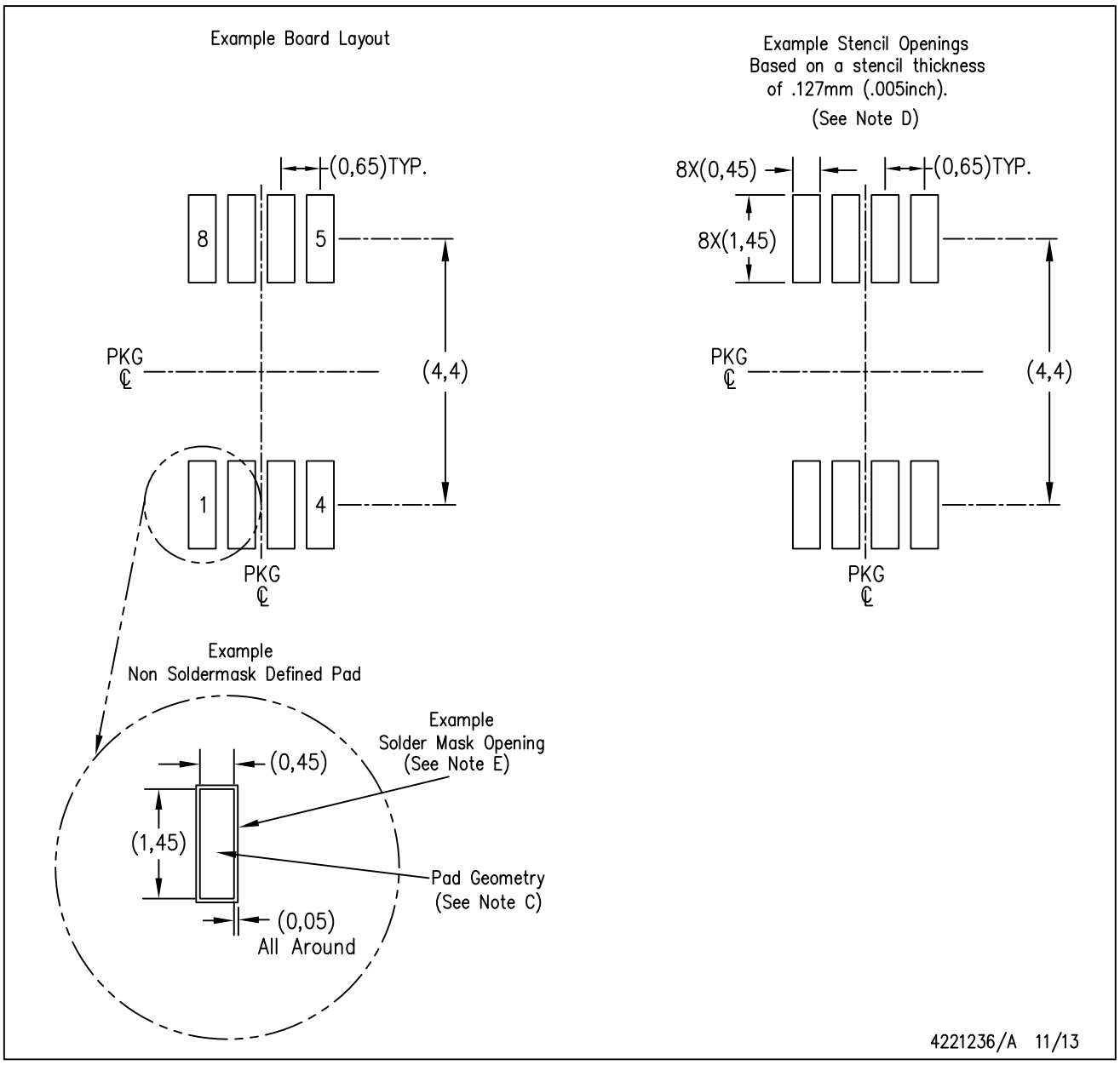
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

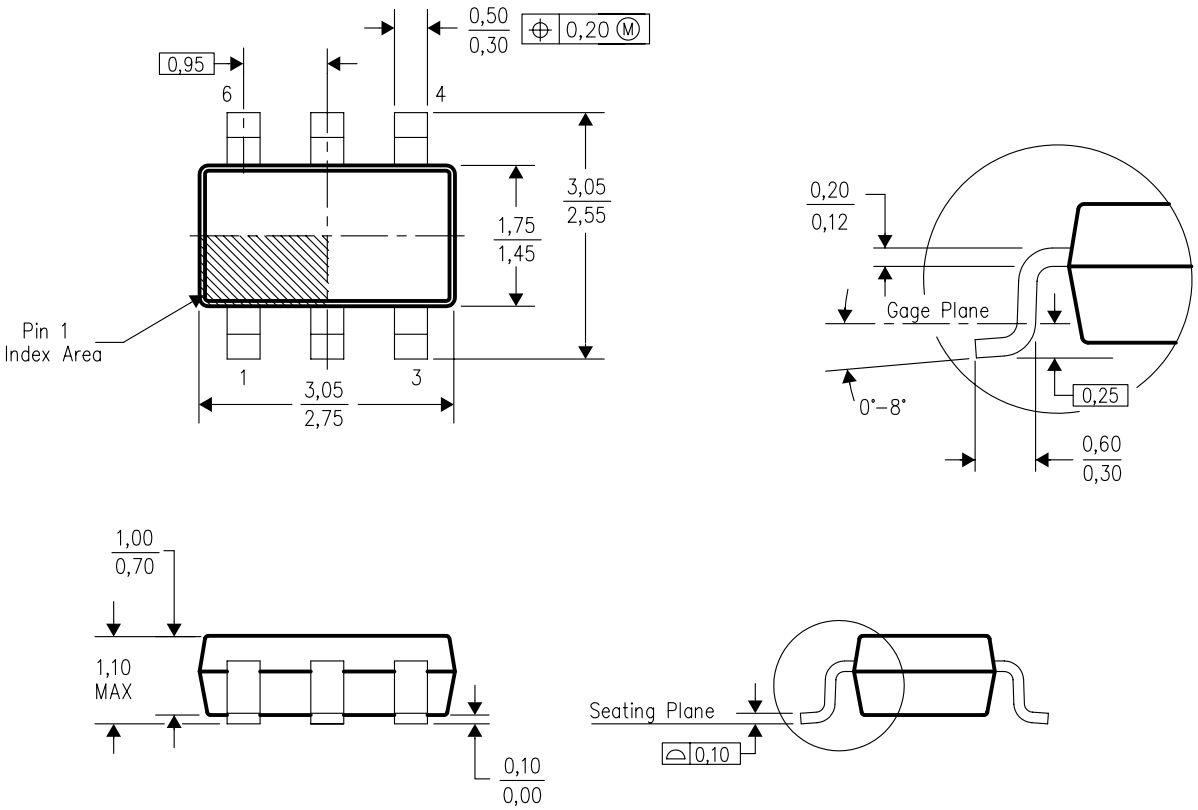
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

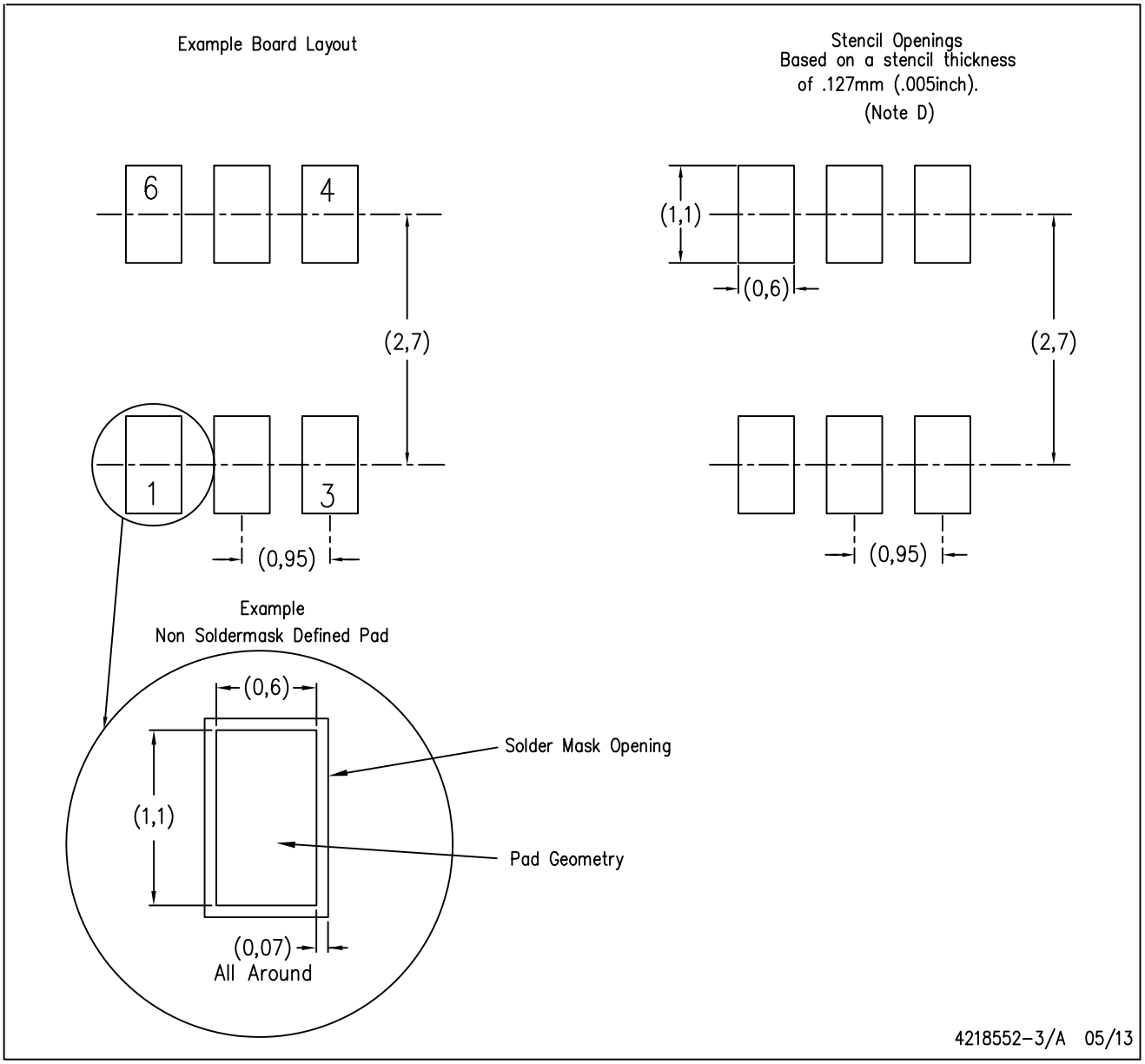
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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