8-Bit, 165 MSPS TxDAC® D/A Converter

Preliminary Technical Data — AD9748*

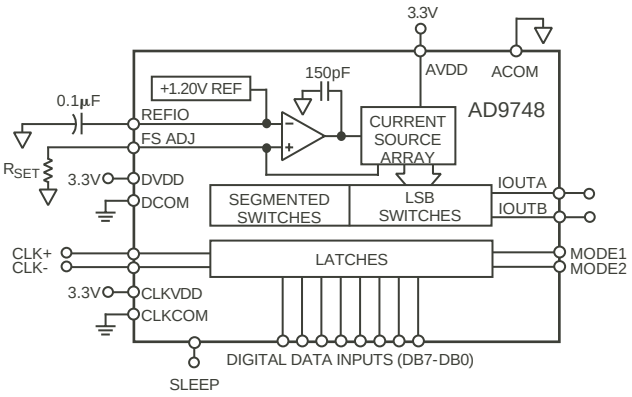
FEATURES

High-Performance Member of Pin-Compatible TxDAC Product Family
Excellent Spurious-Free Dynamic Range and Noise Performance
Two's Complement or Straight Binary Data Format
Differential Current Outputs: 2 mA to 20 mA
Power Dissipation: 135 mW @ 3.3 V
Power-Down Mode: 15 mW @ 3.3 V
On-Chip 1.20 V Reference
CMOS-Compatible Digital Interface
Package: 32-Lead Leadframe Chip Scale Package (LFCSP)
Edge-Triggered Latches

APPLICATIONS

Wideband Communication Transmit Channel:
Direct IF
Base Stations
Wireless Local Loop
Digital Radio Link
Direct Digital Synthesis (DDS)
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9748 is a 8-bit resolution, wideband, third generation member of the TxDAC series of high-performance, low power CMOS digital-to-analog converters (DACs). The TxDAC family, consisting of pin-compatible 8-, 10-, 12-, and 14-bit DACs, is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost. The AD9748 offers exceptional ac and dc performance while supporting update rates up to 165 MSPS.

The AD9748's low power dissipation makes it well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 60 mW with a slight degradation in performance by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 15 mW. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated band gap reference have been integrated to provide a complete monolithic DAC solution. The digital inputs support 3 V CMOS logic families.

PRODUCT HIGHLIGHTS

1. New 32-lead LFCSP package.
2. The AD9748 is the 8-bit member of the pin-compatible TxDAC family that offers excellent INL and DNL performance.
3. Differential or single-ended clock input (LVPECL or CMOS).
4. Data input supports two's complement or straight binary data coding.
5. High-speed, single-ended CMOS clock input supports 165 MSPS conversion rate.
6. Low power: Complete CMOS DAC function operates on 135 mW from a 3.0 V to 3.6 V single supply. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for low power idle periods.
7. On-chip voltage reference: The AD9748 includes a 1.2 V temperature-compensated band gap voltage reference.

REV. PrA

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AD9748-SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
RESOLUTION	8			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)	TBD	±0.25	TBD	LSB
Differential Nonlinearity (DNL)	TBD	±0.25	TBD	LSB
ANALOG OUTPUT				
Offset Error	–0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	–0.5	±0.1	+0.5	% of FSR
Gain Error (With Internal Reference)	–0.5	±0.1	+0.5	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		+1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current [3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (Ext. Ref)		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	3.0	3.3	3.6	V
DVDD	3.0	3.3	3.6	V
Analog Supply Current (I_{AVDD})		33	36	mA
Digital Supply Current (I_{DVDD})[4]		8	TBD	mA
Supply Current Sleep Mode (I_{AVDD})		5	6	mA
Power Dissipation[4]		135	145	mW
Power Dissipation[5]		145		mW
Power Supply Rejection Ratio—AVDD[6]	–1		+1	% of FSR/V
Power Supply Rejection Ratio—DVDD[6]	–0.04		+0.04	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES

[1]Measured at IOUTA, driving a virtual ground.

[2]Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.

[3]An external buffer amplifier with input bias current <100 nA should be used to drive any external load.

[4]Measured at f_{CLOCK} = 25 MSPS and f_{OUT} = 1.0 MHz.

[5]Measured as unbuffered voltage output with I_{OUTFS} = 20 mA and 50 Ω R_{LOAD} at IOUTA and IOUTB, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz.

[6]±5% Power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS

(T_{MIN} to T_{MAX} , AVDD = 3.3 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	165			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		11		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)[2]		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)[2]		30		pA/√Hz
Noise Spectral Density[3]		TBD		dBm/Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output	TBD	TBD		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 1.00 MHz		TBD		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.51 MHz		TBD		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 10 MHz		TBD		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 15 MHz		TBD		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 25 MHz		TBD		dBc
f_{CLOCK} = 165 MSPS; f_{OUT} = 21 MHz		TBD		dBc
f_{CLOCK} = 165 MSPS; f_{OUT} = 41 MHz		TBD		dBc
Total Harmonic Distortion				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz		TBD	TBD	dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.00 MHz		TBD		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.00 MHz		TBD		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 2.00 MHz		TBD		dBc
Signal-to-Noise Ratio				
f_{CLOCK} = 65 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		TBD		dB
f_{CLOCK} = 65 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		TBD		dB
f_{CLOCK} = 125 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		TBD		dB
f_{CLOCK} = 125 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		TBD		dB
f_{CLOCK} = 165 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		TBD		dB
f_{CLOCK} = 165 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		TBD		dB

NOTES

[1]Measured single-ended into 50 ý load.

[2]Output noise is measured with a full-scale output set to 20 mA with no conversion activity. It is a measure of the thermal noise only.

[3]Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic "1" Voltage	2.1	3		V
Logic "0" Voltage		0	0.9	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW})	1.5			ns

Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
AVDD	ACOM	–0.3	+3.9	V
DVDD	DCOM	–0.3	+3.9	V
ACOM	DCOM	–0.3	+0.3	V
AVDD	DVDD	–3.9	+3.9	V
CLOCK, SLEEP	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
IOUTA, IOUTB	ACOM	–1.0	AVDD + 0.3	V
REFIO, REFLO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD9748XCP	–40°C to +85°C	32-Lead LFCSP	CP-32

*CP = Leadframe Chip Scale Package

THERMAL CHARACTERISTICS

Thermal Resistance

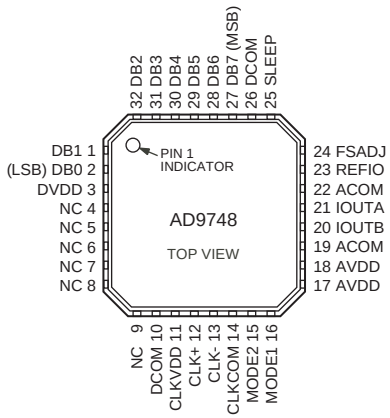
32-Lead LFCSP

θ_{JA} = TBD°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9748 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
27	DB7	Most Significant Data Bit (MSB)
28-32, 1	DB6–DB1	Data Bits 6-1
2	DB0	Least Significant Data Bit (LSB)
25	SLEEP	Power-Down Control Input. Active high. Contains active pull-down circuit; it may be left unterminated if not used.
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., tie REFLO to AGND). Requires 0.1 µF capacitor to AGND when internal reference activated.
24	FS ADJ	Full-Scale Current Output Adjust
4-9	NC	No Internal Connection
19, 22	ACOM	Analog Common
20	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
21	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
17, 18	AVDD	Analog Supply Voltage (3.3 V)
15	MODE2	Selects Input Data Format. Connect to CLKGND for straight binary, CLKVDD for two's complement.
16	MODE1	Clock Mode Selection. Connect to CLKGND for single ended clock receiver (drive clk+ and float clk-). Connect to CLKVDD for differential receiver. Float for PECL receiver (terminations on-chip).
10, 26	DCOM	Digital Common
3	DVDD	Digital Supply Voltage (3.3 V)
12	CLK+	Differential Clock Input.
13	CLK-	Differential Clock Input.
11	CLKVDD	Clock Supply Voltage (3.3 V)
14	CLKCOM	Clock Common

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called the offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio
The spurious free dynamic range containing multiple carrier tones of equal amplitude. It is measures as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

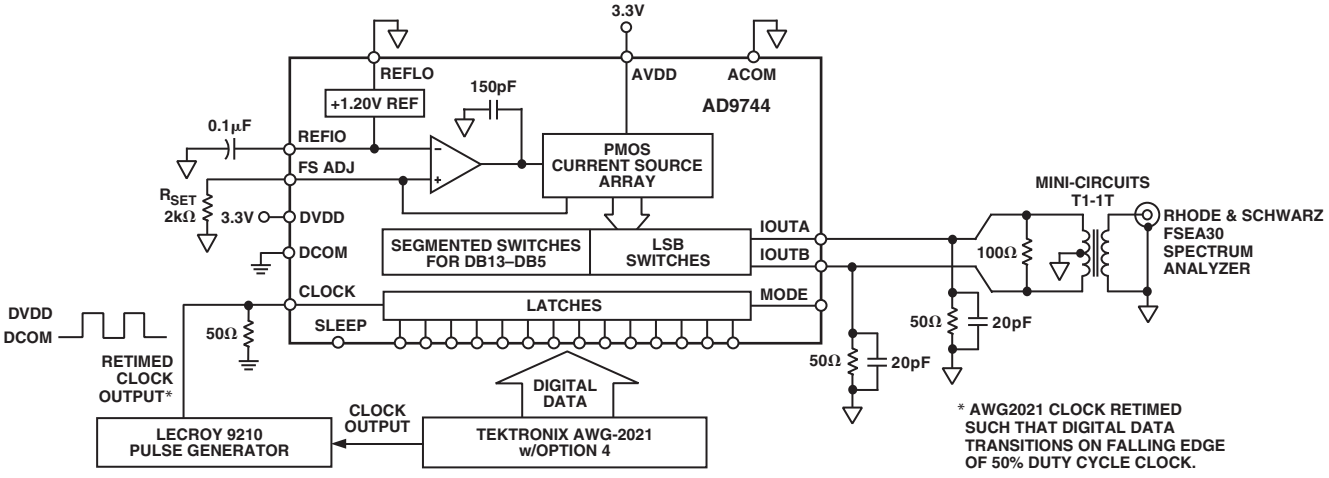


Figure 2. Basic AC Characterization Test Set-Up

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

32-Lead Leadframe Chip Scale Package (LFCSP)
(CP-28)