4-Channel, LVDS, Dual-Output, Laser Diode Driver with Oscillator

AD9665

FEATURES

- Dual, current-controlled output current sources with 4 input channels
- TTL-selectable output
- Stable on-chip oscillators with independent frequency and amplitude control
- TTL- or LVDS-selectable write channel enables negative logic
- Independent TTL oscillator enables positive logic
- 170 mA minimum output current for the read channel
- 510 mA minimum output current for Write Channel 1
- 330 mA minimum output current for Write Channel 2
- 165 mA minimum output current for Write Channel 3
- 950 mA typical total output current
- Typical rise time/fall time of 0.8 ns
- Low power consumption
- Single 5 V power supply (±10%)

APPLICATIONS

- DVD-R, DVD+R, DVD-RW, DVD+RW, DVD-RAM supercombo drives
- Magneto-optical (MO) drives
- Laser diode current switching

GENERAL DESCRIPTION

The AD9665 is a laser diode driver for high performance CD-RW and DVD recordable drives. It includes four channels for four different optical power levels: the read channel generates a continuous output power level, whereas Channel 1, Channel 2, and Channel 3 can be used as write channels that can be controlled with an LVDS or TTL interface. The WxDIS and $\overline{\text{RDIS}}$ pins are active low logic. The OSCEN pin is controlled by an active high TTL signal. All active channels are summed at the output where Write Channel 1 can contribute at least 325 mA output current, and Write Channel 2 and Write Channel 3 can contribute at least 250 mA and 150 mA, respectively. The level of the output current is set by an external resistor, which converts this voltage into a current at the WxSET pin.

An on-chip oscillator is provided to allow output current modulation and to reduce laser-mode hopping. Four external resistors permit the setting of two distinct values for the frequency and swing of the oscillator. The oscillator can output up to 100 mA p-p of current (push-pull oscillator) with a frequency range of 200 MHz to 500 MHz.

FUNCTIONAL BLOCK DIAGRAM

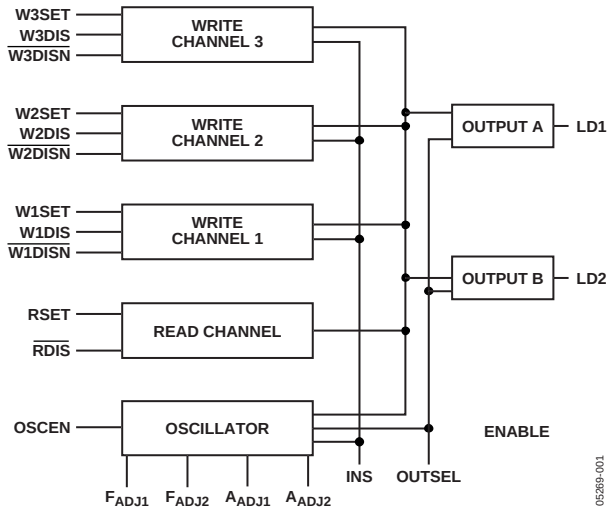
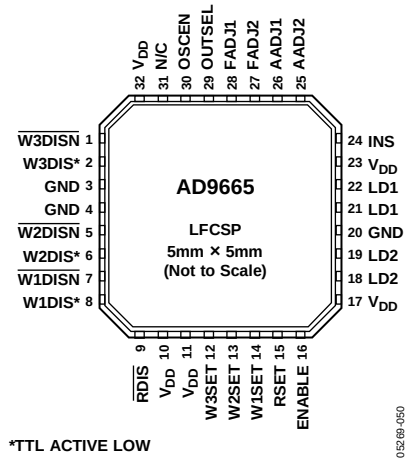


Figure 1. 4-Channel, LVDS, Laser Driver Block Diagram



NOTES
1. THE EXPOSED PAD SHOULD BE CONNECTED TO GROUND.

Figure 2. 4-Channel, LVDS, Laser Driver Pin Configuration

Rev. E

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
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IMPORTANT LINKS for the AD9665*

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DOCUMENTATION
4-Channel, LVDS, Dual-Output, Laser Diode Driver with Oscillator (AD9665 Product Highlight)

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REVISION HISTORY

8/10—Revision E: Initial Version

SPECIFICATIONS

At 25°C, V_{DD} = 5 V, ENABLE = 1, OSCEN = 0, F_{ADJ} = 6.81 kΩ, A_{ADJ} = 5.76 kΩ, V_{OUT} = 2.5 V, I_{OUT} = 50 mA (Read), $\overline{RDIS}$ = 0, unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
LASER AMPLIFIER					
Output Current Read Channel	Output is sourcing, I_{IN} = 2 mA	170	190		mA
	Output is sourcing, V_{OUT} = 3.5 V, I_{IN} = 2 mA	150	170		mA
Output Current Write Channel 1	Output is sourcing, I_{IN} = 2 mA	510	540		mA
	Output is sourcing, V_{OUT} = 3.5 V, I_{IN} = 2 mA	450	480		mA
Output Current Write Channel 2	Output is sourcing, I_{IN} = 2 mA	330	360		mA
	Output is sourcing, V_{OUT} = 3.5 V, I_{IN} = 2 mA	290	320		mA
Output Current Write Channel 3	Output is sourcing, I_{IN} = 2 mA	165	185		mA
	Output is sourcing, V_{OUT} = 3.5 V, I_{IN} = 2 mA	145	165		mA
Total Output Current (See Figure 11)	All channels sourcing, I_{IN} = 1.45 mA	875	950		mA
	All channels sourcing, V_{OUT} = 3.5 V, I_{IN} = 1.45 mA	775	850		mA
Output Current Linearity Error	Read channel or Write Channel 3[1]	−1.5	±0.4	+1.5	%
	Write Channel 1[2] or Write Channel 2[3]	−1.0	±0.2	+1.0	%
	Write Channel 1, V_{OUT} = 3.5 V, I_{IN} = 2 mA[4]	−15	−9		%
Best-Fit Current Gain	Read channel[1]	85	105	115	mA/mA
	Write Channel 1[2]	265	300	335	mA/mA
	Write Channel 2[3]	165	200	225	mA/mA
	Write Channel 3[1]	80	100	110	mA/mA
Best-Fit Current Offset	Read channel or Write Channel 3[1]	−7	−2	+4	mA
	Write Channel 1[2]	−17	−3	+11	mA
	Write Channel 2[3]	−11	−1	+8	mA
I_{IN} Input Impedance (R_{IN}), All Channels	R_{IN} to GND, I_{OUT} = 0 mA	140	200	260	Ω
I_{OUT} Current Output Noise	f = 300 MHz		100		pA/√Hz
I_{OUT} Supply Sensitivity, (PSRR) Read Mode	V_{DD} = 5 V ± 10%		3.5		%/V
I_{OUT} Supply Sensitivity, (PSRR) Write Mode	I_{OUT} = 100 mA, 50 mA read channel, 50 mA any write channel, V_{DD} = 5 V ± 10%		3.5		%/V
I_{OUT} Temperature Sensitivity, Read Mode			175		ppm/°C
I_{OUT} Temperature Sensitivity, Write Mode	I_{OUT} = 100 mA (50 mA read channel, 50 mA Write Channel 1)		150		ppm/°C
	I_{OUT} = 100 mA (50 mA read channel, 50 mA Write Channel 2)		390		ppm/°C
	I_{OUT} = 100 mA (50 mA read channel, 50 mA Write Channel 3)		350		ppm/°C
LASER AMPLIFIER AC SPECIFICATIONS					
Write Rise Time	I_{OUT} = 50 mA (read channel), 150 mA (Write Channel 1)[5]		0.75	0.95	ns
	I_{OUT} = 65 mA (read channel), 375 mA (Write Channel 1), V_{DD} = 5 V, V_{OUT} = 3.5 V[6]		0.8	1.3	ns
	I_{OUT} = 50 mA (read channel), 100 mA (Write Channel 2)[5]		0.6	0.8	ns
	I_{OUT} = 50 mA (read channel), 50 mA (Write Channel 3)[5]		0.55	0.75	ns
Write Fall Time	I_{OUT} = 50 mA (read channel), 150 mA (Write Channel 1)[7]		0.55	0.75	ns
	I_{OUT} = 65 mA (read channel), 375 mA (Write Channel 1), V_{DD} = 5 V, V_{OUT} = 3.5 V[8]		0.4	0.6	ns
	I_{OUT} = 50 mA (read channel), 100 mA (Write Channel 2)[7]		0.55	0.75	ns
	I_{OUT} = 50 mA (read channel), 50 mA (Write Channel 3)[7]		0.45	0.65	ns
I_{OUT} ON Propagation Delay (LVDS Mode)	Logic at 50% of final value to I_{OUT} at 50% of final value		5.2		ns
I_{OUT} OFF Propagation Delay (LVDS Mode)	Logic at 50% of final value to I_{OUT} at 50% of final value		6.3		ns
Disable Time	ENABLE 50% H-L to I_{OUT} at 50% of final value		3.8		ns
Enable Time	ENABLE 50% L-H to I_{OUT} at 50% of final value		5.5		ns
Output Switching Time	OUTSEL 50% to I_{OUT} at 50% of final value		3		ns
OSCILLATOR SPECIFICATIONS					
Oscillator Frequency	OSCEN = 1	280	315	340	MHz
Oscillator Amplitude	OSCEN = 1		50		mA p-p
Oscillator Temperature Coefficient	Oscillator amplitude, OSCEN = 1		60		µA p-p/°C
	Oscillator frequency, OSCEN = 1		195		kHz/°C

Parameter	Conditions						Min	Typ	Max	Unit
Disable Time Oscillator	OSCEN 50% H-L to I_{OUT} at 50% of final value, OSCEN = 1							2		ns
Enable Time Oscillator	OSCEN 50% L-H to I_{OUT} at 50% of final value, OSCEN = 1							4		ns
LOGIC SPECIFICATIONS										
INS = 1 (LVDS Mode)										
Minimum Differential Input Voltage	Magnitude						100			mV
Maximum Differential Input Voltage	Magnitude								600	mV
Valid Input Voltage	Relative to GND						0		2.4	V
OUTEN										
Logic HI Threshold	Temperature stabilized						2.0			V
Logic LO Threshold	Temperature stabilized								0.8	V
SUPPLY CURRENT[9]	**ENABLE**	**OSCEN**	**$\overline{\text{RDIS}}$**	**W1DIS[10]**	**W2DIS[10]**	**W3DIS[10]**				
INS = 1 (LVDS Mode)										
Power Down	0	0	1	1	1	1		8.6		mA
Inputs Disabled, Read Enabled	1	0	0	1	1	1		26		mA
Inputs Disabled, Oscillator Enabled	1	1	1	1	1	1		46		mA
Read Mode, Oscillator Enabled[11]	1	1	0	1	1	1		54		mA
I_{OUT} = 50 mA										
Write Mode[11]	1	0	1	0	0	0		49		mA
I_{OUT} = 150 mA (50 mA Write Channel 1, Write Channel 2, Write Channel 3)										
INS = 0 (TTL Mode)										
Power-Down	0	0	1	1	1	1		9.5		mA
Inputs Disabled, Read Enabled	1	0	0	1	1	1		23		mA
Inputs Disabled, Oscillator Enabled	1	1	1	1	1	1		43		mA
Read Mode, Oscillator Enabled[11]	1	1	0	1	1	1		51		mA
I_{OUT} = 50 mA										
Write Mode[11]	1	0	1	0	0	0		43		mA
I_{OUT} = 150 mA (50 mA Write Channel 1, Write Channel 2, Write Channel 3)										
OPERATING CONDITIONS										
Supply Voltage Range							4.5		5.5	V
Operating Temperature Range							−25		+85	°C

[1] Output linearity, offset current, and gain are calculated using the best-fit method at 30 mA, 60 mA, and 90 mA. The transfer function is $I_{OUT} = (I_{IN} \times GAIN) + I_{OS}$.
[2] Output linearity, offset current, and gain are calculated using the best-fit method at 90 mA, 120 mA, and 150 mA. The transfer function is $I_{OUT} = (I_{IN} \times GAIN) + I_{OS}$.
[3] Output linearity, offset current, and gain are calculated using the best-fit method at 60 mA, 90 mA, and 120 mA. The transfer function is $I_{OUT} = (I_{IN} \times GAIN) + I_{OS}$.
[4] Output linearity is calculated using the best-fit method, which is calculated at 90 mA, 120 mA, and 150 mA, extrapolated to I_{IN} = 2 mA.
[5] Measured electrically from 10% to 90% of final value. Sharp Diode—GH06550B2B (see Figure 14).
[6] Measured electrically from 10% to 90% of final value. Mitsubishi Diode—ML101J26. R_L = 0.66 Ω (see Figure 14).
[7] Measured electrically from 90% to 10% of final value. Sharp Diode—GH06550B2B (see Figure 14).
[8] Measured electrically from 90% to 10% of final value. Mitsubishi Diode—ML101J26. R_L = 0.66 Ω (see Figure 14).
[9] See the Shutdown Supply Current Variation section for more information.
[10] WxDIS = 0 means channel is off regardless of mode: TTL or LVDS (see Table 3). WxDIS = 1 means channel is on regardless of mode: TTL or LVDS (see Table 3).
[11] The value specified does not include the output current.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Range
Supply Voltage ($+V_{DD}$)	
Pins 10, 11, 17, 23, 32	6 V
Input Pins	
Pins 12, 13, 14, 15	2.2 mA
Pins 1, 2, 5, 6, 7, 8, 9, 16, 24, 29, 30	−0.8 V to $+V_{DD}$
Internal Power Dissipation[1]	
5 mm × 5 mm, 32-Lead, Pad-Up LFCSP	2 W
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] Power dissipation is specified on semistandard 4-layer board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

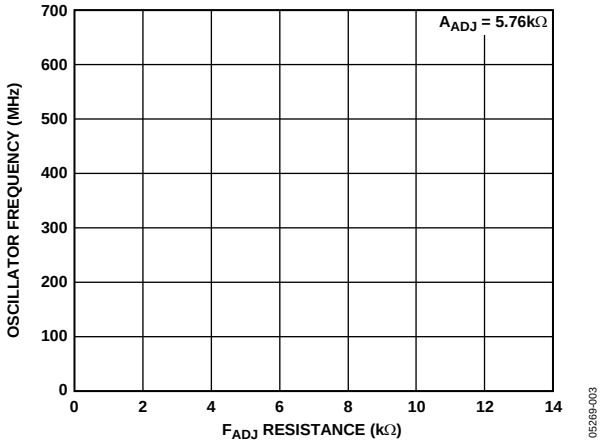


Figure 3. Oscillator Frequency vs. F_{ADJ}

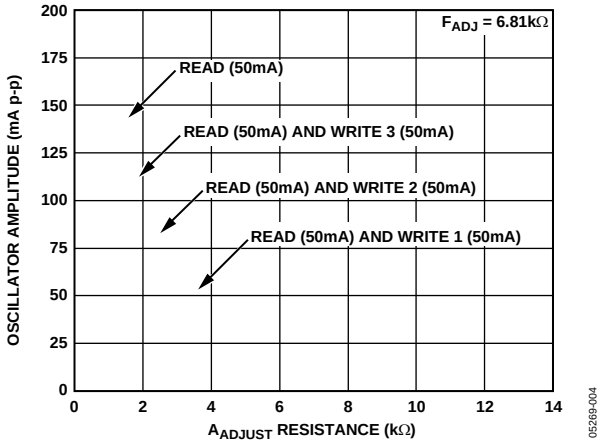


Figure 6. Oscillator Amplitude vs. A_{ADJ}

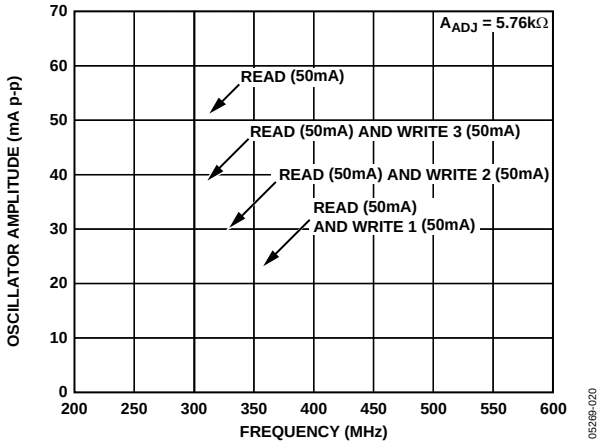


Figure 4. Oscillator Amplitude vs. Frequency

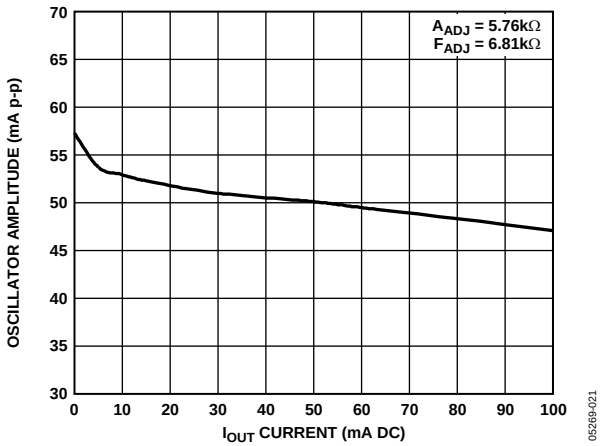


Figure 7. Oscillator Amplitude vs. I_{OUT-DC}

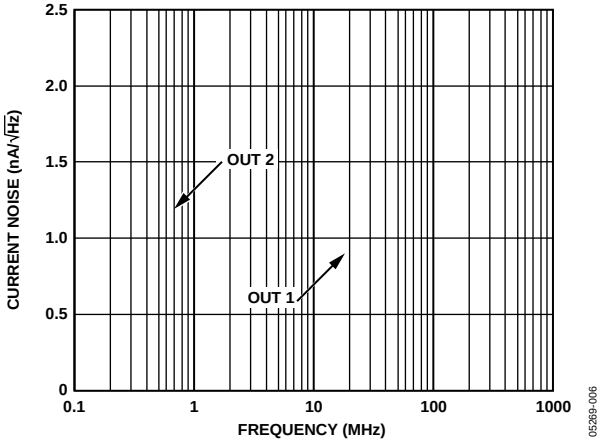


Figure 5. I_{OUT} Current Noise

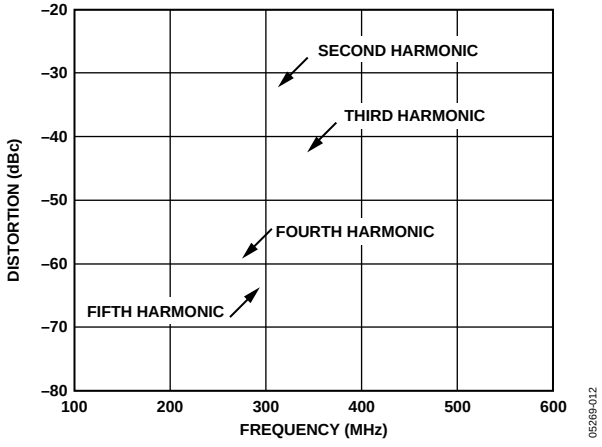


Figure 8. Oscillator Distortion vs. Frequency

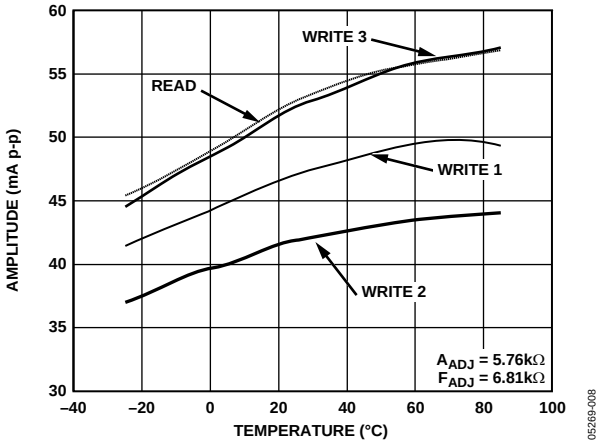


Figure 9. Oscillator Amplitude vs. Temperature

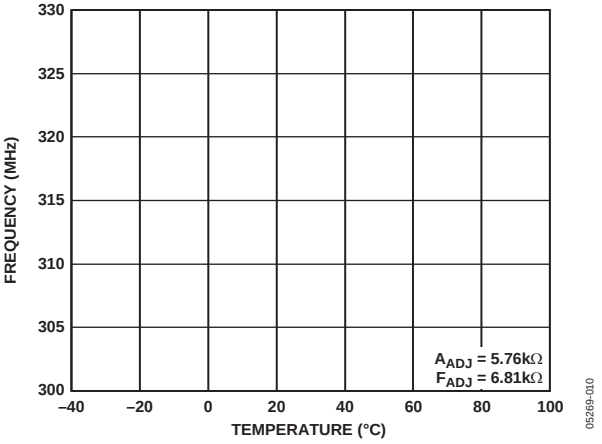


Figure 12. Oscillator Frequency vs. Temperature

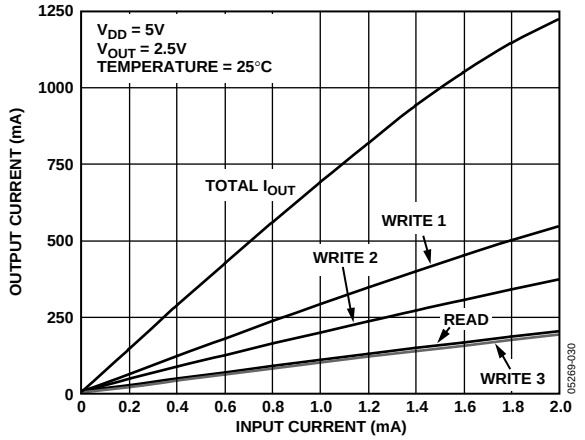


Figure 10. Output Current vs. Input Current for Each Channel, V_{OUT} = 2.5 V

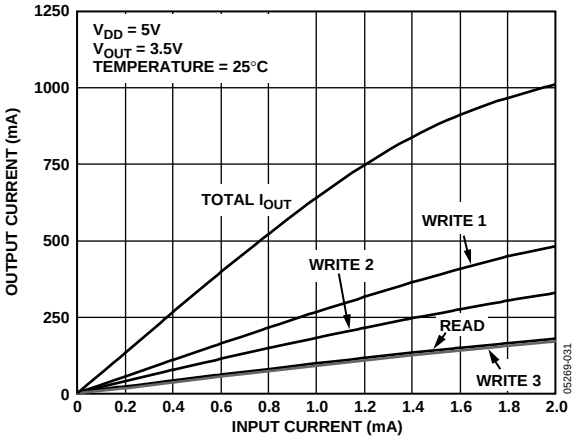


Figure 13. Output Current vs. Input Current for Each Channel, V_{OUT} = 3.5 V

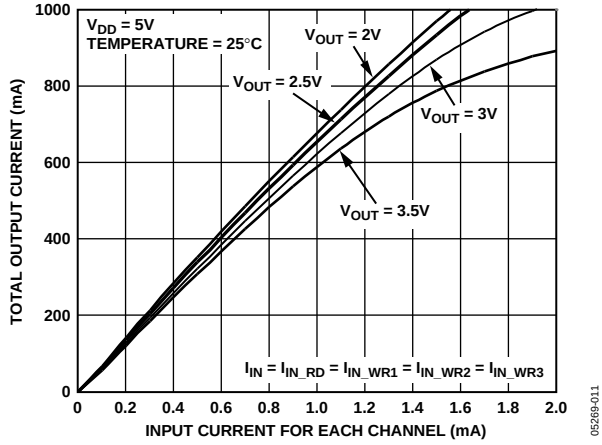


Figure 11. Total I_{OUT} vs. I_{IN}

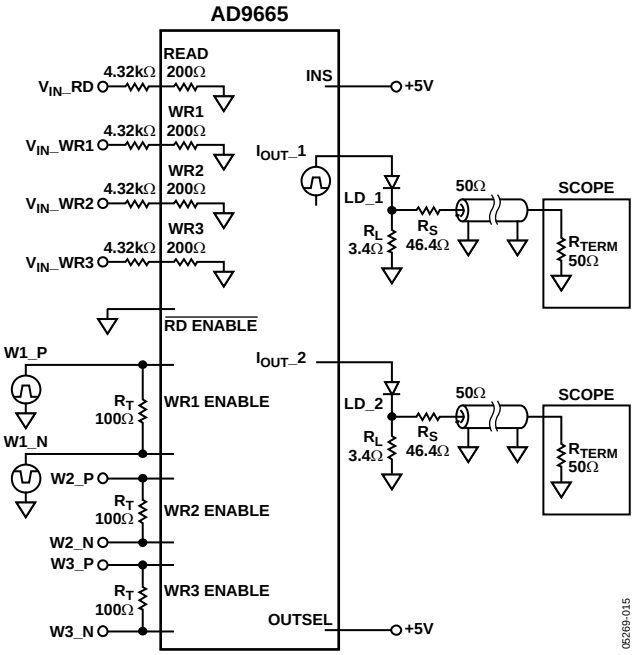


Figure 14. Electrical LVDS Pulse Response Schematic

LOGIC TABLE

Table 3.

ENABLE	OUTSEL	OSCEN	INS	$\overline{\text{RDIS}}$	W1DIS	$\overline{\text{W1DISN}}$	W2DIS	$\overline{\text{W2DISN}}$	W3DIS	$\overline{\text{W3DISN}}$	OSC	LD1	LD2
L	x	x	x	x	x	x	x	x	x	x	x	OFF	OFF
H	L	L	L	L	H	x	H	x	H	x	OFF	OFF	$I_{RSET} \times 100mA/mA$
H	L	H	L	L	H	x	H	x	H	x	ON	OFF	$I_{RSET} \times 100mA/mA + I_{OSC}(F_{ADJ2} + A_{ADJ2})$
H	L	H	L	H	L	x	H	x	H	x	ON	OFF	$I_{W1SET} \times 300mA/mA + I_{OSC}(F_{ADJ2} + A_{ADJ2})$
H	L	H	L	H	H	x	L	x	H	x	ON	OFF	$I_{W2SET} \times 200mA/mA + I_{OSC}(F_{ADJ2} + A_{ADJ2})$
H	L	H	L	H	H	x	H	x	L	x	ON	OFF	$I_{W3SET} \times 100mA/mA + I_{OSC}(F_{ADJ2} + A_{ADJ2})$
H	L	H	L	H	H	x	H	x	H	x	ON	OFF	$I_{OSC}(F_{ADJ2} + A_{ADJ2})$ (NOT RECOMMENDED)
H	L	L	H	L	H	L	H	L	H	L	OFF	OFF	$I_{RSET} \times 100mA/mA$
H	L	H	H	L	H	L	H	L	H	L	ON	OFF	$I_{RSET} \times 100mA/mA + I_{OSC}(F_{ADJ2} + A_{ADJ2})$
H	L	H	H	H	L	H	H	L	H	L	ON	OFF	$I_{W1SET} \times 300mA/mA + I_{OSC}(F_{ADJ2} + A_{ADJ2})$
H	L	H	H	H	H	L	L	H	H	L	ON	OFF	$I_{W2SET} \times 200mA/mA + I_{OSC}(F_{ADJ2} + A_{ADJ2})$
H	L	H	H	H	H	L	H	L	L	H	ON	OFF	$I_{W3SET} \times 100mA/mA + I_{OSC}(F_{ADJ2} + A_{ADJ2})$
H	L	H	H	H	H	x	H	x	H	x	ON	OFF	$I_{OSC}(F_{ADJ2} + A_{ADJ2})$ (NOT RECOMMENDED)
H	H	L	L	L	H	x	H	x	H	x	OFF	$I_{RSET} \times 100mA/mA$	OFF
H	H	H	L	L	H	x	H	x	H	x	ON	$I_{RSET} \times 100mA/mA + I_{OSC}(F_{ADJ1} + A_{ADJ1})$	OFF
H	H	H	L	H	L	x	H	x	H	x	ON	$I_{W1SET} \times 300mA/mA + I_{OSC}(F_{ADJ1} + A_{ADJ1})$	OFF
H	H	H	L	H	H	x	L	x	H	x	ON	$I_{W2SET} \times 200mA/mA + I_{OSC}(F_{ADJ1} + A_{ADJ1})$	OFF
H	H	H	L	H	H	x	H	x	L	x	ON	$I_{W3SET} \times 100mA/mA + I_{OSC}(F_{ADJ1} + A_{ADJ1})$	OFF
H	H	H	L	H	H	x	H	x	H	x	ON	$I_{OSC}(F_{ADJ1} + A_{ADJ1})$ (NOT RECOMMENDED)	OFF
H	H	L	H	L	H	L	H	L	H	L	OFF	$I_{RSET} \times 100mA/mA$	OFF
H	H	H	H	L	H	L	H	L	H	L	ON	$I_{RSET} \times 100mA/mA + I_{OSC}(F_{ADJ1} + A_{ADJ1})$	OFF
H	H	H	H	H	L	H	H	L	H	L	ON	$I_{W1SET} \times 300mA/mA + I_{OSC}(F_{ADJ1} + A_{ADJ1})$	OFF
H	H	H	H	H	H	L	L	H	H	L	ON	$I_{W2SET} \times 200mA/mA + I_{OSC}(F_{ADJ1} + A_{ADJ1})$	OFF
H	H	H	H	H	H	L	H	L	L	H	ON	$I_{W3SET} \times 100mA/mA + I_{OSC}(F_{ADJ1} + A_{ADJ1})$	OFF
H	H	H	H	H	H	L	H	L	H	L	ON	$I_{OSC}(F_{ADJ1} + A_{ADJ1})$ (NOT RECOMMENDED)	OFF

OUTSEL
H = LD1 OUTPUT
L = LD2 OUTPUT

INS
H = LVDS
L = TTL

OSCEN
H = OSCILLATOR ON
L = OSCILLATOR OFF

TTL
USE LVDS + INPUT

05269-051

APPLICATIONS

The AD9665 uses the current at one or more of its four inputs, RSET, W1SET, W2SET, and W3SET, and generates an output current proportional to the sum of the input currents. The read channel has a typical gain of 105 mA/mA, Write Channel 1 has a typical gain of 300 mA/mA, Write Channel 2 has a typical gain of 200 mA/mA, and Write Channel 3 has a typical gain of 100 mA/mA. The input impedance of all the channels is typically 200 Ω. In most cases, a voltage output DAC can be used to drive these channels. In this case, a series resistance should be placed between each of the DAC channels and the respective input on the AD9665. These resistances should be selected to scale the desired maximum output current for each channel with an appropriate voltage from the DAC without excessively loading it.

BOARD LAYOUT

Due to the fast rise and fall time (<1 ns) required for the operation of high speed drives, trace lengths carrying high speed signals, such as $\overline{\text{RDIS}}$, W1DIS, W2DIS, and W3DIS, and the output current should be kept as short as possible to minimize series inductance. A decoupling capacitor should be located near each V_{DD} pin, and the ground return for the cathode of the laser diode should be kept as short as possible.

An S11 measurement of a piece of flexible printed circuit board (FPC) can show the inductance associated with that section of the FPC. In Table 4, an S11 measurement of two different pieces of a 19 mm (0.75 in) FPC was taken. The first piece is a single layer of an FPC with 0.5 ounce copper and 25.4 micron (1 mil) thick Kapton® and coverlay. The second piece is an FPC with 2 layers of 0.5 ounce copper and 25.4 micron (1 mil) thick Kapton and coverlay.

Table 4. Inductance of FPC

S11	L, nH @ 10 MHz	L, nH @ 300 MHz
Single-layer FPC	8.8	8.5
Double-layer FPC	4.3	4.2

As indicated by the measurement results, using two layers of copper in an FPC can reduce inductance by over 50%. Using the basic circuit equation

$$V = L\frac{di}{dt}$$

it can be seen that increasing the amplitude of a current step increases the voltage drop across the inductor. For example, on the single-layer FPC, a 200 mA pulse with a rise time of 1 ns generates a voltage drop of 1.86 V, assuming an additional 0.5 nH of inductance due to the laser diode itself. Increase this current to 250 mA, and the voltage drop is greater than 2.3 V.

Add this to the ~2 V of operating voltage that is required for the laser diode, and voltage headroom can become a problem if operating on a 5 V supply. Because the di/dt term seems to be a system requirement, L is the only contributor that can be changed when trying to reduce the voltage drop. Decreasing the inductance of the FPC can be done by either making the trace wider or by making it shorter. Because the distance from the laser diode driver (LDD) to the laser diode is fixed, using a wider trace is the only option. This can be accomplished by changing from a single-layer FPC design to a double-layer FPC design. This additional layer allows the full width of the FPC from the LDD to the laser diode to be used for the drive current, while the bottom layer can be used entirely for the return path (see Figure 15).

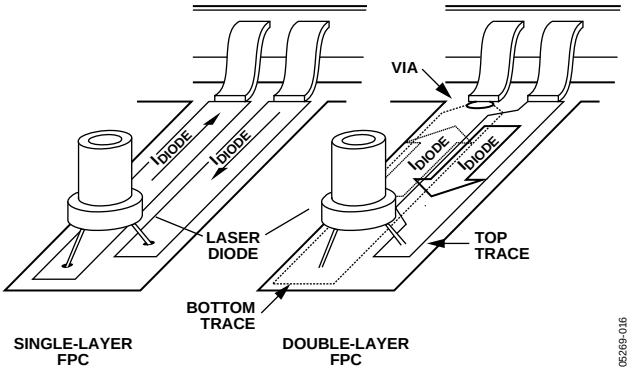


Figure 15. Single-Layer and Double-Layer Flexible Printed Circuit Boards

TEMPERATURE CONSIDERATIONS

The AD9665 is available in a 32-lead LFCSP with an exposed heat pad on top of the package. Using a 4-layer JEDEC standard test board, the θ_{JA} of this package was determined without any external heat sink attached to the exposed pad. This board is made of FR4, is 1.60 mm thick, and consists of four copper layers. The two internal layers are solid copper (1 oz/in^2 or 0.35 mm thick). The two surface layers (containing the component and back side traces) use 2 oz/in^2 (0.70 mm thick) of copper. This method of construction yields a θ_{JA} for the AD9665 of approximately 110°C/W. An integrated circuit dissipating 500 mW and packaged in an LFCSP, while operating in an ambient environment of 85°C, would have an internal junction temperature of approximately 140°C.

$$85°C + 0.5\ W \times 110°C/W = 140°C$$

This junction temperature is within the maximum recommended operating junction temperature of 150°C. This can be improved by attaching an external heat sink to the exposed heat pad of the package. Of course, this is not a realistic method for mounting a laser diode driver in an optical storage device.

In an actual application, the laser diode driver would most likely be mounted to a flexible circuit board. The θ_{JA} of a system is highly dependent on the board layout, material, and heat sink. The user must consider these conditions carefully.

Some of the circuitry of the AD9665 can be used to monitor the internal junction temperature.

The AD9665 uses a combination of diodes and transistors to protect it from electrostatic discharge (ESD). All input pins have a diode between them and ground, with the anode connected to ground and the cathode connected to the particular input pin. The base-emitter junction of a PNP transistor is used for ESD protection for each pin to V_{DD}. The collector is electrically connected to the substrate of the die (see Figure 16). The base-emitter junction of this transistor can be used to monitor the internal die temperature of the IC.

Using a 10 V source at the enable pin to forward-bias the base-emitter junction and a 1 MΩ resistor to limit the current, a 2-point measurement can be used to calculate the junction temperature of the IC. Because the enable pin (ENABLE) needs to be high for normal operation, the AD9665 can be operated normally with the 10 V applied through the 1 MΩ resistor. For this experiment, V1 and V2 were measured between the ENABLE pin (Pin 16) and the closest V_{DD} pin (Pin 17).

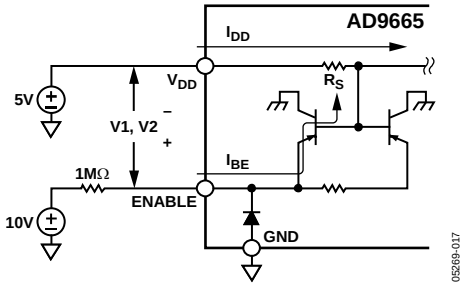


Figure 16. Junction Temperature Measurement Circuit

The most important aspect of measuring junction temperature on the AD9665 is that only one variable in the system is changed at a time. In this case, the only variable is the amount of power being dissipated by the AD9665. Therefore, the ambient temperature should be held constant. For example, to measure the junction temperature of the AD9665 while operating at 60°C ambient, the ambient temperature must be held constant for both the initial measurement, V1, and the final measurement, V2. This is true because of the relationship between temperature and V_{BE}. For the process with which the AD9665 is fabricated, the change in V_{BE} (ΔV_{BE}) is related to the die temperature by −1.9 mV/°C (note the negative coefficient). Therefore, die temperature is directly related to ambient temperature and the power dissipated.

While the power to the AD9665 is disconnected, the AD9665 should be allowed to reach thermal equilibrium (at the desired ambient temperature). With all channels turned off such that I_{OUT} = 0 mA, measure V1 as shown in Figure 16 (note the polarity).

The second point of the 2-point measurement is obtained when the AD9665 is operated under load, for example, while driving a laser. Before taking the measurement, the AD9665 must be allowed adequate time to reach a thermal equilibrium.

As seen in Figure 16, the AD9665 has a finite parasitic resistance (R_S) between V_{DD} (Pin 17) and the base of the PNP transistor. This resistance is typically 120 mΩ. Because the goal of the experiment is to measure ΔV_{BE} of the transistor, the voltage drop across this resistance must be taken into account to get an accurate representation of the actual ΔV_{BE}. This voltage drop varies depending on the output current of the AD9665 operating under load. Therefore, the actual supply current (I_{DD}) must be measured for each measurement.

$$V_{DROP} = I_{DD} \times R_S$$

So the resulting ΔV_{BE} can be found as

$$\Delta V_{BE} = (V2 + V_{DROP2}) - (V1 + V_{DROP1})$$

For increasing temperature, this result should be negative.

From ΔV_{BE}, the final junction temperature is determined by

$$T_J = T_A + \left| \frac{\Delta V_{BE}}{-1.9 \text{ mV/°C}} \right|$$

From the resulting temperature rise in addition to the measured power dissipation, the thermal resistance from the junction to ambient can be calculated as

$$P_D = V_{DD} \times I_{DD} - V_{LOAD} \times I_{LOAD}$$

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

SHUTDOWN SUPPLY CURRENT VARIATION

The AD9665 defaults to TTL input mode when the ENABLE pin is tied low (ENABLE = 0), regardless of the position of the INS pin. Because of this, there can be additional supply current due to the applied voltage on the read, write, or OSCEN enable pins, the cause of which is an inverter located on the TTL input ENABLE pins (see Figure 17).

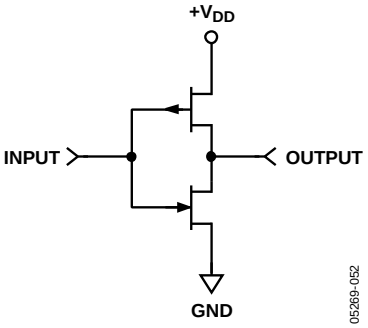


Figure 17. Inverter Circuit

Voltages close to GND or V_{DD} are not sufficient to turn on both transistors. However, as voltages vary from these extremes, significant current can flow. Figure 18 shows how the power-down current varies with voltage applied on the read, write, or OSCEN enable pins.

Therefore, to ensure the lowest possible shutdown current, the read, write, and OSCEN voltages should be tied to either 0 V or 5 V.

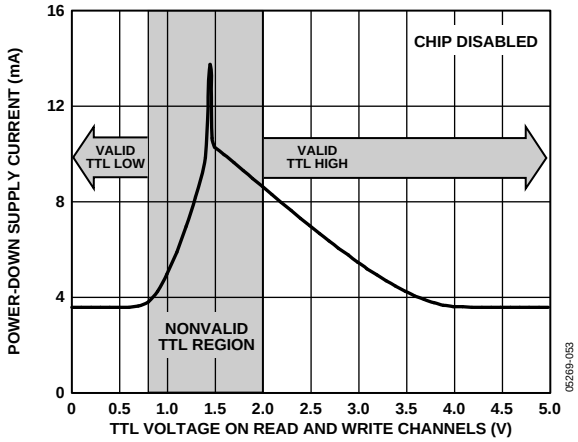


Figure 18. Read and Write TTL Enable Voltage vs. Supply Current

EVALUATION BOARD

SCHEMATIC

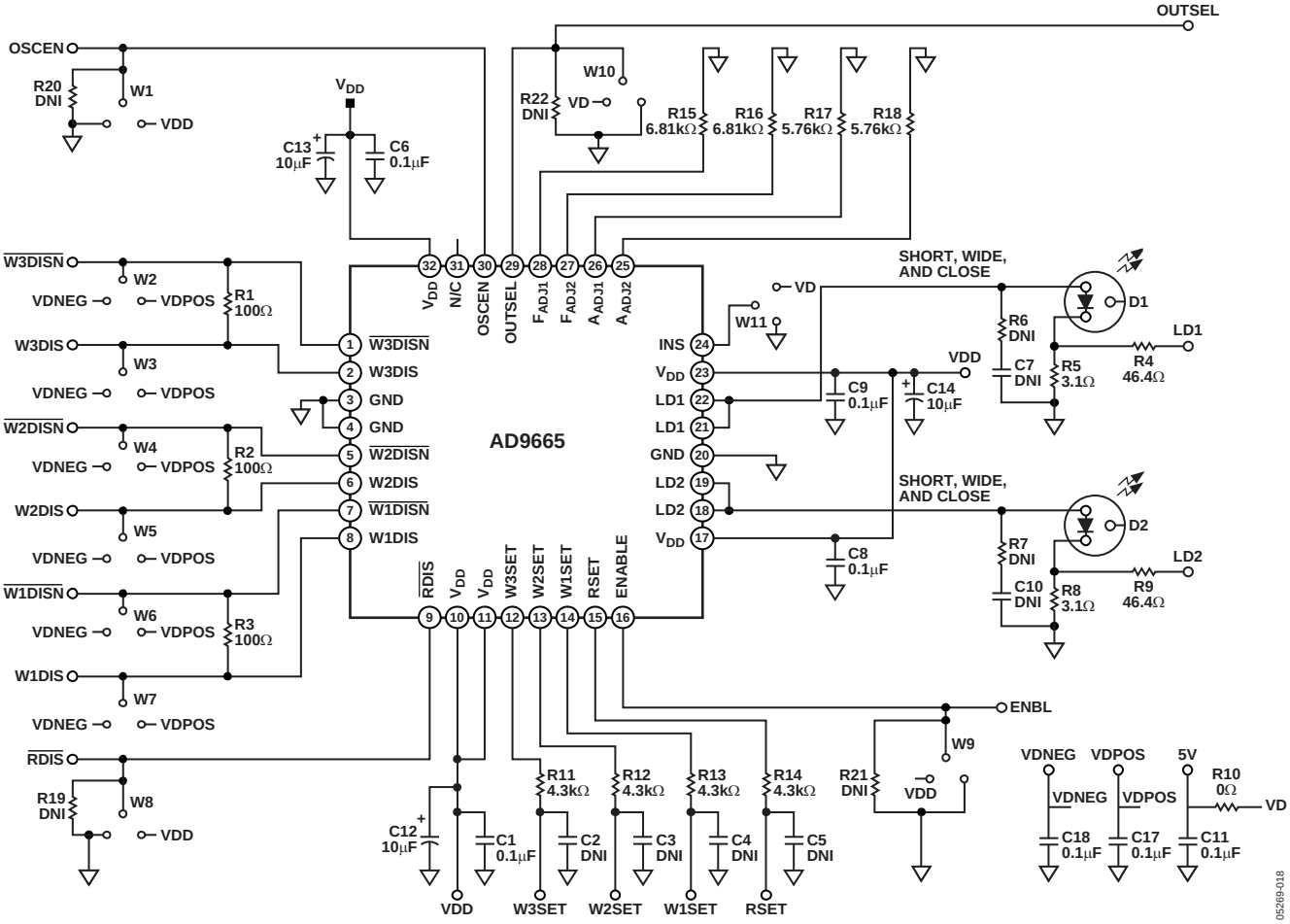


Figure 19. AD9665ACPZ-32 Evaluation Board Schematic

OPERATION

PIN DESCRIPTIONS

Table 5.

Pin No.	Mnemonic	Description
1	$\overline{\text{W3DISN}}$	Negative enable for Write Channel 3 (LVDS mode only)
2	W3DIS	Positive enable for Write Channel 3 (LVDS mode), enable (TTL mode)
3, 4	GND	GND
5	$\overline{\text{W2DISN}}$	Negative enable for Write Channel 2 (LVDS mode only)
6	W2DIS	Positive enable for Write Channel 2 (LVDS mode), enable (TTL mode)
7	$\overline{\text{W1DISN}}$	Negative enable for Write Channel 1 (LVDS mode only)
8	W1DIS	Positive enable for Write Channel 1 (LVDS mode), enable (TTL mode)
9	$\overline{\text{RDIS}}$	Enable for R Channel (TTL only)
10	V_{DD}	5 V supply and dc logic level for $\overline{\text{RDIS}}$ and ENABLE
11	V_{DD}	5 V supply and dc logic level for $\overline{\text{RDIS}}$ and ENABLE
12	W3SET	Input for Write Channel 3 (R_{IN} = 200 Ω)
13	W2SET	Input for Write Channel 2 (R_{IN} = 200 Ω)
14	W1SET	Input for Write Channel 1 (R_{IN} = 200 Ω)
15	RSET	Input for Read Channel (R_{IN} = 200 Ω)
16	ENABLE	Chip enable—active high
17	V_{DD}	Output stage supply, 5 V
18, 19	LD2	Output 2
20	GND	GND
21, 22	LD1	Output 1
23	V_{DD}	Output stage supply, 5 V
24	INS	Logic mode select (0 = TTL, 1 = LVDS)
25	A_{ADJ2}	Amplitude resistor set for Oscillator 2
26	A_{ADJ1}	Amplitude resistor set for Oscillator 1
27	F_{ADJ2}	Frequency resistor set for Oscillator 2
28	F_{ADJ1}	Frequency resistor set for Oscillator 1
29	OUTSEL	Output select (0 = LD2, 1 = LD1)
30	OSCEN	Oscillator enable—active high
31	N/C	No connection
32	V_{DD}	5 V supply and dc logic level for OSCEN
N/A	EPAD	The exposed pad should be connected to ground.

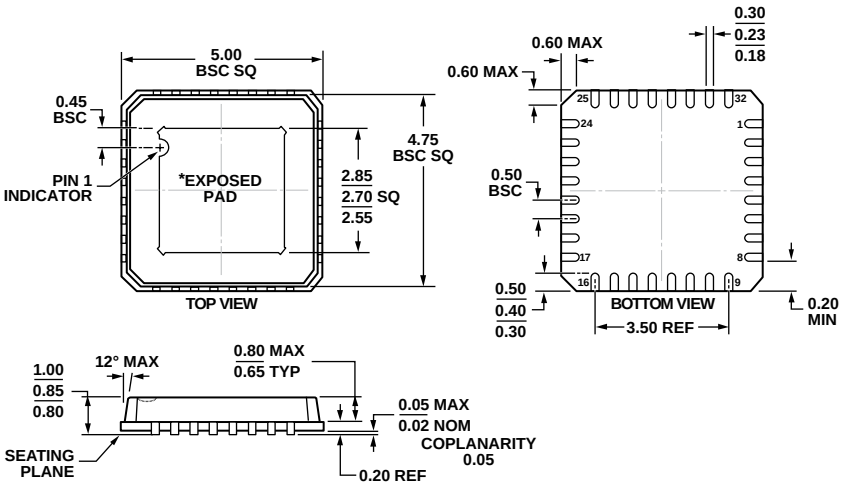
The logic signals, WxDIS, $\overline{\text{WxDISN}}$, $\overline{\text{RDIS}}$, ENABLE, INS, OUTSEL, and OSCEN, can be driven with pulsed sources or can be set to a steady state level with jumpers. For steady state operation, the logic levels for the WxDIS and $\overline{\text{WxDISN}}$ pins are set with voltages applied to the VDPOS and VDNEG pins on the evaluation board. For LVDS mode (INS = 1), VDPOS and VDNEG should be at a level greater than 50 mV and less than 2.45 V (0.050 V < VDPOS < 2.45 V and 0.05 V < VDNEG < 2.45 V), with the differential voltage greater than 100 mV and less than 600 mV. For TTL operation (INS = 0), VDPOS should be greater than 2.5 V and VDNEG should be less than 0.8 V. Under TTL operation, it may be convenient to put VDPOS at 5 V and VDNEG at 0 V. The pin labeled 5 V is the logic level for INS and OUTSEL.

The V_{DD} pins are connected together in the IC and can be connected to the same external supply. Although they are all connected internally, there must be a direct connection to each of these pins through their vector pins externally, which are also labeled V_{DD}.

A jumper set to the right side of a 3-lead connection applies the VDPOS voltage to the applicable pin on the IC. A jumper set to the left side of a 3-lead connection applies the VDNEG voltage.

Evaluation boards are shipped with 100 Ω termination resistors across the LVDS inputs and without 50 Ω resistors on the other logic traces. Resistors R5 and R8 can be connected between ground and the cathodes of Diode 1 and Diode 2, respectively. To monitor diode current with an oscilloscope, a 3.1 Ω resistor can be placed in each of these positions. The series 46.4 Ω resistors at R4 and R9 present a 50 Ω impedance to measurement equipment. This results in the oscilloscope displaying the diode current with a conversion factor of 1.558 mV/mA. If this capability is not desired, 0 Ω resistors can be installed in the R5 and R8 positions.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220 WITH EXCEPTION TO PADDLE ORIENTATION. FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION SECTION OF THIS DATA SHEET.

09-18-2008-A

Figure 20. 32-Lead Pad-Up, Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9665ACPZ-REEL	−25°C to +85°C	32-Lead, Pad-Up, Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-1
AD9665ACPZ-REEL7	−25°C to +85°C	32-Lead, Pad-Up, Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-1

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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