Digitally Programmable Sensor Signal Amplifier with EMI Filters

Data Sheet **AD8556**

FEATURES

- EMI filters at input pins
- Specified from −40°C to +140°C
- Low offset voltage: 10 µV maximum
- Low input offset voltage drift:
  - 65 nV/°C maximum
- High CMRR: 94 dB minimum
- Digitally programmable gain and output offset voltage
- Programmable output clamp voltage
- Open and short wire fault detection
- Low-pass filtering
- Single-wire serial interface
- Stable with any capacitive load
- SOIC_N and LFCSP_WQ packages
- 4.5 V to 5.5 V operation

APPLICATIONS

- Pressure and position sensors
- Precision current sensing
- Strain gages

FUNCTIONAL BLOCK DIAGRAM

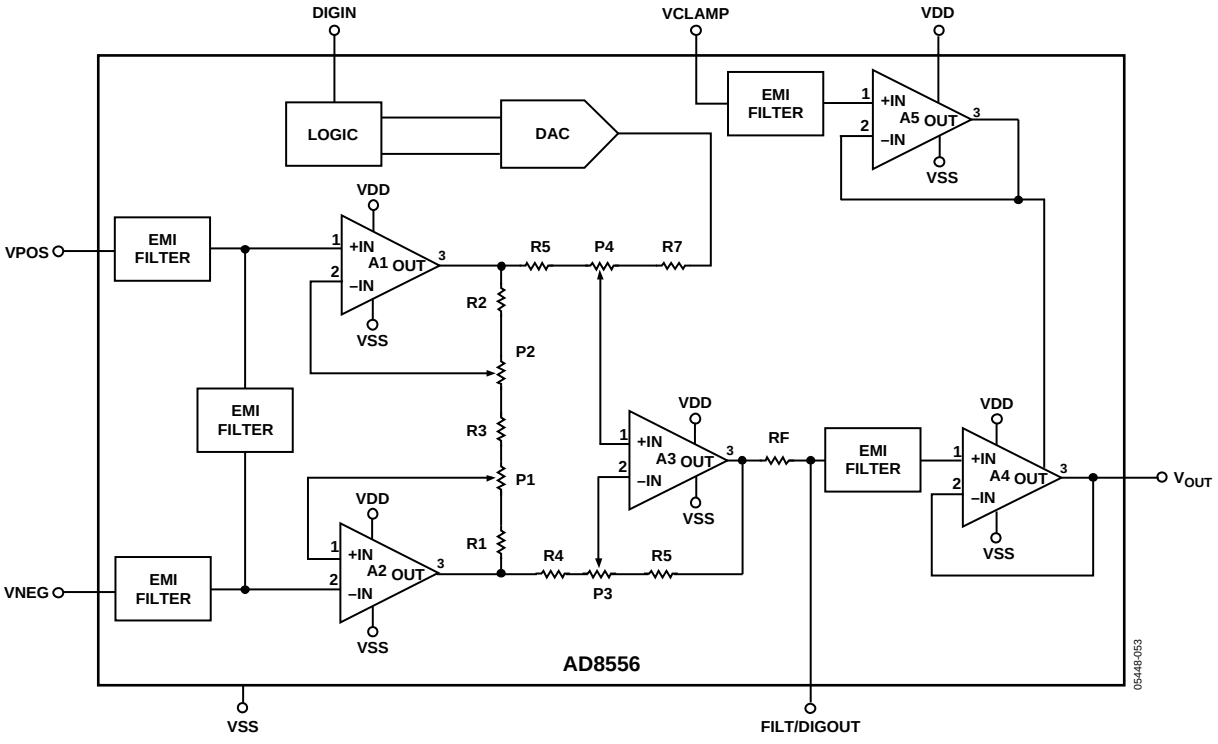

Figure 1.

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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Comparable Parts

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Evaluation Kits

- AD8555/AD8556/AD8557 Evaluation Board

Documentation

Data Sheet

- AD8556: Digitally Programmable Sensor Signal Amplifier with EMI Filters Data Sheet

Technical Books

- A Designer's Guide to Instrumentation Amplifiers, 3rd Edition, 2006

Reference Materials

Technical Articles

- Auto-Zero Amplifiers
- High-performance Adder Uses Instrumentation Amplifiers

Design Resources

- AD8556 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

2/15—Rev. A to Rev. B

Changed LFCSP_VQ Package to LFCSP_WQ Package ... Throughout
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Added Table 5; Renumbered Sequentially ... 8
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12/07—Rev. 0 to Rev. A

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5/05—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD8556 is a zero-drift, sensor signal amplifier with digitally programmable gain and output offset. Designed to easily and accurately convert variable pressure sensor and strain bridge outputs to a well-defined output voltage range, the AD8556 accurately amplifies many other differential or single-ended sensor outputs. The AD8556 uses the Analog Devices, Inc. patented low noise, auto-zero and DigiTrim® technologies to create an incredibly accurate and flexible signal processing solution in a very compact footprint.

Gain is digitally programmable in a wide range from 70 to 1280 through a serial data interface. Gain adjustment can be fully simulated in-circuit and then permanently programmed with reliable polyfuse technology. Output offset voltage is also digitally programmable and is ratiometric to the supply voltage. The AD8556 also features internal EMI filters on the VNEG, VPOS, FILT and VCLAMP pins.

In addition to extremely low input offset voltage, low input offset voltage drift, and very high dc and ac CMRR, the AD8556 also includes a pull-up current source at the input pins and a pull-down current source at the VCLAMP pin, which allows open wire and shorted wire fault detection. A low-pass filter function is implemented via a single low cost external capacitor. Output clamping set via an external reference voltage allows the AD8556 to drive lower voltage ADCs safely and accurately.

When used in conjunction with an ADC referenced to the same supply, the system accuracy becomes immune to normal supply voltage variations. Output offset voltage can be adjusted with a resolution of better than 0.4% of the difference between VDD and VSS. A lockout trim after gain and offset adjustment further ensures field reliability.

The AD8556 is fully specified from −40°C to +140°C. Operating from single-supply voltages of 4.5 V to 5.5 V, the AD8556 is offered in the 8-lead SOIC_N and 4 mm × 4 mm 16-lead LFCSP_WQ.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 5.0 V, VSS = 0.0 V, V_{CM} = 2.5 V, V_O = 2.5 V, −40°C ≤ T_A ≤ +140°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT STAGE						
Input Offset Voltage	V_{OS}	−40°C ≤ T_A ≤ +125°C		2	10	µV
		−40°C ≤ T_A ≤ +140°C		3	12	µV
Input Offset Voltage Drift	T_CV_{OS}			25	65	nV/°C
Input Bias Current	I_B	T_A = 25°C	38	49	54	nA
		−40°C ≤ T_A ≤ +125°C			58	nA
		−40°C ≤ T_A ≤ +140°C			60	nA
Input Offset Current	I_{OS}	T_A = 25°C		0.2	2.5	nA
		−40°C ≤ T_A ≤ +125°C			3.0	nA
		−40°C ≤ T_A ≤ +140°C			4.0	nA
Input Voltage Range			2.1		2.9	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 2.1 V to 2.9 V, A_V = 70	80	92		dB
		V_{CM} = 2.1 V to 2.9 V, A_V = 1280	94	112		dB
Linearity		V_O = 0.2 V to 3.4 V		20		ppm
		V_O = 0.2 V to 4.8 V		1000		ppm
Differential Gain Accuracy		Second stage gain = 17.5 to 100		0.35	1.6	%
		Second stage gain = 140 to 200		0.5	2.5	%
Differential Gain Temperature Coefficient		Second stage gain = 17.5 to 100		7	20	ppm/°C
		Second stage gain = 140 to 200		10	40	ppm/°C
RF			14	18	22	kΩ
RF Temperature Coefficient				600		ppm/°C
DAC						
Accuracy		A_V = 70, offset codes = 8 to 248		0.2	0.6	%
Ratiometricity		A_V = 70, offset codes = 8 to 248		50		ppm
Output Offset		A_V = 70, offset codes = 8 to 248		5	35	mV
Temperature Coefficient		−40°C ≤ T_A ≤ +125°C		3.3	15	ppm FS/°C
		−40°C ≤ T_A ≤ +140°C			25	ppm FS/°C
VCLAMP						
Input Bias Current		T_A = 25°C, VCLAMP = 5 V		200		nA
		−40°C ≤ T_A ≤ +125°C, VCLAMP = 5 V			500	nA
		−40°C ≤ T_A ≤ +140°C, VCLAMP = 5 V			550	nA
Input Voltage Range			1.2		4.94	V
OUTPUT BUFFER STAGE						
Buffer Offset				3	7	mV
Short-Circuit Current	I_{SC}		5		10	mA
Output Voltage, Low	V_{OL}	R_L = 10 kΩ to 5 V			20	mV
Output Voltage, High	V_{OH}	R_L = 10 kΩ to 0 V	4.94			V
POWER SUPPLY						
Supply Current	I_{SY}	−40°C ≤ T_A ≤ +125°C, V_O = 2.5 V, VPOS = VNEG = 2.5 V, VDAC code = 128		2.0	2.7	mA
		−40°C ≤ T_A ≤ +140°C, V_O = 2.5 V, VPOS = VNEG = 2.5 V, VDAC Code = 128			2.78	mA
Power Supply Rejection Ratio	PSRR	A_V = 70	109	125		dB
Supply Voltage Required During Programming		10°C < T_{PROG} < 40°C, supply capable of driving 250 mA	5.0	5.25	5.5	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	First gain stage, T_A = 25°C		2		MHz
		Second gain stage, T_A = 25°C		8		MHz
		Output buffer stage, T_A = 25°C		1.5		MHz
Output Buffer Slew Rate	SR	A_V = 70, R_L = 10 kΩ, C_L = 100 pF, T_A = 25°C		1.2		V/µs
Settling Time	t_s	To 0.1%, A_V = 70, 4 V output step, T_A = 25°C		8		µs
NOISE PERFORMANCE						
Input Referred Noise		T_A = 25°C, f = 1 kHz		32		nV/√Hz
Low Frequency Noise	e_n p-p	f = 0.1 Hz to 10 Hz, T_A = 25°C		0.5		µV p-p
Total Harmonic Distortion	THD	V_{IN} = 16.75 mV rms, f = 1 kHz, A_V = 100, T_A = 25°C		−100		dB
DIGITAL INTERFACE						
Input Current				2		µA
DIGIN Pulse Width to Load 0	tw_0	T_A = 25°C	0.05		10	µs
DIGIN Pulse Width to Load 1	tw_1	T_A = 25°C	50			µs
Time Between Pulses at DIGIN	tw_s	T_A = 25°C	10			µs
DIGIN Low		T_A = 25°C			1	V
DIGIN High		T_A = 25°C	4			V
DIGOUT Logic 0		T_A = 25°C			1	V
DIGOUT Logic 1		T_A = 25°C	4			V

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	VSS − 0.3 V to VDD + 0.3 V
Differential Input Voltage[1]	±5.0 V
Output Short-Circuit Duration to VSS or VDD	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +150°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature	300°C

[1] Differential input voltage is limited to ±5.0 V or ± the supply voltage, whichever is less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead SOIC_N (R)	158	43	°C/W
16-Lead LFCSP_WQ (CP)	44	31.5	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for LFCSP_WQ package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

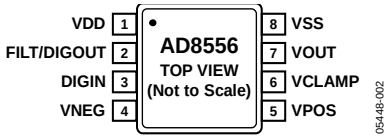

Figure 2. 8-Lead SOIC_N Pin Configuration

Table 4. 8-Lead SOIC_N Pin Function Descriptions

SOIC_N	Mnemonic	Description
1	VDD	Positive Supply Voltage.
2	FILT/DIGOUT	Unbuffered Amplifier Output in Series with a Resistor RF. Adding a capacitor between FILT and VDD or VSS implements a low-pass filtering function. In read mode, this pin functions as a digital output.
3	DIGIN	Digital Input.
4	VNEG	Negative Amplifier Input (Inverting Input).
5	VPOS	Positive Amplifier Input (Noninverting Input).
6	VCLAMP	Set Clamp Voltage at Output.
7	VOUT	Buffered Amplifier Output. Buffered version of the signal at the FILT/DIGOUT pin. In read mode, VOUT is a buffered digital output.
8	VSS	Negative Supply Voltage.

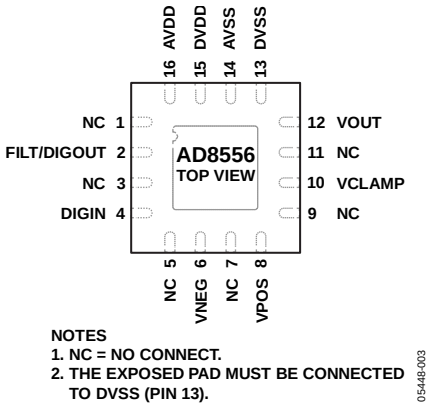

Figure 3. 16-Lead LFCSP_WQ Pin Configuration

Table 5. 16-Lead LFCSP_WQ Pin Function Descriptions

LFCSP_WQ	Mnemonic	Description
0	EPAD	Exposed Pad. The exposed pad must be connected to DVSS (Pin 13).
1, 3, 5, 7, 9, 11	NC	Do Not Connect.
2	FILT/DIGOUT	Unbuffered Amplifier Output in Series with a Resistor RF. Adding a capacitor between FILT and VDD or VSS implements a low-pass filtering function. In read mode, this pin functions as a digital output.
4	DIGIN	Digital Input.
6	VNEG	Negative Amplifier Input (Inverting Input).
8	VPOS	Positive Amplifier Input (Noninverting Input).
10	VCLAMP	Set Clamp Voltage at Output.
12	VOUT	Buffered Amplifier Output. Buffered version of the signal at the FILT/DIGOUT pin. In read mode, VOUT is a buffered digital output.
	VSS	Negative Supply Voltage.
13, 14	DVSS, AVSS	Negative Supply Voltage.
15, 16	DVDD, AVDD	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

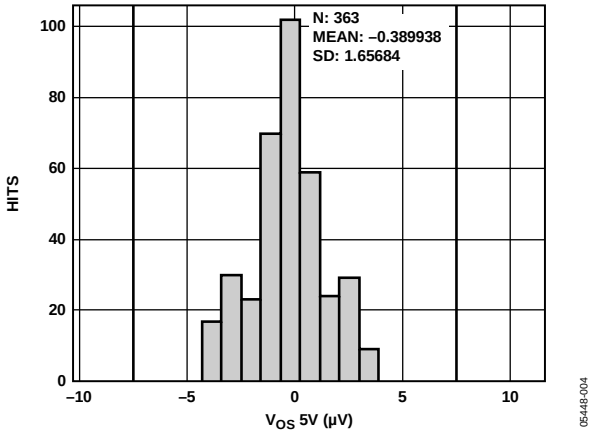

Figure 4. Input Offset Voltage Distribution

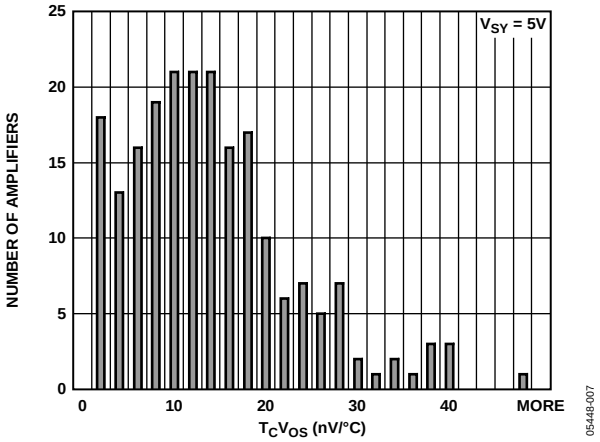

Figure 7. T_CV_{OS} at V_{SY} = 5 V

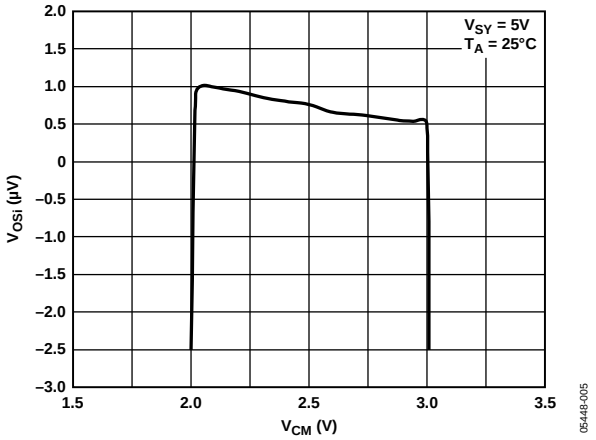

Figure 5. Input Offset Voltage vs. Common-Mode Voltage

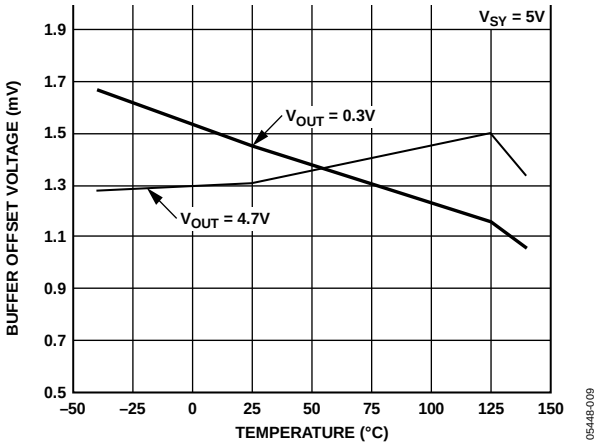

Figure 8. Output Buffer Offset Voltage vs. Temperature

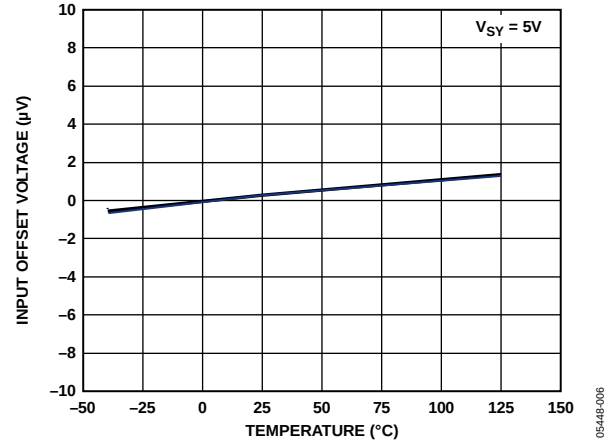

Figure 6. Input Offset Voltage vs. Temperature

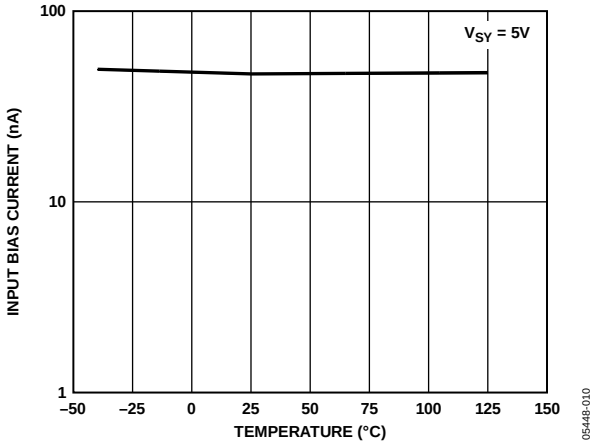

Figure 9. Input Bias Current at VPOS, VNEG vs. Temperature

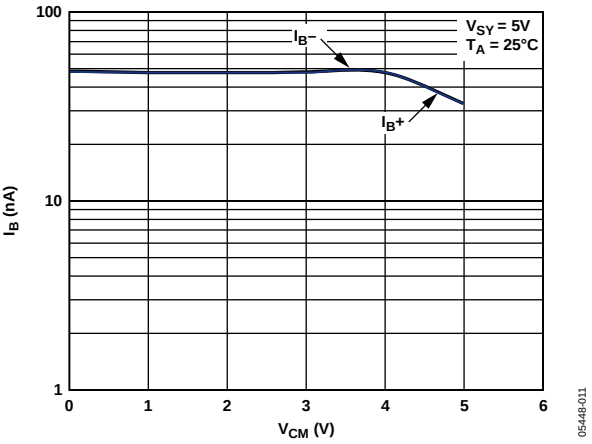

Figure 10. Input Bias Current at VPOS, VNEG vs. Common-Mode Voltage

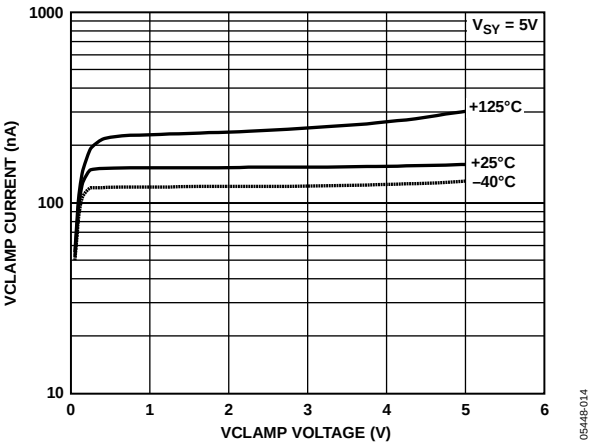

Figure 13. VCLAMP Current over Temperature at V_S = 5 V vs. VCLAMP Voltage

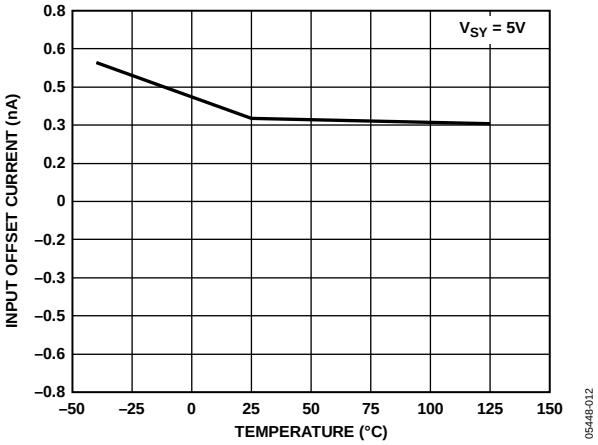

Figure 11. Input Offset Current vs. Temperature

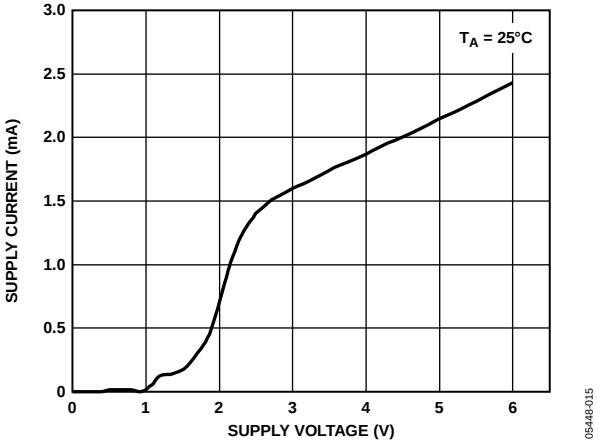

Figure 14. Supply Current (I_{SY}) vs. Supply Voltage

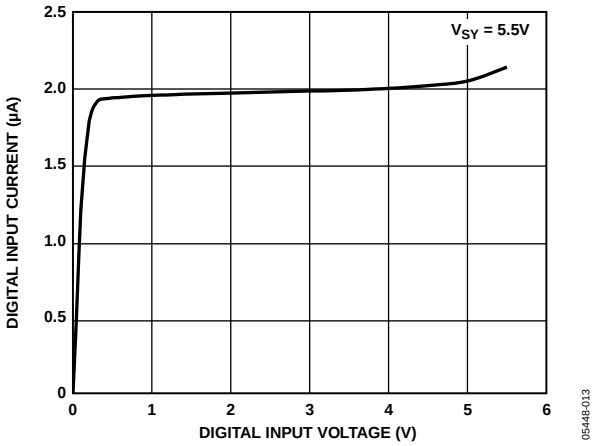

Figure 12. Digital Input Current vs. Digital Input Voltage (Pin 4)

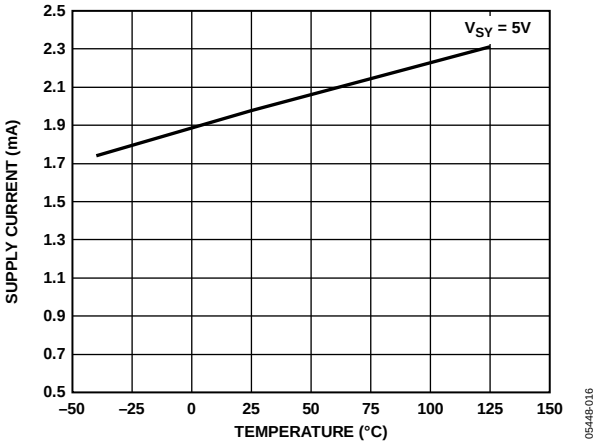

Figure 15. Supply Current (I_{SY}) vs. Temperature

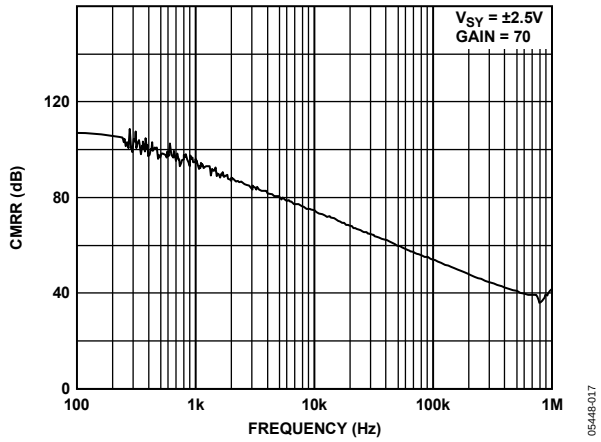

Figure 16. CMRR vs. Frequency

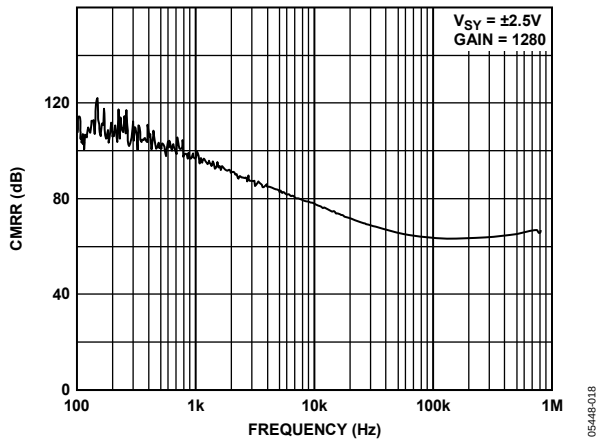

Figure 17. CMRR vs. Frequency

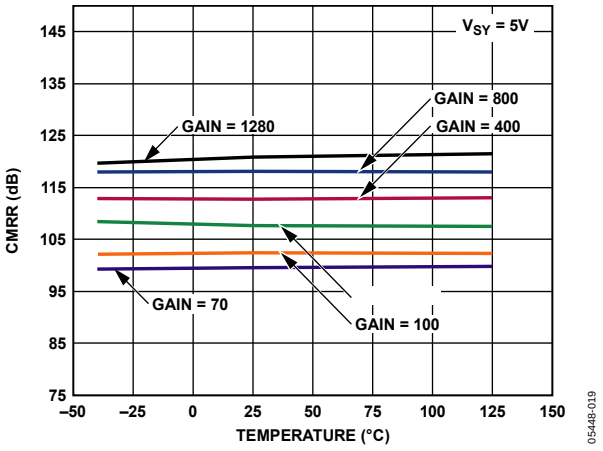

Figure 18. CMRR vs. Temperature at Different Gains

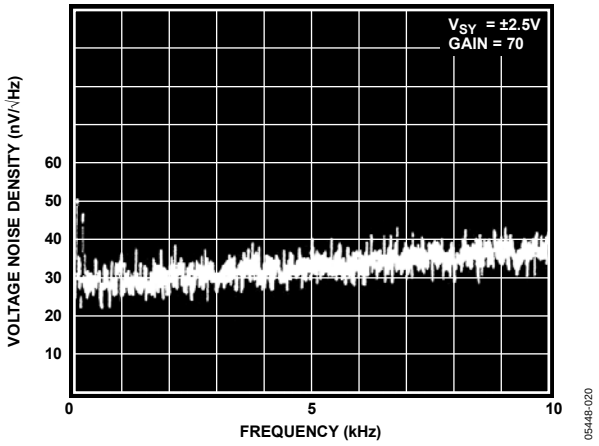

Figure 19. Voltage Noise Density vs. Frequency (0 Hz to 10 kHz)

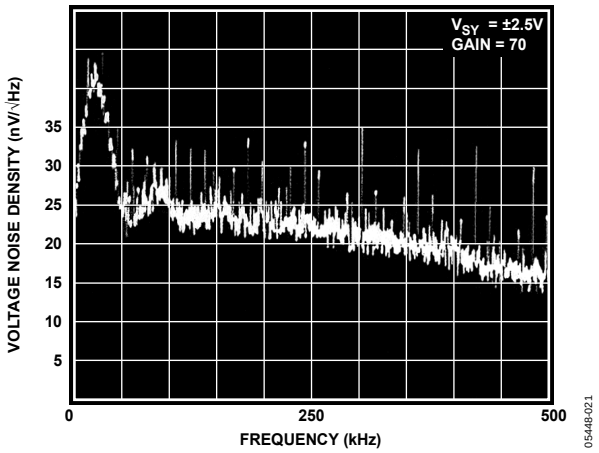

Figure 20. Voltage Noise Density vs. Frequency (0 Hz to 500 kHz)

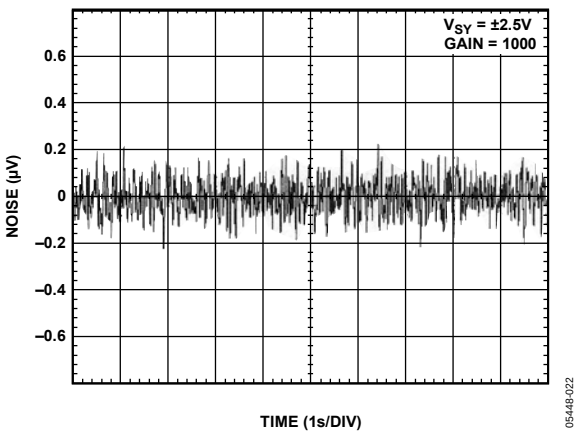

Figure 21. Low Frequency Input Voltage Noise (0.1 Hz to 10 Hz)

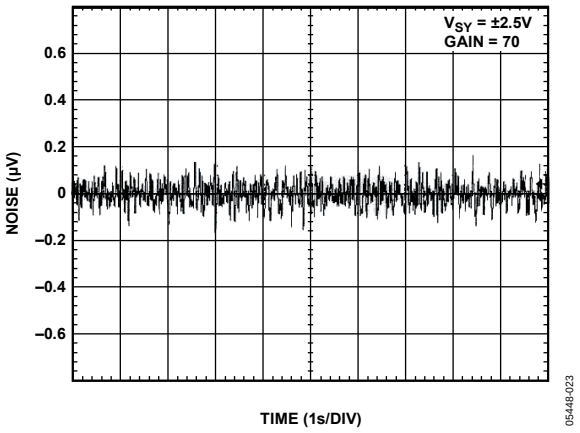

Figure 22. Low Frequency Input Voltage Noise (0.1 Hz to 10 Hz)

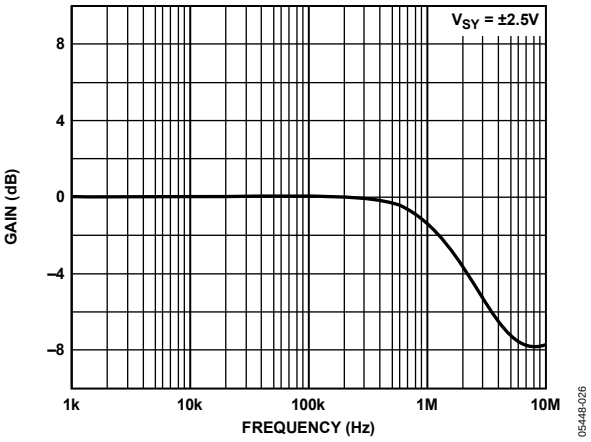

Figure 25. Output Buffer Gain vs. Frequency

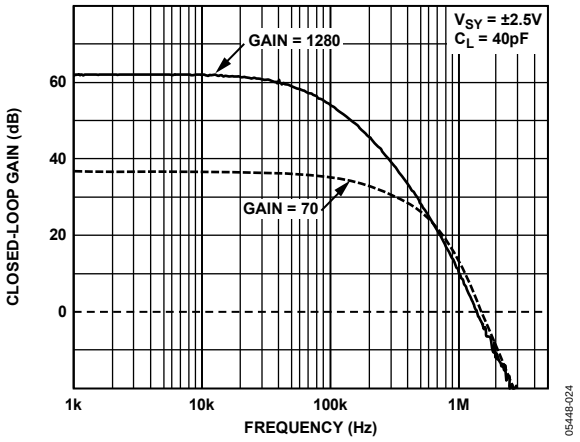

Figure 23. Closed-Loop Gain vs. Frequency Measured at FILT/DIGOUT Pin

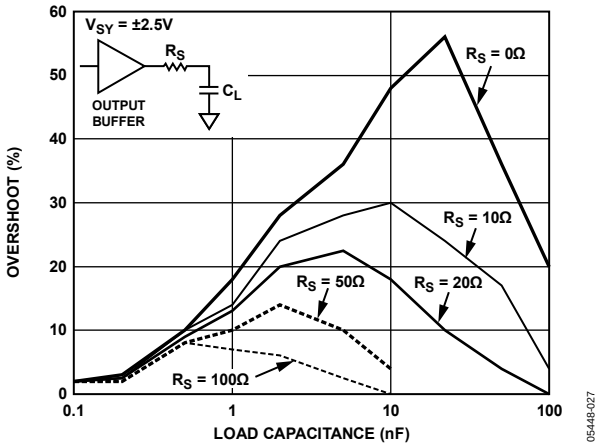

Figure 26. Output Buffer Positive Overshoot

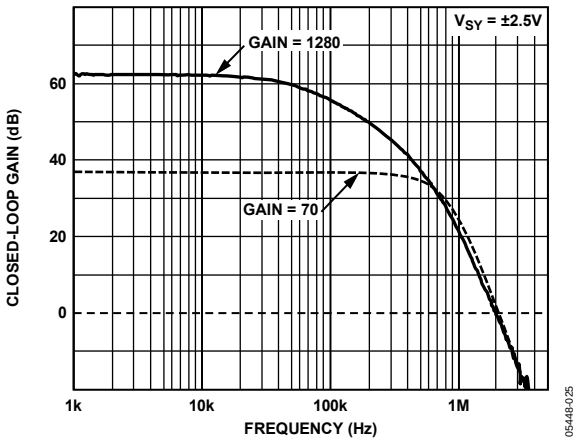

Figure 24. Closed-Loop Gain vs. Frequency Measured at VOUT Pin

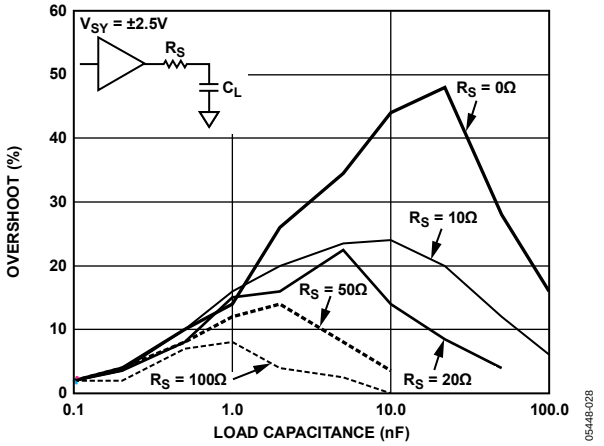

Figure 27. Output Buffer Negative Overshoot

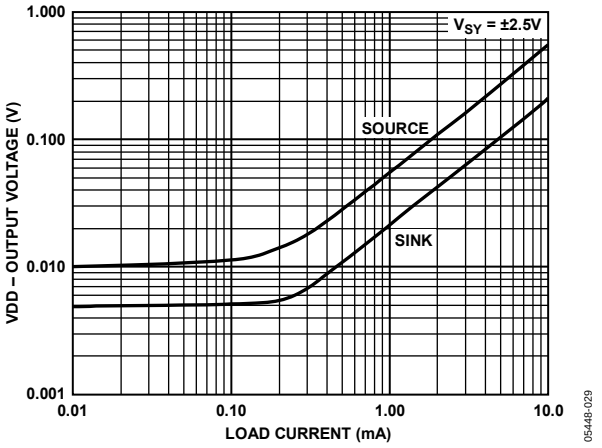

Figure 28. Output Voltage to Supply Rail vs. Load Current

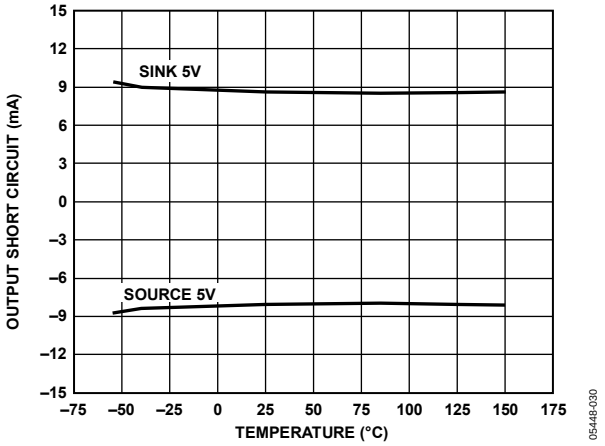

Figure 29. Output Short Circuit vs. Temperature

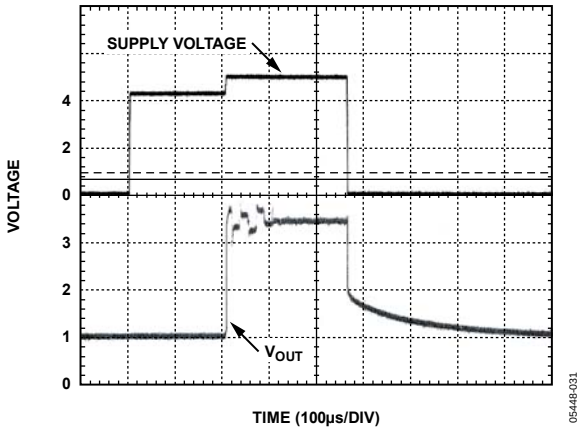

Figure 30. Power-On Response at 25°C

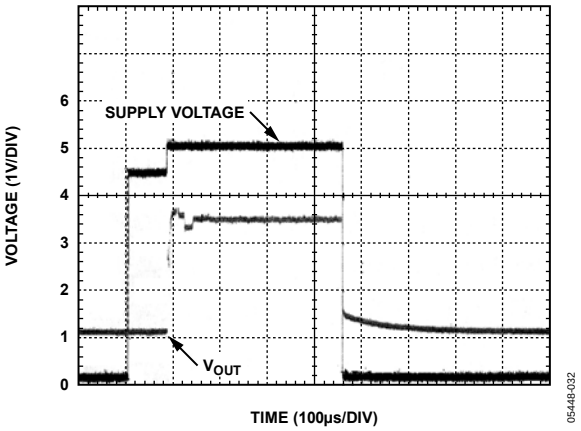

Figure 31. Power-On Response at 125°C

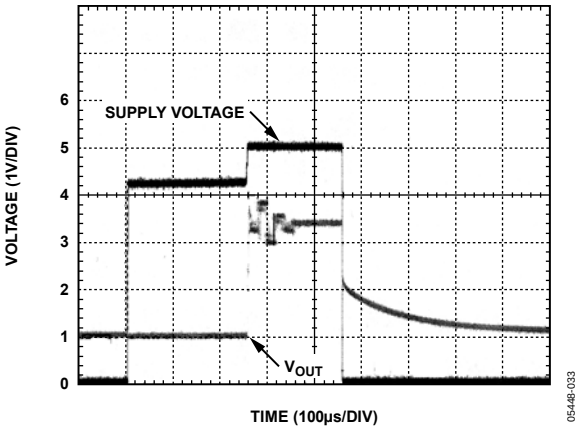

Figure 32. Power-On Response at –40°C

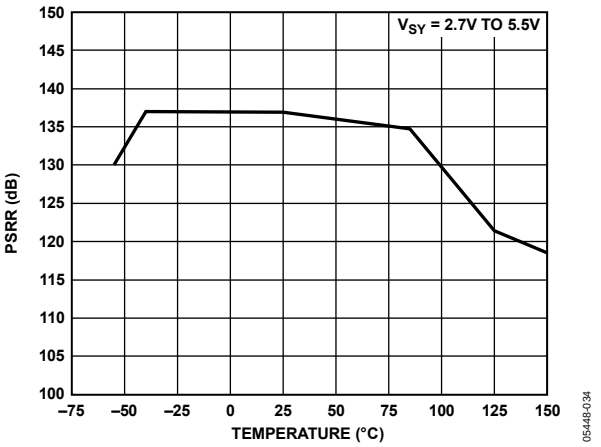

Figure 33. PSRR vs. Temperature

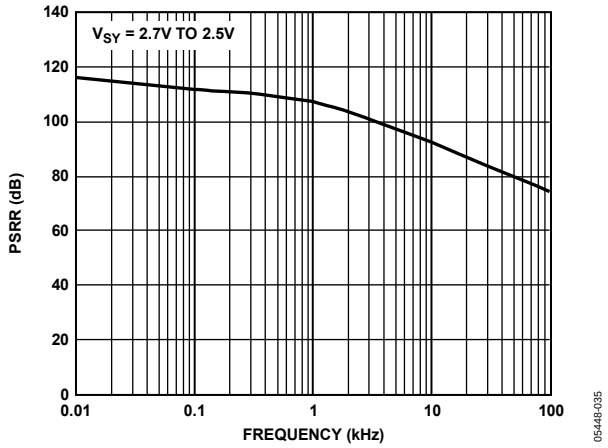

Figure 34. PSRR vs. Frequency

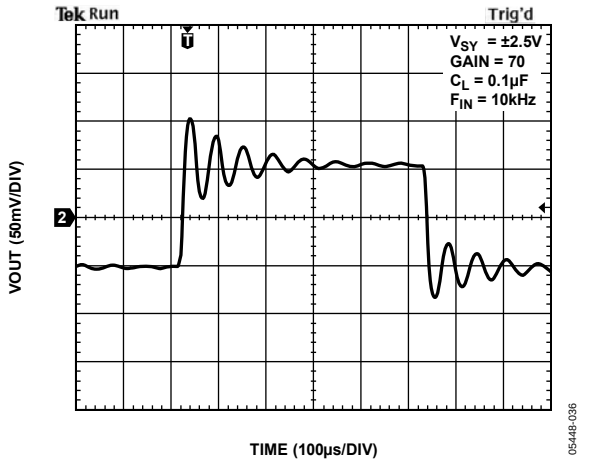

Figure 35. Small Signal Response at C_L = 0.1 µF and F_{IN} = 10 kHz

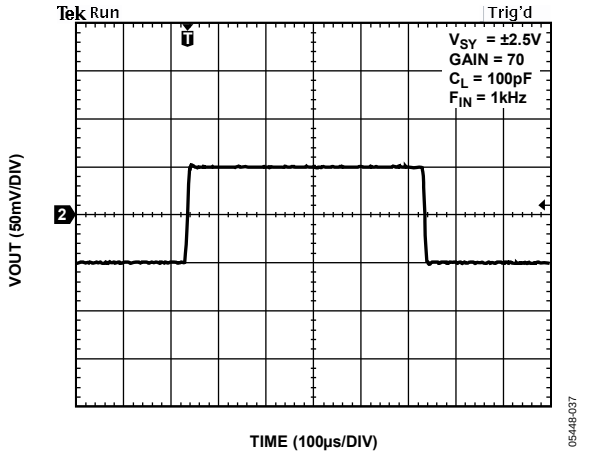

Figure 36. Small Signal Response at C_L = 100 pF and F_{IN} = 1 kHz

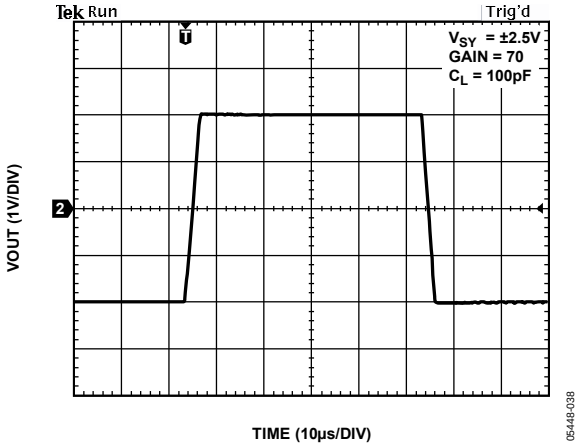

Figure 37. Large Signal Response at C_L = 100 pF

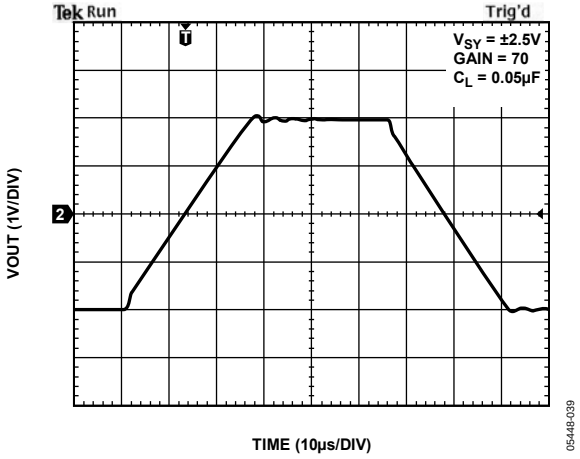

Figure 38. Large Signal Response at C_L = 0.05 µF

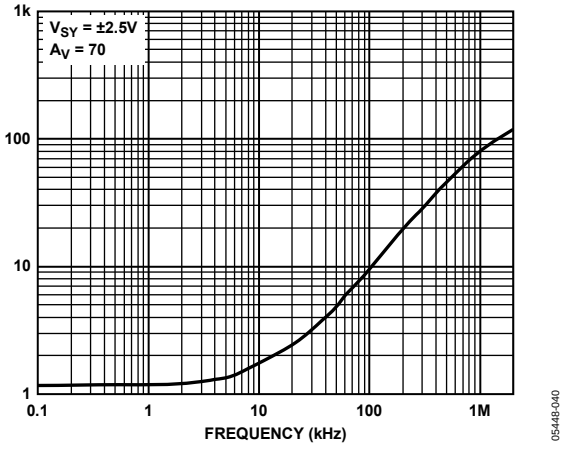

Figure 39. Output Impedance vs. Frequency

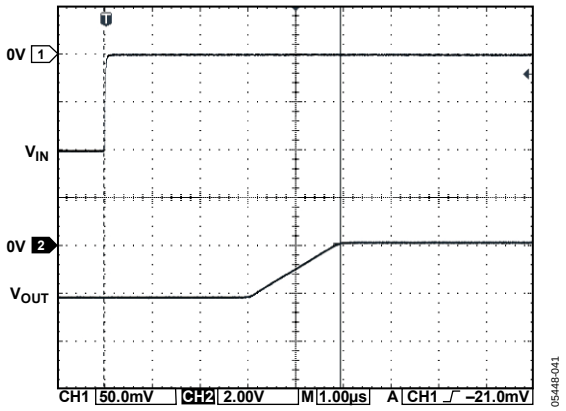

Figure 40. Negative Overload Recovery (Gain = 70)

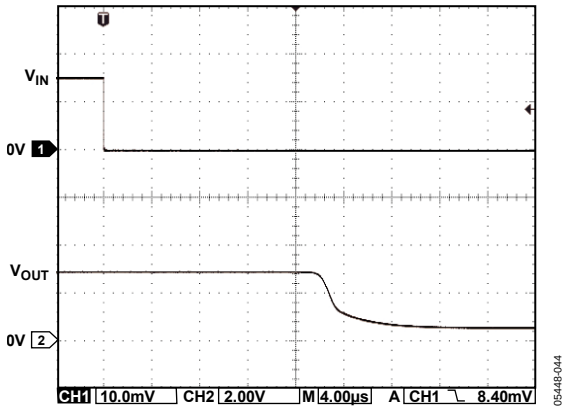

Figure 43. Positive Overload Recovery (Gain = 1280)

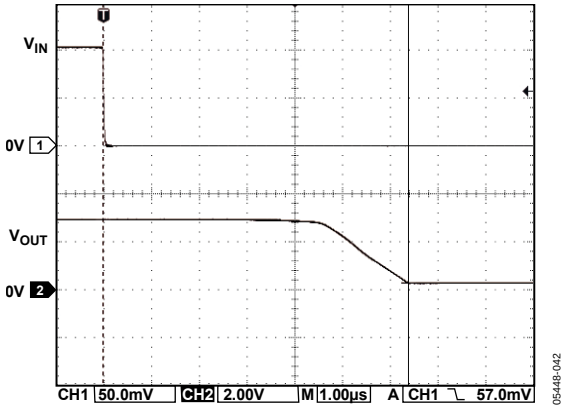

Figure 41. Positive Overload Recovery (Gain = 70)

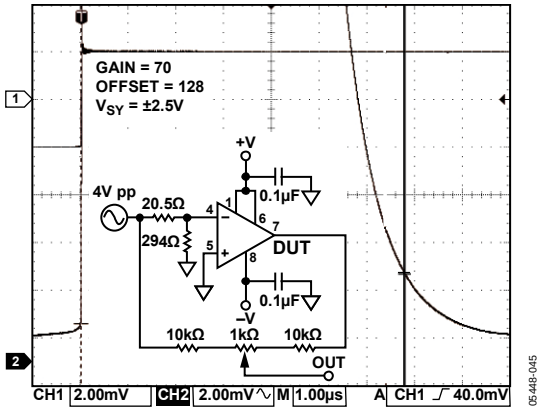

Figure 44. Settling Time 0.1%

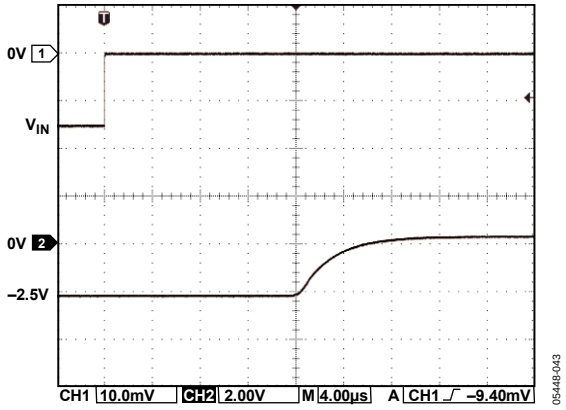

Figure 42. Negative Overload Recovery (Gain = 1280)

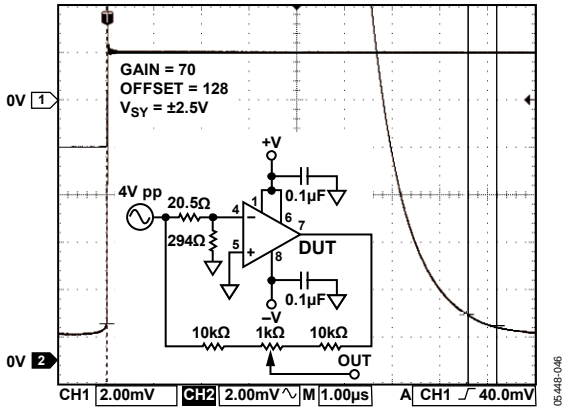

Figure 45. Settling Time 0.01%

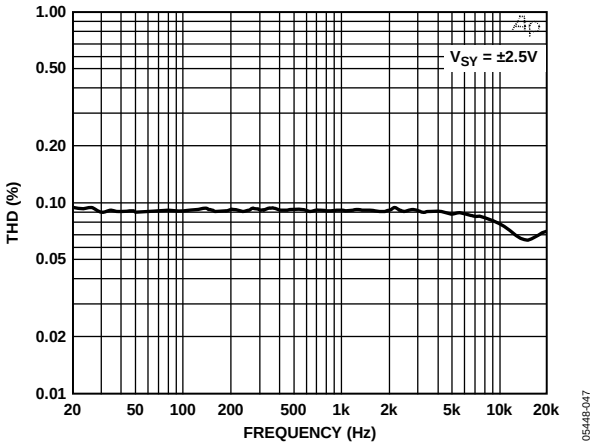

Figure 46. THD vs. Frequency

THEORY OF OPERATION

A1, A2, R1, R2, R3, P1, and P2 form the first gain stage of the differential amplifier. A1 and A2 are auto-zeroed op amps that minimize input offset errors. P1 and P2 are digital potentiometers, guaranteed to be monotonic. Programming P1 and P2 allows the first stage gain to be varied from 4.0 to 6.4 with 7-bit resolution (see Table 6 and Equation 1), giving a fine gain adjustment resolution of 0.37%. R1, R2, R3, P1, and P2 each have a similar temperature coefficient; therefore, the first stage gain temperature coefficient is lower than 100 ppm/°C.

$$GAIN1 \approx 4 \times \left(\frac{6.4}{4}\right)^{\left(\frac{Code}{127}\right)} \quad (1)$$

A3, R4, R5, R6, R7, P3, and P4 form the second gain stage of the differential amplifier. A3 is also an auto-zeroed op amp that minimizes input offset errors. P3 and P4 are digital potentiometers that allow the second stage gain to be varied from 17.5 to 200 in eight steps (see Table 7). R4, R5, R6, R7, P3, and P4 each have a similar temperature coefficient; therefore, the second stage gain temperature coefficient is lower than 100 ppm/°C.

RF together with an external capacitor, connected between FILT/DIGOUT and VSS or VDD, form a low-pass filter. The filtered signal is buffered by A4 to give a low impedance output at VOUT. RF is nominally 18 kΩ, allowing an 880 Hz low-pass filter to be implemented by connecting a 10 nF external capacitor between FILT/DIGOUT and VSS or between FILT/DIGOUT and VDD. If low-pass filtering is not needed, the FILT/DIGOUT pin must be left floating.

A5 implements a voltage buffer that provides the positive supply to A4, the amplifier output buffer. Its function is to limit VOUT to a maximum value, useful for driving ADCs operating on supply voltages lower than VDD. The input to A5, VCLAMP, has a very high input resistance. It should be connected to a known voltage and not left floating. However, the high input impedance allows the clamp voltage to be set using a high impedance source, such as a potential divider. If the maximum value of VOUT does not need to be limited, VCLAMP should be connected to VDD.

A4 implements a rail-to-rail input and output unity-gain voltage buffer. The output stage of A4 is supplied from a buffered version of VCLAMP instead of VDD, allowing the positive swing to be limited. The maximum output current is limited between 5 mA to 10 mA.

An 8-bit DAC is used to generate a variable offset for the amplifier output. This DAC is guaranteed to be monotonic. To preserve the ratiometric nature of the input signal, the DAC references are driven from VSS and VDD, and the DAC output can swing from VSS (Code 0) to VDD (Code 255). The 8-bit resolution is equivalent to 0.39% of the difference between VDD and VSS, for example, 19.5 mV with a 5 V supply. The DAC output voltage (VDAC) is given approximately by

$$VDAC \approx \left(\frac{Code + 0.5}{256}\right)(VDD - VSS) + VSS \quad (2)$$

where the temperature coefficient of VDAC is lower than 200 ppm/°C.

The amplifier output voltage (VOUT) is given by

$$VOUT = GAIN\ (VPOS - VNEG) + VDAC \quad (3)$$

where GAIN is the product of the first and second stage gains.

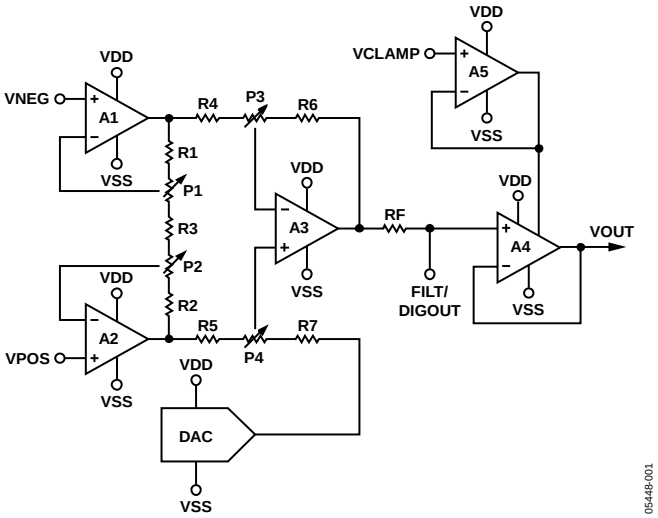

Figure 47. Functional Schematic

GAIN VALUES

Table 6. First Stage Gain vs. First Stage Gain Code

First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain
0	4.000	32	4.503	64	5.069	96	5.706
1	4.015	33	4.520	65	5.088	97	5.727
2	4.030	34	4.536	66	5.107	98	5.749
3	4.045	35	4.553	67	5.126	99	5.770
4	4.060	36	4.570	68	5.145	100	5.791
5	4.075	37	4.587	69	5.164	101	5.813
6	4.090	38	4.604	70	5.183	102	5.834
7	4.105	39	4.621	71	5.202	103	5.856
8	4.120	40	4.638	72	5.221	104	5.878
9	4.135	41	4.655	73	5.241	105	5.900
10	4.151	42	4.673	74	5.260	106	5.921
11	4.166	43	4.690	75	5.280	107	5.943
12	4.182	44	4.707	76	5.299	108	5.965
13	4.197	45	4.725	77	5.319	109	5.988
14	4.213	46	4.742	78	5.339	110	6.010
15	4.228	47	4.760	79	5.358	111	6.032
16	4.244	48	4.778	80	5.378	112	6.054
17	4.260	49	4.795	81	5.398	113	6.077
18	4.276	50	4.813	82	5.418	114	6.099
19	4.291	51	4.831	83	5.438	115	6.122
20	4.307	52	4.849	84	5.458	116	6.145
21	4.323	53	4.867	85	5.479	117	6.167
22	4.339	54	4.885	86	5.499	118	6.190
23	4.355	55	4.903	87	5.519	119	6.213
24	4.372	56	4.921	88	5.540	120	6.236
25	4.388	57	4.939	89	5.560	121	6.259
26	4.404	58	4.958	90	5.581	122	6.283
27	4.420	59	4.976	91	5.602	123	6.306
28	4.437	60	4.995	92	5.622	124	6.329
29	4.453	61	5.013	93	5.643	125	6.353
30	4.470	62	5.032	94	5.664	126	6.376
31	4.486	63	5.050	95	5.685	127	6.400

Table 7. Second Stage Gain and Gain Ranges vs. Second Stage Gain Code

Second Stage Gain Code	Second Stage Gain	Minimum Combined Gain	Maximum Combined Gain
0	17.5	70	112
1	25	100	160
2	35	140	224
3	50	200	320
4	70	280	448
5	100	400	640
6	140	560	896
7	200	800	1280

OPEN WIRE FAULT DETECTION

The inputs to A1 and A2, VNEG and VPOS, each have a comparator to detect whether VNEG or VPOS exceeds a threshold voltage, nominally VDD − 2.0 V. If (VNEG > VDD − 2.0 V) or (VPOS > VDD − 2.0 V), VOUT is clamped to VSS. The output current limit circuit is disabled in this mode, but the maximum sink current is approximately 10 mA when VDD = 5 V. The inputs to A1 and A2, VNEG and VPOS, are also pulled up to VDD by currents IP1 and IP2. These are both nominally 49 nA and matched to within 3 nA. If the inputs to A1 or A2 are accidentally left floating, as with an open wire fault, IP1 and IP2 pull them to VDD, which would cause VOUT to swing to VSS, allowing this fault to be detected. It is not possible to disable IP1 and IP2, nor the clamping of VOUT to VSS, when VNEG or VPOS approaches VDD.

SHORTED WIRE FAULT DETECTION

The AD8556 provides fault detection when VPOS, VNEG, or VCLAMP shorts to VDD and VSS. Figure 48 shows the voltage regions at VPOS, VNEG, and VCLAMP that trigger an error condition. When an error condition occurs, the VOUT pin is shorted to VSS. Table 8 lists the voltage levels shown in Figure 48.

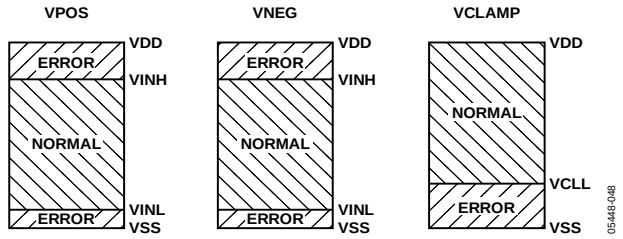

Figure 48. Voltage Regions at VPOS, VNEG, and VCLAMP that Trigger a Fault Condition

Table 8. Typical VINL, VINH, and VCLL Values (VDD = 5 V)

Voltage	Min (V)	Typ (V)	Max (V)	VOUT Condition
VINH	2.95	3.0	3.05	Short to VSS fault detection
VINL	1.95	2.0	2.05	Short to VSS fault detection
VCLL	1.05	1.1	1.15	Short to VSS fault detection

FLOATING VPOS, VNEG, OR VCLAMP FAULT DETECTION

A floating fault condition at the VPOS, VNEG, or VCLAMP pins is detected by using a low current to pull a floating input into an error voltage range, defined in the Shorted Wire Fault Detection section. In this way, the VOUT pin is shorted to VSS when a floating input is detected. Table 9 lists the currents used.

Table 9. Floating Fault Detection at VPOS, VNEG, and VCLAMP

Mnemonic	Typical Current	Goal of Current
VPOS	49 nA pull-up	Pull VPOS above VINH
VNEG	49 nA pull-up	Pull VNEG above VINH
VCLAMP	0.2 µA pull-down	Pull VCLAMP below VCLL

DEVICE PROGRAMMING

Digital Interface

The digital interface allows the first stage gain, second stage gain, and output offset to be adjusted and allows desired values for these parameters to be permanently stored by selectively blowing polysilicon fuses. To minimize pin count and board space, a single-wire digital interface is used. The digital input pin, DIGIN, has hysteresis to minimize the possibility of inadvertent triggering with slow signals. It also has a pull-down current sink to allow it to be left floating when programming is not being performed. The pull-down ensures inactive status of the digital input by forcing a dc low voltage on DIGIN.

A short pulse at DIGIN from low to high and back to low again, such as between 50 ns and 10 µs long, loads 0 into the shift register. A long pulse at DIGIN, such as 50 µs or longer, loads 1 into the shift register. The time between pulses should be at least 10 µs. Assuming VSS = 0 V, voltages at DIGIN between VSS and 0.2 × VDD are recognized as a low, and voltages at DIGIN between 0.8 × VDD and VDD are recognized as a high. The timing diagram example in Figure 49 shows the waveform for entering code 010011 into the shift register.

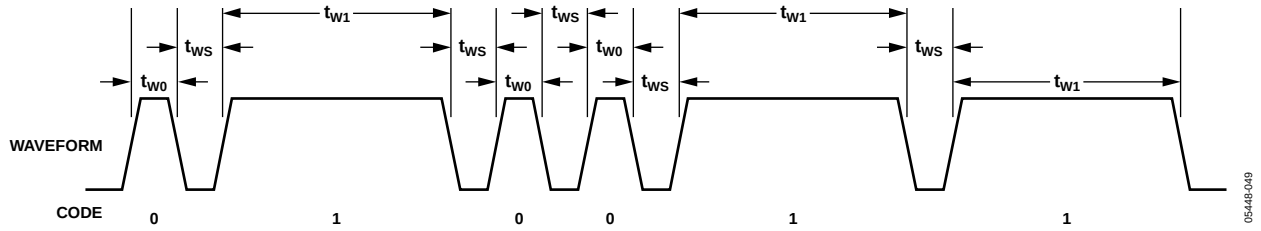

Figure 49. Timing Diagram for Code 010011

Table 10. Timing Specifications

Timing Parameter	Description	Specification
t_{W0}	Pulse width for loading 0 into shift register	Between 50 ns and 10 µs
t_{W1}	Pulse width for loading 1 into shift register	≥50 µs
t_{WS}	Width between pulses	≥10 µs

Table 11. 38-Bit Serial Word Format

Field No.	Bits	Description
0	0 to 11	12-Bit Start of Packet 1000 0000 0001
1	12 to 13	2-Bit Function 00: Change Sense Current 01: Simulate Parameter Value 10: Program Parameter Value 11: Read Parameter Value
2	14 to 15	2-Bit Parameter 00: Second Stage Gain Code 01: First Stage Gain Code 10: Output Offset Code 11: Other Functions
3	16 to 17	2-Bit Dummy 10
4	18 to 25	8-Bit Value Parameter 00 (Second Stage Gain Code): 3 LSBs Used Parameter 01 (First Stage Gain Code): 7 LSBs Used Parameter 10 (Output Offset Code): All 8 Bits Used Parameter 11 (Other Functions) Bit 0 (LSB): Master Fuse Bit 1: Fuse for Production Test at Analog Devices Bit 2: Parity Fuse
5	26 to 37	12-Bit End of Packet 0111 1111 1110

A 38-bit serial word is used, divided into 6 fields. Assuming each bit can be loaded in 60 µs, the 38-bit serial word transfers in 2.3 ms. Table 11 summarizes the word format.

Field 0 and Field 5 are the start-of-packet field and end-of-packet field, respectively. Matching the start-of-packet field with 1000 0000 0001 and the end-of-packet field with 0111 1111 1110 ensures that the serial word is valid and enables decoding of the other fields.

Field 3 breaks up the data and ensures that no data combination can inadvertently trigger the start-of-packet and end-of-packet fields. Field 0 should be written first and Field 5 written last.

Within each field, the MSB must be written first and the LSB written last. The shift register features power-on reset to minimize the risk of inadvertent programming; power-on reset occurs when VDD is between 0.7 V and 2.2 V.

Initial State

Initially, all the polysilicon fuses are intact. Each parameter has the value 0 assigned (see Table 12).

Table 12. Initial State Before Programming

Second Stage Gain Code = 0	Second Stage Gain = 17.5
First stage gain code = 0	First stage gain = 4.0
Output offset code = 0	Output offset = VSS
Master fuse = 0	Master fuse not blown

When power is applied to a device, parameter values are taken either from internal registers, if the master fuse is not blown, or from the polysilicon fuses, if the master fuse is blown. Programmed values have no effect until the master fuse is blown. The internal registers feature power-on reset; therefore, the unprogrammed devices enter a known state after power-up. Power-on reset occurs when VDD is between 0.7 V and 2.2 V.

Simulation Mode

The simulation mode allows any parameter to be temporarily changed. These changes are retained until the simulated value is reprogrammed, the power is removed, or the master fuse is blown. Parameters are simulated by setting Field 1 to 01, selecting the desired parameter in Field 2, and the desired value for the parameter in Field 4. Note that a value of 11 for Field 2 is ignored during the simulation mode. Examples of temporary settings are as follows:

- Setting the second stage gain code (Parameter 00) to 011 and the second stage gain to 50 produces:
  1000 0000 0001 01 00 10 0000 0011 0111 1111 1110.
- Setting the first stage gain code (Parameter 01) to 000 1011 and the first stage gain to 4.166 produces:
  1000 0000 0001 01 01 10 0000 1011 0111 1111 1110.

  A first stage gain of 4.166 with a second stage gain of 50 gives a total gain of 208.3. This gain has a maximum tolerance of 2.5%.
- Set the output offset code (Parameter 10) to 0100 0000 and the output offset to 1.260 V when VDD = 5 V and VSS = 0 V. This output offset has a maximum tolerance of 0.8%:
  1000 0000 0001 01 10 10 0100 0000 0111 1111 1110.

Programming Mode

Intact fuses give a bit value of 0. Bits with a desired value of 1 need to have the associated fuse blown. Because a relatively large current is needed to blow a fuse, only one fuse can be reliably blown at a time. Therefore, a given parameter value may need several 38-bit words to allow reliable programming. A 5.25 V (±0.25 V) supply is required when blowing fuses to minimize the on resistance of the internal MOS switches that blow the fuse. The power supply voltage must not exceed the absolute maximum rating and must be able to deliver 250 mA of current.

At least 10 μF (tantalum type) of decoupling capacitance is needed across the power pins of the device during programming. The capacitance can be on the programming apparatus as long as it is within 2 inches of the device being programmed. An additional 0.1 μF (ceramic type) in parallel with the 10 μF is recommended within ½ inch of the device being programmed. A minimum period of 1 ms should be allowed for each fuse to blow. There is no need to measure the supply current during programming.

The best way to verify correct programming is to use the read mode to read back the programmed values. Then, remeasure the gain and offset to verify these values. Programmed fuses have no effect on the gain and output offset until the master fuse is blown. After blowing the master fuse, the gain and output offset are determined solely by the blown fuses, and the simulation mode is permanently deactivated.

Parameters are programmed by setting Field 1 to 10, selecting the desired parameter in Field 2, and selecting a single bit with the value 1 in Field 4.

As an example, suppose the user wants to permanently set the second stage gain to 50. Parameter 00 needs to have the value 0000 0011 assigned. Two bits have the value 1; therefore, two fuses need to be blown. Because only one fuse can be blown at a time, this code can be used to blow one fuse:
1000 0000 0001 10 00 10 0000 0010 0111 1111 1110.

The MOS switch that blows the fuse closes when the complete packet is recognized and opens when the start-of-packet, dummy, or end-of-packet fields are no longer valid. After 1 ms, this second code is entered to blow the second fuse:
1000 0000 0001 10 00 10 0000 0001 0111 1111 1110.

To permanently set the first stage gain to a nominal value of 4.151, Parameter 01 needs to have the value 000 1011 assigned. Three fuses need to be blown, and the following codes are used, with a 1 ms delay after each code:
1000 0000 0001 10 01 10 0000 1000 0111 1111 1110
1000 0000 0001 10 01 10 0000 0010 0111 1111 1110
1000 0000 0001 10 01 10 0000 0001 0111 1111 1110.

To permanently set the output offset to a nominal value of 1.260 V when VDD = 5 V and VSS = 0 V, Parameter 10 needs to have the value 0100 0000 assigned. If one fuse needs to be blown, use the following code:
1000 0000 0001 10 10 10 0100 0000 0111 1111 1110.

Finally, to blow the master fuse to deactivate the simulation mode and prevent further programming, use code:
1000 0000 0001 10 11 10 0000 0001 0111 1111 1110.

There are 20 programmable fuses. Because each fuse requires 1 ms to blow, and each serial word can be loaded in 2.3 ms, the maximum time needed to program the fuses can be as low as 66 ms.

Parity Error Detection

A parity check is used to determine whether the programmed data of an AD8556 is valid, or whether data corruption has occurred in the nonvolatile memory. Figure 50 shows the schematic implemented in the AD8556.

VA0 to VA2 is the 3-bit control signal for the second stage gain, VB0 to VB6 is the 7-bit control signal for the first stage gain, and VC0 to VC7 is the 8-bit control signal for the output offset. PFUSE is the signal from the parity fuse, and MFUSE is the signal from the master fuse.

The function of the 2-input AND gate (Cell AND2) is to ignore the output of the parity circuit (PAR_SUM signal) when the master fuse is not blown. PARITY_ERROR is set to 0 when MFUSE = 0. In the simulation mode, for example, parity check is disabled. After the master fuse is blown, that is, after the AD8556 is programmed, the output from the parity circuit (PAR_SUM signal) is fed to PARITY_ERROR. When PARITY_ERROR is 0, the AD8556 behaves as a programmed amplifier. When PARITY_ERROR is 1, a parity error is detected, and VOUT is connected to VSS.

The 18-bit data signal (VA0 to VA2, VB0 to VB6, and VC0 to VC7) is fed to an 18-input exclusive-OR gate (Cell EOR18). The output of Cell EOR18 is the DAT_SUM signal. If there is an even number of 1s in the 18-bit word, DAT_SUM = 0; and if there is an odd number of 1s in the 18-bit word, DAT_SUM = 1. See Table 13 for examples.

After the second stage gain, first stage gain, and output offset are programmed, compute DAT_SUM and set the parity bit equal to DAT_SUM. If DAT_SUM is 0, the parity fuse should not be blown in order for the PFUSE signal to be 0. If DAT_SUM is 1, the parity fuse should be blown to set the PFUSE signal to 1. The code to blow the parity fuse is:
1000 0000 0001 10 11 10 0000 0100 01111111 1110.

After setting the parity bit, the master fuse can be blown to prevent further programming, using the code:
1000 0000 0001 10 11 10 0000 0001 0111 1111 1110.

Signal PAR_SUM is the output of the 2-input exclusive-OR gate (Cell EOR2). After the master fuse is blown, set PARITY_ERROR to PAR_SUM. As previously mentioned, the AD8556 behaves as a programmed amplifier when PARITY_ERROR = 0 (no parity error). On the other hand, VOUT is connected to VSS when a parity error is detected, that is, when PARITY_ERROR = 1.

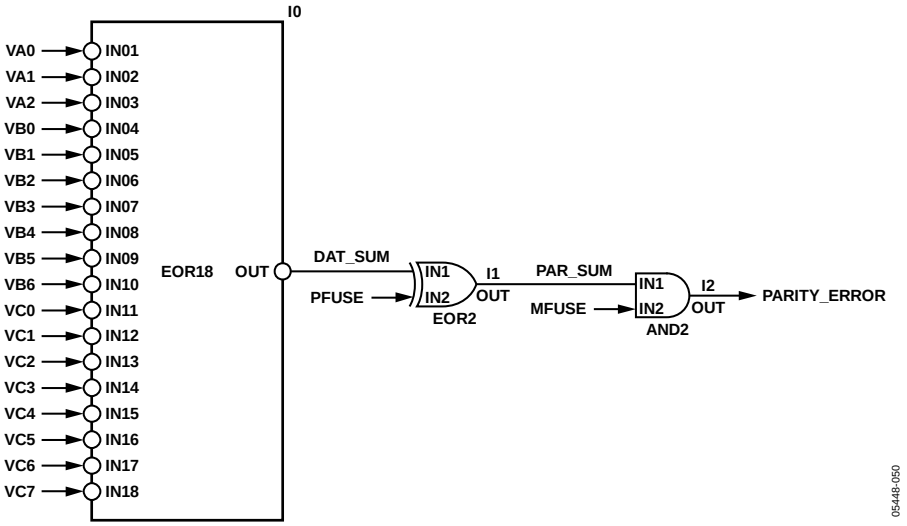

Figure 50. Functional Circuit of AD8556 Parity Check

Table 13. Examples of DAT_SUM

Second Stage Gain Code	First Stage Gain Code	Output Offset Code	Number of Bits with 1	DAT_SUM
000	000 0000	0000 0000	0	0
000	000 0000	1000 0000	1	1
000	000 0000	1000 0001	2	0
000	000 0001	0000 0000	1	1
000	100 0001	0000 0000	2	0
001	000 0000	0000 0000	1	1
001	000 0001	1000 0000	3	1
111	111 1111	1111 1111	18	0

Read Mode

The values stored by the polysilicon fuses can be sent to the FILT/DIGOUT pin to verify correct programming. Normally, the FILT/DIGOUT pin is only connected to the second gain stage output via RF. During read mode, however, the FILT/DIGOUT pin is also connected to the output of a shift register to allow the polysilicon fuse contents to be read. Because VOUT is a buffered version of FILT/DIGOUT, VOUT also outputs a digital signal during read mode.

Read mode is entered by setting Field 1 to 11 and selecting the desired parameter in Field 2. Field 4 is ignored. The parameter value, stored in the polysilicon fuses, is loaded into an internal shift register, and the MSB of the shift register is connected to the FILT/DIGOUT pin. Pulses at DIGIN shift out the shift register contents to the FILT/DIGOUT pin, allowing the 8-bit parameter value to be read after seven additional pulses; shifting occurs on the falling edge of DIGIN. An eighth pulse at DIGIN disconnects FILT/DIGOUT from the shift register and terminates the read mode. If a parameter value is less than eight bits long, the MSBs of the shift register are padded with 0s.

For example, to read the second stage gain, this code is used: 1000 0000 0001 11 00 10 0000 0000 0111 1111 1110. Because the second stage gain parameter value is only three bits long, the FILT/DIGOUT pin has a value of 0 when this code is entered, and remains 0 during four additional pulses at DIGIN. The fifth, sixth, and seventh pulses at DIGIN return the 3-bit value at FILT/DIGOUT, the seventh pulse returns the LSB. An eighth pulse at DIGIN terminates the read mode.

Sense Current

A sense current is sent across each polysilicon fuse to determine whether it has been blown. When the voltage across the fuse is less than approximately 1.5 V, the fuse is considered not blown, and Logic 0 is output from the OTP cell. When the voltage across the fuse is greater than approximately 1.5 V, the fuse is considered blown, and Logic 1 is output.

When the AD8556 is manufactured, all fuses have a low resistance. When a sense current is sent through the fuse, a voltage less than 0.1 V is developed across the fuse, which is much lower than 1.5 V; therefore, Logic 0 is output from the OTP cell. When a fuse is electrically blown, it should have a very high resistance. When the sense current is applied to the blown fuse, the voltage across the fuse should be larger than 1.5 V; therefore, Logic 1 is output from the OTP cell.

It is theoretically possible, though very unlikely, for a fuse to be incompletely blown during programming, assuming the required conditions are met. In this situation, the fuse could have a medium resistance, neither low nor high, and a voltage of approximately 1.5 V could be developed across the fuse. Therefore, the OTP cell could output Logic 0 or Logic 1, depending on temperature, supply voltage, and other variables.

To detect this undesirable situation, the sense current can be lowered by a factor of 4 using a specific code. The voltage developed across the fuse would then change from 1.5 V to 0.38 V, and the output of the OTP would be Logic 0 instead of the expected Logic 1 from a blown fuse. Fuses blown correctly would still output Logic 1. In this way, fuses blown incorrectly can be detected. Another specific code would return the sense current to the normal (larger) value. The sense current cannot be permanently programmed to the low value. When the AD8556 is powered up, the sense current defaults to the high value.

The low sense current code is:
1000 0000 0001 00 00 10 XXXX XXX1 0111 1111 1110.

The normal (high) sense current code is:
1000 0000 0001 00 00 10 XXXX XXX0 0111 1111 1110.

Programming Procedure

For reliable fuse programming, it is imperative to follow the programming procedure requirements, especially the proper supply voltage during programming.

1. When programming the AD8556, the temperature of the device must be between 10°C and 40°C.
2. Set VDD and VSS to the desired values in the application. Use simulation mode to test and determine the desired codes for the second stage gain, first stage gain, and output offset. The nominal values for these parameters are shown in Table 6, Table 7, Equation 2, and Equation 3; use the codes corresponding to these values as a starting point. However, because actual parameter values for given codes vary from device to device, some fine tuning is necessary for the best possible accuracy.

   One way to choose these values is to set the output offset to an approximate value, such as Code 128 for midsupply, to allow the required gain to be determined. Then set the second stage gain so the minimum first stage gain (Code 0) gives a lower gain than required, and the maximum first stage gain (Code 127) gives a higher gain than required. After choosing the second stage gain, the first stage gain can be chosen to fine tune the total gain. Finally, the output offset can be adjusted to give the desired value. After determining the desired codes for second stage gain, first stage gain, and output offset, the device is ready for permanent programming.

Important: Once a programming attempt is made for any fuse, there should be no further attempt to blow that fuse. If a fuse does not program to the expected state, discard the unit. The expected incidence rate of attempted but unblown fuses is very small when following the proper programming procedure and conditions.

3. Set VSS to 0 V and VDD to 5.25 V (±0.25 V). Power supplies should be capable of supplying 250 mA at the required voltage and properly bypassed as described in the Programming Mode section. Use program mode to permanently enter the desired codes for the first stage gain, second stage gain, and output offset. Blow the parity bit fuse if necessary (see Parity Error Detection section). Blow the master fuse to allow the AD8556 to read data from the fuses and to prevent further programming.
4. Set VDD and VSS to the desired values in the application. Use read mode with low sense current followed by high sense current to verify programmed codes.
5. Measure gain and offset to verify correct functionality.

Determining Optimal Gain and Offset Codes

First, determine the desired gain:

1. Determine the desired gain, G_A (using the measurements obtained from the simulation).
2. Use Table 7 to determine G_2, the second stage gain, such that $(4.00 \times 1.04) < (G_A/G_2) < (6.4/1.04)$. This ensures the first and last codes for the first stage gain are not used, thereby allowing enough first stage gain codes within each second stage gain range to adjust for the 3% accuracy.

Next, set the second stage gain:

1. Use the simulation mode to set the second stage gain to G_2.
2. Set the output offset to allow the AD8556 gain to be measured, for example, use Code 128 to set it to midsupply.
3. Use Table 6 or Equation 1 to set the first stage gain code C_{G1}, so the first stage gain is nominally G_A/G_2.
4. Measure the resulting gain, G_B. G_B should be within 3% of G_A.
5. Calculate the first stage gain error (in relative terms) $E_{G1} = G_B/G_A - 1$.
6. Calculate the error (in the number of the first stage gain codes) $C_{EG1} = E_{G1}/0.00370$.
7. Set the first stage gain code to $C_{G1} - C_{EG1}$.
8. Measure the gain, G_C. G_C should be closer to G_A than to G_B.
9. Calculate the error (in relative terms) $E_{G2} = G_C/G_A - 1$.
10. Calculate the error (in the number of the first stage gain codes) $C_{EG2} = E_{G2}/0.00370$.
11. Set the first stage gain code to $C_{G1} - C_{EG1} - C_{EG2}$. The resulting gain should be within one code of G_A.

Finally, determine the desired output offset:

1. Determine the desired output offset O_A (using the measurements obtained from the simulation).
2. Use Equation 2 to set the output offset code C_{O1} such that the output offset is nominally O_A.
3. Measure the output offset, O_B. O_B should be within 3% of O_A.
4. Calculate the error (in relative terms) $E_{O1} = O_B/O_A - 1$.
5. Calculate the error (in the number of the output offset codes) $C_{EO1} = E_{O1}/0.00392$.
6. Set the output offset code to $C_{O1} - C_{EO1}$.
7. Measure the output offset, O_C. O_C should be closer to O_A than to O_B.
8. Calculate the error (in relative terms) $E_{O2} = O_C/O_A - 1$.
9. Calculate the error (in the number of the output offset codes) $C_{EO2} = E_{O2}/0.00392$.
10. Set the output offset code to $C_{O1} - C_{EO1} - C_{EO2}$. The resulting offset should be within one code of O_A.

EMI/RFI PERFORMANCE

Real-world applications must work with ever increasing radio/magnetic frequency interference (RFI and EMI). In situations where signal strength is low and transmission lines are long, instrumentation amplifiers, such as the AD8556, are needed to extract weak, small differential signals riding on common-mode noise and interference. Additionally, wires and PCB traces act as antennas and pick up high frequency EMI signals. The longer the wire, the larger the voltage it picks up. The amount of voltages picked up is dependent on the impedances at the wires, as well as the EMI frequency. These high frequency voltages are then passed into the in-amp through its pins. All instrumentation amplifiers can rectify high frequency out-of-band signals. Unfortunately, the EMI/RFI rectification occurs because amplifiers do not have any significant common-mode rejection above 100 kHz. Once these high frequency signals are rectified, they appear as dc offset errors at the output.

The AD8556 features internal EMI filters on the VNEG, VPOS, FILT, and VCLAMP pins. These built-in filters on the pins limit the interference bandwidth and provide good RFI suppression without reducing performance within the pass-band of the instrumentation amplifier. A functional diagram of the AD8556 along with its EMI/RFI filters is shown in Figure 51.

The AD8556 has built-in filters on its inputs, VCLAMP, and filter pins. The first-order, low-pass filters inside the AD8556 are useful to reject high frequency EMI signals picked up by wires and PCB traces outside the AD8556. The most sensitive pin of any amplifier to RFI/EMI signal is the noninverting pin. Signals present at this pin appear as common-mode signals and create problems.

The filters built at the input of the AD8556 have two different bandwidths: common mode and differential mode. The common-mode bandwidth defines what a common-mode RF signal sees between the two inputs tied together and ground. The EMI filters placed on the input pins of the AD8556 reject EMI/RFI suppressions that appear as common-mode signals.

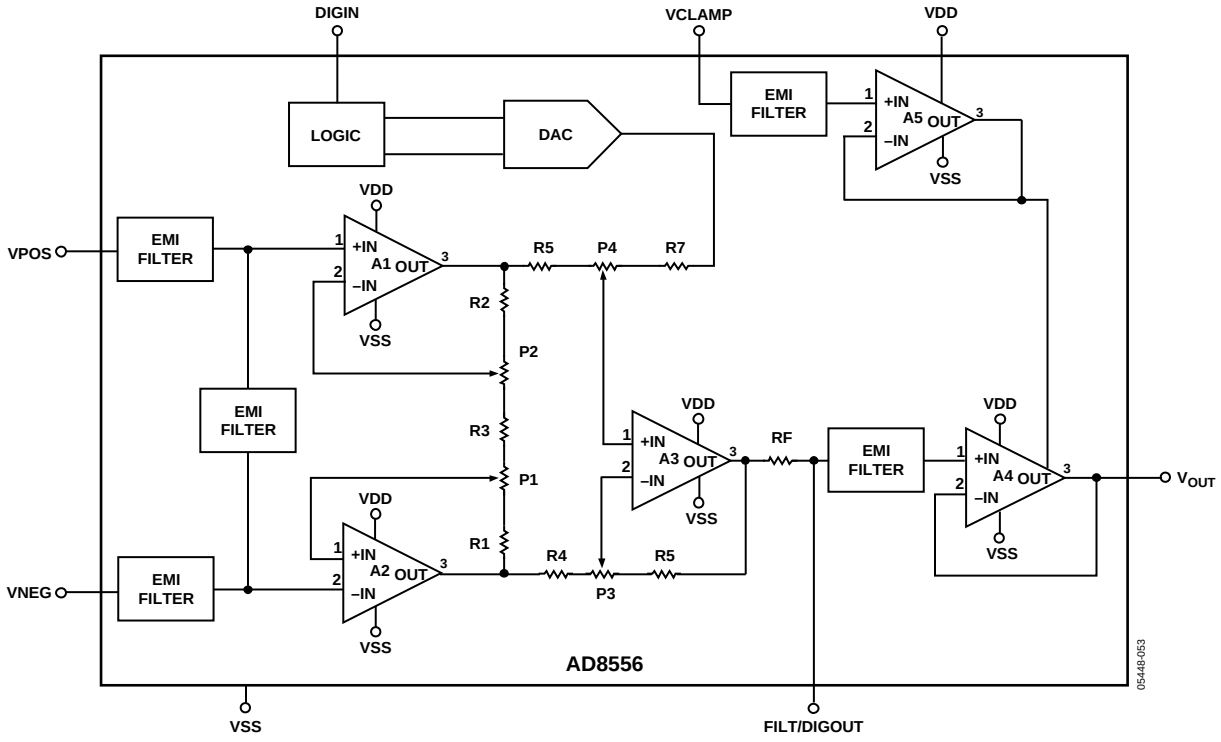

Figure 51. Block Diagram Showing EMI/RFI Built-In Filters

To show the benefits that the AD8556 brings to new applications where EMI/RFI signals are present, a part was programmed with a gain of 70 and a dc offset of 2.5 V to produce a VOUT of 0 V. A test circuit like that shown in Figure 52 was used.

Figure 52 simulates the presence of a noisy common-mode signal, and Figure 53 shows the response dc values at VOUT.

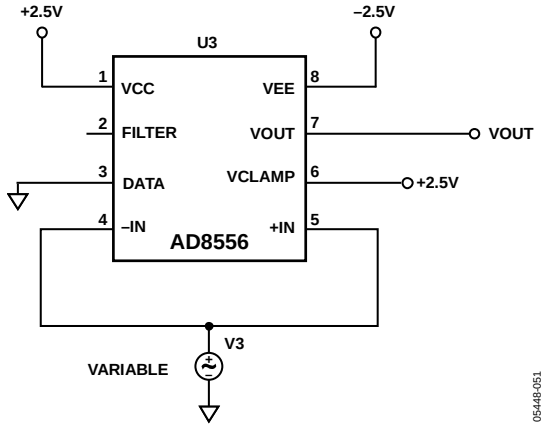

Figure 52. Test Circuit to Show AD8556 Performance Exposed to Common-Mode RFI/EMI Signals

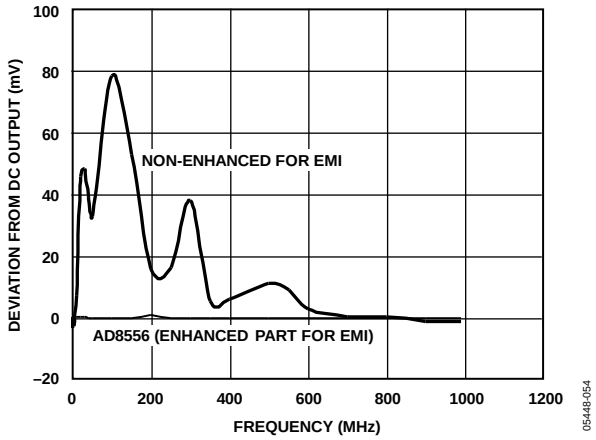

Figure 53. DC Offset Values at VOUT Caused by Frequency Seep of Input

The differential bandwidth defines the frequency response of the filters with a differential signal applied between the two inputs, VPOS (that is, +IN) and VNEG (that is, –IN). Figure 54 shows the circuit used to test for AD8556 EMI/RFI susceptibility. The part is programmed as previously stated during the common-mode testing.

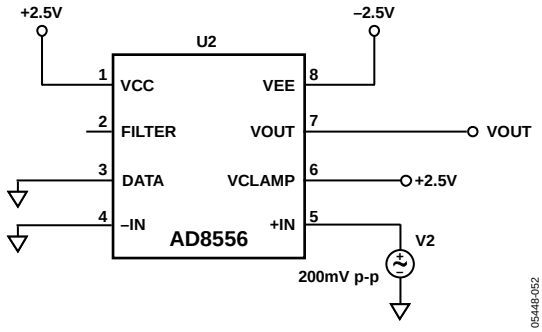

Figure 54. Test Circuit to Show AD8556 Performance Exposed to Differential Mode RFI/EMI Signals

The response of AD8556 to EMI/RFI differential signals is shown in Figure 55.

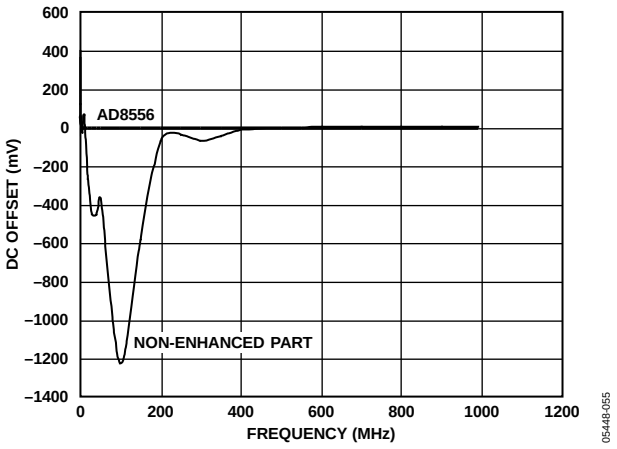

Figure 55. Response of AD8556 to EMI/RFI Differential Signals

To make a board robust against EMI, the leads at VPOS and VNEG should be as similar as possible. In this way, any EMI received by the VPOS and VNEG pins will be similar (that is, a common-mode input), and rejected by the AD8556. Furthermore, additional filtering at the VPOS and VNEG pins should give a better reduction of unwanted behavior compared with filtering at the other pins.

OUTLINE DIMENSIONS

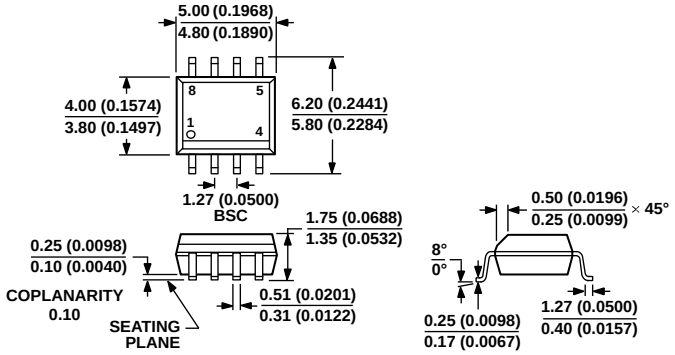

Figure 56. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

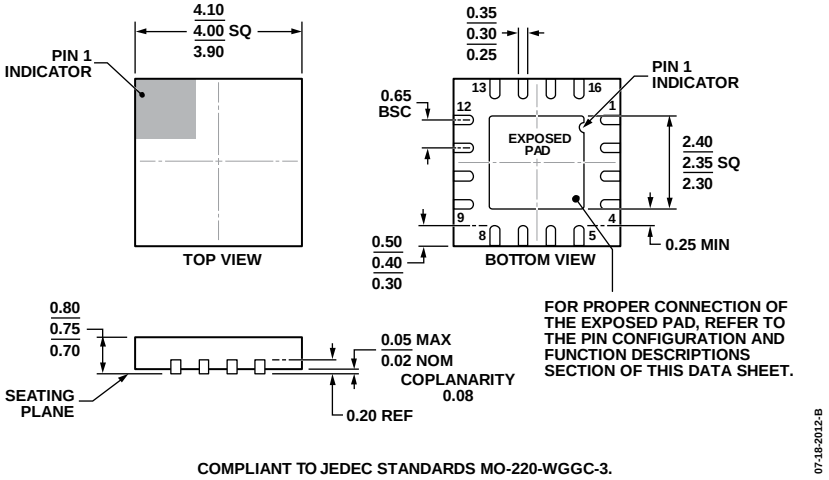

Figure 57. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8556ARZ	−40°C to +140°C	8-Lead SOIC_N	R-8
AD8556ARZ-REEL	−40°C to +140°C	8-Lead SOIC_N	R-8
AD8556ARZ-REEL7	−40°C to +140°C	8-Lead SOIC_N	R-8
AD8556ACPZ-R2	−40°C to +140°C	16-Lead LFCSP_WQ	CP-16-20
AD8556ACPZ-REEL7	−40°C to +140°C	16-Lead LFCSP_WQ	CP-16-20

[1] Z = RoHS Compliant Part.