DC to 50 MHz, Dual I/Q Demodulator and Phase Shifter

AD8333

FEATURES

Dual integrated I/Q demodulator
16 phase select on each output (22.5° per step)
Quadrature demodulation accuracy
- **Phase accuracy: ±0.1°**
- **Amplitude balance: ±0.05 dB**

Bandwidth
- **4 LO: 100 kHz to 200 MHz**
- **RF: dc to 50 MHz**
- **Baseband: determined by external filtering**

Output dynamic range: 161 dB/Hz
LO drive > 0 dBm (50 Ω); 4 LO > 1 MHz
Supply: ±5 V
Power consumption: 190 mW/channel (380 mW total)
Power down

APPLICATIONS

Medical imaging (CW ultrasound beamforming)
Phased array systems (radar and adaptive antennas)
Communication receivers

FUNCTIONAL BLOCK DIAGRAM

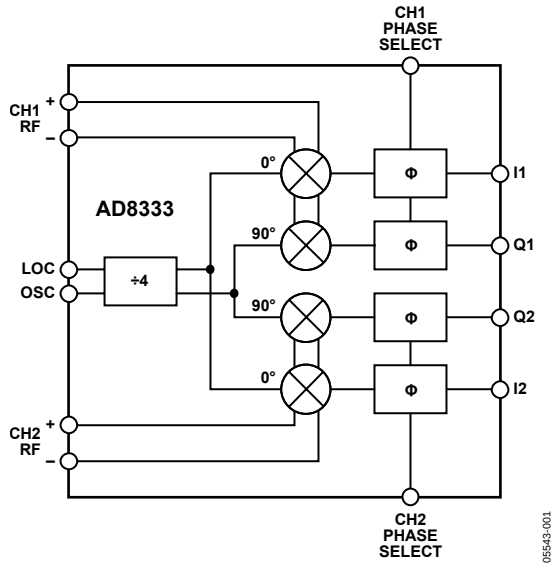

Figure 1.

GENERAL DESCRIPTION

The AD8333 is a dual-phase shifter and I/Q demodulator that enables coherent summing and phase alignment of multiple analog data channels. It is the first solid-state device suitable for beamformer circuits, such as those used in high performance medical ultrasound equipment featuring CW Doppler. The RF inputs interface directly with the outputs of the dual-channel, low noise preamplifiers included in the AD8332.

A divide-by-four circuit generates the internal 0° and 90° phases of the LO that drive the mixers of a pair of matched I/Q demodulators.

The AD8333 can be applied as a major element in analog beamformer circuits in medical ultrasound equipment.

The AD8333 features an asynchronous reset pin. When used in arrays, the reset pin sets all the LO dividers in the same state. Sixteen discrete phase rotations in 22.5° increments can be selected independently for each channel. For example, if CH1 is used as a reference and the RF signal applied to CH2 has an I/Q phase lead of 45°, then the user can phase align CH2 with CH1 by choosing the correct code.

Phase shift is defined by the output of one channel relative to another. For example, if the code of Channel 1 is adjusted to 0000 and that of Channel 2 to 0001 and the same signal is applied to both RF inputs, the output of Channel 2 leads that of Channel 1 by 22.5°.

The I and Q outputs are provided as currents to facilitate summation. The summed current outputs are converted to voltages by a high dynamic-range, current-to-voltage (I-V) converter, such as the AD8021, configured as a transimpedance amplifier. The resultant signal is then applied to a high resolution ADC, such as the AD7665 (16 bit/570 kSPS).

The two I/Q demodulators can be used independently in other nonbeamforming applications. In that case, a transimpedance amplifier is needed for each of the I and Q outputs, four in total for the dual I/Q demodulator.

The dynamic range is 161 dB/Hz at each I and Q output, but the following transimpedance amplifier is an important element in maintaining the overall dynamic range, and attention needs to be paid to optimal component selection and design.

The AD8333 is available in a 32-lead LFCSP (5 mm × 5 mm) package for the industrial temperature range of −40°C to +85°C.

Rev. A

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REVISION HISTORY

5/06—Rev. 0 to Rev. A
Changes to Figure 62 ... 26

10/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, T_A = 25°C, 4 f_{LO} = 20 MHz, f_{RF} = 5.01 MHz, f_{BB} = 10 kHz, P_{LO} ≥ 0 dBm, single-ended, sine wave; per channel performance, dBm (50 Ω), unless otherwise noted (see Figure 41).

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO Frequency Range	4× internal LO at Pin 4LOP and Pin 4LON				
	Square wave	0.01		200	MHz
	Sine wave, see Figure 22	2		200	MHz
RF Frequency Range	Mixing	DC		50	MHz
Baseband Bandwidth	Limited by external filtering	DC		50	MHz
LO Input Level	See Figure 22		0	13	dBm
V_{SUPPLY} (V_S)		±4.5	±5	±6	V
Temperature Range		−40		+85	°C
DEMODULATOR PERFORMANCE					
RF Differential Input Impedance			6.7||6.5		kΩ||pF
LO Differential Input Capacitance			0.6		pF
Transconductance	Demodulated I_{OUT}/V_{IN}, each Ix or Qx output after low-pass filtering measured from RF inputs				
	All phases		2.17		mS
Dynamic Range	IP1dB, input referred noise (dBm)		161		dB/Hz
Maximum RF Input Swing	Differential; inputs biased at 2.5 V; Pin RFxP and Pin RFxN		2.8		V p-p
Peak Output Current (No Filtering)	0° phase shift		±4.7		mA
	45° phase shift		±6.6		mA
Input P1dB	Ref = 50 Ω		14.5		dBm
	Ref = 1 V_{RMS}		1.5		dBV
Third-Order Intermodulation (IM3)	f_{RF1} = 5.010 MHz, f_{RF2} = 5.015 MHz, f_{LO} = 5.023 MHz				
Equal Input Levels	Baseband tones: −7 dBm @ 8 kHz and 13 kHz		−75		dBc
Unequal Input Levels	Baseband tones: −1 dBm @ 8 kHz and −31 dBm @ 13 kHz		−77		dBc
Third-Order Input Intercept (IP3)	Same conditions as IM3		30		dBm
LO Leakage	Measured at RF inputs, worst phase, measured into50 Ω (limited by measurement)		<−97		dBm
	Measured at baseband outputs, worst phase, 8021 disabled, measured into 50 Ω		−60		dBm
Conversion Gain	All codes, see Figure 41		4.7		dB
Input Referred Noise	Output noise/conversion gain, see Figure 41		10		nV/√Hz
Output Current Noise	Output noise ÷ 787 Ω		22		pA/√Hz
Noise Figure	With AD8332 LNA				
	R_S = 50 Ω, R_{FB} = ∞		7.8		dB
	R_S = 50 Ω, R_{FB} = 1.1 kΩ		9.0		dB
	R_S = 50 Ω, R_{FB} = 274 Ω		11.0		dB
Bias Current	Pin 4LOP and Pin 4LON		−3		µA
	Pin RFxP and Pin RFxN		−70		µA
LO Common-Mode Voltage Range	Pin 4LOP and Pin 4LON (each pin)	0.2		3.8	V
RF Common-Mode Voltage	For maximum differential swing; Pin RFxP and Pin RFxN (dc-coupled to AD8332 LNA output)		2.5		V
Output Compliance Range	Pin IxPO and Pin QxPO	−1.5		+0.7	V

Parameter	Conditions	Min	Typ	Max	Unit
PHASE ROTATION PERFORMANCE					
	One CH is reference, other is stepped				
Phase Increment	16 phase steps per channel		22.5		Degrees
Quadrature Phase Error	I1 to Q1 and I2 to Q2, 1σ	−2	±0.1	+2	Degrees
I/Q Amplitude Imbalance	I1 to Q1 and I2 to Q2, 1σ		±0.05		dB
Channel-to-Channel Matching	Phase match I1/I2 and Q1/Q2; −40°C < T_A < 85°C		±1		Degrees
	Amplitude match I1/I2 and Q1/Q2; −40°C < T_A < 85°C		±0.25		dB
LOGIC INTERFACES					
Logic Level High	Pin PHxx, Pin RSET, and Pin ENBL	1.7		5	V
Logic Level Low	Pin PHxx, Pin RSET, and Pin ENBL	0		1.3	V
Bias Current					
Pin PHxx and Pin ENBL	Logic high	10	40	90	µA
	Logic low	−30	−7	+10	µA
Pin RSET	Logic high	50	120	180	µA
	Logic low	−70	−20	0	µA
Input Resistance	Pin PHxx and Pin ENBL		60		kΩ
	Pin RSET		20		kΩ
Reset Hold Time	Reset is asynchronous; clock disabled when RSET goes HI until 300 ns after RSET goes LO	300			ns
Minimum Reset Pulse Width		300			ns
Reset Response Time	See Figure 35		300		ns
Phase Response Time	See Figure 38		5		µs
Enable Response Time	See Figure 34		300		ns
POWER SUPPLY	Pin VPOS and Pin VNEG				
Supply Voltage		±4.5	±5	±6	V
Quiescent Current, All Phase Bits = 0	@25°C				
	Pin VPOS	38	44	51	mA
	Pin VNEG	−24	−20	−16	mA
Over Temperature	−40°C < T_A < 85°C				
	Pin VPOS, all phase bits = 0	40		54	mA
	Pin VNEG	−24		−19	mA
Quiescent Power	Per channel, all phase bits = 0		170		mW
	Per channel, any 0 or 1 combination of phase bits		190		mW
Disable Current					
	All channels disabled				
	Pin VPOS	1.0	1.25	1.5	mA
	Pin VNEG	−300	−200	−100	µA
PSRR					
	Pin VPOS to Ix/Qx outputs (measured @ AD8021 output)		−81		dB
	Pin VNEG to Ix/Qx outputs (measured @ AD8021 output)		−75		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltages	
Supply Voltage V_S	6 V
RF Pins Input	V_S, GND
LO Inputs	V_S, GND
Code Select Inputs V	V_S, GND
Thermal Data—4-Layer JEDEC Board No Air Flow (Exposed Pad Soldered to PC Board)	
θ_{JA}	41.0°C/W
θ_{JB}	23.6°C/W
θ_{JC}	4.4°C/W
Ψ_{JT}	0.4°C/W
Ψ_{JB}	22.4°C/W
Maximum Junction Temperature	150°C
Maximum Power Dissipation (Exposed Pad Soldered to PC Board)	1.5 W
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

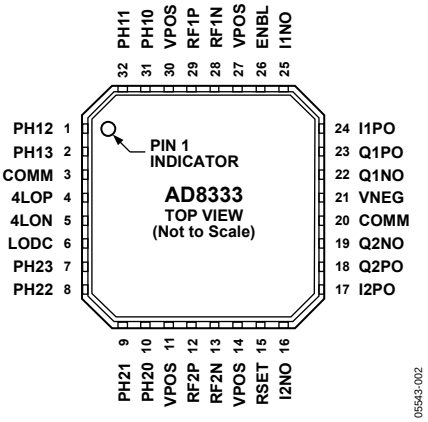

Figure 2. 32-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 7, 8	PH12, PH13 PH23, PH22	Quadrant Select LSB, MSB. Binary code. These logic inputs select the quadrant: 0° to 90°, 90° to180°, 180° to 270°, 270° to 360° (see Table 4). Logic threshold is at about 1.5 V and therefore can be driven by 3 V CMOS logic (see Figure 3).
3, 20	COMM	Ground. These two pins are internally tied together.
4, 5	4LOP, 4LON	LO Inputs. No internal bias; therefore, these pins need to be biased by external circuitry. For optimum performance, these inputs should be driven differentially with a signal level that is not less than what is shown in Figure 22. Bias current is only −3 μA. Single-ended drive is also possible if the inputs are biased correctly (see Figure 4).
6	LODC	Decoupling Pin for LO. A 0.1 μF capacitor should be connected between this pin and ground (see Figure 5).
9, 10, 31, 32	PH21, PH20 PH10, PH11	Phase Select LSB, MSB. Binary code. These logic inputs select the phase for a given quadrant: 0°, 22.5°, 45°, 67.5° (see Table 4). Logic threshold is at about 1.5 V and therefore can be driven by 3 V CMOS logic (see Figure 3).
11, 14, 27, 30	VPOS	Positive Supply. These pins should be decoupled with a ferrite bead in series with the supply, plus a 0.1 μF and 100 pF capacitor between the VPOS pins and ground. Because the VPOS pins are internally connected, one set of supply decoupling components for all four pins should be sufficient.
12, 13, 28, 29	RF2P, RF2N RF1N, RF1P	RF Inputs. These pins are biased internally; however, it is recommended that they be biased by dc coupling to the output pins of the AD8332 LNA. The optimum common-mode voltage for maximum symmetrical input differential swing is 2.5 V if ±5 V supplies are used (see Figure 6).
15	RSET	Reset for Divide-by-Four in LO Interface. Logic threshold is at about 1.5 V and therefore can be driven by 3 V CMOS logic (see Figure 3).
16, 19, 22, 25	I2NO, Q2NO Q1NO, I1NO	Negative I/Q Outputs. These outputs are not connected for normal usage but can be used for filtering if needed. Together with the positive I/Q outputs, they allow bypassing the internal current mirror if a lower noise output circuit is available; VNEG needs to be tied to GND to disable the current mirror (see Figure 7).
17, 18, 23, 24	I2PO, Q2PO Q1PO, I1PO	Positive I/Q Outputs. These outputs provide a bidirectional current that can be converted back to a voltage via a transimpedance amplifier. Multiple outputs can be summed together by simply connecting them together. The bias voltage should be set to 0 V or less by the transimpedance amplifier (see Figure 7).
21	VNEG	Negative Supply. This pin should be decoupled with a ferrite bead in series with the supply, plus a 0.1 μF and 100 pF capacitor between the pin and ground.
26	ENBL	Chip Enable. Logic threshold is at about 1.5 V and therefore it can be driven by 3 V CMOS logic (see Figure 3).

EQUIVALENT INPUT CIRCUITS

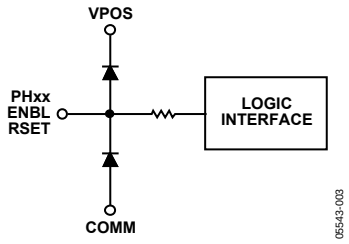

Figure 3. Logic Inputs

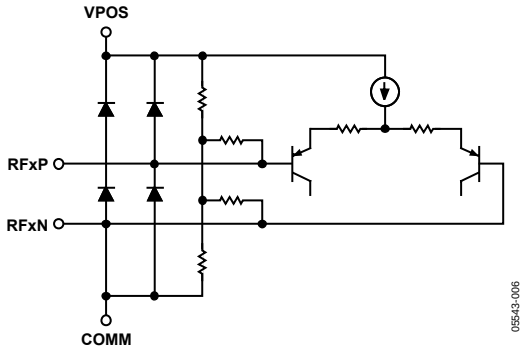

Figure 6. RF Inputs

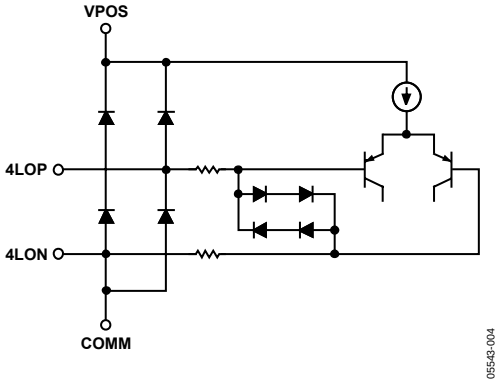

Figure 4. Local Oscillator Inputs

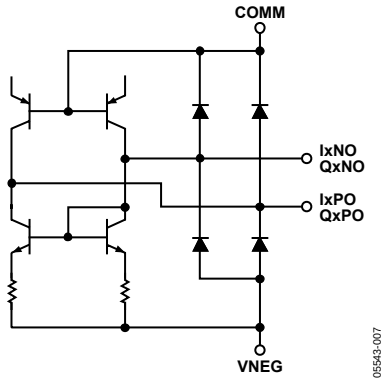

Figure 7. Output Drivers

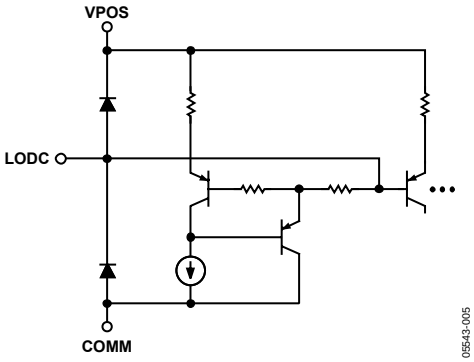

Figure 5. LO Decoupling Pin

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, T_A = 25°C, $4f_{LO}$ = 20 MHz, f_{LO} = 5 MHz, f_{RF} = 5.01 MHz, f_{BB} = 10 kHz, P_{LO} ≥ 0 dBm (50 Ω); single-ended sine wave; per channel performance, differential voltages, dBm (50 Ω), phase select code = 0000, unless otherwise noted (see Figure 41).

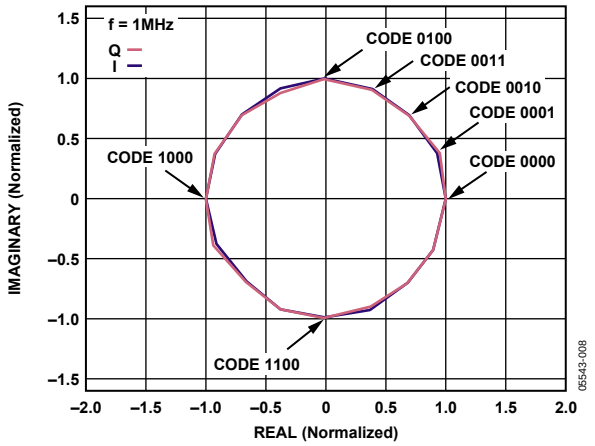

Figure 8. Normalized Vector Plot of Phase, CH2 with Respect to CH1; CH1 Is Fixed at 0°, CH2 Stepped 22.5°/Step, All Codes Displayed

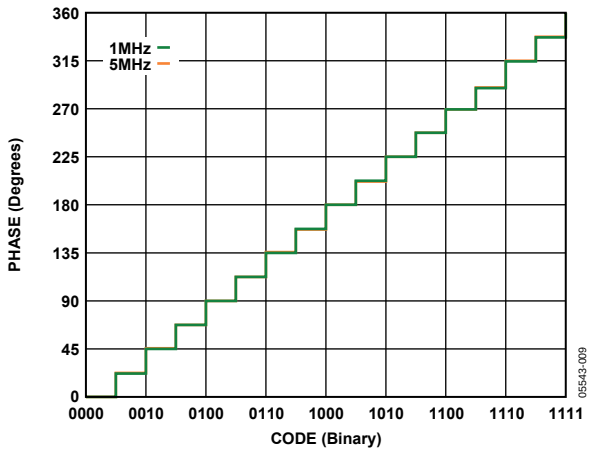

Figure 9. Phase of CH2 with Respect to CH1 vs. Code, at 1 MHz and 5 MHz

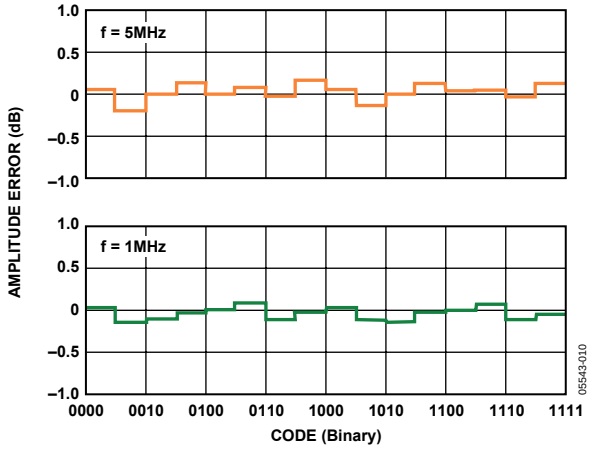

Figure 10. Amplitude Error of CH2 with Respect to CH1 vs. Code at 1 MHz and 5 MHz

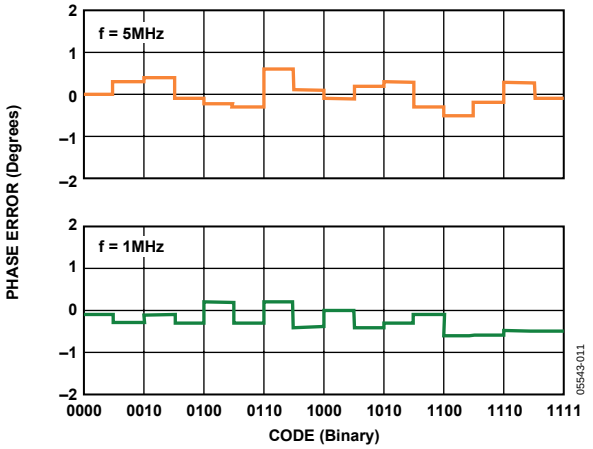

Figure 11. Phase Error of CH2 with Respect to CH1 vs. Code at 1 MHz and 5 MHz

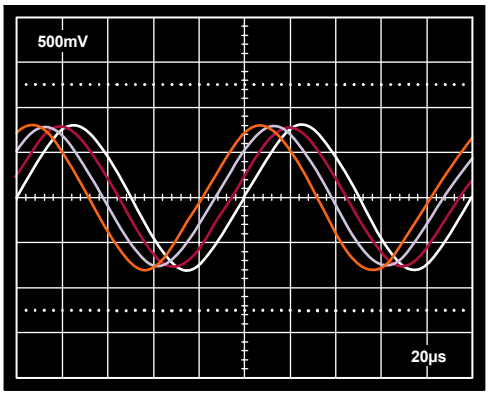

Figure 12. I or Q Output of CH2 with Respect to CH1, First Quadrant Shown

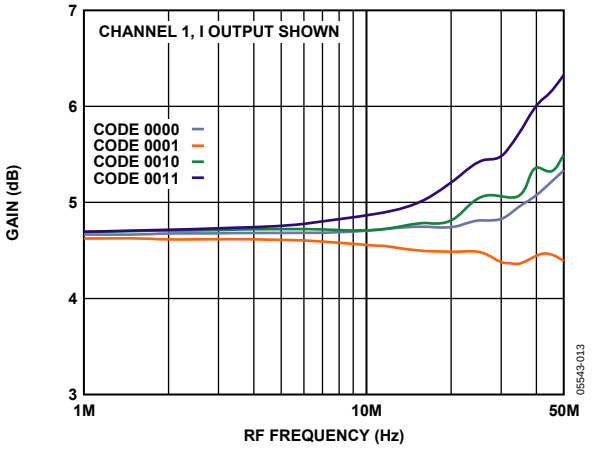

Figure 13. Conversion Gain vs. RF Frequency, First Quadrant, Baseband Frequency = 10 kHz

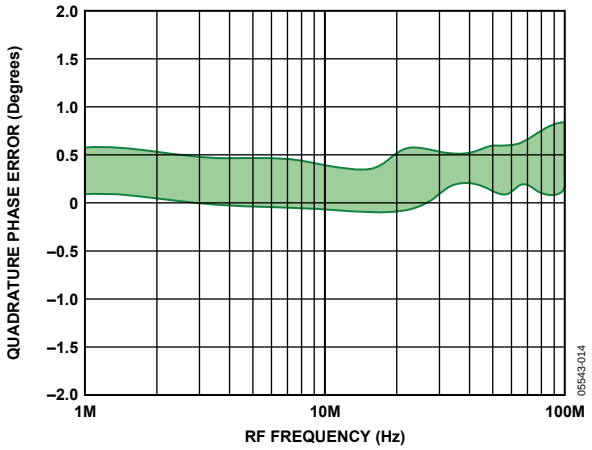

Figure 14. Representative Range of Quadrature Phase Errors vs. RF Frequency, CH1 or CH2, All Codes

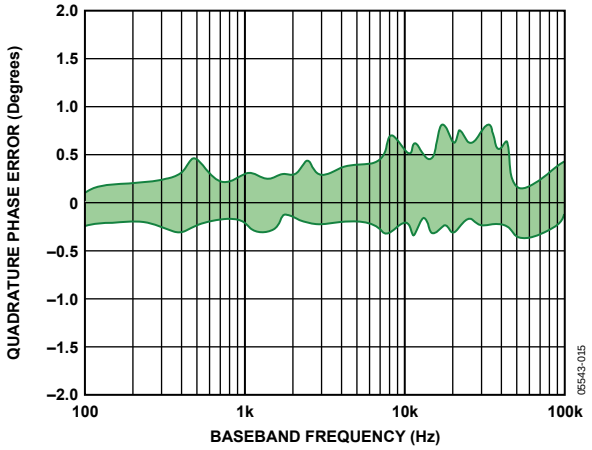

Figure 15. Range of Quadrature Phase Error vs. Baseband Frequency, CH1 and CH2 (see Figure 43)

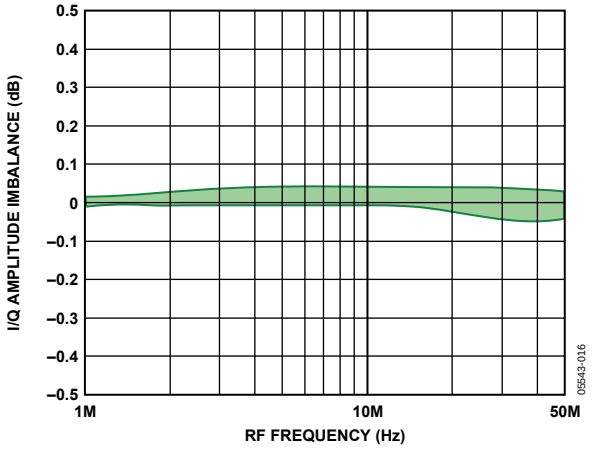

Figure 16. Representative Range of Amplitude Imbalance of I/Q vs. RF Frequency, CH1 or CH2, All Codes

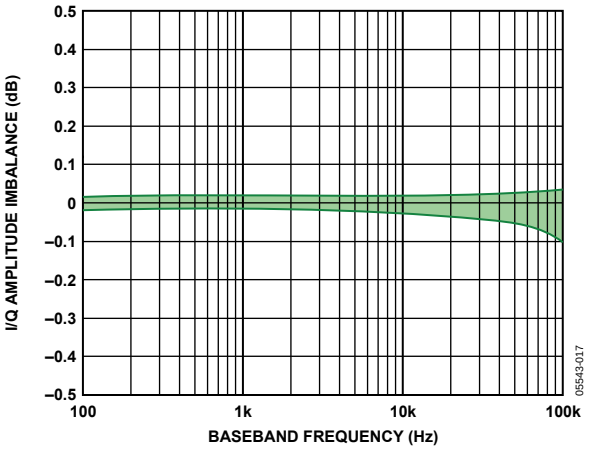

Figure 17. Representative Range of I/Q Amplitude Imbalance vs. Baseband Frequency, CH1 and CH2 (see Figure 43)

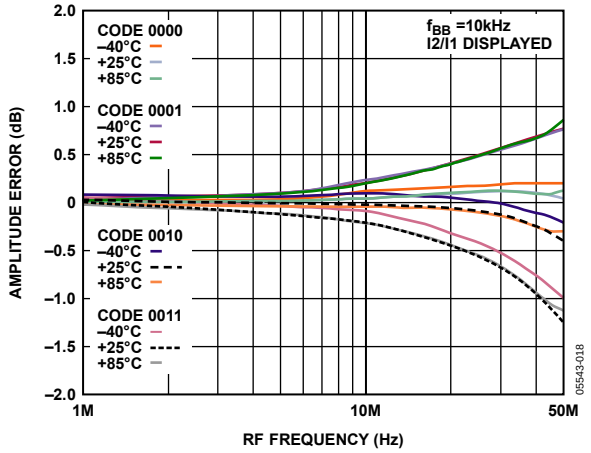

Figure 18. Typical I2/I1 or Q2/Q1 Amplitude Match vs. RF Frequency First Quadrant, at Three Temperatures

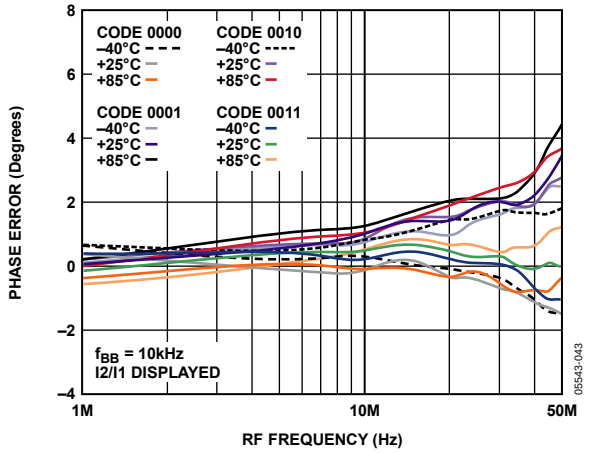

Figure 19. I2/I1 or Q2/Q1 Phase Error vs. RF Frequency, Baseband Frequency = 10 kHz, at Three Temperatures

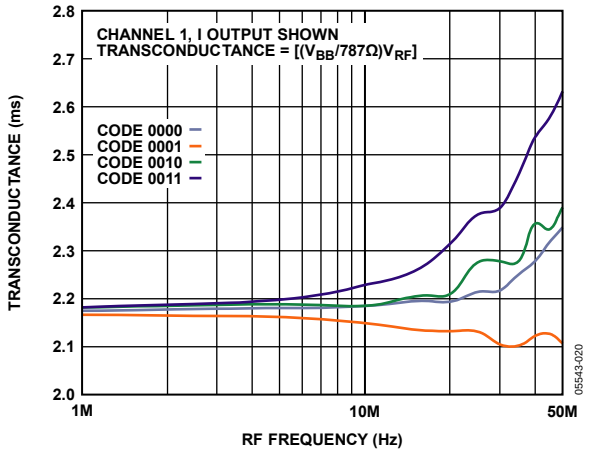

Figure 20. Transconductance vs. RF Frequency, First Quadrant

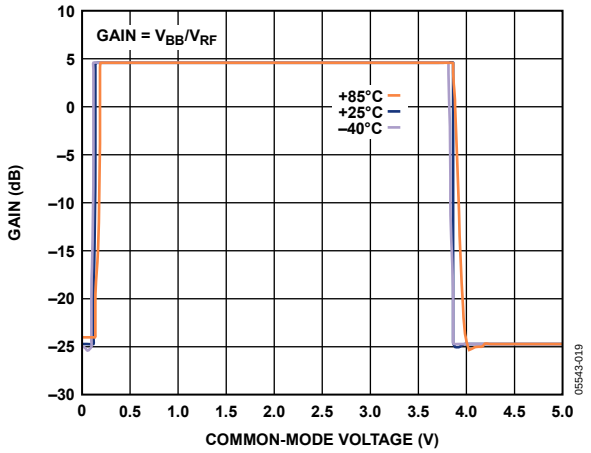

Figure 23. LO Common-Mode Range at Three Temperatures

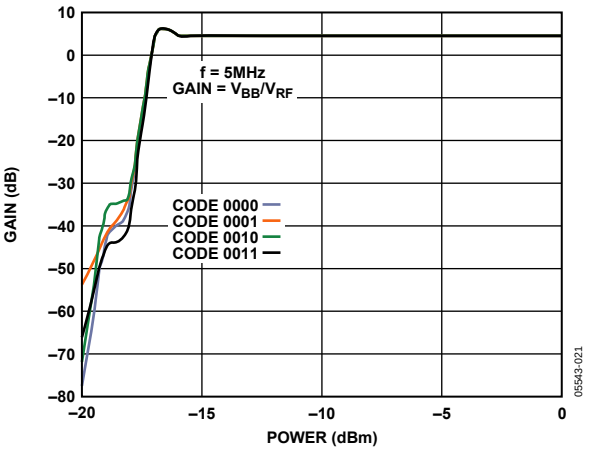

Figure 21. Conversion Gain vs. LO Level, First Quadrant

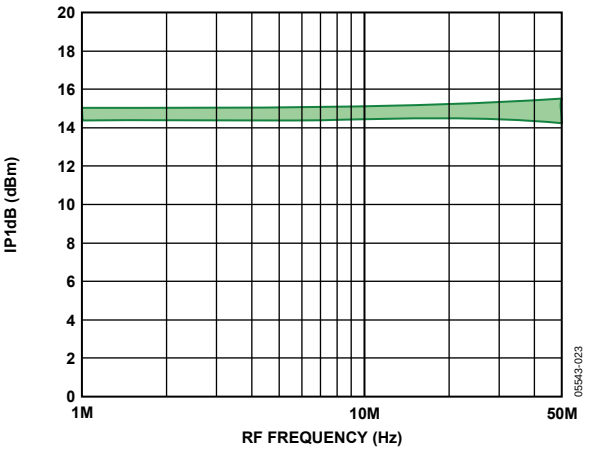

Figure 24. IP1dB vs. Frequency, Baseband Frequency = 10 kHz, First Quadrant (see Figure 42)

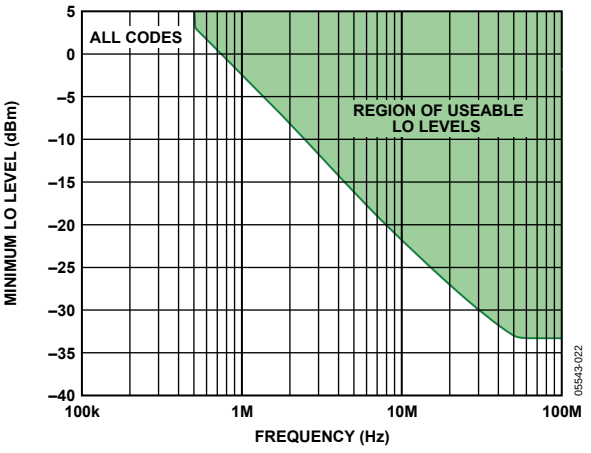

Figure 22. Minimum LO Level vs. RF Frequency, Single-Ended, Sine Wave LO Drive to Pin 4LOP or Pin 4LON

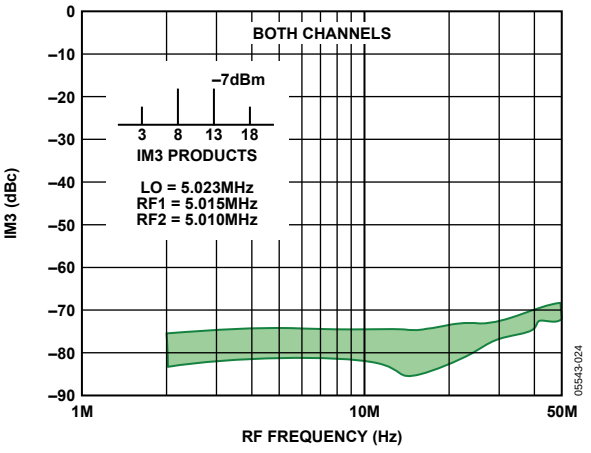

Figure 25. Representative Range of IM3 vs. RF Frequency, First Quadrant (see Figure 49)

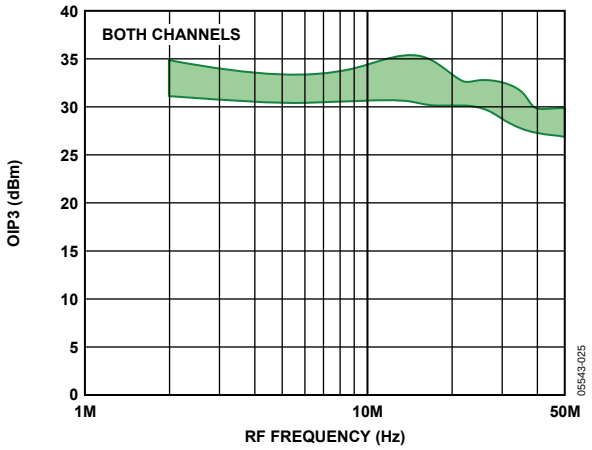

Figure 26. Representative Range of OIP3 vs. RF Frequency, First Quadrant (see Figure 49)

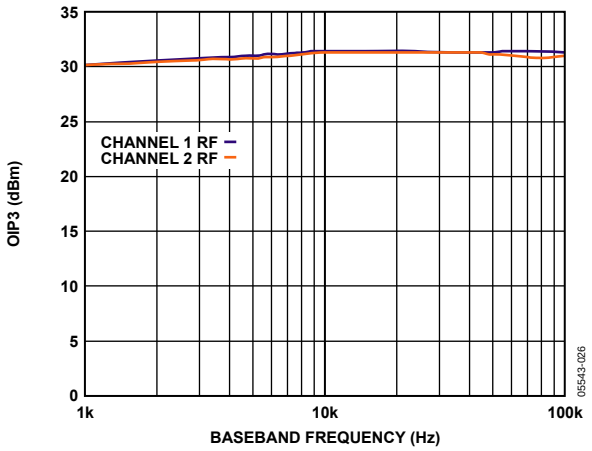

Figure 27. OIP3 vs. Baseband Frequency (see Figure 48)

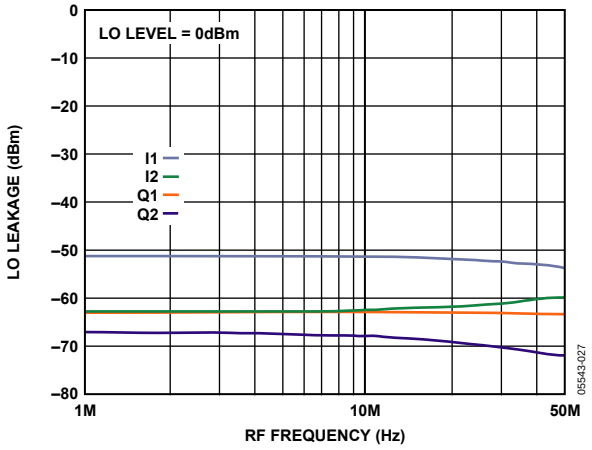

Figure 28. LO Leakage vs. RF Frequency at Baseband Outputs

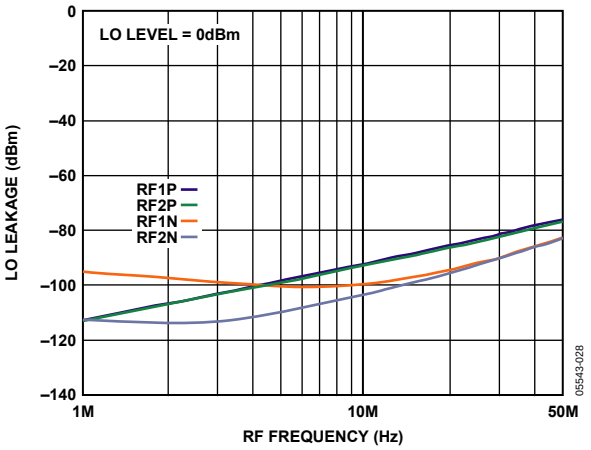

Figure 29. LO Leakage vs. RF Frequency at RF Inputs

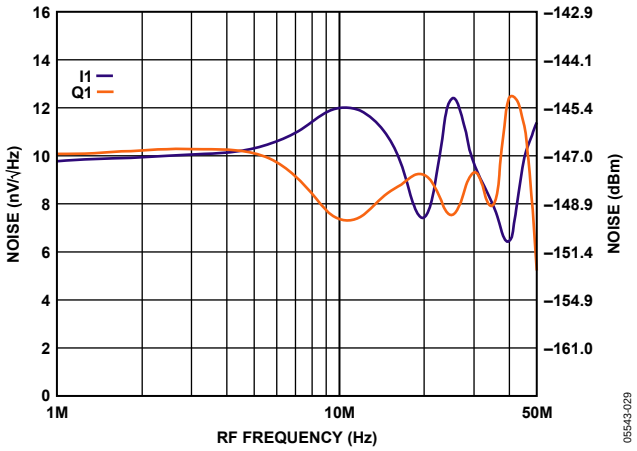

Figure 30. Input Referred Noise vs. RF Frequency

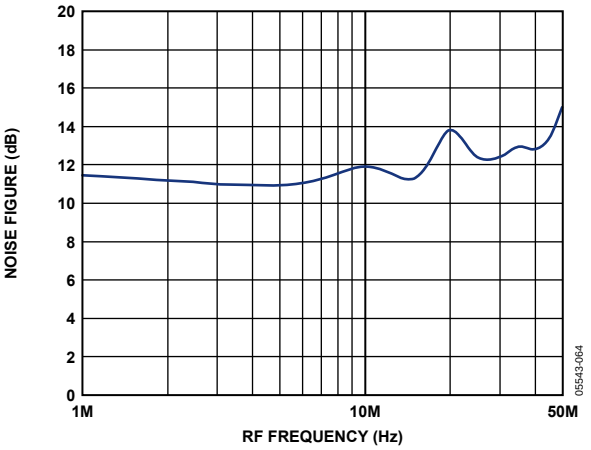

Figure 31. Noise Figure vs. RF Frequency with AD8332 LNA

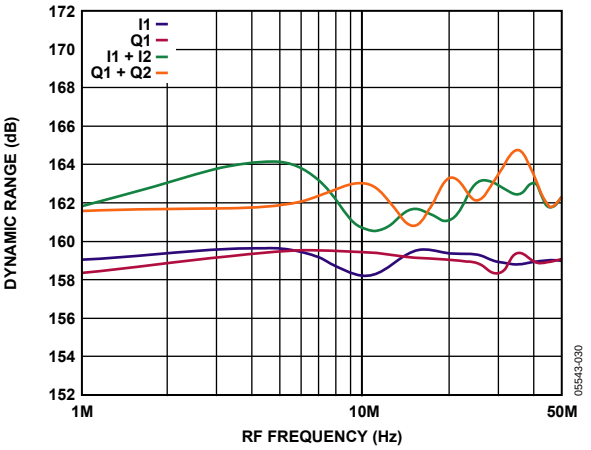

Figure 32. Dynamic Range vs. RF Frequency, IP1dB Minus Noise Level, Single Channel and Two Channels Summed

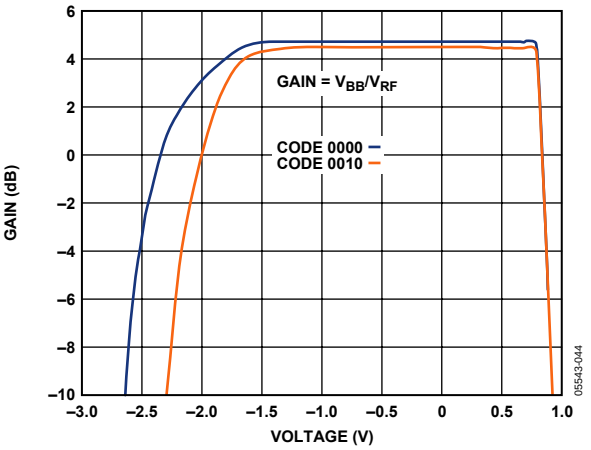

Figure 33. Output Compliance Range (IxPO, QxPO) (see Figure 50)

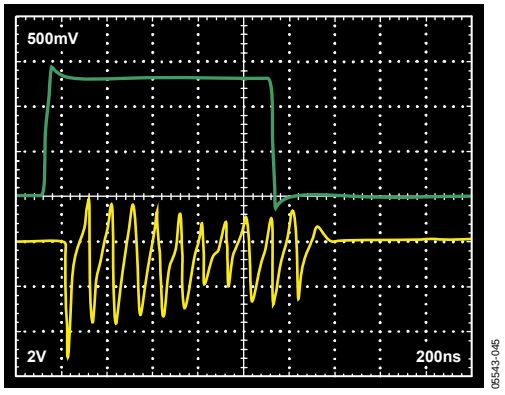

Figure 34. Enable Response—Top: Enable Signal Bottom: Output Signal (see Figure 44)

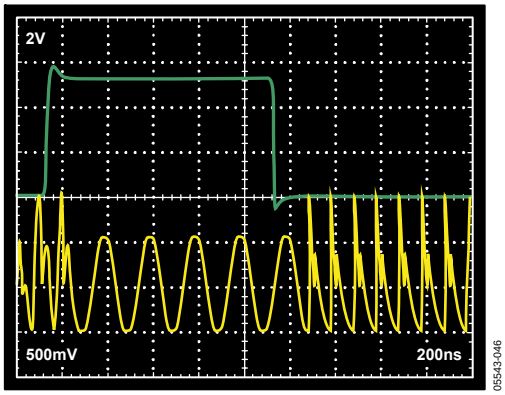

Figure 35. Reset Response—Top: Signal at Reset Pin Bottom: Output Signal (see Figure 45)

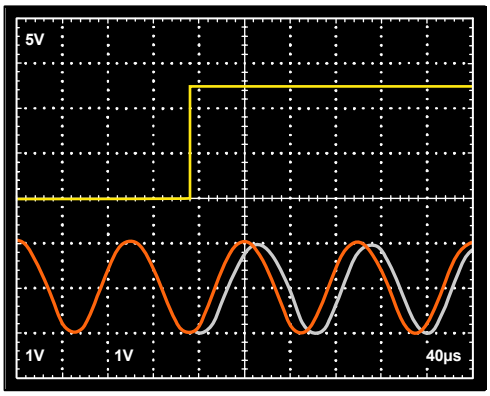

Figure 36. Phase Switching Response—CH2 Leads CH1 by 45°, Top: Input to PH21, Select Code = 0010 Red: Ref CH1 IOUT; Gray: CH2 IOUT Phase Shifted 45°, CH1 Ref Phase Select Code = 0000

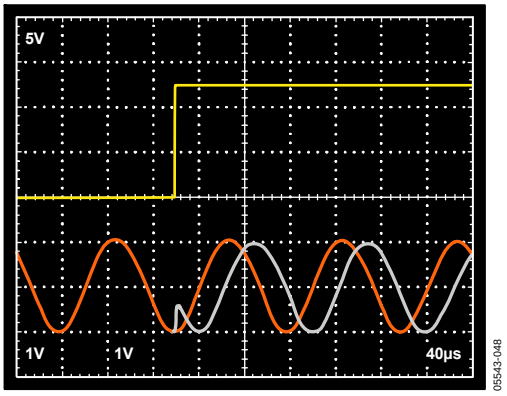

Figure 37. Phase Shifting Response—CH2 Leads CH1 by 90°, Top: Input to PH21, Select Code = 0100 Red: Ref CH1 IOUT, Gray: CH2 IOUT Phase Shifted 90°, CH1 Ref Phase Code = 0000

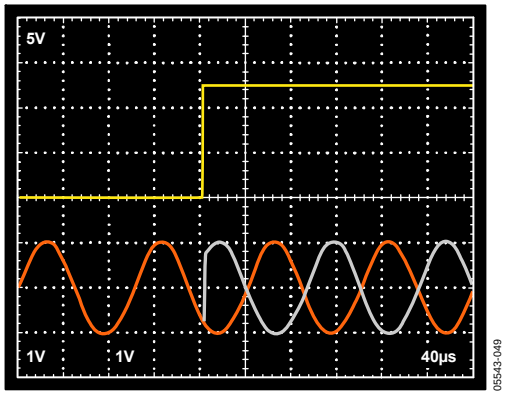

Figure 38. Phase Shifting Response—CH2 Leads CH1 by 180°,
Top: Input to PH23 Select Code = 1000
Red: Ref CH1 IOUT, Gray: CH2 IOUT Phase Shifted 180°,
CH1 Ref Phase Code = 0000

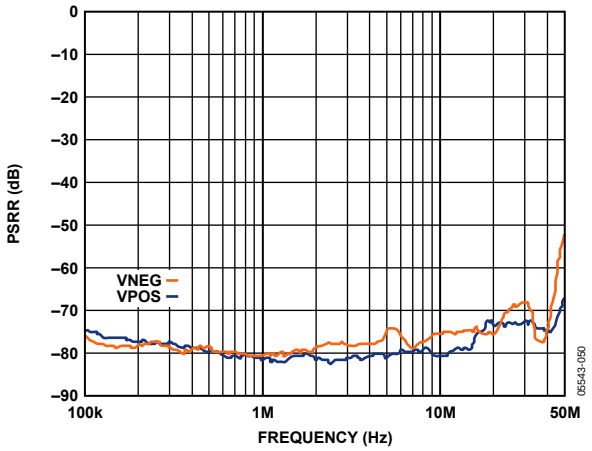

Figure 39. PSRR vs. Frequency (see Figure 51)

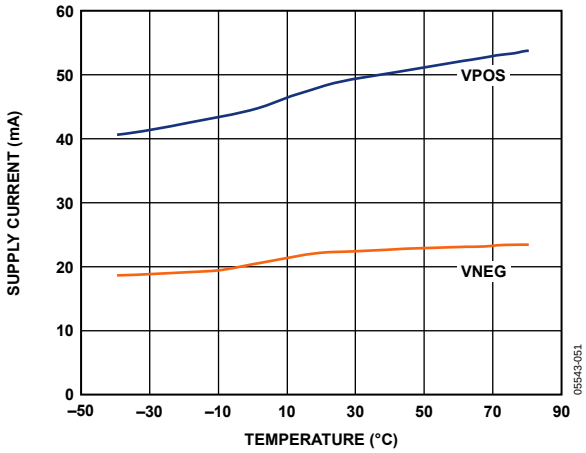

Figure 40. Quiescent Supply Current vs. Temperature

TEST CIRCUITS

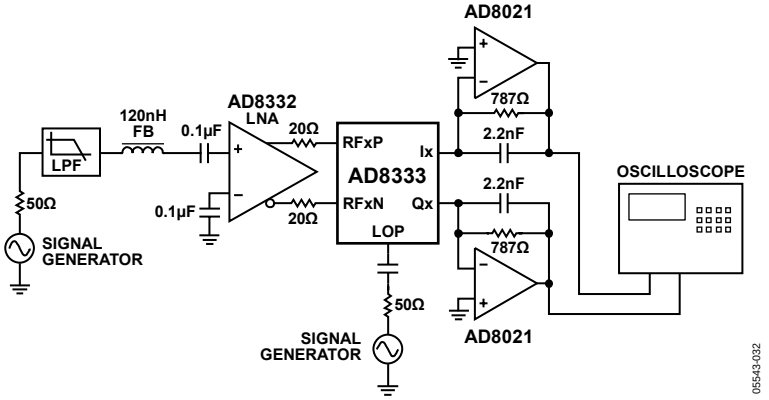

Figure 41. Default Test Circuit

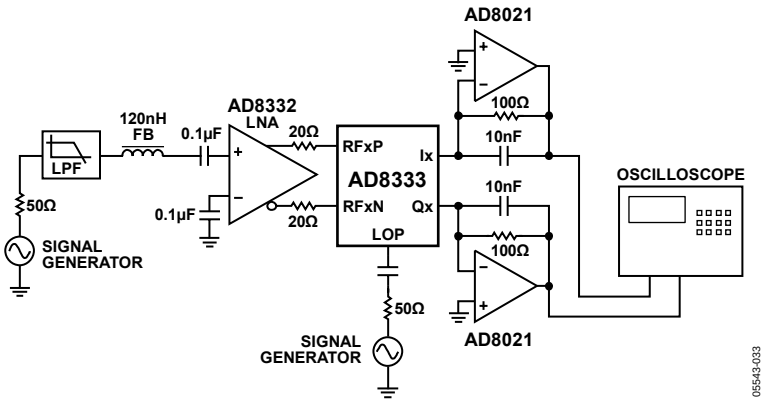

Figure 42. P1dB Test Circuit

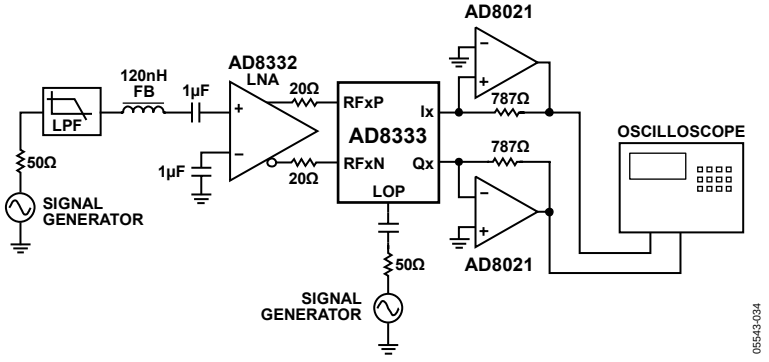

Figure 43. Phase and Amplitude vs. Baseband Frequency

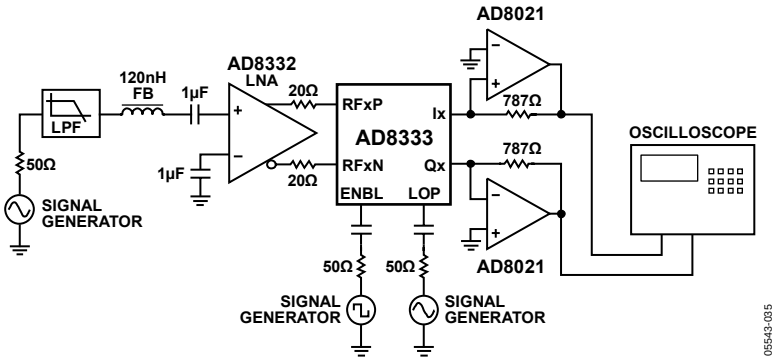

Figure 44. Enable Response

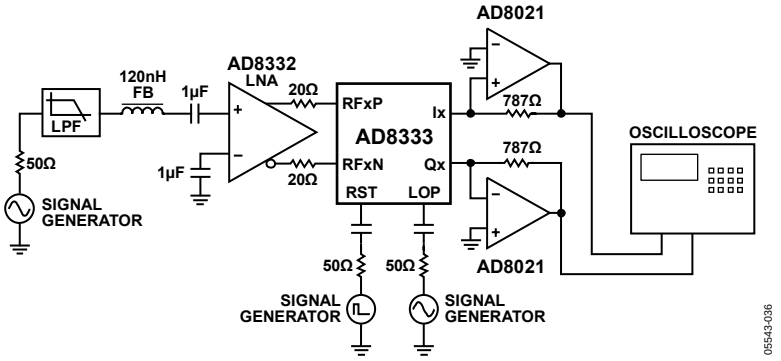

Figure 45. Reset Response

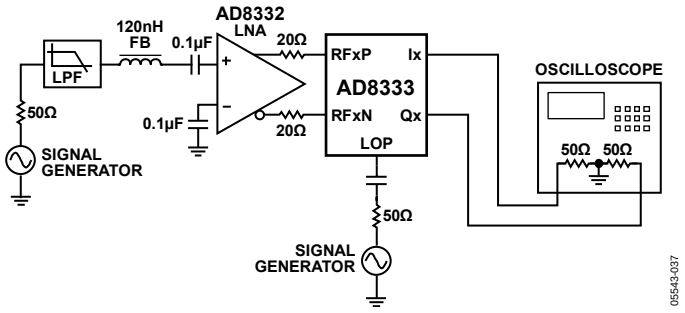

Figure 46. RF Input Range

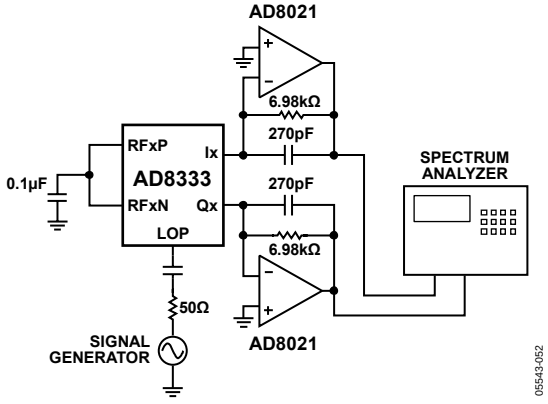

Figure 47. Noise Test Circuit

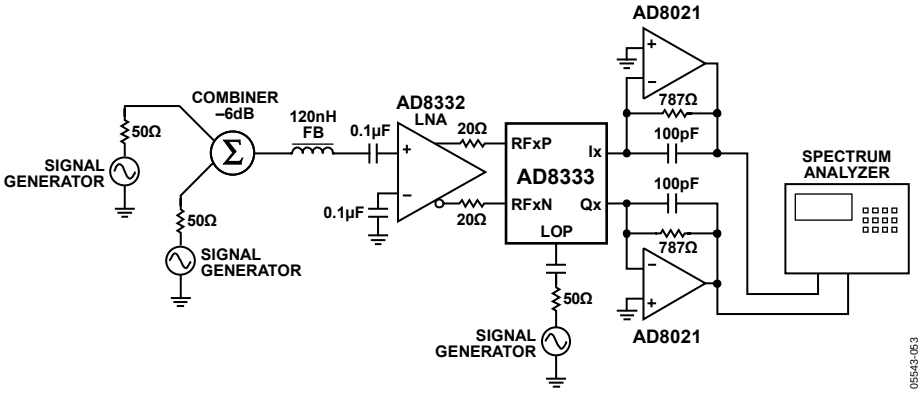

Figure 48. OIP3 vs. Baseband Frequency

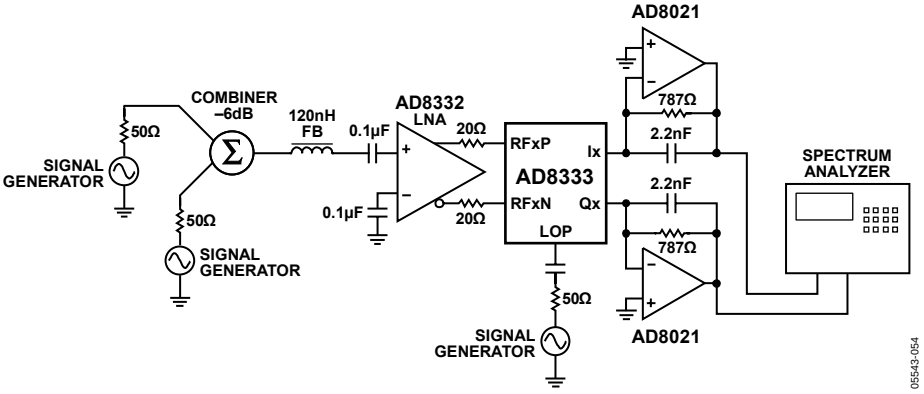

Figure 49. OIP3 and IM3 vs. RF Frequency

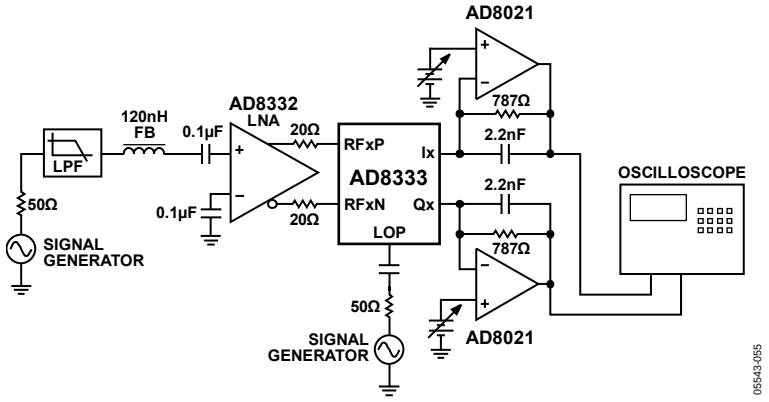

Figure 50. Output Compliance Range

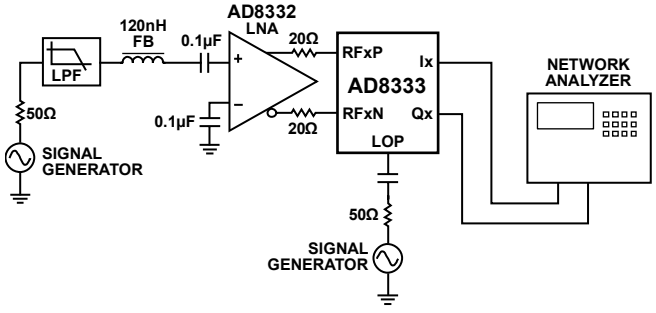

Figure 51. PSRR Test Circuit

THEORY OF OPERATION

The AD8333 is a dual I/Q demodulator with a programmable phase shifter for each channel. The primary applications are phased array beamforming in medical ultrasound, phased array radar, and smart antennas for mobile communications. The AD8333 can also be used in applications that require two well-matched I/Q demodulators.

Figure 52 shows the block diagram and pinout of the AD8333. Three analog and nine quasi-logic level inputs are required. Two RF inputs accept signals from the RF sources and a local oscillator (applied to the differential input pins marked 4LOx) common to both channels comprise the analog inputs. Four logic inputs per channel define one of 16 delay states/360° (or 22.5°/step) selectable with the PHx0 to PHx3. The reset input is used to synchronize AD8333s used in arrays.

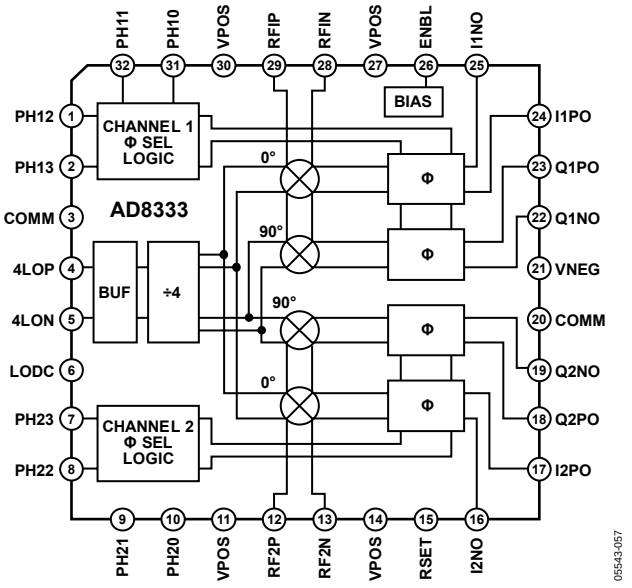

Figure 52. Block Diagram and Pinout

Each of the current formatted I and Q outputs sum together for beamforming applications. Multiple channels are summed and converted to a voltage using a transimpedance amplifier. If desired, channels can also be used individually.

QUADRATURE GENERATION

The internal 0° and 90° LO phases are digitally generated by a divide-by-4 logic circuit. The divider is dc-coupled and inherently broadband; the maximum LO frequency is limited only by its switching speed. The duty cycle of the quadrature LO signals is intrinsically 50% and is unaffected by the asymmetry of the externally connected 4LOx inputs. Furthermore, the divider is implemented such that the 4LOx signals reclock the final flip-flops that generate the internal LO signals and thereby minimizes noise introduced by the divide circuitry.

For optimum performance, the 4LOx inputs are driven differentially but can also be driven single ended. A good choice for a drive is an LVDS device. The common-mode range on each pin is approximately 0.2 V to 3.8 V with nominal ±5 V supplies.

The minimum LO level is frequency dependent (see Figure 22). For optimum noise performance, it is important to ensure that the LO source has very low phase noise (jitter) and adequate input level to assure stable mixer-core switching. The gain through the divider determines the LO signal level vs. RF frequency. The AD8333 can be operated to very low frequencies at the LO inputs if a square wave is used to drive the LO.

Beamforming applications require a precise channel-to-channel phase relationship for coherence among multiple channels. A reset pin (RSET) is provided to synchronize the 4LOx divider circuits when the AD8333s are used in arrays. The RSET pin resets the counters to a known state after power is applied to multiple AD8333s. A logic input must be provided to the RSET pin when using more than one AD8333. See the Reset Input section for more details.

I/Q DEMODULATOR AND PHASE SHIFTER

The I/Q demodulators consist of double-balanced Gilbert cell mixers. The RF input signals are converted into currents by transconductance stages that have a maximum differential input signal capability of 2.8 V p-p. These currents are then presented to the mixers, which convert them to baseband: RF − LO and RF + LO. The signals are phase shifted according to the code applied to Pin PHx0 to Pin PHx3 (see Table 4). The phase shift function is an integral part of the overall circuit (patent pending). The phase shift listed in Column 1 of Table 4 is defined as being between the baseband I or Q channel outputs. As an example, for a common signal applied to the RF inputs of an AD8333, the baseband outputs are in phase for matching phase codes. However, if the phase code for Channel 1 is 0000 and that of Channel 2 is 0001, then Channel 2 leads Channel 1 by 22.5°.

Following the phase shift circuitry, the differential current signal is converted from differential to single ended via a current mirror. An external transimpedance amplifier is needed to convert the I and Q outputs to voltages.

Table 4. Phase Select Code for Channel-to-Channel Phase Shift

ϕ-Shift	PHx3	PHx2	PHx1	PHx0
0°	0	0	0	0
22.5°	0	0	0	1
45°	0	0	1	0
67.5°	0	0	1	1
90°	0	1	0	0
112.5°	0	1	0	1
135°	0	1	1	0
157.5°	0	1	1	1
180°	1	0	0	0
202.5°	1	0	0	1
225°	1	0	1	0
247.5°	1	0	1	1
270°	1	1	0	0
292.5°	1	1	0	1
315°	1	1	1	0
337.5°	1	1	1	1

DYNAMIC RANGE AND NOISE

Figure 53 is an interconnection block diagram of the AD8333. For optimum system noise performance, the RF input signal is provided by a very low noise amplifier, such as the LNA of the AD8332 or the preamplifier of the AD8335. In beamformer applications, the I and Q outputs of a number of receiver channels are summed (for example, the two channels illustrated in Figure 53). The dynamic range of the system increases by the factor $10\log_{10}(N)$, where N is the number of channels (assuming random uncorrelated noise.) The noise in the two channel example of Figure 53 is increased by 3 dB while the signal doubles (6 dB), yielding an aggregate SNR improvement of (6 − 3) = 3 dB.

Judicious selection of the RF amplifier ensures the least degradation in dynamic range. The input referred spectral voltage noise density (e_n) of the AD8333 is nominally 9 nV/√Hz to 10 nV/√Hz. For the noise of the AD8333 to degrade the system noise figure (NF) by 1 dB, the combined noise of the source and the LNA should be about twice that of the AD8333 or 18 nV/√Hz. If the noise of the circuitry before the AD8333 is <18 nV/√Hz, then the system NF degrades more than 1 dB. For example, if the noise contribution of the LNA and source is equal to the AD8333, or 9 nV/√Hz, the degradation is 3 dB. If the circuit noise preceding the AD8333 is 1.3× as large as that of the AD8333 (or about 11.7 nV/√Hz), the degradation is 2 dB. For a circuit noise 1.45× that of the AD8333 (13.1 nV/√Hz) degradation is 1.5 dB.

To determine the input referred noise, it is important to know the active low-pass filter (LPF) values RFILT and CFILT, shown in Figure 53. Typical filter values (for example, those used on the evaluation board) are 787 Ω and 2.2 nF and implement a 90 kHz single-pole LPF. If the RF and LO are offset by 10 kHz, the demodulated signal is 10 kHz and is passed by the LPF. The single-channel mixing gain, from the RF input to the AD8021 output (for example, I1′, Q1′) is approximately 1.7 × (4.7 dB). This together with the 9 nV/√Hz AD8333 noise results in about 15.3 nV/√Hz at the AD8021 output. Because the AD8021, including the 787 Ω feedback resistor, contributes another 4.4 nV/√Hz, the total output referred noise is about 16 nV/√Hz. This value can be adjusted by increasing the filter resistor while maintaining the corner frequency, thereby increasing the gain. The factor limiting the magnitude of the gain is the output swing and drive capability of the op amp selected for the I-to-V converter, in this instance the AD8021.

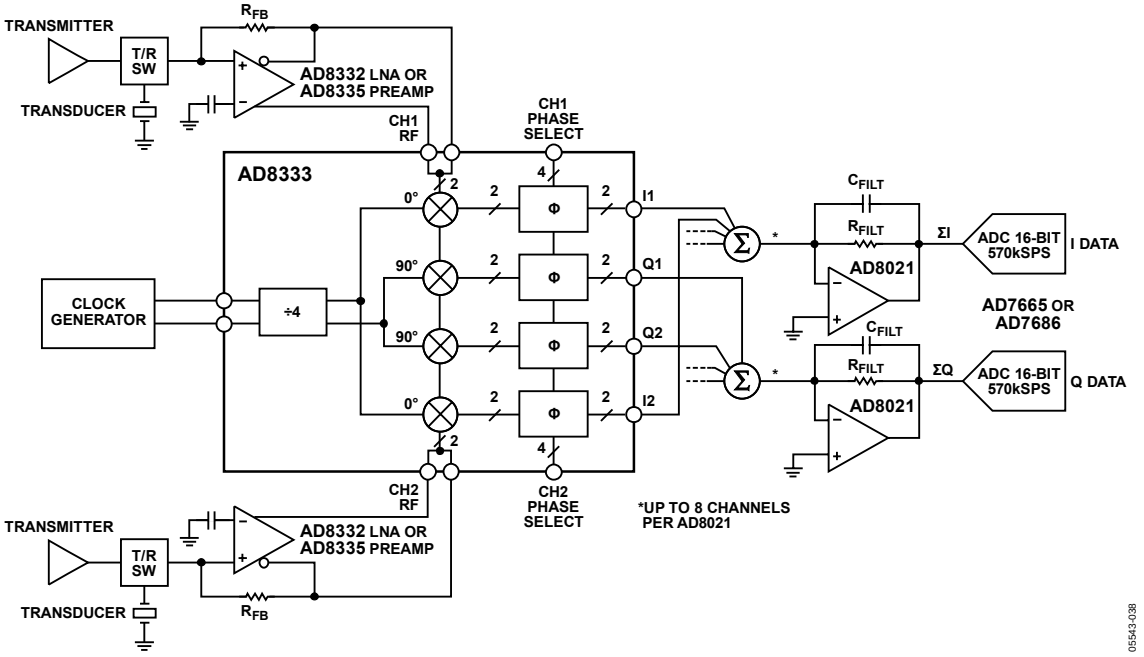

Figure 53. Interconnection Block Diagram

SUMMATION OF MULTIPLE CHANNELS (ANALOG BEAMFORMING)

Beamforming, as applied to medical ultrasound, is defined as the phase alignment and summation of signals generated from a common source but received at different times by a multielement ultrasound transducer. Beamforming has two functions: it imparts directivity to the transducer, enhancing its gain, and it defines a focal point within the body from which the location of the returning echo is derived. The primary application for the AD8333 is in analog beamforming circuits for ultrasound.

PHASE COMPENSATION AND ANALOG BEAMFORMING

Modern ultrasound machines used for medical applications employ a 2^n binary array of receivers for beamforming, with typical array sizes of 16 or 32 receiver channels phase-shifted and summed together to extract coherent information. When used in multiples, the desired signals from each of the channels can be summed to yield a larger signal (increased by a factor N, where N is the number of channels), while the noise is increased by the square root of the number of channels. This technique enhances the signal-to-noise performance of the machine. The critical elements in a beamformer design are the means to align the incoming signals in the time domain, and the means to sum the individual signals into a composite whole.

In traditional analog beamformers incorporating Doppler, a V-to-I converter per channel and a crosspoint switch precede passive delay lines used as a combined phase shifter and summing circuit. The system operates at the receive frequency (RF) through the delay line, and then the signal is down-converted by a very large dynamic range I/Q demodulator.

The resultant I and Q signals are filtered and sampled by two high resolution ADCs. The sampled signals are processed to extract the relevant Doppler information.

Alternatively, the RF signal can be processed by downconversion on each channel individually, phase shifting the downconverted signal, and then combining all channels. The AD8333 provides the means to implement this architecture. The downconversion is done by an I/Q demodulator on each channel, and the summed current output is the same as in the delay line approach. The subsequent filters after the I-to-V conversion and the ADCs are similar.

The AD8333 integrates the phase shifter, frequency conversion, and I/Q demodulation into a single package and directly yields the baseband signal. To illustrate, Figure 54 is a simplified diagram showing two channels. The ultrasound wave USW is received by two transducer elements, TE1 and TE2, in an ultrasound probe and generates signals E1 and E2. In this example, the phase at TE1 leads the phase at TE2 by 45°.

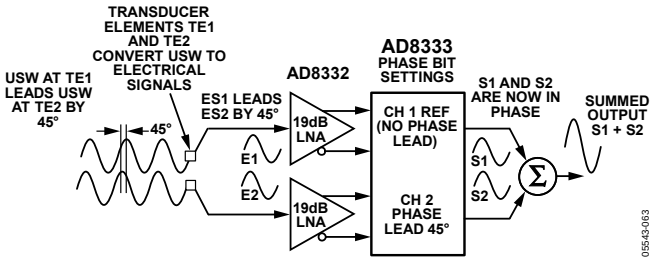

Figure 54. Simplified Example of the AD8333 Phase Shifter

In a real application, the phase difference depends on the element spacing, λ (wavelength), speed of sound, angle of incidence, and other factors. The signals ES1 and ES2 are amplified 19 dB by the low noise amplifiers in the AD8332. For optimum signal-to-noise performance, the output of the LNA is applied directly to the input of the AD8333. To sum the signals ES1 and ES2, ES2 is shifted 45° relative to ES1 by setting the phase code in Channel 2 to 0010. The phase-aligned current signals at the output of the AD8333 are summed in an I-to-V converter to provide the combined output signal with a theoretical improvement in dynamic range of 3 dB for the sum of two channels.

CHANNEL SUMMING

In a beamformer using the AD8333, the bipolar currents at the I and Q outputs are summed directly. Figure 55 illustrates 16 summed channels (for clarity shown as current sources) as an example of an active current summing circuit using the AD8333, AD8021s as first-order current summing circuits, and AD797s as low noise second-order summing circuits. Beginning with the op amps, there are a few important considerations in the circuit shown in Figure 55.

The op amps selected for the first-order summing amplifiers must have good frequency response over the full operating frequency range of the AD8333s and be able to source the current required at the AD8333 I and Q outputs.

The total current of each of the AD8333s is 6.6 mA for the multiples of the 45° phase settings (Code 0010, Code 0110, Code 1010, and Code 1110) and divided about equally between the baseband frequencies (including a dc component) and the second harmonic of the local oscillator frequency. The desired CW signal tends to be much less (<40 dB) than the unwanted interfering signals. When determining the large signal requirements of the first-order summing amplifiers and low-pass filters, the very small CW signal can be ignored. The number of channels that can be summed is limited by the output drive current capacity of the op amp selected: 60 mA to 70 mA for a linear output current for ±5 V and ±12 V, respectively, for the AD8021. Because the AD8021 implements an active LPF together with R1 and C1, it must absorb the worst-case current provided by the AD8333, for example, 6.6 mA. Thus, the maximum number of channels that the AD8021 can sum is 10 for ±12 V or eight for ±5 V supplies. In practical applications, CW channels are used in powers of two, thus the maximum number per AD8021 is eight.

Another consideration for the op amp selected as an I-to-V converter is the compliance voltage of the AD8333 I and Q outputs. The maximum compliance voltage is 0.5 V, and a dc bias must be provided at these pins. The AD8021 active LPF satisfies these requirements; it keeps the outputs at 0 V via the virtual ground at the op amp inverting input while providing any needed dc bias current.

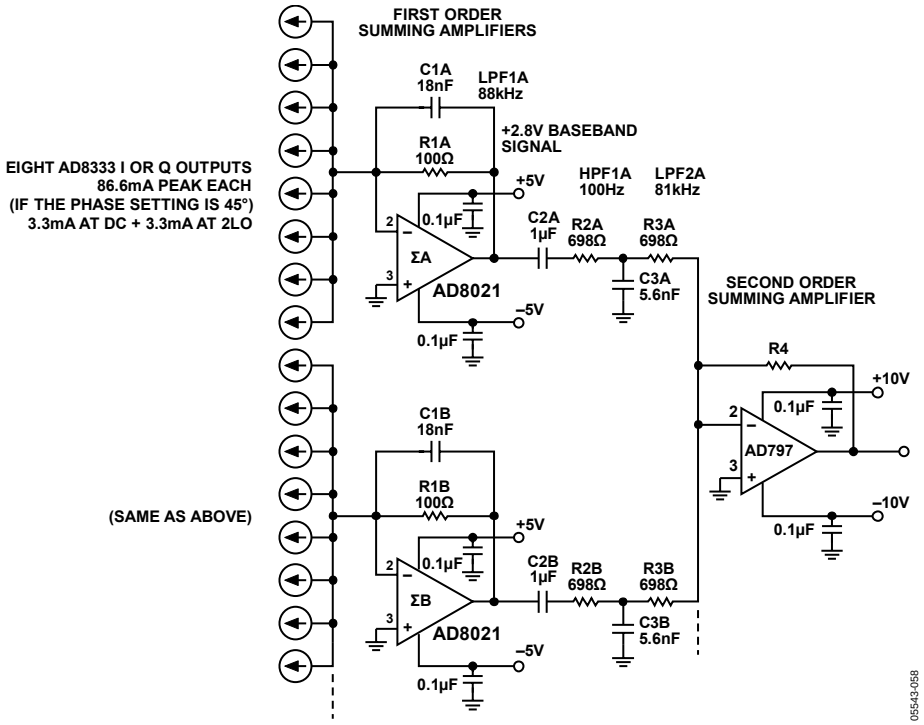

Figure 55. A 16-Channel Beamformer

As previously noted, a typical CW signal has a large dc and very low frequency component compared to its desired low CW Doppler baseband frequency, and another unwanted component at the 2 × LO. The dc component flows through the gain resistors R1x, while the 2 × LO flows through the capacitors C1x. The smaller desired CW Doppler baseband signal is in the frequency range of 1 kHz to 50 kHz.

Because the output current of the AD8333 contains the baseband frequency, a dc component, and the 2 × LO frequency voltages, the desired small amplitude baseband signal must be extracted after a series of filters. These are shown in Figure 55 as LPFn, HPFn, and gain stages.

Before establishing the value of C_{LPF1}, the resistor R_{LPF1} is selected based on the peak operating current and the linear range of the op amp. Because the peak current for each AD8333 is 6.6 mA and there are eight channels to be summed, the total peak current required is 52.8 mA. Approximately half of this current is dc and the other half at a frequency of 2 × LO. Therefore, about 26.4 mA flows through the resistor while the remaining 26.4 mA flows through the capacitor. Resistor R1 was selected as 100 Ω and, after filtering, generates a peak dc and very low frequency voltage of 2.64 V at the AD8021 output. For power supplies of ±5 V, 100 Ω is a good choice for R1.

However, because the CW signal needs to be amplified as much as possible, and the noise degradation of the signal path minimized, the value of R1 should be as large as possible. A larger supply helps in this regard, and the only factor limiting the largest supply voltage is the required power.

For a ±10 V supply on the AD8021, R1 can be increased to 301 Ω and realize the same headroom as with a ±5 V supply. If a higher value of R1 is used, C1 must be adjusted accordingly (in this example 1/3 the value of the original value) to maintain the desired LPF roll-off. The principal advantage of a higher supply is greater dynamic range, and the trade-off is power consumption. The user must weigh the trade-offs associated with the supply voltage, R1, C1, and the following circuitry. A suggested design sequence is:

- Select a low noise, high speed op amp. The spectral density noise (e_n) should be <2nV/√Hz and the 3 dB BW ≥ 3 × the expected maximum 2 × LO frequency.
- Divide the maximum linear output current by 6.6 mA to determine the maximum number of AD8333 channels that can be summed.
- Select the largest value of R1 that permits the output voltage swing within the power supply rails.
- Calculate the value of C1 to implement the LPF corner that allows the CW Doppler signal to pass with maximum attenuation of the 2 × LO signal.

The filter LPF1 establishes the upper frequency limit of the baseband frequency and is selected well below the 2 × LO frequency, typically 100 kHz or less, or, as an example, 88 kHz as shown in Figure 55.

A useful equation for calculating C1 is

$$C1 = \frac{1}{2\pi R1 f_{LPF1}} \quad (1)$$

As previously mentioned, the AD8333 output current contains a dc current component. This dc component is converted to a large dc voltage by the AD8021 LPF. Capacitor C2 filters this dc component and, with R2 + R3, establishes a high-pass filter with a low frequency cutoff of about 100 Hz. Capacitor C3 is much smaller than C2 and, consequently, can be neglected. C2 can be calculated by

$$C2 = \frac{1}{2\pi(R2 + R3) f_{HPF1}} \quad (2)$$

To achieve maximum attenuation of the 2 × LO frequency, a second low-pass filter, LPF2, is established using the parallel combination of R2 and R3, and C3. Its −3 dB frequency is simply

$$f_{LPF2} = \frac{1}{2\pi(R2 \,||\, R3)C3} \quad (3)$$

In the example shown in Figure 55, f_{LPF2} = 81 kHz.

Finally, the feedback resistor of the AD797 must be calculated. This is a function of the input current (number of channels) and the supply voltage.

The second-order summing amplifier requires a very low noise op amp, such as the AD797, with 0.9 nV/√Hz, because the amplifier gain is determined by Feedback Resistor R4 divided by the parallel combination of the LPF2 resistors seen looking back toward the AD8021s. Referring to Figure 55, the AD797 inband (100 Hz to 88 kHz) gain is expressed as

$$\frac{R4}{\left[(R2A + R3A) \,||\, (R2B + R2B)\right]} \quad (4)$$

The AD797 noise gain can increase to unacceptable levels, because the denominator of the gain equation is the parallel resistance of all the R2 + R3 resistors in the AD8021 outputs. For example, for a 64-channel beamformer, the resistance seen looking back toward the AD8021s is about 1.4 kΩ/8 = 175 Ω. For this reason, the value of (R2x + R3x) should be as large as possible to minimize the noise gain of the AD797. (Note that this is the case for the AD8021 stages because they look back into the high impedance current sources of the AD8333s.)

Due to these considerations, it is advantageous to increase the gain of the AD8021s as much as possible, because the value of (R2x + R3x) can be increased proportionally. Resistors (R2x + R3x) convert the CW voltages to currents that are summed at the inverting inputs of the AD797 op amp and amplified and converted to voltages by R4.

The value of R4 needs to be chosen iteratively as follows:

- Determine the number of AD8021 first-order summing amplifiers. In Figure 55, there are two; for a 32-channel beamformer, there would be four, and for a 64-channel beamformer, there would be eight.
- Determine the output noise after the AD8021s. A first-order calculation can be based on a value of AD8333 output current noise of about 20 pA/√Hz. For the values in Figure 55, this results is about 6 nV/√Hz for eight channels after the AD8021s. Adding the noise of the AD8021 and the 100 Ω feedback resistor results in about 6.5 nV/√Hz total noise after the AD8021 LPF in the CW Doppler band.
- Determine the noise of the circuitry after the AD797 and the desired signal level.
- Determine the voltage and current noise of the second-order summing amplifiers.
- Choose a value for R2x + R3x and for R4. Determine the resulting output noise after the AD797 for one channel and then multiply by the square root of the number of summed AD8021s. Next, check AD797 output noise (both current and voltage noise). Ideally, the sum of the noise of the resistors and the AD797 is less than a factor-of-3 than the noise due to the AD8021 outputs.
- Check the following stages output noise against the calculated noise from the combiner circuit and AD8333s; ideally the noise from the following stage should be less than 1/3 of the calculated noise.
- If the combined noise is too large, experiment with increasing/decreasing values for R2x + R3x and R4.

To simplify, the user can also simulate or build a combiner circuit for optimum performance. It should be noted that the ~20 pA/√Hz out of the AD8333 is for the AD8333 with shorted RF inputs. In an actual system, the current noise out of the AD8333 is most likely dominated by the noise from the AD8332 LNA and the noise from the source and other circuitry before the LNA. This helps ease the design of the combiner. The preceding procedures for determining the optimum values for the combiner are based on the noise floor of the AD8333 only.

As an example, for a 32-channel beamformer using four low-pass filters, as shown in Figure 55, (R2x + R3x) = 1.4 kΩ and R4 = 6.19 kΩ. The theoretical noise increase of √N is degraded by only about 1 dB.

DYNAMIC RANGE INFLATION

Although all 64 channels could theoretically be summed together at a single amplifier, it is important to realize that the dynamic range of the summed output increases by $10\times\log_{10}(N)$ if all channels have uncorrelated noise, where *N* is the number of channels to be summed.

The summed signal level increases by a factor of N while the noise increases only as √N. In the case of 64 channels, this is an increase in dynamic range of 18 dB. Note that the AD8333 dynamic range is already about 160 dB/Hz; the summed dynamic range is 178 dB/Hz (equivalent to about 29.5 b/Hz). In a 50 kHz noise bandwidth, this is 131 dB (21.7 bits).

DISABLING THE CURRENT MIRROR AND DECREASING NOISE

The noise contribution of the AD8333 can potentially be reduced if the current mirrors that convert the internal differential signals to single ended are bypassed (see Figure 56). Current mirrors interface to the AD8021 I-V converters shown in Figure 53, and output capacitors across the positive and negative outputs provide low-pass filtering. The AD8021s force the AD8333 output voltage to 0 V and process the bipolar output current; however, the internal current mirrors introduce a significant amount of noise. This noise can be reduced if they are disabled and the outputs externally biased.

The mirrors are disabled by connecting VNEG to ground and providing external bias networks, as shown in Figure 56. The larger the drop across the resistors, the less noise they contribute to the output; however, the voltage on the IxxO and QxxO nodes cannot exceed 0.5 V. Voltages exceeding approximately 0.7 V turn on the PNP devices and forward bias the ESD protection diodes. Inductors provide an alternative to resistors, enabling reduced static power by eliminating the power dissipation in the bias resistors.

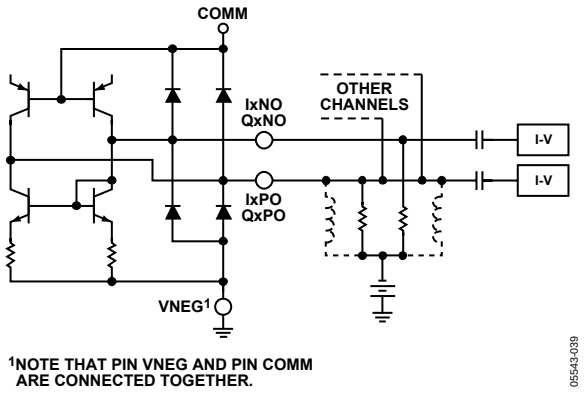

Figure 56. Bypassing the Internal Current Mirrors

With inductors, the main limitation might be low frequency operation, as is the case in CW Doppler in ultrasound where the frequency range of interest goes from a few hundred Hertz to about 30 kHz. In addition, it is still important to provide enough gain through the I-to-V circuitry to ensure that the bias resistor and I-to-V converter noise do not contribute significantly to the noise from the AD8333 outputs. Another approach could be to provide a single external current mirror that combines all channels; it would also be possible to implement a high-pass filter with this circuit to help with offset and low frequency reduction.

The main disadvantage of the external bias approach is that now two I-V amplifiers are needed because of the differential output (see Figure 56). For beamforming applications, the outputs would still be summed as before but now there is twice the number of lines. Only two bias resistors are needed for all outputs that are connected together. The resistors are scaled by dividing the value of a single output bias resistor through N, the number of channels connected in parallel. The bias current depends on the phase selected: for phase 0°, this is about 2.5 mA per side, while in the case of 45°, this is about 3.5 mA per side. The bias resistors should be chosen based on the larger bias current value of 3.5 mA and the chosen VNEG. VNEG should be at least −5 V and can be larger for additional noise reduction.

Excessive noise or distortion at high signal levels degrades the dynamic range of the signal. Transmitter leakage and echoes from slow moving tissue generate the largest signal amplitudes in ultrasound CW Doppler mode and are largest near dc and at low frequencies. A high-pass filter introduced immediately following the AD8333 reduces the dynamic range. This is shown by the two coupling capacitors after the external bias resistors in Figure 56. Users have to determine what is acceptable in their particular application. Care must be taken in designing the external circuitry to avoid introducing noise via the external bias and low frequency reduction circuitry.

APPLICATIONS

The AD8333 is the key component of a phase-shifter system that aligns time-skewed information contained in RF signals. Combined with a variable gain amplifier (VGA) and low noise amplifier (LNA), the AD8333 forms a complete analog receiver for a high performance ultrasound system. Figure 57 is a block diagram of a complete receiver using the AD8333 and the AD8332 family.

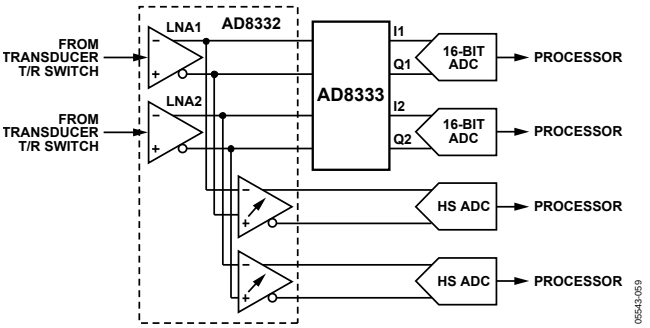

Figure 57. Block Diagram—Ultrasound Receiver Using the AD8333 and AD8332 LNA

As a major element of an ultrasound system, it is important to consider the many I/O options of the AD8333 necessary to perform its intended function. Figure 61 shows the basic connections.

LOGIC INPUTS AND INTERFACES

The logic inputs of the AD8333 are all bipolar-level sensitive inputs. They are not edge triggered, nor are they to be confused with classic TTL or other logic family input topologies. The voltage threshold for these inputs is VPOS × 0.3, so for a 5 V supply the threshold is 1.5 V, with a hysteresis of ±0.2 V. Although the inputs are not of themselves logic inputs, any 5 V logic family can drive them.

RESET INPUT

The RSET pin is used to synchronize the LO dividers in AD8333 arrays. Because they are driven by the same internal LO, the two channels in any AD8333 are inherently synchronous. However, when multiple AD8333s are used, it is possible that their dividers wake up in different phase states. The function of the RSET pin is to phase align all the LO signals in multiple AD8333s.

The 4 × LO divider of each AD8333 can initiate in one of four possible states 0°, 90°, 180°, and 270°. The internally generated I/Q signals of each AD8333 LO is always at a 90° angle relative to each other, but a phase shift can occur during power up between the internal LOs of the different AD8333s.

The RSET pin provides an asynchronous reset of the LO dividers by forcing the internal LO to hang. This mechanism also allows the measurement of nonmixing gain from the RF input to the output.

The rising edge of the active high RSET pulse can occur at any time; however, the duration must be ≥ 300 ns minimum (t_{PW-MIN}). When the RSET pulse transitions from high to low, the LO dividers are reactivated; however, there is a short delay until the divider recovers to a valid state. To guarantee synchronous operation of an array of AD8333s, the 4 LO clock must be disabled when the RSET transitions high and remain disabled for at least 300 ns after RSET transitions low.

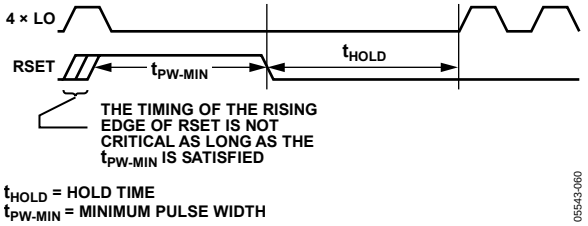

Figure 58. Timing of the RSET Signal to 4 LO

Synchronization of multiple AD8333s can be checked as follows:

- Set the phase code of all AD8333 channels the same, for example, 0000.
- Apply a test signal to a single channel that generates a sine wave in the baseband output and measure the output.
- Apply the same test signal to all channels simultaneously and measure the output.
- Since all the phase codes of the AD8333s are the same, the combined signal should be N times bigger than the single channel. The combined signal is less than N times one channel if any of the LO phases of individual AD8333s are in error.

CONNECTING TO THE LNA OF THE AD8331/ AD8332/AD8334/AD8335 VGAs

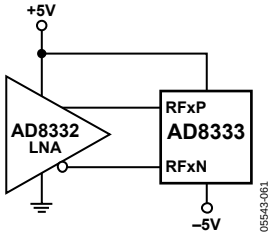

Figure 59. Connecting the AD8333 to the LNA of an AD8332

The RFxx inputs (Pin 12, Pin 13, Pin 28, and Pin 29) are optimized for maximum dynamic range when dc-coupled to the differential output pins of the LNA of the AD8331/AD8332/AD8334 or the AD8335 series of variable gain amplifiers and can be connected directly, as shown in Figure 59.

If amplifiers other than the AD8332 LNA are connected to the input, attention must be paid to their bias and drive levels. For maximum input signal swing, the optimum bias level is 2.5 V, and the RF input must not exceed 5 V to avoid turning on the ESD protection circuitry. If ac coupling is used, a bias circuit, such as that illustrated in Figure 60, is recommended. An internal bias network is provided, however, additional external biasing can center the RF input at 2.5 V.

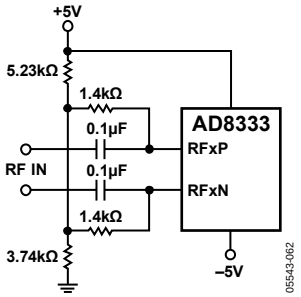

Figure 60. AC Coupling the AD8333 RF Input

LO INPUT

The local oscillator (LO) input is a high speed, fully differential, analog input that responds to differences in the input levels (and not logic levels). The LO inputs can be driven with a low common-mode voltage amplifier, such as the National DS90C401 LVDS driver.

The graphs shown in Figure 22 and Figure 23 show the range of common-mode voltages and useable LO levels when the LO input is driven with a single-ended sine wave. Logic families, such as TTL or CMOS, are unsuitable for direct coupling to the LO input.

EVALUATION BOARD

Figure 61 and Figure 62 show the evaluation board schematics; they include an AD8332 to allow tests either directly, as one would use it in an actual application, or by applying signals via connectors directly to the RF inputs. For best performance, it is recommended that the RF inputs be driven differentially. Although the 4 × LO input can be driven single-ended, differential drive is recommended. The 4 × LO inputs require very low bias currents and can be supplied by a multidrop LVDS driver, LV-PECL, or any other high speed differential signal that stays within the common-mode range of the inputs (0.2 V to 3.8 V).

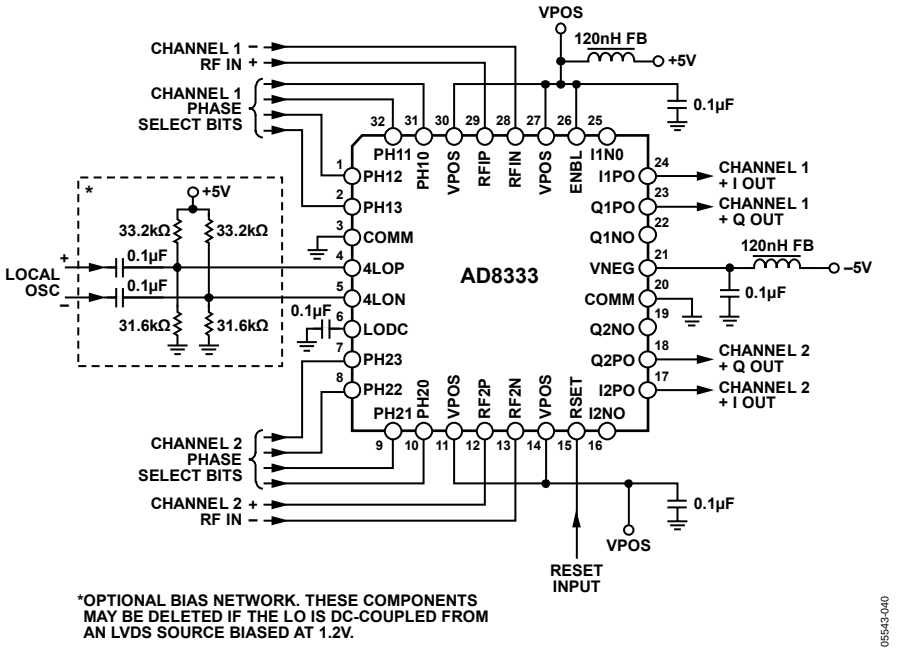

Figure 61. AD8333 Basic Connections

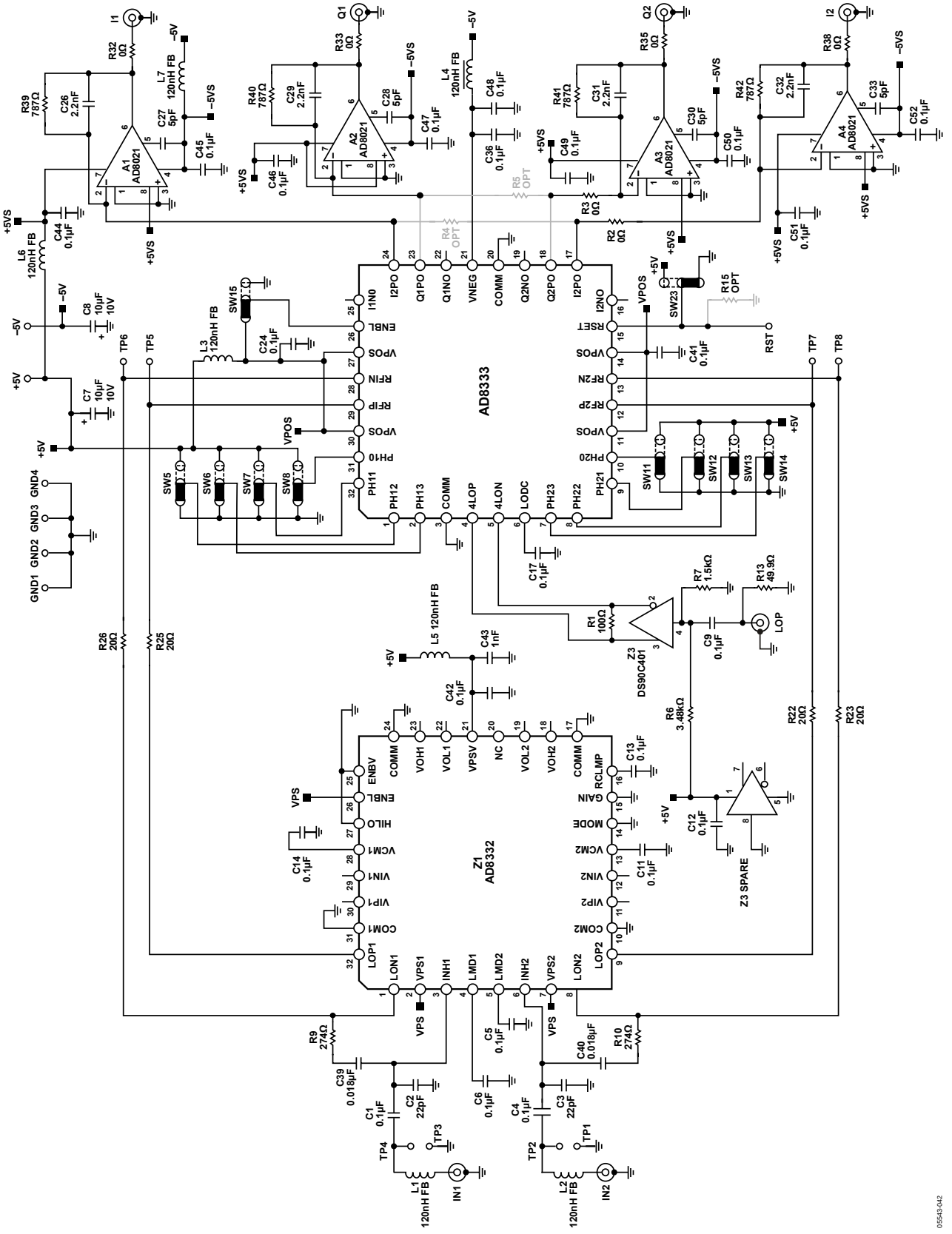

Figure 62. AD8333 Evaluation Board Schematic

OUTLINE DIMENSIONS

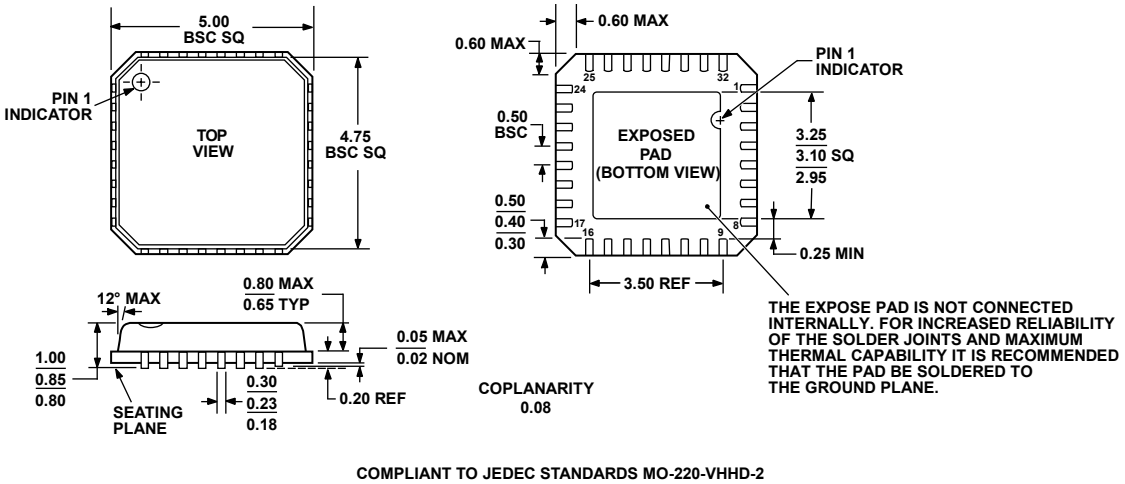

Figure 63. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm x 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8333ACPZ-REEL[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
AD8333ACPZ-REEL7[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
AD8333ACPZ-WP[1, 2]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
AD8333-EVAL		Evaluation Board	

[1] Z = Pb-free part.
[2] WP = Waffle pack.

NOTES

D05543-0-5/06(A)