50 µA, 2 mm × 1.7 mm WLCSP, Low Noise, Heart Rate Monitor for Wearable Products

Data Sheet **AD8233**

FEATURES

- Fully integrated, single-lead electrocardiogram (ECG) front end
- Low quiescent supply current: 50 µA (typical)
- Leads on/off detection while in shutdown (<1 µA)
- Common-mode rejection ratio: 80 dB (dc to 60 Hz)
- 2 or 3 electrode configurations
- High signal gain (G = 100) with dc blocking capabilities
- 2-pole adjustable high-pass filter
- Accepts up to ±300 mV of half cell potential
- Fast restore feature improves filter settling
- Uncommitted op amp
- 3-pole adjustable low-pass filter with adjustable gain
- Integrated right leg drive (RLD) amplifier with shutdown
- Single-supply operation: 1.7 V to 3.5 V
- Integrated reference buffer generates virtual ground
- Rail-to-rail output
- Internal RFI filter
- 8 kV human body model (HBM) ESD rating
- Shutdown pin
- 2 mm × 1.7 mm WLCSP

APPLICATIONS

- Fitness and activity heart rate monitors
- Portable ECG
- Wearable and remote health monitors
- Gaming peripherals
- Biopotential signal acquisition, such as EMG

FUNCTIONAL BLOCK DIAGRAM

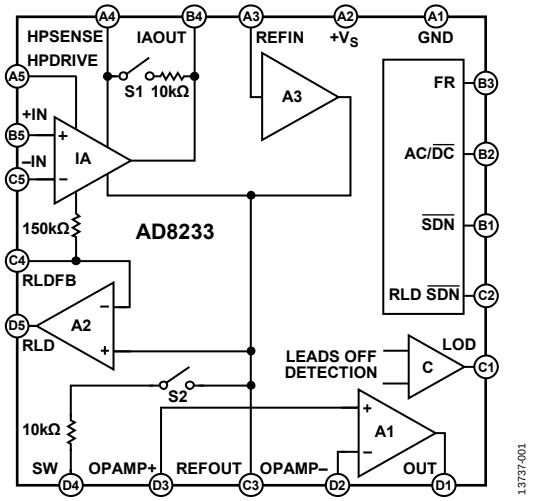

Figure 1.

GENERAL DESCRIPTION

The AD8233 is an integrated signal conditioning block for ECG and other biopotential measurement applications. It is designed to extract, amplify, and filter small biopotential signals in the presence of noisy conditions, such as those created by motion or remote electrode placement. This design allows an ultralow power analog-to-digital converter (ADC) or an embedded microcontroller to easily acquire the output signal.

The AD8233 implements a two-pole high-pass filter for eliminating motion artifacts and the electrode half cell potential. This filter is tightly coupled with the instrumentation architecture of the amplifier to allow both large gain and high-pass filtering in a single stage, thereby saving space and cost.

An uncommitted operational amplifier enables the AD8233 to create a three-pole, low-pass filter to remove additional noise. The user can select the frequency cutoff of all filters to suit different types of applications.

To improve the common-mode rejection of the line frequencies in the system and other undesired interferences, the AD8233 includes an amplifier for driven lead applications, RLD.

The AD8233 includes a fast restore function that reduces the duration of the otherwise long settling tails of the high-pass filters. After an abrupt signal change that rails the amplifier (such as a leads off condition), the AD8233 automatically adjusts to a higher filter cutoff. This feature allows the AD8233 to recover quickly, and therefore, to take valid measurements soon after connecting the electrodes to the subject.

The AD8233 is available in a 2 mm × 1.7 mm, 20-ball WLCSP package. Performance is specified from 0°C to 70°C and is operational from −40°C to +85°C.

Table 1. AD8232 vs. AD8233 Comparison

Parameter	AD8232	AD8233
Supply Current	170 µA	50 µA
Peak-to-Peak Voltage Noise (f = 0.5 Hz to 40 Hz)	14 µV p-p	8.5 µV
Leads On/Off Detection in Shutdown	Not included	Included
Right Leg Drive Shutdown	Not included	Included
Package Size	4 mm × 4 mm × 0.75 mm	2 mm × 1.7 mm × 0.5 mm

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Comparable Parts

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Evaluation Kits

- AD8233 Evaluation Board

Documentation

Data Sheet

- AD8233: 50 µA, 2 mm × 1.7 mm WLCSP, Low Noise, Heart Rate Monitor for Wearable Products Data Sheet

User Guides

- UG-1016: Evaluating the AD8233 50 µA, 2 mm × 1.7 mm WLCSP, Low Noise, Heart Rate Monitor for Wearable Products

Tools and Simulations

- AD8232/AD8233 Filter Design Tool
- AD8233 SPICE Macro-Model

Design Resources

- AD8233 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

8/2016—Revision 0: Initial Version

SPECIFICATIONS

$+V_S$ = 1.8 V to 3 V ± 5.5%, V_{REF} = $+V_S/2$, V_{CM} = $+V_S/2$, T_A = 25°C, FR = low, $\overline{SDN}$ = high, AC/$\overline{DC}$ = low, RLD $\overline{SDN}$ = low, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER						
Common-Mode Rejection Ratio, DC to 60 Hz	CMRR	V_{CM} = 0.35 V to $+V_S$ − 150 mV, V_{DIFF} = 0 V	80	86		dB
		V_{CM} = 0.35 V to $+V_S$ − 150 mV, V_{DIFF} = ±0.3 V		80		dB
Power Supply Rejection Ratio	PSRR	$+V_S$ = 1.8 V to 3.5 V	76	90		dB
Offset Voltage (RTI)	V_{OS}					
Instrumentation Amplifier Inputs				1	6	mV
DC Blocking Input[1]				25		µV
Average Offset Drift						
Instrumentation Amplifier Inputs				2		µV/°C
DC Blocking Input[1]				0.05		µV/°C
Input Bias Current	I_B			50	200	pA
		T_A = 0°C to 70°C		1		nA
Input Offset Current	I_{OS}			25	100	pA
		T_A = 0°C to 70°C		1		nA
Input Impedance						
Differential				10‖7.5		GΩ‖pF
Common Mode				5‖15		GΩ‖pF
Input Voltage Noise (RTI)						
Spectral Noise Density		f = 1 kHz		150		nV/√Hz
Peak-to-Peak Voltage Noise		f = 0.1 Hz to 10 Hz		10		µV p-p
		f = 0.5 Hz to 40 Hz		8.5		µV p-p
Input Voltage Range		T_A = 0°C to 70°C	0.2		$+V_S$	V
DC Differential Input Range	V_{DIFF}		−300		+300	mV
Output						
Output Swing		R_L = 50 kΩ	0.1		$+V_S$ − 0.1	V
Short-Circuit Current	I_{OUT}			6.3		mA
Gain	A_V			100		V/V
Gain Error		V_{DIFF} = 0 V		0.4		%
		V_{DIFF} = −300 mV to +300 mV		1	4	%
Average Gain Drift		T_A = 0°C to 70°C		12		ppm/°C
Bandwidth	BW			1		kHz
RFI Filter Cutoff (Each Input)				1		MHz
OPERATIONAL AMPLIFIER (A1)						
Offset Voltage	V_{OS}			1	5	mV
Average Temperature Coefficient	TC	T_A = 0°C to 70°C		1		µV/°C
Input Bias Current	I_B			100		pA
		T_A = 0°C to 70°C		1		nA
Input Offset Current	I_{OS}			100		pA
		T_A = 0°C to 70°C		1		nA
Input Voltage Range			0.1		$+V_S$ − 0.1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.5 V to $+V_S$ − 0.5 V		100		dB
Power Supply Rejection Ratio	PSRR			100		dB
Large Signal Voltage Gain	A_{VO}			110		dB
Output Voltage Range		R_L = 50 kΩ	0.1		$+V_S$ − 0.1	V
Short-Circuit Current Limit	I_{OUT}			12		mA
Gain Bandwidth Product	GBP			15		kHz

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Slew Rate	SR			0.01		V/µs
Voltage Noise Density (RTI)	e_n	f = 1 kHz		120		nV/√Hz
Peak-to-Peak Voltage Noise (RTI)	$e_{n\ p-p}$	f = 0.1 Hz to 10 Hz		7		µV p-p
		f = 0.5 Hz to 40 Hz		9		µV p-p
RIGHT LEG DRIVE AMPLIFIER (A2)						
Quiescent Supply Current				7.5	10	µA
Output Swing		R_L = 50 kΩ	0.1		$+V_S$ – 0.1	V
Short-Circuit Current	I_{OUT}			11		mA
Integrator Input Resistor			120	150	180	kΩ
Gain Bandwidth Product	GDP			20		kHz
REFERENCE BUFFER (A3)						
Offset Error	V_{OS}	R_L > 50 kΩ		1		mV
Input Bias Current	I_B			100		pA
Short-Circuit Current Limit	I_{OUT}			12		mA
Voltage Range		R_L = 50 kΩ	0.1		$+V_S$ – 0.7	V
DC LEADS OFF COMPARATORS						
Threshold Voltage				$+V_S$ – 0.27		V
Hysteresis				125		mV
Propagation Delay				1.5		µs
AC LEADS OFF DETECTOR						
Square Wave Frequency	f_{AC}		50	100	175	kHz
Square Wave Amplitude	I_{AC}			200		nA p-p
Input Currents in Shutdown Mode[2]	I_{DC}	+IN, $\overline{SDN}$ = low		250		nA
		–IN, $\overline{SDN}$ = low		–300		nA
Impedance Threshold		Between +IN and –IN, $\overline{SDN}$ = high	10	20		MΩ
Detection Delay				100		µs
FAST RESTORE CIRCUIT						
Switches		S1 and S2				
On Resistance	R_{ON}		8	10	12	kΩ
Off Leakage				100		pA
Window Comparator						
Threshold Voltage		From either rail		100		mV
Propagation Delay				2		µs
Switch Timing Characteristics						
Feedback Recovery Switch On Time	t_{S1}	$+V_S$ = 3 V		160		ms
		$+V_S$ = 1.8 V		80		
Filter Recovery Switch On Time	t_{S2}	$+V_S$ = 3 V		80		ms
		$+V_S$ = 1.8 V		40		
Fast Restore Reset	t_{RST}	$+V_S$ = 3 V		3		µs
		$+V_S$ = 1.8 V		1.5		
LOGIC INTERFACE						
Input Characteristics						
Input Voltage (AC/$\overline{DC}$, FR, and RLD $\overline{SDN}$)						
Low	V_{IL}			0.41 × $+V_S$		V
High	V_{IH}			0.45 × $+V_S$		V
Input Voltage ($\overline{SDN}$)						
Low	V_{IL}			0.6 × $+V_S$		V
High	V_{IH}			0.3 × $+V_S$		V
Output Characteristics		LOD terminal				
Output Voltage		R_L = 100 kΩ				
Low	V_{OL}			0.05		V
High	V_{OH}			$+V_S$ – 0.05		V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM SPECIFICATIONS						
Quiescent Supply Current				50	70	μA
		T_A = 0°C to 70°C		60		μA
Wakeup Current		$\overline{SDN}$ = low, LOD = low		0.65	1.5	μA
		T_A = 0°C to 70°C		0.75		μA
Shutdown Current		$\overline{SDN}$ = low, LOD = high		0.5	1	μA
		T_A = 0°C to 70°C		0.6		μA
Peak-to-Peak Voltage Noise (RTI)		V_{DIFF} = 0 V				
		f = 0.5 Hz to 40 Hz		9		μV p-p
		f = 0.05 Hz to 150 Hz		15		μV p-p
		V_{DIFF} = ±0.3 V				
		f = 0.5 Hz to 40 Hz		11		μV p-p
		f = 0.05 Hz to 150 Hz		21		μV p-p
Supply Range			1.7		3.5	V
Specified Temperature Range			0		70	°C
Operational Temperature Range			−40		+85	°C

[1] Offset referred to the input of the instrumentation amplifier inputs.
[2] In ac leads off and shutdown mode, the dc leads off comparator at the +IN pin trips the LOD pin.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	3.6 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage, Any Terminal[1]	$+V_S$ + 0.3 V
Minimum Voltage, Any Terminal[1]	−0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	140°C
ESD Rating	
HBM	8 kV
Charged Device Model (FICDM)	1 kV

[1] This level or the maximum specified supply voltage, whichever is the lesser, indicates the superior voltage limit for any terminal. If input voltages beyond the specified minimum or maximum voltages are expected, place resistors in series with the inputs to limit the current to less than 5 mA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	PCB	Power (W)	θ_{JA} (°C/W)			θ_{JC} (°C/W)
			0 ms	1 ms	2 ms	
CP-20-13	1S0P[1]	0.25	108.5	89.0	82.3	0.6
		1.25	101.1	87.3	87.3	0.6
	2S2P[2]	0.25	47.9	43.4	42.1	0.7
		1.25	46.8	43.3	42.1	0.7

[1] Simulated thermal numbers per JESD51-9: 1-layer PCB (1S0P), low effective thermal conductivity test board.
[2] 4-layer PCB (2S2P), high effective thermal conductivity test board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

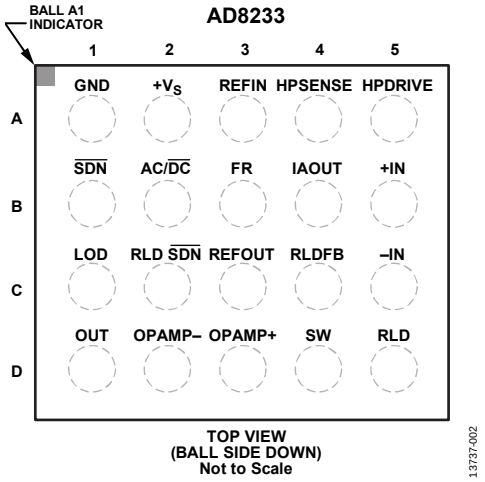

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	GND	Power Supply Ground.
A2	$+V_S$	Power Supply Terminal.
A3	REFIN	Reference Buffer Input. Use REFIN, a high impedance input terminal, to set the level of the reference buffer.
A4	HPSENSE	High-Pass Sense Input for Instrumentation Amplifier. Connect HPSENSE to the junction of R and C that sets the corner frequency of the dc blocking circuit.
A5	HPDRIVE	High-Pass Driver Output. Connect HPDRIVE to the capacitor in the first high-pass filter. The AD8233 drives this pin to keep HPSENSE at the same level as the reference voltage.
B1	$\overline{SDN}$	Shutdown Control Input. Drive $\overline{SDN}$ low to enter the low power shutdown mode.
B2	AC/$\overline{DC}$	Leads Off Mode Control Input. Drive the AC/$\overline{DC}$ pin low for dc leads off mode. Drive the AC/$\overline{DC}$ pin high for ac leads off mode.
B3	FR	Fast Restore Control Input. Drive FR high to enable fast recovery mode; otherwise, drive it low.
B4	IAOUT	Instrumentation Amplifier Output Terminal.
B5	+IN	Instrumentation Amplifier, Positive Input. +IN is typically connected to the left arm (LA) electrode.
C1	LOD	Leads Off Detection (LOD) Comparator Output.
C2	RLD $\overline{SDN}$	Right Leg Drive Shutdown Control Input. Drive RLD $\overline{SDN}$ low to power down the RLD amplifier.
C3	REFOUT	Reference Buffer Output. The instrumentation amplifier output is referenced to this potential. Use REFOUT as a virtual ground for any point in the circuit that requires a signal reference.
C4	RLDFB	Right Leg Drive Feedback Input. RLDFB is the feedback terminal for the right leg drive circuit.
C5	–IN	Instrumentation Amplifier, Negative Input. –IN is typically connected to the right arm (RA) electrode.
D1	OUT	Operational Amplifier Output. The fully conditioned heart rate signal is present at this output. OUT can be connected to the input of an ADC.
D2	OPAMP–	Operational Amplifier Inverting Input.
D3	OPAMP+	Operational Amplifier Noninverting Input.
D4	SW	Fast Restore Switch Terminal. Connect this terminal to the output of the second high-pass filter.
D5	RLD	Right Leg Drive Output. Connect the driven electrode (typically, right leg) to the RLD pin.

TYPICAL PERFORMANCE CHARACTERISTICS

$+V_S$ = 3 V, V_{REF} = 1.5 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

INSTRUMENTATION AMPLIFIER PERFORMANCE CHARACTERISTICS

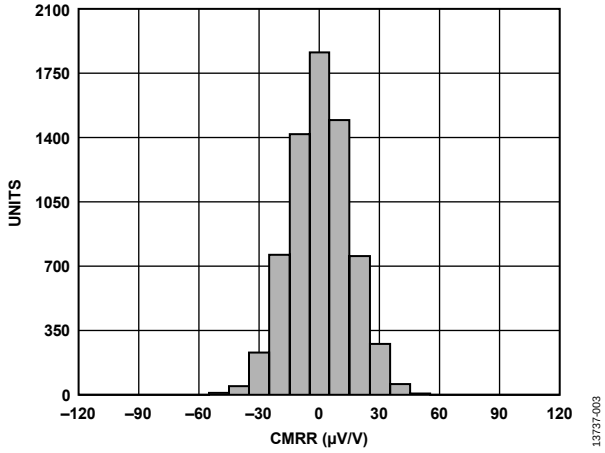

Figure 3. CMRR Distribution

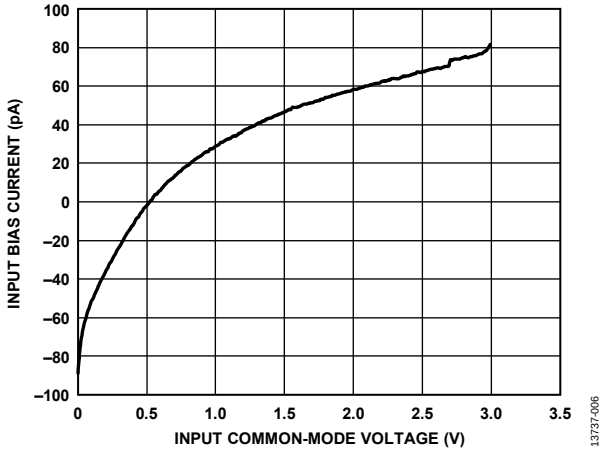

Figure 6. Input Bias Current vs. Input Common-Mode Voltage

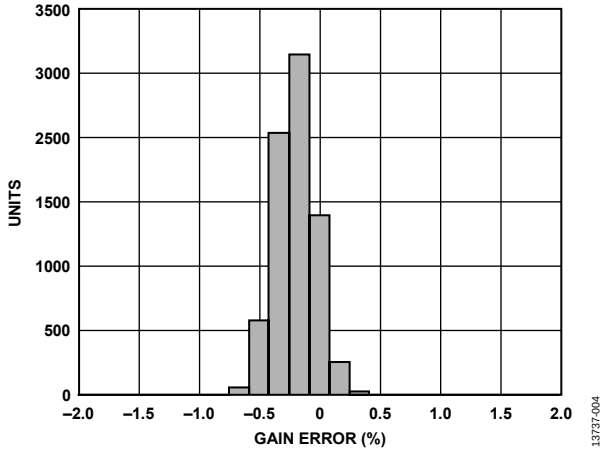

Figure 4. Gain Error Distribution

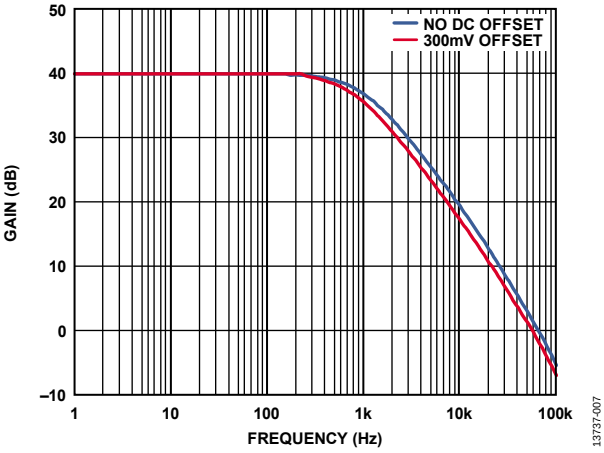

Figure 7. Gain vs. Frequency

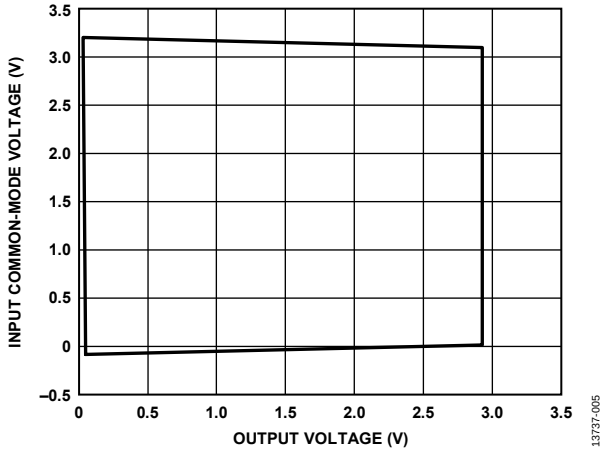

Figure 5. Input Common-Mode Voltage vs. Output Voltage

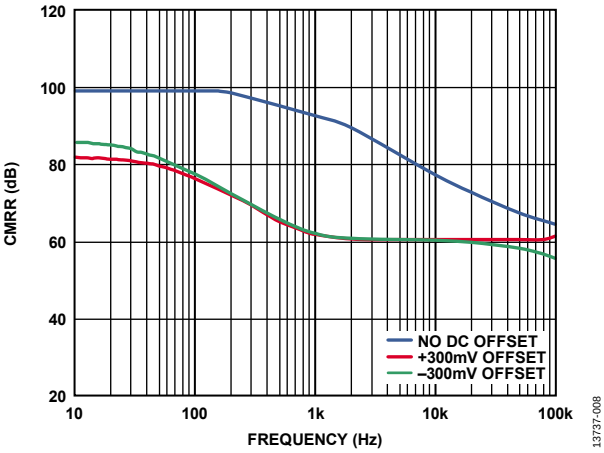

Figure 8. CMRR vs. Frequency (RTI)

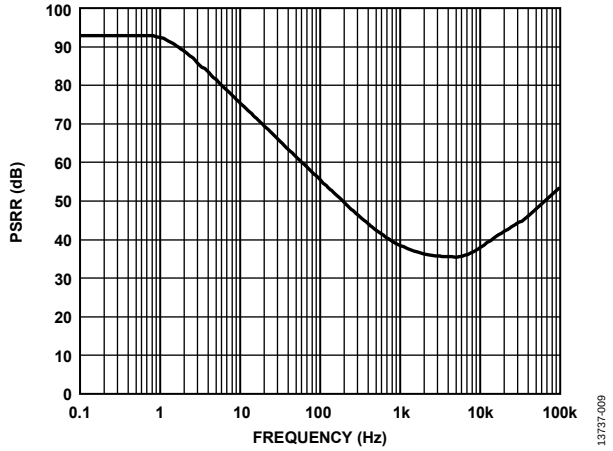

Figure 9. PSRR vs. Frequency (RTI)

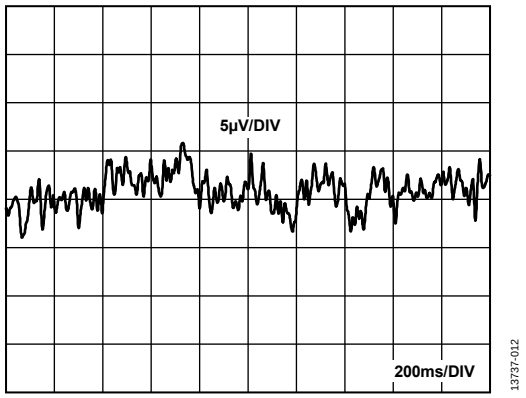

Figure 12. 0.5 Hz to 40 Hz Noise (RTI)

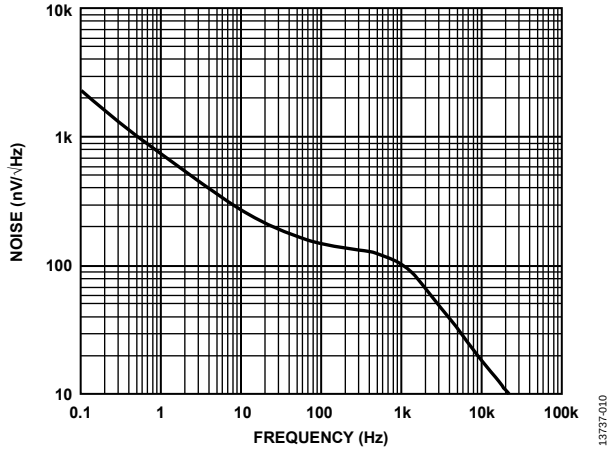

Figure 10. Voltage Noise Spectral Density (RTI)

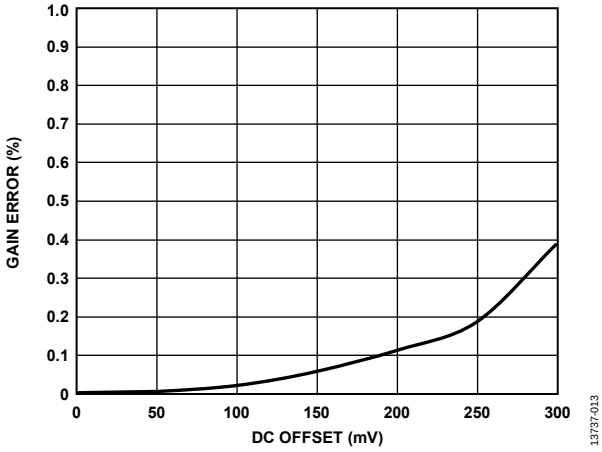

Figure 13. Gain Error vs. DC Offset

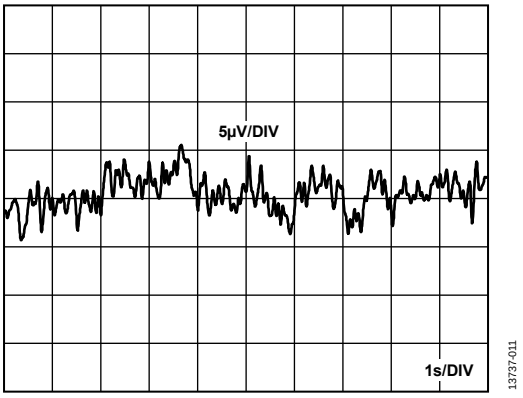

Figure 11. 0.1 Hz to 10 Hz Noise (RTI)

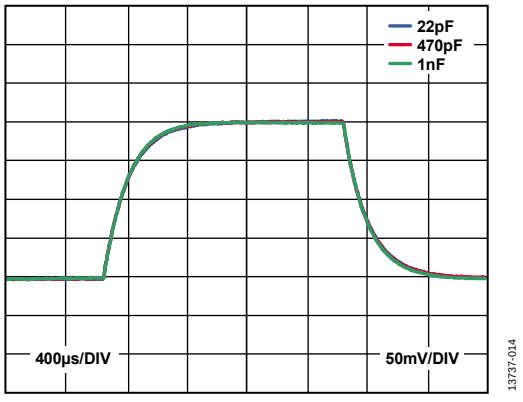

Figure 14. Small Signal Pulse Response

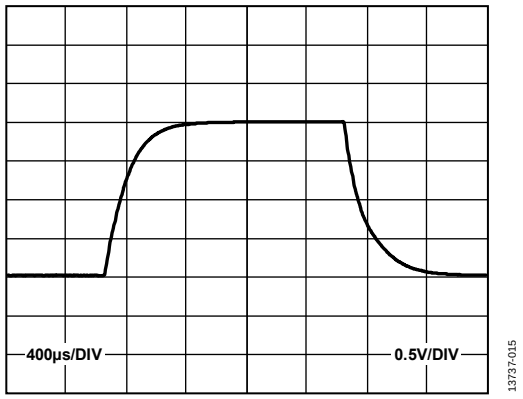

Figure 15. Large Signal Pulse Response

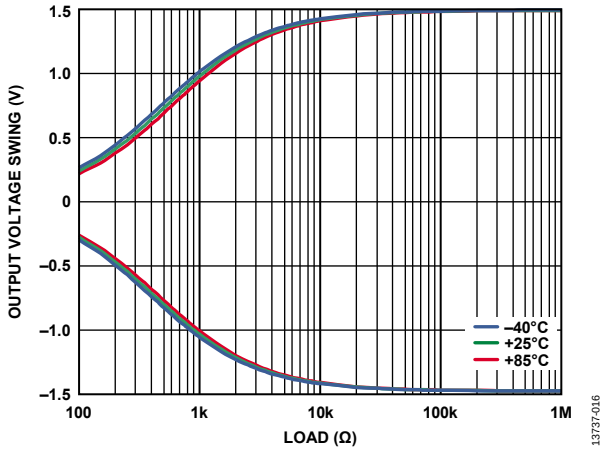

Figure 16. Output Voltage Swing vs. Load

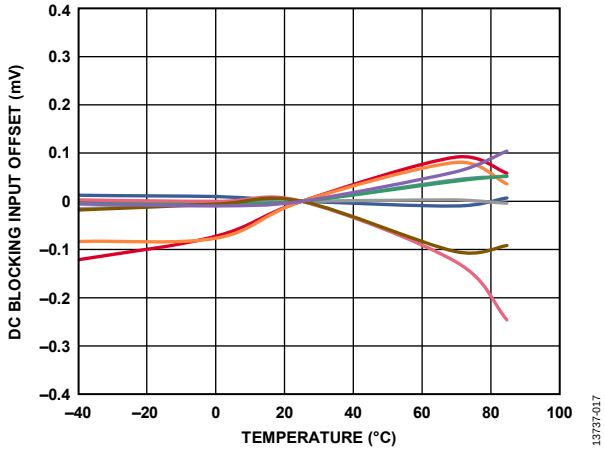

Figure 17. DC Blocking Input Offset Drift

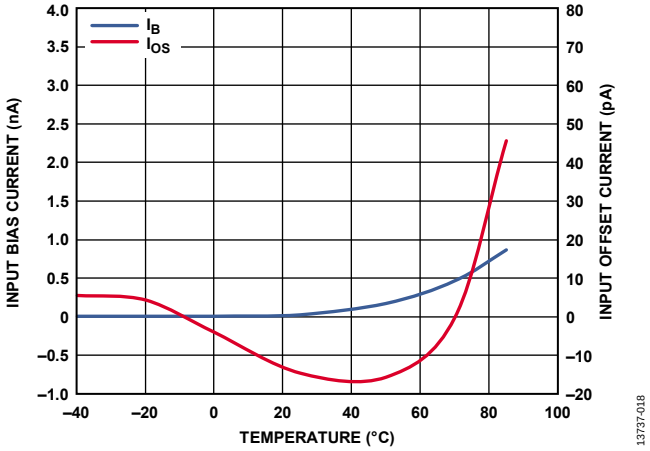

Figure 18. Input Bias Current (I_B) and Input Offset Current (I_{OS}) vs. Temperature

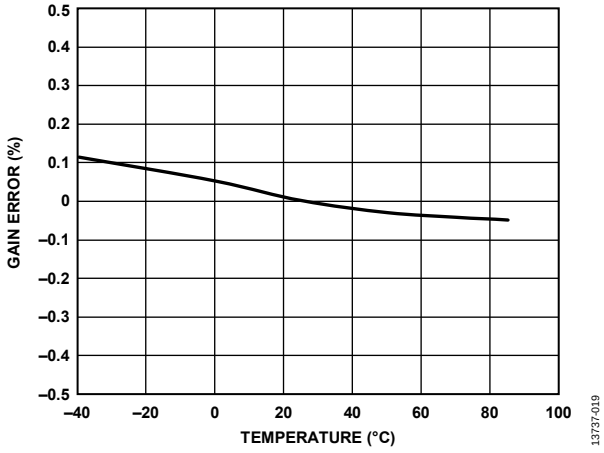

Figure 19. Gain Error vs. Temperature

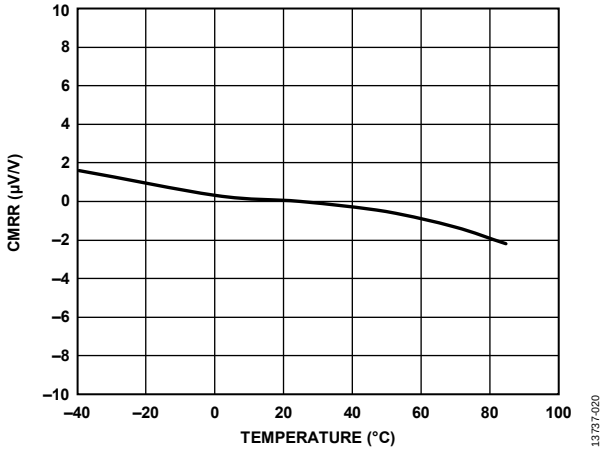

Figure 20. CMRR vs. Temperature

OPERATIONAL AMPLIFIER PERFORMANCE CHARACTERISTICS

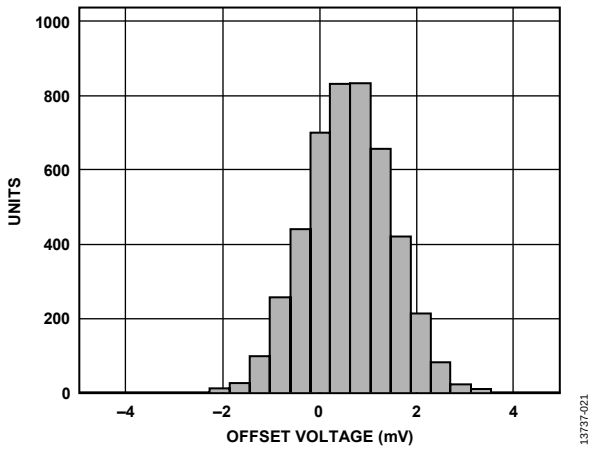

Figure 21. Offset Distribution

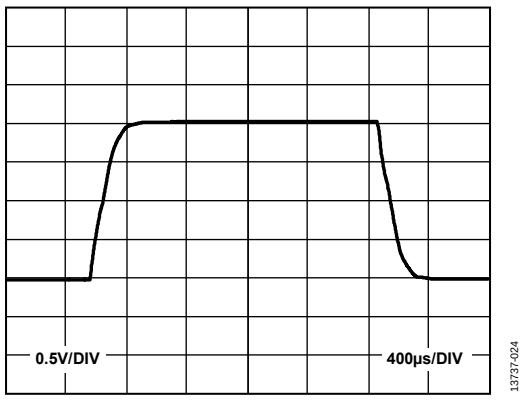

Figure 24. Large Signal Transient Response

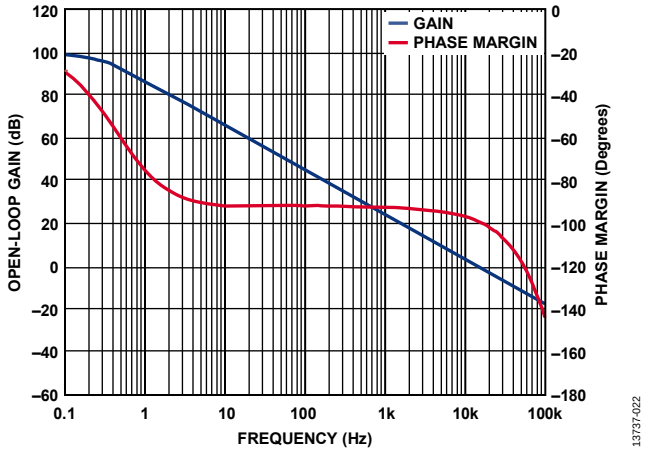

Figure 22. Open-Loop Gain and Phase Margin vs. Frequency

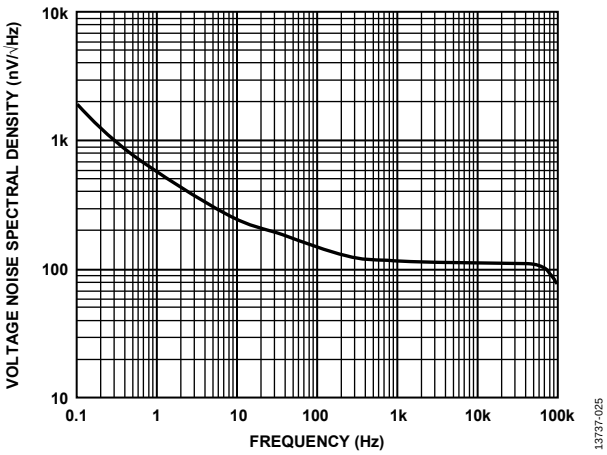

Figure 25. Voltage Noise Spectral Density vs. Frequency

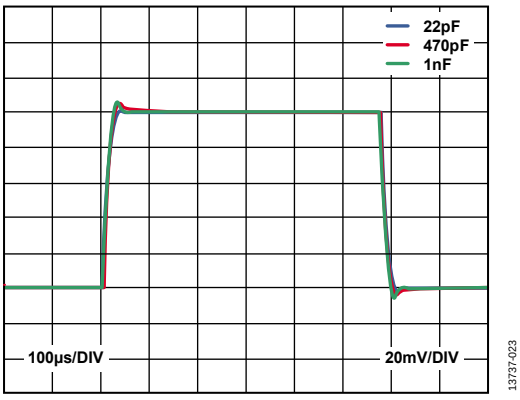

Figure 23. Small Signal Response for Various Capacitive Loads

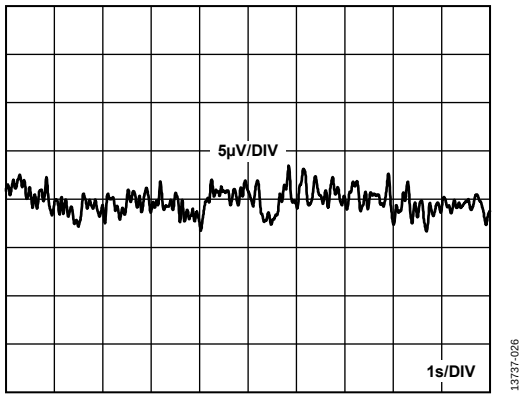

Figure 26. 0.1 Hz to 10 Hz Noise

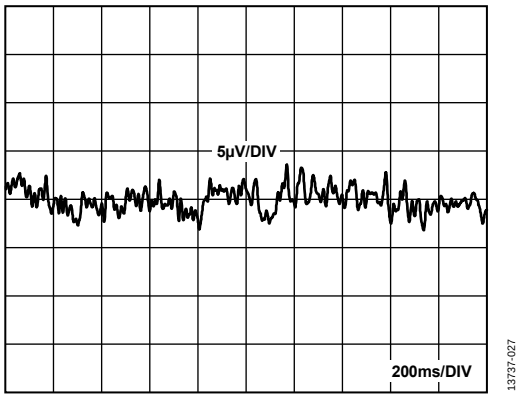

Figure 27. 0.5 Hz to 40 Hz Noise

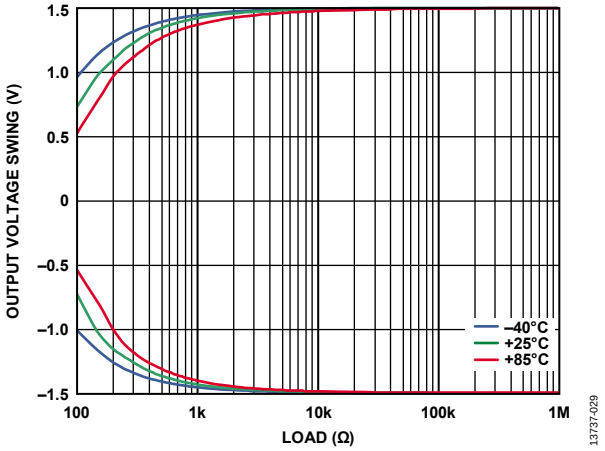

Figure 29. Output Voltage Swing vs. Load

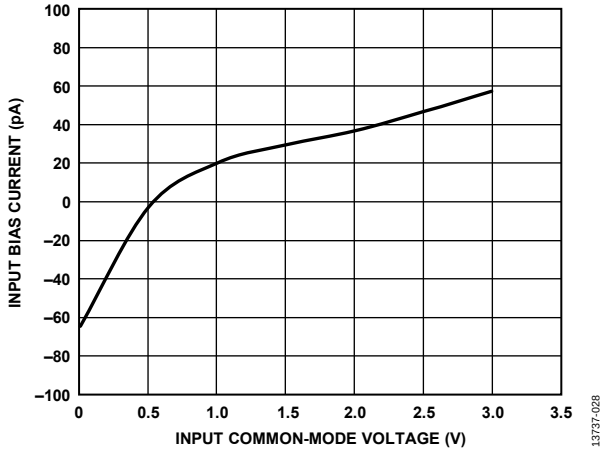

Figure 28. Input Bias Current vs. Input Common-Mode Voltage

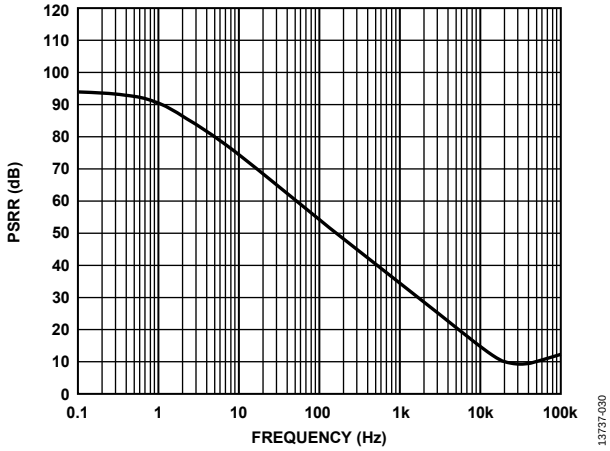

Figure 30. Power Supply Rejection Ratio

Figure 31. Load Transient Response (100 µA Load Change)

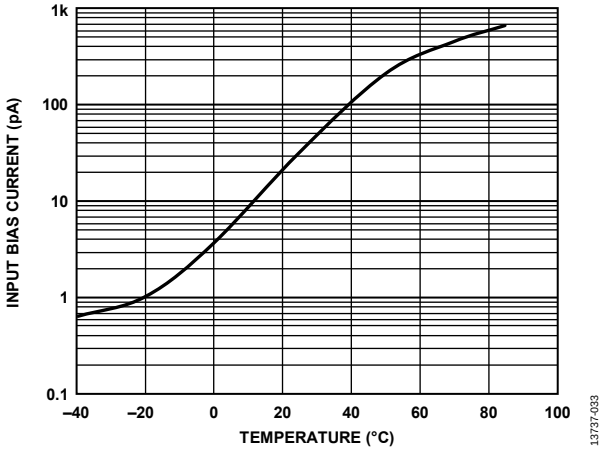

Figure 33. Input Bias Current vs. Temperature

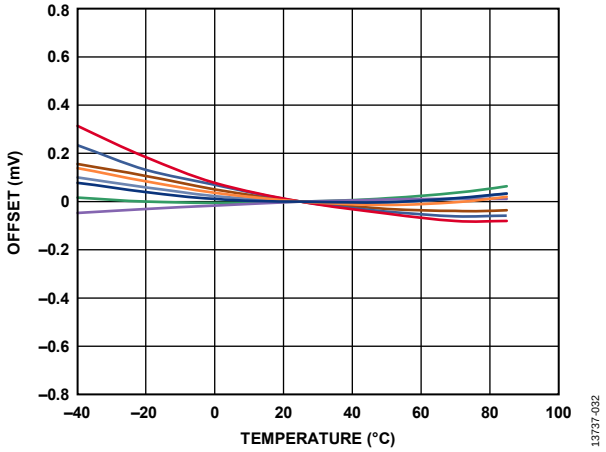

Figure 32. Offset vs. Temperature

RIGHT LEG DRIVE (RLD) AMPLIFIER PERFORMANCE CHARACTERISTICS

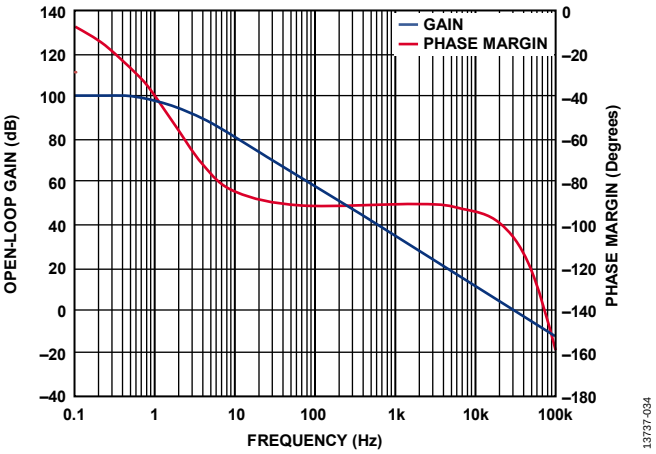

Figure 34. Open-Loop Gain and Phase Margin vs. Frequency

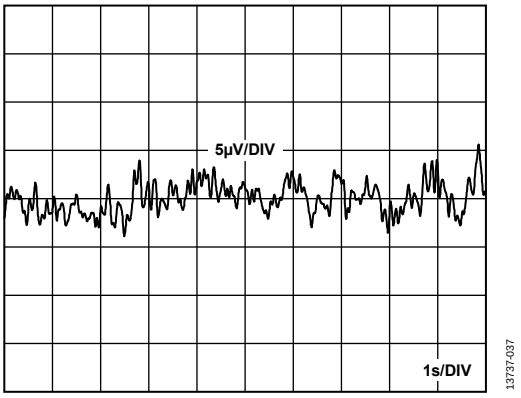

Figure 37. 0.1 Hz to 10 Hz Noise

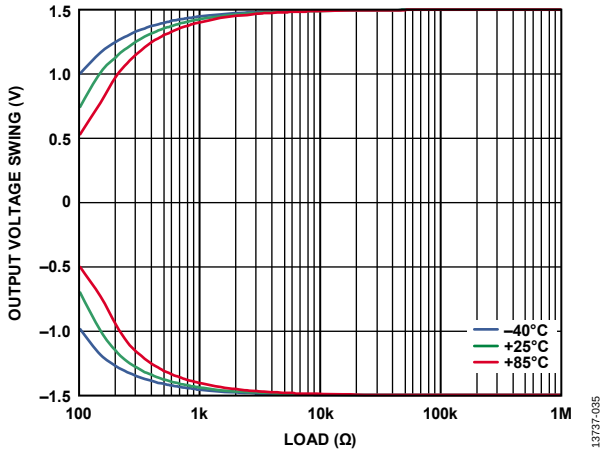

Figure 35. Output Voltage Swing vs. Load

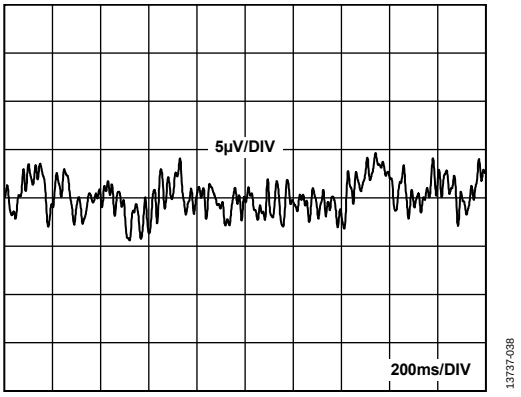

Figure 38. 0.5 Hz to 40 Hz Noise

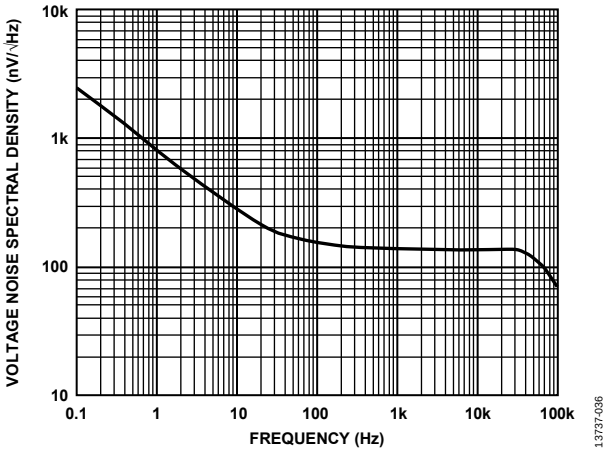

Figure 36. Voltage Spectral Noise Density vs. Frequency

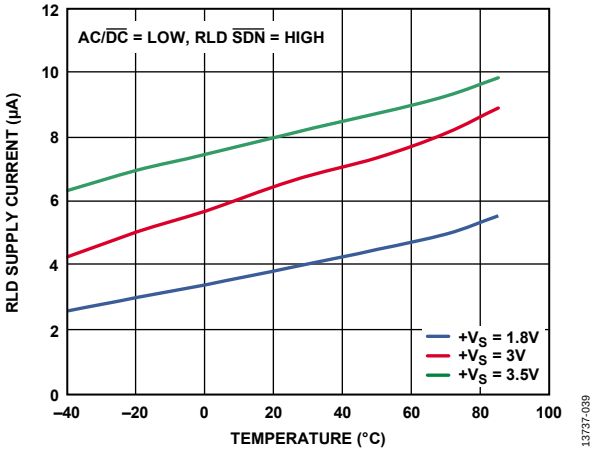

Figure 39. RLD Supply Current vs. Temperature

REFERENCE BUFFER PERFORMANCE CHARACTERISTICS

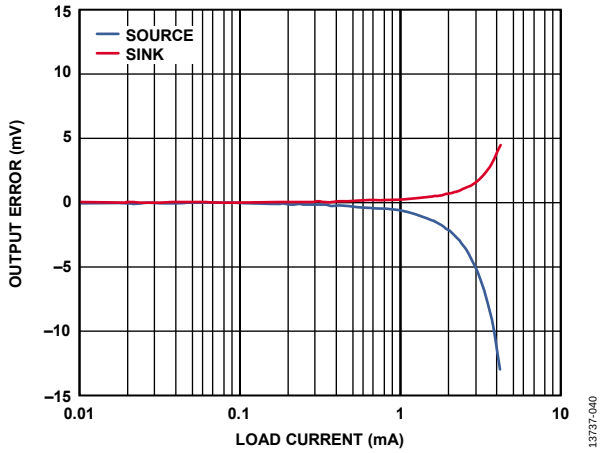

Figure 40. Load Regulation

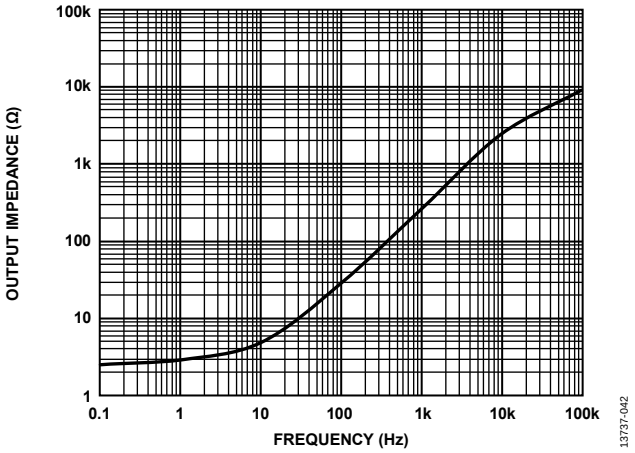

Figure 42. Output Impedance vs. Frequency

Figure 41. Load Transient Response (100 µA Load Change)

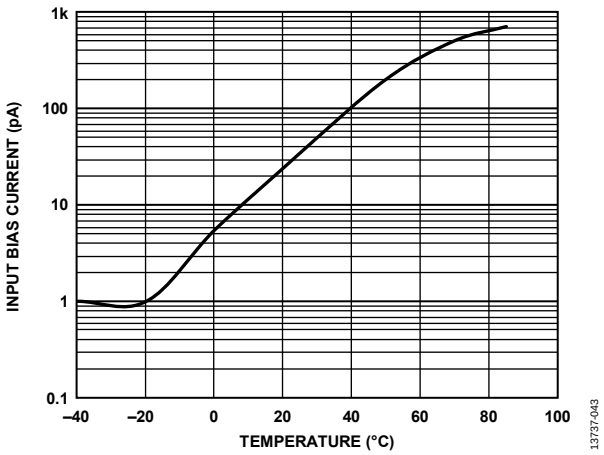

Figure 43. Input Bias Current vs. Temperature

SYSTEM PERFORMANCE CHARACTERISTICS

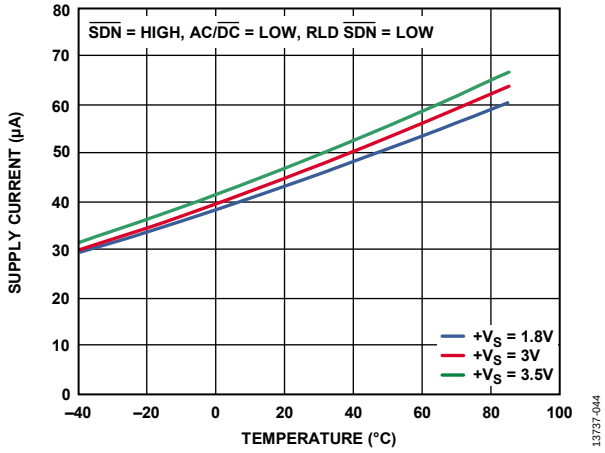

Figure 44. Supply Current vs. Temperature

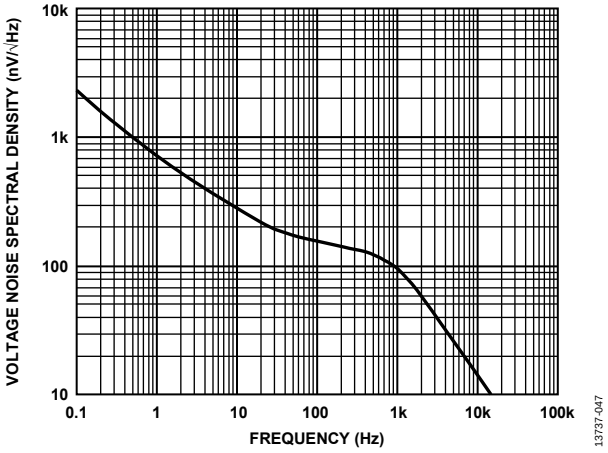

Figure 47. Voltage Noise Spectral Density (RTI) (Measured at IAOUT)

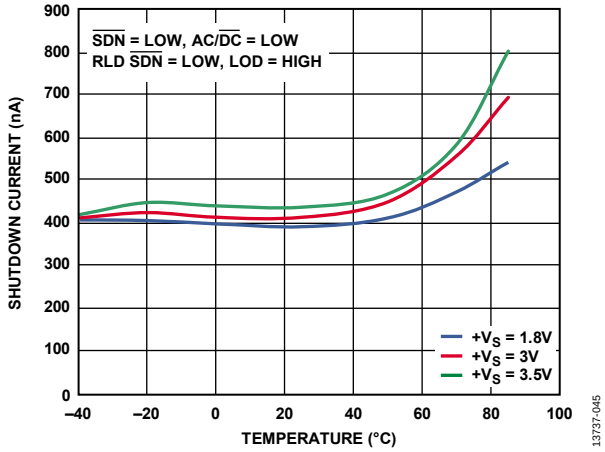

Figure 45. Shutdown Current vs. Temperature

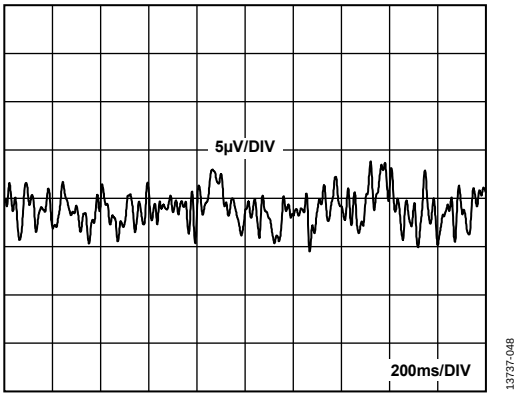

Figure 48. 0.5 Hz to 40 Hz Noise (RTI) (Measured at IAOUT)

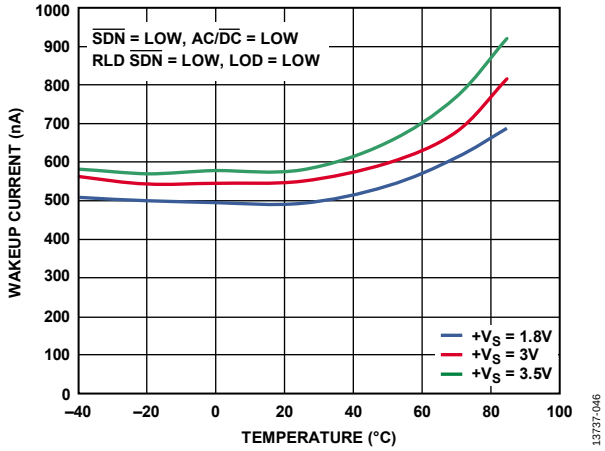

Figure 46. Wakeup Current vs. Temperature

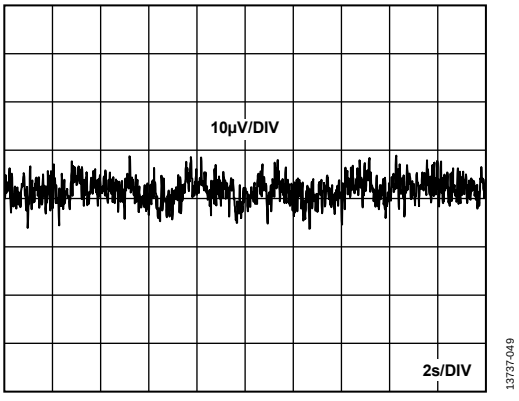

Figure 49. 0.05 Hz to 150 Hz Noise (RTI) (Measured at IAOUT)

THEORY OF OPERATION

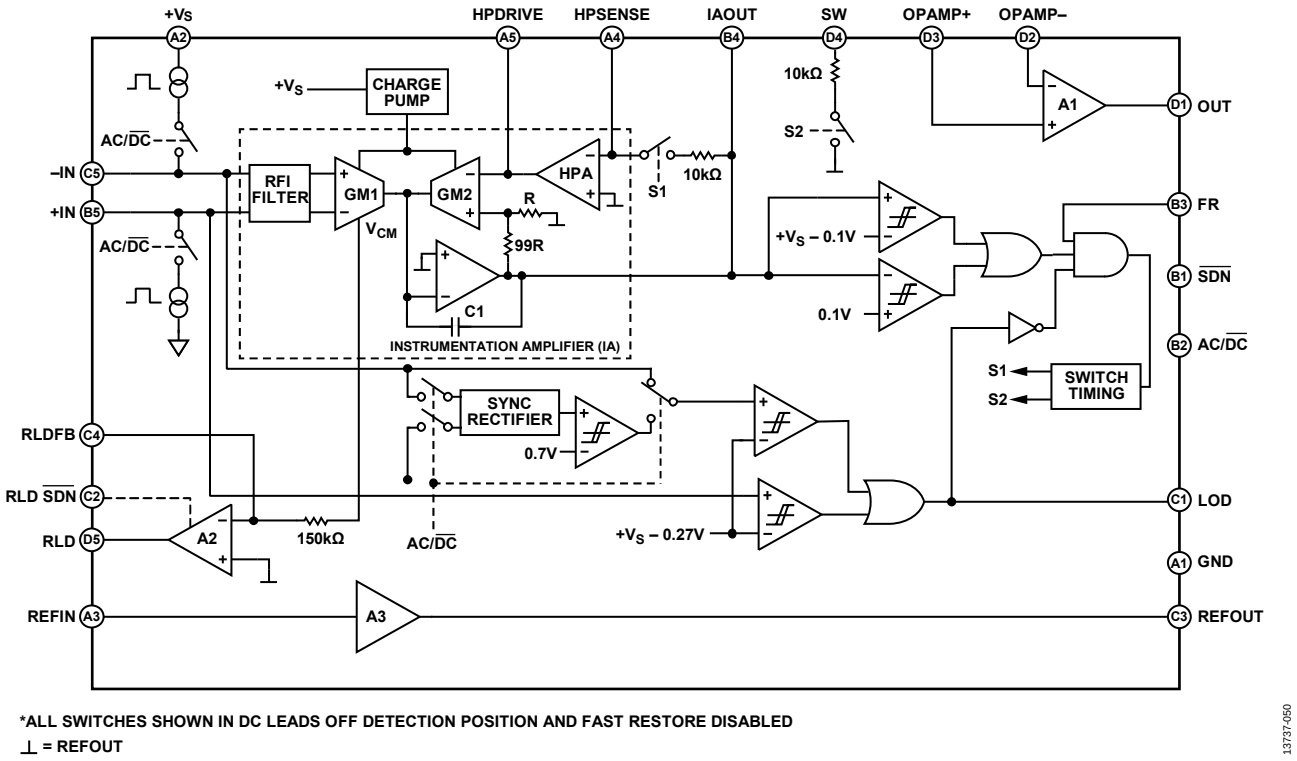

Figure 50. Simplified Schematic Diagram

ARCHITECTURE OVERVIEW

The AD8233 is an integrated front end for signal conditioning of cardiac biopotentials for heart rate monitoring. It consists of a specialized instrumentation amplifier (IA), an operational amplifier (A1), a right leg drive amplifier (A2), and a midsupply reference buffer (A3). In addition, the AD8233 includes leads on/off detection circuitry and an automatic fast restore circuit that restores the signal shortly after leads are reconnected.

The AD8233 contains a specialized instrumentation amplifier that amplifies the ECG signal while rejecting the electrode half cell potential on the same stage. The amplification of the ECG signal and the rejection of the electrode half cell potential are possible with an indirect current feedback architecture, which reduces size and power compared with traditional implementations.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is shown in Figure 50 as comprised by two well matched transconductance amplifiers (GM1 and GM2), the dc blocking amplifier (HPA), and an integrator formed by C1 and an op amp. The transconductance amplifier, GM1, generates a current that is proportional to the voltage present at its inputs. When the feedback is satisfied, an equal voltage appears across the inputs of the transconductance amplifier, GM2, thereby matching the current generated by GM1. The difference generates an error current that is integrated across Capacitor C1. The resulting voltage appears at the output of the instrumentation amplifier.

The feedback of the amplifier is applied via GM2 through two separate paths: the two resistors divide the output signal to set an overall gain of 100, whereas the dc blocking amplifier integrates any deviation from the reference level. Consequently, dc offsets as large as ±300 mV across the GM1 inputs appear inverted and with the same magnitude across the inputs of GM2, all without saturating the signal of interest.

To increase the common-mode voltage range of the instrumentation amplifier, a charge pump boosts the supply voltage for the two transconductance amplifiers. This boost in supply voltage further prevents saturation of the amplifier in the presence of large common-mode signals, such as line interference. The charge pump runs from an internal oscillator, the frequency of which is set around 500 kHz.

OPERATIONAL AMPLIFIER

The general-purpose operational amplifier (A1) is a rail-to-rail device that can be used for low-pass filtering and to add additional gain. The following sections provide details and example circuits that use this amplifier.

RIGHT LEG DRIVE AMPLIFIER

The right leg drive (RLD) amplifier inverts the common-mode signal that is present at the instrumentation amplifier inputs. When the right leg drive output current is injected into the subject, it counteracts common-mode voltage variations, thus improving the common-mode rejection of the system.

The common-mode signal that is present across the inputs of the instrumentation amplifier is derived from the transconductance amplifier, GM1. It is then connected to the inverting input of A2 through a 150 kΩ resistor.

An integrator can be built by connecting a capacitor between the RLD FB and RLD terminals. A good starting point is a 1 nF capacitor, which places the crossover frequency at about 1 kHz (the frequency at which the amplifier has an inverting unity gain). This configuration results in about 26 dB of loop gain available at a frequency range from 50 Hz to 60 Hz for common-mode line rejection. Higher capacitor values reduce the crossover frequency, thereby reducing the gain that is available for rejection and, consequently, increasing the line noise. Lower capacitor values move the crossover frequency to higher frequencies, allowing increased gain. The tradeoff is that with higher gain, the system can become unstable and saturate the output of the right leg amplifier.

When using this amplifier to drive an electrode, place a resistor in series with the output to limit the current to be always less than 10 µA, even in fault conditions. For example, if the supply used is 3.0 V, ensure that the resistor is greater than 330 kΩ to account for component and supply variations.

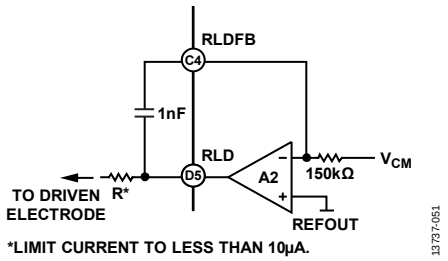

Figure 51. Typical Configuration of Right-Leg Drive Circuit

In two electrode configurations, A2 can be shut down by setting RLD $\overline{\text{SDN}}$ low for additional power savings. If left in shutdown, it is recommended to leave both RLD and RLDFB floating. Alternatively, RLD can be used to bias the inputs through 10 MΩ resistors as described in the Leads On/Off Detection section. When the AD8233 is in shutdown and dc leads off detection mode, RLD pulls down towards ground. This pull-down acts as an LOD wake-up function, pulling the inputs down when the electrodes are reconnected.

REFERENCE BUFFER

The AD8233 operates from a single supply. To simplify the design of single-supply applications, the AD8233 includes a reference buffer to create a virtual ground between the supply voltage and the system ground. The signals present at the output of the instrumentation amplifier are referenced around this voltage. For example, if there is zero differential input voltage, the voltage at the output of the instrumentation amplifier is this reference voltage.

The reference voltage level is set at the REFIN pin. It can be set with a voltage divider or by driving the REFIN pin from some other point in the circuit (for example, from the ADC reference). The voltage is available at the REFOUT pin for the filtering circuits or for an ADC input.

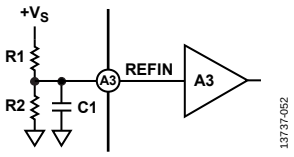

Figure 52. Setting the Internal Reference

To limit the power consumption of the voltage divider, the use of large resistors is recommended, such as 10 MΩ. The designer must keep in mind that high resistor values make it easier for interfering signals to appear at the input of the reference buffer. To minimize noise pickup, it is recommended to place the resistors close to each other and as near as possible to the REFIN terminal. Furthermore, use a capacitor in parallel with the lower resistor on the divider for additional filtering, as shown in Figure 52. Keep in mind that a large capacitor results in better noise filtering but it takes longer to settle the reference after power-up. The total time it takes the reference to settle within 1% can be estimated with the formula

$$t_{SETTLE\_REFERENCE} = 5 \times \frac{R1 \times R2 \times C1}{R1 + R2}$$

Note that disabling the AD8233 with the shutdown terminal does not discharge this capacitor.

FAST RESTORE CIRCUIT

Because of the low cutoff frequency used in high-pass filters in ECG applications, signals may require several seconds to settle. This settling time can result in a frustrating delay for the user after a step response: for example, when the electrodes are first connected.

This fast restore function is implemented internally, as shown in Figure 53. The output of the instrumentation amplifier is connected to a window comparator. The window comparator detects a saturation condition at the output of the instrumentation amplifier when its voltage approaches 0.1 V from either supply rail.

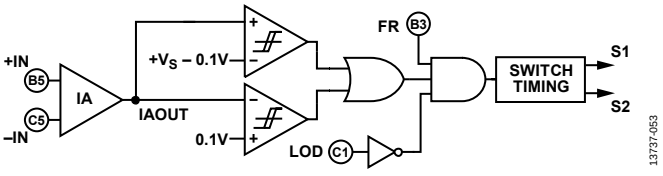

Figure 53. Fast Restore Circuit

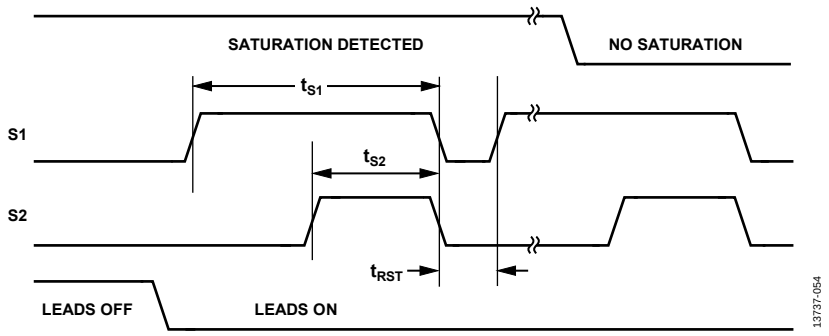

Figure 54. Timing Diagram for Fast Restore Switches (Time Base Not to Scale)

If this saturation condition is present when both input electrodes are attached to the subject, the comparator triggers a timing circuit that automatically closes Switch S1 and Switch S2 (see Figure 54 for a timing diagram).

These two switches (S1 and S2) enable two different 10 kΩ resistor paths: one between HPSENSE and IAOUT and another between SW and REFOUT. During the time Switch S1 and Switch S2 are enabled, these internal resistors appear in parallel with their corresponding external resistors forming high-pass filters. The result is that the equivalent lower resistance shifts the pole to a higher frequency, delivering a quicker settling time. Note that the fast restore settling time depends on how quickly the internal 10 kΩ resistors of the AD8233 can drain the capacitors in the high-pass circuit. Smaller capacitor values result in a shorter settling time.

If, by the end of the timing, the saturation condition persists, the cycle repeats. Otherwise, the AD8233 returns to its normal operation. If either of the leads off comparator outputs is indicating that an electrode is disconnected, the timing circuit is prevented from triggering because it is assumed that no valid signal is present. To disable fast restore, drive the FR pin low or tie it permanently to GND.

LEADS ON/OFF DETECTION

The AD8233 includes leads off detection. It features ac and dc detection modes that both work with two and three electrode configurations. Ultralow power comparators allow the leads on/off detection to remain functional in shutdown mode, allowing power savings at the system level when the LOD output is used as a wake-up signal for the microcontroller.

DC Leads On/Off Detection

The dc leads off detection mode can be used in two or three electrode configurations. It works by sensing when either instrumentation amplifier input voltage is within 0.27 V from the positive rail. The lowest power use case for the AD8233 is two electrode dc mode. A pull-up resistor on +IN and a pull-down resistor on −IN creates a voltage divider when the electrodes are connected, setting the input common mode to midsupply. When the electrodes disconnect, the comparator monitoring +IN sets LOD high when the input pulls to +V_S.

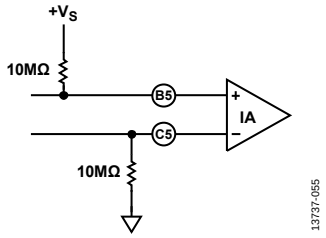

Figure 55. Circuit Configuration for Two Electrode DC Leads Off Detection

For three electrode dc mode, each input must have a pull-up resistor connected to the positive supply. During normal operation, the potential of the subject must be inside the common-mode range of the instrumentation amplifier, which is only possible if a third electrode is connected to the output of the right leg drive amplifier.

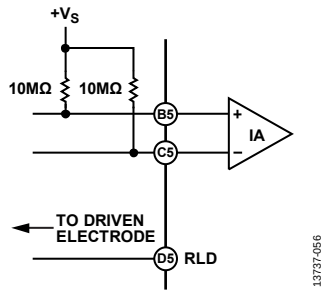

Figure 56. Circuit Configuration for Three Electrode DC Leads Off Detection

The AD8233 indicates when any electrode is disconnected by setting the LOD pin high. To use this mode, connect the AC/$\overline{DC}$ pin to ground.

AC Leads On/Off Detection

The ac leads off detection mode is useful when using two electrodes. In this case, a conduction path must exist between the two electrodes, which is usually formed by two resistors, as shown in Figure 57.

These resistors also provide a path for bias return on each input. Connect each resistor to REFOUT or RLD to maintain the inputs within the common-mode range of the instrumentation amplifier.

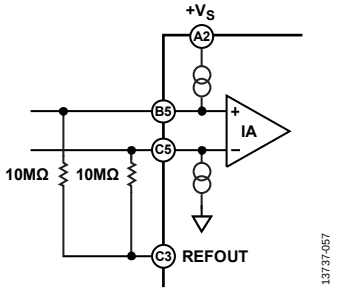

Figure 57. Circuit Configuration for Two Electrode AC Leads Off Detection

The AD8233 detects when an electrode is disconnected by forcing a small 100 kHz current into the input terminals. This current flows through the external resistors from IN+ to IN− and develops a differential voltage across the inputs, which is then synchronously detected and compared to an internal threshold. The recommended value for these external resistors is 10 MΩ. Low resistance values make the differential drop too low to be detected and lower the input impedance of the amplifier. When the electrodes are attached to the subject, the impedance of this path must be less than 3 MΩ to maintain the drop below the threshold of the comparator.

To use the ac leads off mode, tie the AC/$\overline{DC}$ pin to the positive supply rail. Note that, whereas REFOUT is at a constant voltage value, using the RLD output as the input bias may be more effective in rejecting common-mode interference at the expense of additional power.

In three electrode ac leads off detection mode, as shown in Figure 58, pull-up resistors are not required, which improves the input impedance of the circuit. This mode is beneficial for dry electrode applications. The ac mode currents contribute 1/f noise to the system; therefore, depending on the application, it may be advantageous to use ac leads off detection as a spot check and then switching to dc mode for improved ECG acquisition.

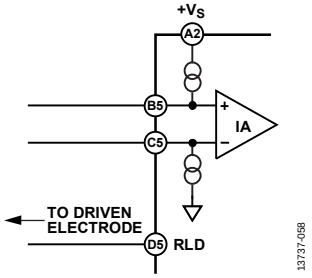

Figure 58. Circuit Configuration for Three Electrode AC Leads Off Detection

The ac leads off detection mode continues to function in shutdown mode as well. To keep the power under 1 µA, the clock is disabled and the ac currents become dc currents. The current source on +IN is 250 nA, while the current sink on −IN is −300 nA. The stronger pull-down current on −IN acts as a wake-up function, pulling LOD low when the electrodes are reconnected.

STANDBY OPERATION

The AD8233 includes a shutdown pin ($\overline{SDN}$) that further enhances the flexibility and ease of use in portable applications where power consumption is critical. A logic level signal can be applied to this pin to switch to shutdown mode, even when the supply is still on.

Driving the $\overline{SDN}$ pin low places the AD8233 in shutdown mode and draws less than 1 µA of supply current, offering considerable power savings. To enter normal operation, drive $\overline{SDN}$ high; when not using this feature, permanently tie $\overline{SDN}$ to $+V_S$.

During shutdown operation, the AD8233 cannot maintain the REFOUT voltage, but it does not drain the REFIN voltage, thereby maintaining this additional conduction path from the supply to ground.

When emerging from a shutdown condition, the charge stored in the capacitors on the high-pass filters can saturate the instrumentation amplifier and subsequent stages. The use of the fast restore feature helps reduce the recovery time and, therefore, minimize on time in power sensitive applications.

Using leads on/off detection in shutdown mode allows system level power saving. The microcontroller enters sleep mode when the electrodes are disconnected, and the LOD signal acts as an interrupt to wake up the microcontroller. An example of this functionality is shown in Figure 59.

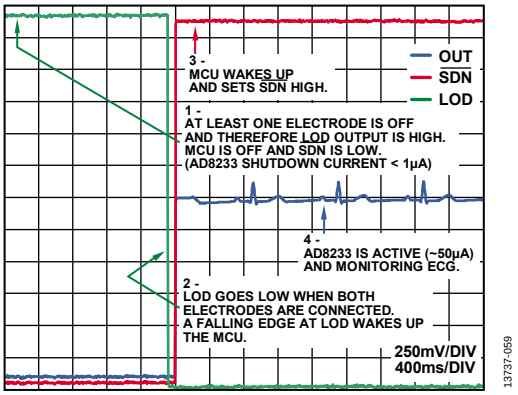

Figure 59. Electrode Connection and System Wakeup Sequence

INPUT PROTECTION

All terminals of the AD8233 are protected against ESD. In addition, the input structure allows dc overload conditions that are a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, use an external resistor in series with each of the inputs to limit current for voltages beyond the supplies. In either scenario, the AD8233 safely handles a continuous 5 mA current at room temperature.

For applications where the AD8233 encounters extreme overload voltages, such as in cardiac defibrillators, use external series resistors and gas discharge tubes (GDT). Neon lamps are commonly used as an inexpensive alternative to GDTs. These devices can handle the application of large voltages but do not maintain the voltage below the absolute maximum ratings for the AD8233. A complete solution includes further clamping to either supply using additional resistors and low leakage diode clamps, such as BAV199 or FJH1100.

As a safety measure, place a resistor between the input pin and the electrode that is connected to the subject to ensure that the current flow never exceeds 10 µA. Calculate the value of this resistor to be equal to the supply voltage across the AD8233 divided by 10 µA.

RADIO FREQUENCY INTERFERENCE (RFI)

Radio frequency (RF) rectification is often a problem in applications where there are large RF signals. The problem appears as a dc offset voltage at the output. The AD8233 has a 15 pF gate capacitance and 10 kΩ resistors at each input. This forms a low-pass filter on each input that reduces rectification at high frequency (see Figure 60) without the addition of external elements.

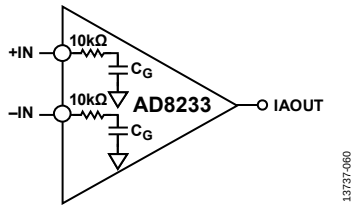

Figure 60. RFI Filter Without External Capacitors

For increased filtering, additional resistors can be added in series with each input. They must be placed as close as possible to the instrumentation amplifier inputs. These can be the same resistors used for overload and patient protection.

POWER SUPPLY REGULATION AND BYPASSING

The AD8233 is designed to be powered directly from a single 3 V battery, such as CR2032 type. It can also operate from rechargeable Li-Ion batteries, but the designer must take into account that the voltage during a charge cycle may exceed the absolute maximum ratings of the AD8233. To avoid damage to the device, use a power switch or a low power, low dropout regulator, such as the ADP150 or ADP160.

In addition, excessive noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the chip power supplies. Place a 0.1 µF capacitor close to the supply pin. A 1 µF capacitor can be used farther away from the device. In most cases, the capacitor can be shared by other integrated circuits. Keep in mind that excessive decoupling capacitance increases power dissipation during power cycling.

INPUT REFERRED OFFSETS

Because of its internal architecture, the instrumentation amplifier must be used always with the dc blocking amplifier, shown as HPA in Figure 50.

As described in the Theory of Operation section, the dc blocking amplifier attenuates the input referred offsets present at the inputs of the instrumentation amplifier; however, this is true only when the dc blocking amplifier is used as an integrator. In this configuration, the input offsets from the dc blocking amplifier dominate appearing directly at the output of the instrumentation amplifier.

If the dc blocking amplifier is used as a follower instead of its intended function as an integrator, the input referred offsets of the in-amp are amplified by a factor of 100.

LAYOUT RECOMMENDATIONS

It is important to follow good layout practices to optimize system performance. In low power applications, most resistors are of a high value to minimize additional supply current. The challenge of using high value resistors is that high impedance nodes become even more susceptible to noise pickup and board parasitics, such as capacitance and surface leakages. Keep all of the connections between high impedance nodes as short as possible to avoid introducing additional noise and errors from corrupting the signal.

To maintain high CMRR over frequency, keep the input traces symmetrical and length matched. Place safety and input bias resistors in the same position relative to each input. In addition, the use of a ground plane significantly improves the noise rejection of the system.

For WLCSP layout best practices, refer to the AN-617 Application Note.

APPLICATIONS INFORMATION

ELIMINATING ELECTRODE OFFSETS

The instrumentation amplifier in the AD8233 is designed to apply gain and to filter out near dc signals simultaneously. This capability allows the device to amplify a small ECG signal by a factor of 100 while rejecting electrode offsets as large as ±300 mV.

To achieve offset rejection, connect an RC network between the output of the instrumentation amplifier, HPSENSE, and HPDRIVE, as shown in Figure 61.

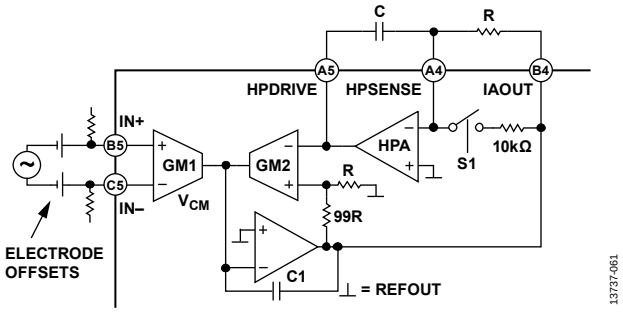

Figure 61. Eliminating Electrode Offsets

This RC network forms an integrator that feeds any near dc signals back into the instrumentation amplifier, thus eliminating the offsets without saturating any node and maintaining high signal gain.

In addition to blocking offsets present across the inputs of the instrumentation amplifier, this integrator also works as a high-pass filter that minimizes the effect of slow moving signals, such as baseline wander. The cutoff frequency of the filter is given by the following equation:

$$f_C = \frac{100}{2\pi RC} \quad (1)$$

where R is in Ω and C is in farads.

Note that the filter cutoff is 100 times higher than is typically expected from a single-pole filter. Because of the feedback architecture of the instrumentation amplifier, the typical filter cutoff equation is modified by a gain of 100 from the instrumentation amplifier.

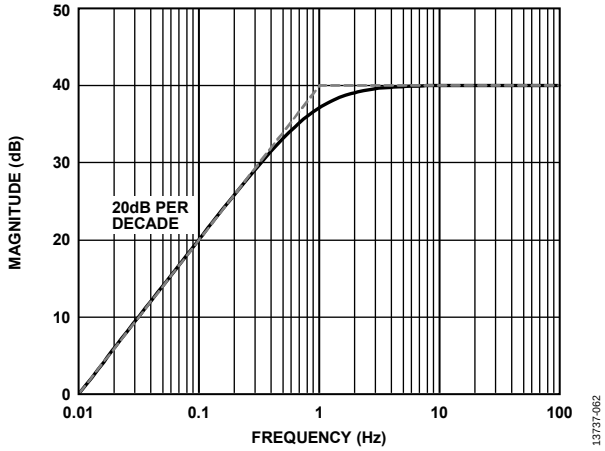

Figure 62. Frequency Response of a Single-Pole DC Blocking Circuit

As with any high-pass filter with low frequency cutoff, a fast change in dc offset requires a long time to settle. If such a change saturates the instrumentation amplifier output, the S1 switch briefly enables the 10 kΩ resistor path, thus moving the cutoff frequency to

$$f_C = \frac{100(R + 10^4)}{2\pi RC(10^4)} \quad (2)$$

For values of R greater than 100 kΩ, the expression in Equation 2 can be approximated by

$$f_C = \frac{1}{200\,\pi C} \quad (3)$$

This higher cutoff frequency reduces the settling time and enables faster recovery of the ECG signal. For more information, see the Fast Restore Circuit section.

HIGH-PASS FILTERING

The AD8233 can implement higher order high-pass filters. A higher filter order yields better artifact rejection at the cost of increased signal distortion and more passive components on the PCB.

Two-Pole High-Pass Filter

A two-pole architecture can be implemented by adding a simple ac coupling RC at the output of the instrumentation amplifier, as shown in Figure 63.

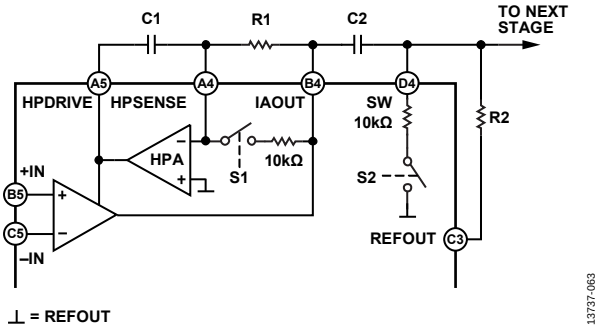

Figure 63. Schematic for a Two-Pole High-Pass Filter

Note that the right side of C2 connects to the SW terminal. As with S1, S2 reduces the recovery time for this ac coupling network by placing 10 kΩ in parallel with R2. See the Fast Restore Circuit section for additional details on switch timing and trigger conditions.

Note that, if this passive network is not buffered, it exhibits higher output impedance at the input of a subsequent low-pass filter, such as with Sallen-Key filter topologies. Careful component selection results in reliable performance without a buffer. See the Low-Pass Filtering and Gain section for additional information on component selection.

Additional High-Pass Filtering Options

In addition to the topologies explained in the previous sections, an additional pole may be added to the dc blocking circuit for the rejection of low frequency signals. This configuration is shown in Figure 64.

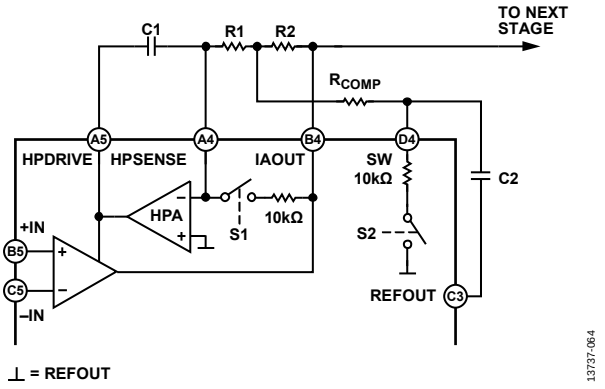

Figure 64. Schematic for an Alternative Two-Pole, High-Pass Filter

An extra benefit of this circuit topology is that it allows a lower cutoff frequency with lower R and C values. The resistor, R_{COMP}, can also be used to control the quality factor (Q) of the filter to achieve narrow band-pass filters (for heart rate detection) or maximum pass-band flatness (for cardiac monitoring).

With this circuit topology, the filter attenuation reverts to a single-pole roll-off at very low frequencies. Because the initial roll-off is 40 dB per decade, this reversion to 20 dB per decade has little impact on the ability of the filter to reject out of band low frequency signals.

The designer may choose different values to achieve the desired filter performance. To simplify the design process, use the following recommendations as a starting point for component value selection.

$$R1 = R2 \geq 100\ \text{k}\Omega$$

$$C1 = C2$$

$$R_{COMP} = 0.14 \times R1$$

The cutoff frequency is located at

$$f_C = \frac{10}{2\pi\sqrt{R1 \times C1 \times R2 \times C2}}$$

The selection of R_{COMP} to be 0.14 times the value of the other two resistors optimizes the filter for a maximally flat pass band. Reduce the value of R_{COMP} to increase the Q and, consequently, the peaking of the filter. Note that a very low R_{COMP} value may result in an unstable circuit. The selection of values based on these criteria results in a transfer function similar to what is shown in Figure 65. When additional low frequency rejection is desired, a high-order, high-pass filter can be implemented by adding an ac coupling network at the output of the instrumentation amplifier, as shown in Figure 65. The SW terminal is connected to the ac coupling network to obtain the best settling time response when fast restore engages.

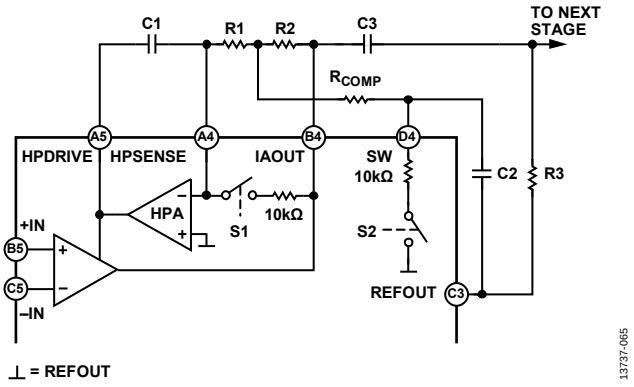

Figure 65. Schematic for a Three-Pole, High-Pass Filter

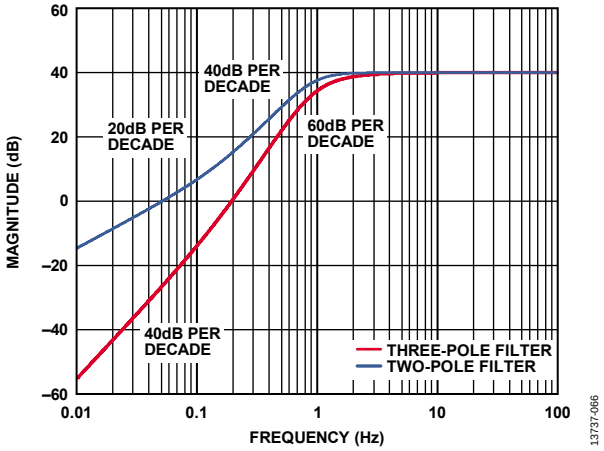

Figure 66. Frequency Response of the Circuits Shown in Figure 64 and Figure 65

Careful analysis and adjustment of all of the component values in practice is recommended to optimize the filter characteristics. To reduce the value of R_{COMP}, increase the peaking of the active filter to overcome the additional roll-off introduced by the ac coupling network. Proper adjustment yields the best pass-band flatness.

Table 6. Comparison of High-Pass Filtering Options

Figure to Reference	Filter Order	Component Count	Low Frequency Rejection	Capacitor Sizes/Values	Signal Distortion[1]	Output Impedance[2]
Figure 61	1	2	Good	Large	Low	Low
Figure 63	2	4	Better	Large	Medium	Higher
Figure 64	2	5	Better	Smaller	Medium	Low
Figure 65	3	7	Best	Smaller	Highest	Higher

[1] The signal distortion is for the equivalent corner frequency location.
[2] Output impedance refers to the drive capability of the high-pass filter before the low-pass filter. Low output impedance is desirable to allow flexibility in the selection of values for a low-pass filter, as explained in the Low-Pass Filtering and Gain section.

The design of the high-pass filter involves trade-offs between signal distortion, component count, low frequency rejection, and component size. For example, a single-pole, high-pass filter results in the least distortion to the signal, but the associated rejection of low frequency artifacts is the lowest of the available filter options. Table 6 compares the recommended filtering options.

LOW-PASS FILTERING AND GAIN

The AD8233 includes an uncommitted op amp that can be used for extra gain and filtering. For applications that do not require a high order filter, a simple RC low-pass filter is sufficient, and the op amp can buffer or further amplify the signal.

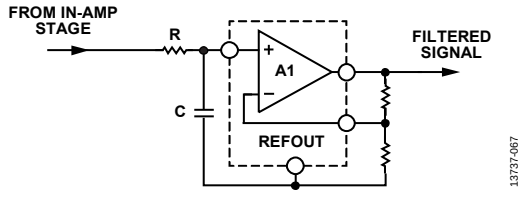

Figure 67. Schematic for a Single-Pole, Low-Pass Filter and Additional Gain

A Sallen-Key filter topology can be implemented for applications that require a steeper roll-off or a sharper cutoff frequency, as shown in Figure 68.

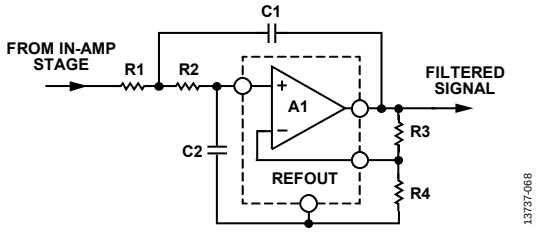

Figure 68. Schematic for a Two-Pole, Low-Pass Filter

The following equations describe the low-pass cutoff frequency (f_C), gain, and Q:

$$f_C = 1/(2\pi\sqrt{(R1 \times C1 \times R2 \times C2)})$$

$$Gain = 1 + R3/R4$$

$$Q = \frac{\sqrt{R1 \times C1 \times R2 \times C2}}{R1 \times C2 \times R2 \times C2 + R1 \times C1(1 - Gain)}$$

Note that changing the gain has an effect on Q and vice versa. Common values for Q are 0.5, to avoid peaking, or 0.7 for maximum flatness and a sharp cutoff frequency. Use a high Q value in narrow-band applications to increase peaking and the selectivity of the band-pass filter.

A common design procedure is to set R1 = R2 = R and C1 = C2 = C, simplifying the expressions for the cutoff frequency and Q to

$$f_C = 1/(2\pi RC)$$

$$Q = \frac{1}{3 - Gain}$$

Note that Q can be controlled by setting the gain with R3 and R4; however, this limits the gain to be less than 3. For gain values equal to or greater than 3, the circuit becomes unstable. A simple modification that allows higher gains is to make the value of C2 at least four times larger than C1.

Note that these design equations only hold true in a case where the output impedance of the previous stage is much lower than the input impedance of the Sallen-Key filter. The design equations do not hold true when using an ac coupling network between the instrumentation amplifier output and the input of the low-pass filter without a buffer.

To connect these two filtering stages properly without a buffer, make the value of R1 at least 10 times larger than the resistor of the ac coupling network (labeled as R2 in Figure 63).

Driving ADCs

The ability of AD8233 to drive capacitive loads makes it ideal for driving an ADC without an additional buffer. However, depending on the input architecture of the ADC, a simple, low-pass RC network may be required to decouple the transients from the switched capacitor input typical of modern ADCs. This RC network also acts as an additional filter that can help reduce noise and aliasing. Follow the recommended guidelines from the ADC data sheet for the selection of proper R and C values. Table 7 lists compatible ADCs by category.

Table 7. Compatible ADCs by Category

Analog-to-Digital Converters	Microcontrollers	Optical Sensors	Accelerometers
AD7091	ADuCM350	ADPD103	ADXL363
AD7988-1		ADPD105	

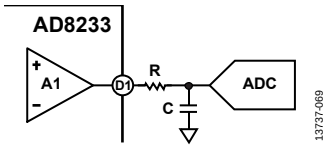

Figure 69. Driving an ADC

DRIVEN ELECTRODE

A driven lead (or reference electrode) is often used to minimize the effects of common-mode voltages induced by the power line and other interfering sources. The AD8233 extracts the common-mode voltage from the instrumentation amplifier inputs and makes it available through the RLD amplifier to drive an opposing signal into the patient. This functionality maintains the voltage between the patient and the AD8233 at a near constant, greatly improving the CMRR.

As a safety measure, place a resistor between the RLD pin (Pin D5) and the electrode connected to the subject to ensure that current flow never exceeds 10 μA. Calculate the value of this resistor to be equal to the supply voltage across the AD8233 divided by 10 μA.

The AD8233 implements an integrator formed by an internal 150 kΩ resistor and an external capacitor to drive this electrode. The choice of the integrator capacitor is a trade-off between line rejection capability and stability. It is recommended that the capacitor be small to maintain as much loop gain as possible, around 50 Hz and 60 Hz, which is typical for line frequencies. For stability, it is recommended that the gain of the integrator be less than unity gain at the frequency of any other poles in the loop, such as those formed by the capacitance and the safety resistors of the patient. The suggested application circuits use a 1 nF capacitor, which results in a loop gain of about 20 at line frequencies, with a crossover frequency of about 1 kHz.

In a 2-lead configuration, the RLD pin (Pin D5) amplifier can be shut down or used to drive the bias current resistors on the inputs. Although not as effective as a true driven electrode, this configuration can provide some common-mode rejection improvement if the sense electrode impedance is small and well matched.

APPLICATION CIRCUITS

HEART RATE MEASUREMENT (HRM) NEXT TO THE HEART

For wearable exercise devices, the AD8233 is typically placed in a pod near the heart. The two sense electrodes are placed under the pectoral muscles; no driven electrode is used. Because the distance from the heart to the AD8233 is small, the heart signal is strong and there is less muscle artifact interference.

In this wearable device configuration, space is at a premium. By using as few external components as possible, the circuit in Figure 70 is optimized for size.

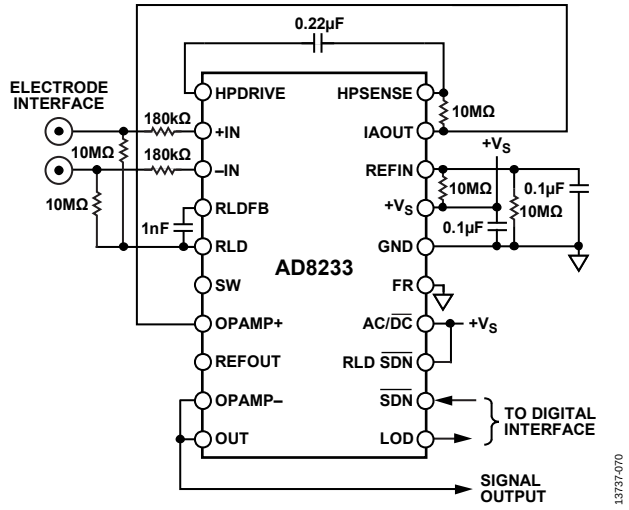

Figure 70. Circuit for HRM Next to the Heart

A shorter distance from the AD8233 to the heart makes this application less vulnerable to common-mode interference. However, because RLD (Pin D5) is not used to drive an electrode, it can be used to improve the common-mode rejection by maintaining the midscale voltage through the 10 MΩ bias resistors. Alternatively, tie RLD $\overline{\text{SDN}}$ low to save power, and tie the bias resistors to REFOUT.

A single-pole, high-pass filter is set at 7 Hz, and there is no low-pass filter. No gain is used on the output op amp, thereby reducing the number of resistors for a total system gain of 100. (see Figure 71).

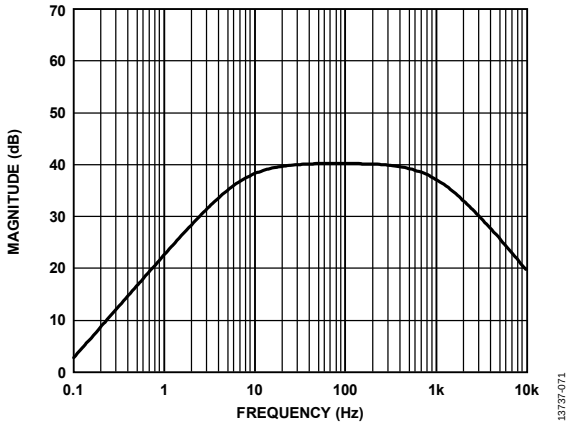

Figure 71. Frequency Response for HRM Next to the Heart Circuit

The input terminals in this configuration use two 180 kΩ resistors to protect the user from fault conditions. Two 10 MΩ resistors provide input bias. Use higher values for electrodes with high output impedance, such as cloth electrodes.

The schematic also shows two 10 MΩ resistors to set the midscale reference voltage. If there is already a reference voltage available, it can be driven into the REFIN input to eliminate these two 10 MΩ resistors.

EXERCISE APPLICATION—HEART RATE MEASURED AT THE HANDS

In this application, the heart rate signal is measured at the hands with stainless steel electrodes. The arm and upper body movement of the user create large motion artifacts, and the long lead length makes the system susceptible to common-mode interference. A very narrow band-pass characteristic is required to separate the heart signal from the interferers.

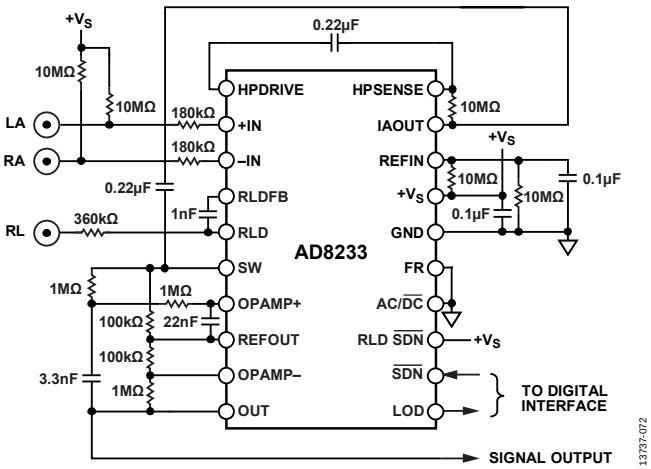

Figure 72. Circuit for HRM at Hands

The circuit in Figure 72 uses a two-pole, high-pass filter set at 7 Hz. A two-pole, low-pass filter at 24 Hz follows the high-pass filters to eliminate any other artifacts and line noise.

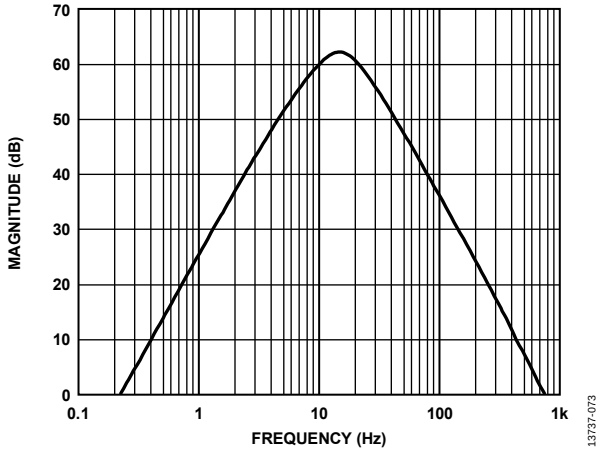

Figure 73. Frequency Response for HRM Circuit Taken at the Hands

The overall narrow-band nature of the two-pole, low-pass filter filter combination distorts the ECG waveform significantly. Therefore, it is only suitable to determine the heart rate, and not to analyze the ECG signal characteristics.

The low-pass filter stage also includes a gain of 11, bringing the total system gain close to 1100. Because the ECG signal is measured at the hands, it is weaker than when measured closer to the heart.

The RLD circuit drives to the third electrode, which can also be located at the hands, to cancel common-mode interference.

HOLTER MONITOR CONFIGURATION

The circuit in Figure 75 is designed for monitoring the shape of the ECG waveform.

To obtain an ECG waveform with minimal distortion, the AD8233 is configured with a 0.5 Hz, single-pole, high-pass filter, followed by a two-pole, 40 Hz, low-pass filter. A third electrode is driven for optimum common-mode rejection.

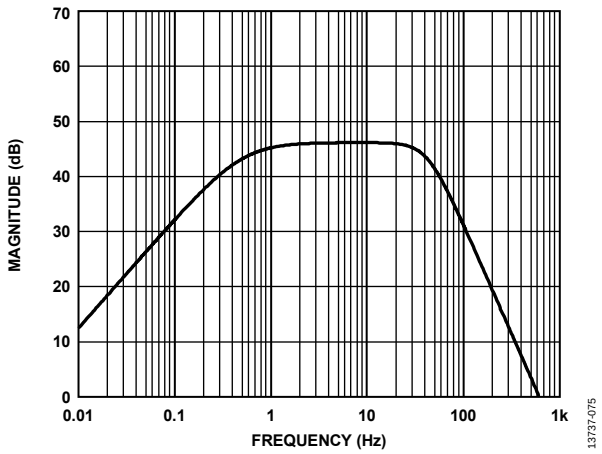

Figure 74. Frequency Response of Holter Monitor Circuit

In addition to 40 Hz filtering, the op amp stage is configured for a gain of 2, resulting in a total system gain of 200. Keeping the gain lower helps with any motion artifacts picked up in band. To optimize the dynamic range of the system, the gain level is adjustable, depending on the input signal amplitude (which may vary with electrode placement) and ADC input range.

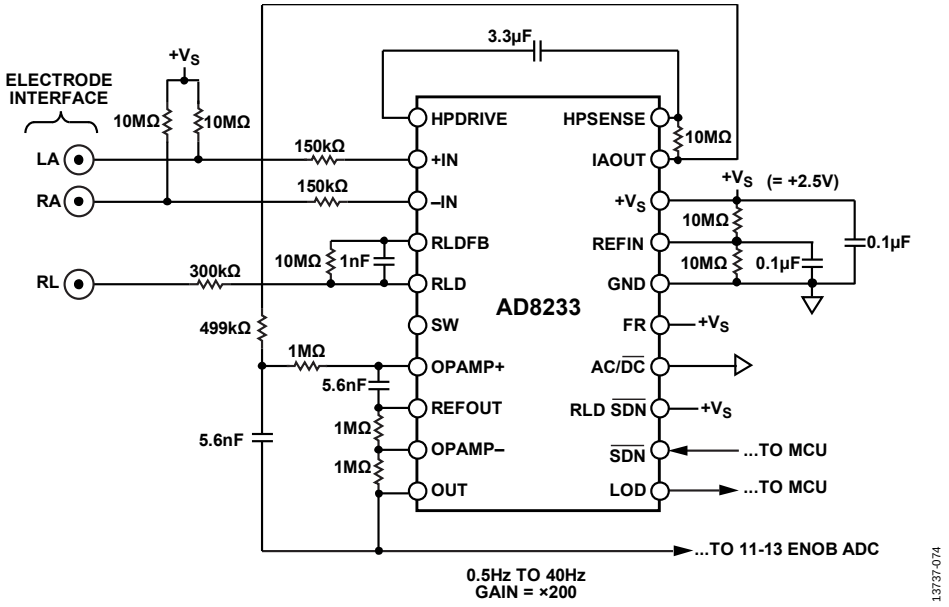

Figure 75. Holter Monitor Circuit

SYNCHRONIZED ECG AND PPG MEASUREMENT

In wearable devices developed for monitoring the health care of patients, it is often necessary to have synchronized measurements of biomedical signals. For example, a synchronous measurement of a ECG and photoplethysmograph (PPG) can be used to determine the pulse wave transit time (PWTT), which can then be used to estimate blood pressure.

The circuit shown in Figure 77 shows a synchronous ECG and PPG measurement using the AD8233 and the ADPD105 photometric front end. The AD8233 implements a two-pole, high-pass filter with a cutoff frequency of 0.3 Hz, and a two-pole, low-pass filter with a cutoff frequency of 37 Hz. The output of the AD8233 is fed to one of the current inputs of the ADPD105 through a 50 kΩ resistor to convert the voltage output of the AD8233 into a current. The PPG signal is acquired by the ADPD105, which is a complete optical transceiver with integrated LED drivers, multiple photodiode current inputs, an integrated, 14-bit, successive approximation (SAR) ADC, and a FIFO. In the circuit shown, the chip scale ADPD105 is used; the ADPD105 is a two input device. The ADPD105 is configured to alternately measure the photodiode signal and the ECG signal from the AD8233 on consecutive time slots to provide fully synchronized PPG and ECG measurements. Data can be read out of the on-chip FIFO or straight from the data registers. The ADPD105 channel that processes the ECG signal must be set up in either pulse connect mode or transimpedance amplifier (TIA) ADC mode, and the input bias voltage must be set to the 0.9 V setting. The TIA gain setting can be set to optimize the dynamic range of the signal path. The channel used to process the PPG signal is configured in its normal operating mode. Figure 76 shows a plot of a synchronized ECG and PPG measurement using the AD8233 with the ADPD105.

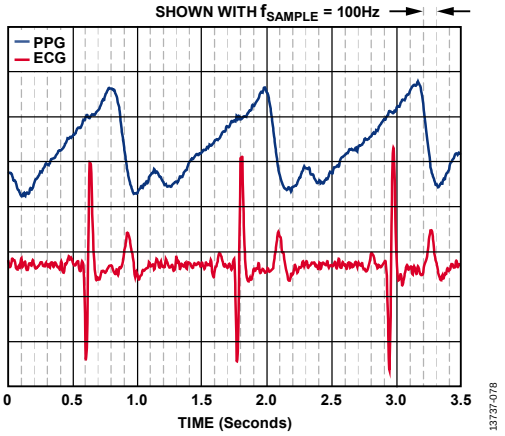

Figure 76. Synchronous ECG and PPG Measurement Using the AD8233 with the ADPD105

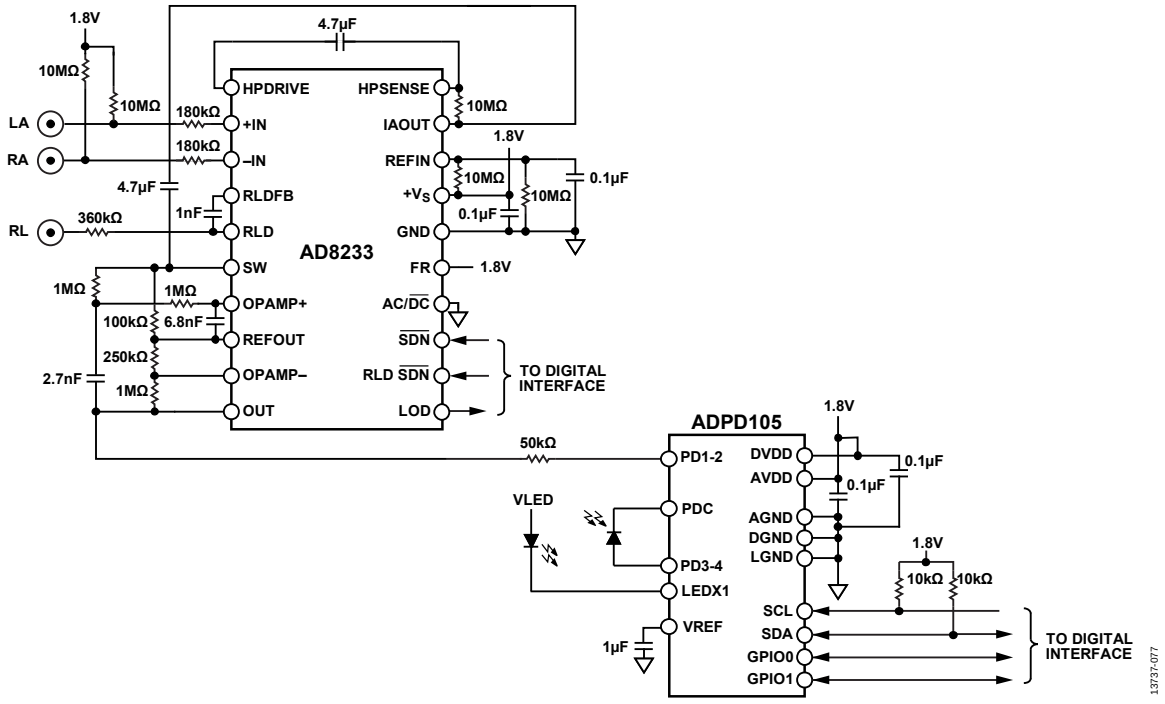

Figure 77. Synchronous ECG and PPG Measurement Circuit

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

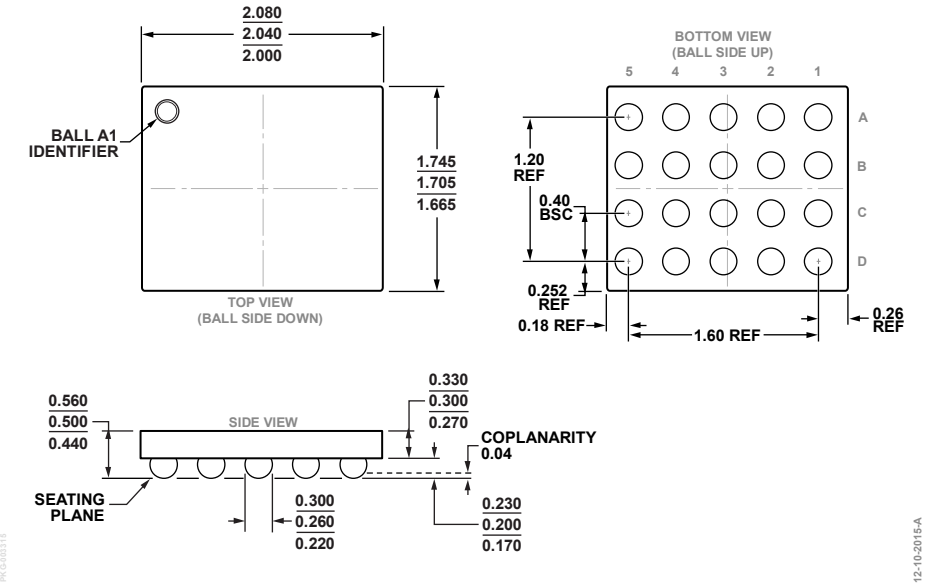

Figure 78. 20-Ball, Backside-Coated, Wafer Level Chip Scale Package [WLCSP]
(CB-20-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8233ACBZ-R7	−40°C to +85°C	20-Ball, Backside-Coated, Wafer Level Chip Scale Package [WLCSP]	CP-20-13
AD8233CB-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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