2.7 V to 5.5 V, 2.3 μs, 10-Bit ADC in 8-Lead microSOIC/DIP

AD7810

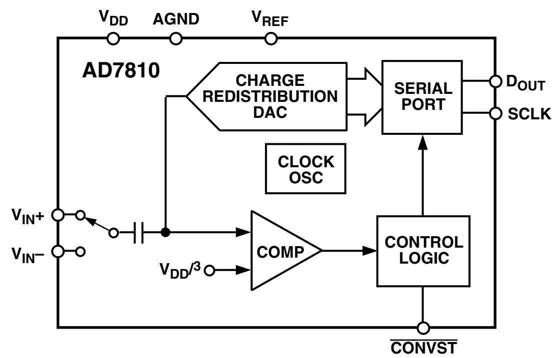
FEATURES

10-Bit ADC with 2.3 μs Conversion Time
Small Footprint 8-Lead microSOIC Package
Specified Over a –40°C to +105°C Temperature Range
Inherent Track-and-Hold Functionality
Operating Supply Range: 2.7 V to 5.5 V
Specifications at 2.7 V to 5.5 V
Microcontroller-Compatible Serial Interface
Optional Automatic Power-Down at End of Conversion
Low Power Operation
270 μW at 10 kSPS Throughput Rate
2.7 mW at 100 kSPS Throughput Rate
Analog Input Range: 0 V to V_{REF}
Reference Input Range: 0 V to V_{DD}

APPLICATIONS

Low Power, Hand-Held Portable Applications that Require Analog-to-Digital Conversion with 10-Bit Accuracy; e.g., Battery Powered Test Equipment, Battery-Powered Communications Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7810 is a high speed, low power, 10-bit A/D converter that operates from a single 2.7 V to 5.5 V supply. The part contains a 2.3 μs successive approximation A/D converter, with inherent track/hold functionality, a pseudo differential input and a high speed serial interface that interfaces to most microcontrollers. The AD7810 is fully specified over a temperature range of –40°C to +105°C.

By using a technique that samples the state of the $\overline{\text{CONVST}}$ (convert start) signal at the end of a conversion, the AD7810 may be used in an automatic power-down mode. When used in this mode, the AD7810 automatically powers down at the end of a conversion and "wakes up" at the start of a new conversion. This feature significantly reduces the power consumption of the part at lower throughput rates. The AD7810 can also operate in a high speed mode where the part is not powered down between conversions. In this high speed mode of operation, the conversion time of the AD7810 is 2.3 μs. The maximum throughput rate is dependent on the speed of the serial interface of the microcontroller.

The part is available in a small 8-lead, 0.3" wide, plastic dual-in-line package (mini-DIP); in an 8-lead, small outline IC (SOIC); and in an 8-lead microSOIC package.

PRODUCT HIGHLIGHTS

1. Complete, 10-Bit ADC in 8-Lead Package
   The AD7810 is a 10-bit 2.3 μs ADC with inherent track/hold functionality and a high speed serial interface—all in an 8-lead microSOIC package. V_{REF} may be connected to V_{DD} to eliminate the need for an external reference. The result is a high speed, low power, space saving ADC solution.
2. Low Power, Single Supply Operation
   The AD7810 operates from a single 2.7 V to 5.5 V supply and typically consumes only 9 mW of power while converting. The power dissipation can be significantly reduced at lower throughput rates by using the automatic power-down mode, e.g., at a throughput rate of 10 kSPS the power consumption is only 270 μW.
3. Automatic Power-Down
   The automatic power-down mode, whereby the AD7810 powers down at the end of a conversion and "wakes up" before the next conversion, means the AD7810 is ideal for battery powered applications. See Power vs. Throughput Rate section.
4. Serial Interface
   An easy to use, fast serial interface allows connection to most popular microprocessors with no external circuitry.

REV. B

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AD7810* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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DOCUMENTATION

Data Sheet

- AD7810: 2.7 V to 5.5 V, 2 ms, 10-Bit ADC in 8-Lead microSOIC/DIP Data Sheet

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7810 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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AD7810–SPECIFICATIONS (GND = 0 V, $V_{REF} = V_{DD}$. All specifications –40°C to +105°C unless otherwise noted.)

Parameter	Y Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz, f_{SAMPLE} = 350 kHz
Signal to (Noise + Distortion) Ratio[1]	58	dB min	
Total Harmonic Distortion[1]	–64	dB max	
Peak Harmonic or Spurious Noise	–64	dB max	
Intermodulation Distortion[2]			fa = 48 kHz, fb = 48.5 kHz
2nd Order Terms	–67	dB typ	
3rd Order Terms	–67	dB typ	
DC ACCURACY			
Resolution	10	Bits	
Relative Accuracy[1]	±1	LSB max	
Differential Nonlinearity (DNL)[1]	±1	LSB max	
Offset Error[1]	±2	LSB max	
Gain Error[1]	±2	LSB max	
Minimum Resolution for Which No Missing Codes Are Guaranteed	10	Bits	
ANALOG INPUT			
Input Voltage Range	0	V min	
	V_{REF}	V max	
Input Leakage Current[2]	±1	µA max	
Input Capacitance[2]	15	pF max	
REFERENCE INPUTS[2]			
V_{REF} Input Voltage Range	1.2	V min	
	V_{DD}	V max	
Input Leakage Current	±3	µA max	
Input Capacitance	20	pF max	
LOGIC INPUTS[2]			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.4	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	8	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
High Impedance Leakage Current	±10	µA max	
High Impedance Capacitance	15	pF max	
CONVERSION RATE			
Conversion Time	2.3	µs max	
Track/Hold Acquisition Time[1]	100	ns max	See DC Acquisition Time Section
POWER SUPPLY			
V_{DD}	2.7–5.5	Volts	For Specified Performance
I_{DD}	3.5	mA max	Sampling at 350 kSPS and Logic
Power Dissipation	17.5	mW max	Inputs at V_{DD} or 0 V. V_{DD} = 5 V
Power-Down Mode			
I_{DD}	1	µA max	V_{DD} = 5 V; V_{DD} = 3 V
Power Dissipation	5	µW max	
Automatic Power Down			
1 kSPS Throughput	27	µW max	
10 kSPS Throughput	270	µW max	
100 kSPS Throughput	2.7	mW max	

NOTES
[1]See Terminology section.
[2]Sample tested during initial release and after any redesign or process change that may affect this parameter.

Specifications subject to change without notice.

Timing Characteristics[1, 2] (–40°C to +105°C, $V_{REF} = V_{DD}$, unless otherwise noted)

Parameter	V_{DD} = 5 V ± 10%	V_{DD} = 3 V ± 10%	Unit	Conditions/Comments
t_1	2.3	2.3	µs (max)	Conversion Time Mode 1 Operation (High Speed Mode)
t_2	20	20	ns (min)	$\overline{\text{CONVST}}$ Pulsewidth
t_3	25	25	ns (min)	SCLK High Pulsewidth
t_4	25	25	ns (min)	SCLK Low Pulsewidth
t_5[3]	5	5	ns (min)	$\overline{\text{CONVST}}$ Rising Edge to SCLK Rising Edge Set-Up Time
t_6[3]	10	10	ns (max)	SCLK Rising Edge to D_{OUT} Data Valid Delay
t_7[3]	5	5	ns (max)	Data Hold Time after Rising Edge SCLK
t_8[3, 4]	20	20	ns (max)	Bus Relinquish Time after Falling Edge of SCLK
	10	10	ns (min)	
$t_{POWER\ UP}$	1.5	1.5	µs (max)	Power-Up Time after Rising Edge of $\overline{\text{CONVST}}$

NOTES
[1]Sample tested to ensure compliance.
[2]See Figures 14, 15 and 16.
[3]These numbers are measured with the load circuit of Figure 1. They are defined as the time required for the o/p to cross 0.8 V or 2.4 V for V_{DD} = 5 V ± 10% and 0.4 V or 2 V for V_{DD} = 3 V ± 10%.
[4]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{DD} to GND . . . . –0.3 V to +7 V
Digital Input Voltage to GND
($\overline{\text{CONVST}}$, SCLK) . . . . –0.3 V, V_{DD} + 0.3 V
Digital Output Voltage to GND
(D_{OUT}) . . . . –0.3 V, V_{DD} + 0.3 V
V_{REF} to GND . . . . –0.3 V, V_{DD} + 0.3 V
Analog Inputs
(V_{IN+}, V_{IN-}) . . . . –0.3 V, V_{DD} + 0.3 V
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . 150°C
Plastic DIP Package, Power Dissipation . . . . 450 mW
θ_{JA} Thermal Impedance . . . . 125°C/W
θ_{JC} Thermal Impedance . . . . 50°C/W
Lead Temperature Soldering (10 sec) . . . . 260°C
SOIC Package, Power Dissipation . . . . 450 mW
θ_{JA} Thermal Impedance . . . . 160°C/W
θ_{JC} Thermal Impedance . . . . 56°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . 215°C
Infrared (15 sec) . . . . 220°C
MicroSOIC Package, Power Dissipation . . . . 450 mW
θ_{JA} Thermal Impedance . . . . 206°C/W
θ_{JC} Thermal Impedance . . . . 44°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . 215°C
Infrared (15 sec) . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Linearity Error (LSB)	Temperature Range	Package Description	Package Options	Branding Information
AD7810YN	±1 LSB	–40°C to +105°C	Plastic DIP	N-8	
AD7810YR	±1 LSB	–40°C to +105°C	Small Outline IC (SOIC)	SO-8	
AD7810YRM	±1 LSB	–40°C to +105°C	microSOIC	RM-8	C1Y

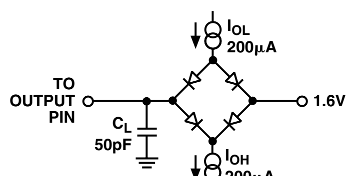
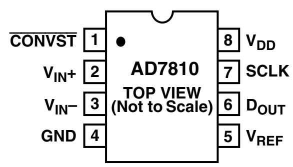


Figure 1. Load Circuit for Digital Output Timing Specifications

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Convert Start. Falling edge puts the track-and-hold into hold mode and initiates a conversion. A rising edge on the $\overline{\text{CONVST}}$ pin enables the serial port of the AD7810. This is useful in multi-package applications where a number of devices share the same serial bus. The state of this pin at the end of conversion also determines whether the part is powered down or not. See Operating Modes section of this data sheet.
2	V_{IN+}	Positive input of the pseudo differential analog input.
3	V_{IN-}	Negative input of the pseudo differential analog input.
4	GND	Ground reference for analog and digital circuitry.
5	V_{REF}	External reference is connected here.
6	D_{OUT}	Serial data is shifted out on this pin.
7	SCLK	Serial Clock. An external serial clock is applied here.
8	V_{DD}	Positive Supply Voltage 2.7 V to 5.5 V.

PIN CONFIGURATION
DIP/SOIC



Typical Performance Characteristics

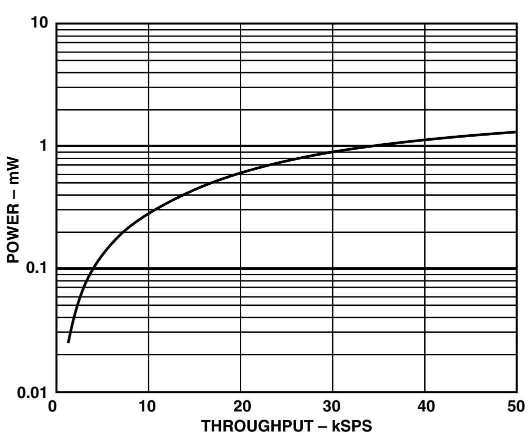


Figure 2. Power vs. Throughput

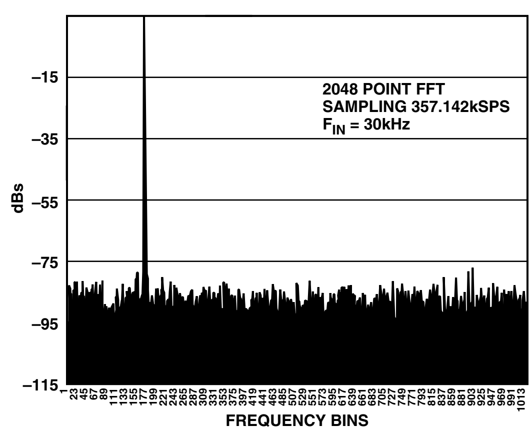


Figure 3. AD7810 SNR

TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for a 10-bit converter, this is 62 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7810 it is defined as:

$$THD(dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and $V_6{}^2$ are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms values of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7810 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Gain Error

This is the deviation of the last code transition (1111 . . . 110) to (1111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time

Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the V_{IN+} input of the AD7810. It means that the user must wait for the duration of the track/hold acquisition time, after the end of conversion or after a step input change to V_{IN+}, before starting another conversion to ensure that the part operates to specification.

CIRCUIT DESCRIPTION

Converter Operation

The AD7810 is a successive approximation analog-to-digital converter based around a charge redistribution DAC. The ADC can convert analog input signals in the range 0 V to V_{DD}. Figures 4 and 5 below show simplified schematics of the ADC. Figure 4 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A; the comparator is held in a balanced condition; and the sampling capacitor acquires the signal on V_{IN+}.

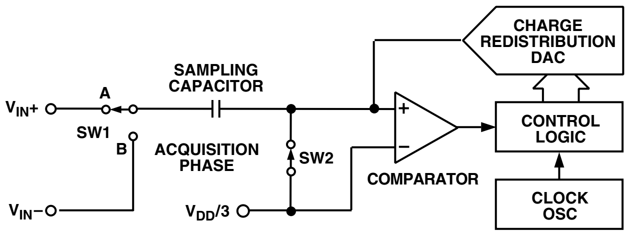


Figure 4. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 5), SW2 will open and SW1 will move to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 11 shows the ADC transfer function.

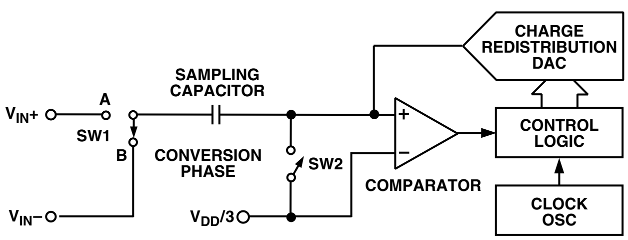


Figure 5. ADC Conversion Phase

TYPICAL CONNECTION DIAGRAM

Figure 6 shows a typical connection diagram for the AD7810. The serial interface is implemented using two wires; the rising edge of $\overline{CONVST}$ enables the serial interface—see Serial Interface section for more details. V_{REF} is connected to a well decoupled V_{DD} pin to provide an analog input range of 0 V to V_{DD}. When V_{DD} is first connected, the AD7810 powers up in a low current mode, i.e., power-down. A rising edge on the $\overline{CONVST}$ input will cause the part to power up—see Operating Modes. If power consumption is of concern, the automatic power-down at the end of a conversion should be used to improve power performance. See Power vs. Throughput Rate section of the data sheet.

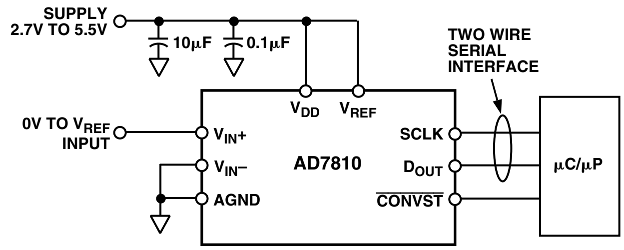


Figure 6. Typical Connection Diagram

Analog Input

Figure 7 shows an equivalent circuit of the analog input structure of the AD7810. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This will cause these diodes to become forward biased and start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 20 mA. The capacitor C2 is typically about 4 pF and can be primarily attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a multiplexer and a switch. This resistor is typically about 125 Ω. The capacitor C1 is the ADC sampling capacitor and has a capacitance of 3.5 pF.

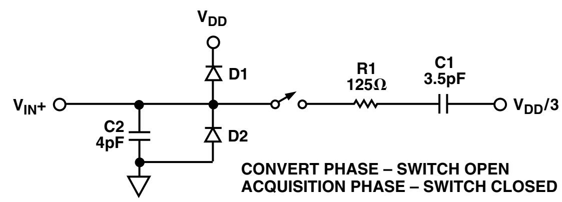


Figure 7. Equivalent Analog Input Circuit

The analog input of the AD7810 is made up of a pseudo differential pair. V_{IN+} pseudo differential with respect to V_{IN-}. The signal is applied to V_{IN+}, but in the pseudo differential scheme the sampling capacitor is connected to V_{IN-} during conversion (see Figure 8). This input scheme can be used to remove offsets that exist in a system. For example, if a system had an offset of 0.5 V, the offset could be applied to V_{IN-} and the signal applied to V_{IN+}. This has the effect of offsetting the input span by 0.5 V. It is only possible to offset the input span when the reference voltage (V_{REF}) is less than $V_{DD} - V_{OFFSET}$.

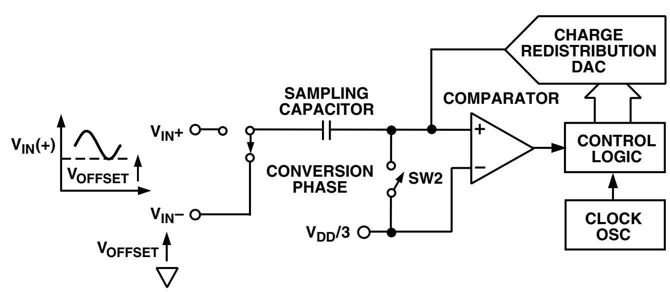


Figure 8. Pseudo Differential Input Scheme

When using the pseudo differential input scheme, the signal on V_{IN-} must not vary by more than a 1/2 LSB during the conversion process. If the signal on V_{IN-} varies during conversion, the conversion result will be incorrect. For single-ended operation, V_{IN-} is always connected to AGND. Figure 9 shows the AD7810 pseudo differential input being used to make a unipolar dc current measurement. A sense resistor is used to convert the current to a voltage and the voltage, is applied to the differential input as shown.

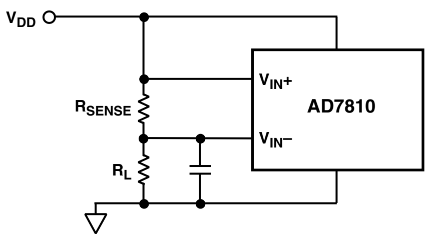


Figure 9. DC Current Measurement Scheme

DC Acquisition Time

The ADC starts a new acquisition phase at the end of a conversion and ends on the falling edge of the $\overline{CONVST}$ signal. At the end of a conversion there is a settling time associated with the sampling circuit. This settling time lasts approximately 100 ns. The analog signal on V_{IN+} is also being acquired during this settling time; therefore, the minimum acquisition time needed is approximately 100 ns.

Figure 10 shows the equivalent charging circuit for the sampling capacitor when the ADC is in its acquisition phase. R2 represents the source impedance of a buffer amplifier or resistive network; R1 is an internal multiplexer resistance and C1 is the sampling capacitor.

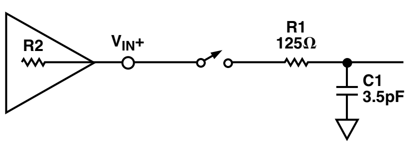


Figure 10. Equivalent Sampling Circuit

During the acquisition phase, the sampling capacitor must be charged to within a 1/2 LSB of its final value. The time it takes to charge the sampling capacitor (t_{CHARGE}) is given by the following formula:

$$t_{CHARGE} = 7.6 \times (R2 + 125\ \Omega) \times 3.5\ pF$$

For small values of source impedance, the settling time associated with the sampling circuit (100 ns) is, in effect, the acquisition time of the ADC. For example, with a source impedance (R2) of 10 Ω, the charge time for the sampling capacitor is approximately 4 ns. The charge time becomes significant for source impedances of 2 kΩ and greater.

AC Acquisition Time

In ac applications it is recommended to always buffer analog input signals. The source impedance of the drive circuitry must be kept as low as possible to minimize the acquisition time of the ADC. Large values of source impedance will cause the THD to degrade at high throughput rates. In addition, better performance can generally be achieved by using an external 1 nF capacitor on V_{IN+}.

ADC TRANSFER FUNCTION

The output coding of the AD7810 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSBs, etc.). The LSB size is = $V_{REF}/1024$. The ideal transfer characteristic for the AD7810 is shown in Figure 11 below.

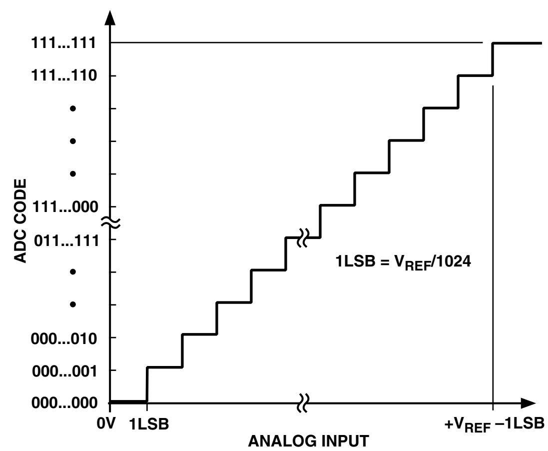


Figure 11. Transfer Characteristic

POWER-UP TIMES

The AD7810 has a 1.5 µs power-up time. When V_{DD} is first connected, the AD7810 is in a low current mode of operation. In order to carry out a conversion, the AD7810 must first be powered up. The ADC is powered up by a rising edge on the $\overline{\text{CONVST}}$ pin. A conversion is initiated on the falling edge of $\overline{\text{CONVST}}$. Figure 12 shows how to power up the AD7810 when V_{DD} is first connected or after the AD7810 is powered down using the $\overline{\text{CONVST}}$ pin.

Care must be taken to ensure that the $\overline{\text{CONVST}}$ pin of the AD7810 is logic low when V_{DD} is first applied.

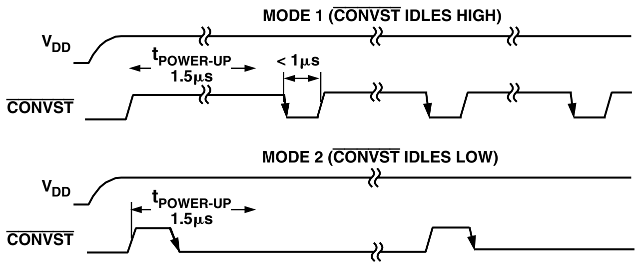


Figure 12. Power-Up Times

POWER VS. THROUGHPUT RATE

By operating the AD7810 in Mode 2, the average power consumption of the AD7810 decreases at lower throughput rates. Figure 13 shows how the automatic power-down is implemented using the $\overline{\text{CONVST}}$ signal to achieve the optimum power performance for the AD7810. As the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

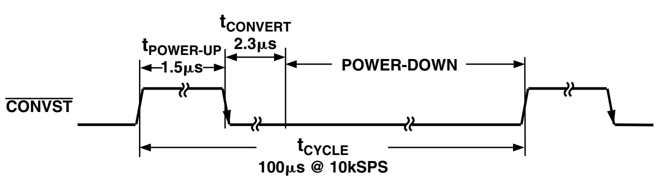


Figure 13. Automatic Power-Down

For example, if the AD7810 is operated in a continuous sampling mode with a throughput rate of 10 kSPS, the power consumption is calculated as follows. The power dissipation during normal operation is 9 mW, V_{DD} = 3 V. If the power-up time is 1.5 µs and the conversion time is 2.3 µs, the AD7810 can be said to dissipate 9 mW for 3.8 µs (worst case) during each conversion cycle. If the throughput rate is 10 kSPS, the cycle time is 100 µs and the average power dissipated during each cycle is $(3.8/100) \times (9\ \text{mW}) = 342\ \mu\text{W}$. Figure 2 shows a graph of Power vs. Throughput.

OPERATING MODES

Mode 1 Operation (High Speed Sampling)

When the AD7810 is used in this mode of operation, the part is not powered down between conversions. This mode of operation allows high throughput rates to be achieved. The timing diagram in Figure 14 shows how this optimum throughput rate is achieved by bringing the $\overline{\text{CONVST}}$ signal high before the end of the conversion. The AD7810 leaves its tracking mode and goes into hold on the falling edge of $\overline{\text{CONVST}}$. A conversion is also initiated at this time. The conversion takes 2.3 µs to complete. At this point, the result of the current conversion is latched into the serial shift register, and the state of the $\overline{\text{CONVST}}$ signal checked. The $\overline{\text{CONVST}}$ signal should be high at the end of the conversion to prevent the part from powering down.

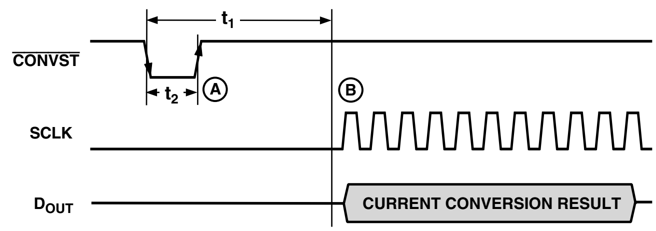


Figure 14. Mode 1 Operation Timing

The serial port on the AD7810 is enabled on the rising edge of the $\overline{\text{CONVST}}$ signal (see Serial Interface section). As explained earlier, this rising edge should occur before the end of the conversion process if the part is not to be powered down. A serial read can take place at any stage after the rising edge of $\overline{\text{CONVST}}$. If a serial read is initiated before the end of the current conversion process (i.e., at time "A"), the result of the previous conversion is shifted out on the D_{OUT} pin. It is possible to allow the serial read to extend beyond the end of a conversion. In this case the new data will not be latched into the output shift register until the read has finished. The dynamic performance of the AD7810 typically degrades by up to 3 dBs while reading during a conversion. If the user waits until the end of the conversion process, i.e., 2.3 µs after falling edge of $\overline{\text{CONVST}}$ (Point "B"), before initiating a read, the current conversion result is shifted out.

Mode 2 Operation (Automatic Power-Down)

When used in this mode of operation, the part automatically powers down at the end of a conversion. This is achieved by leaving the $\overline{\text{CONVST}}$ signal low until the end of the conversion. Because it takes approximately 1.5 μs for the part to power up after it has been powered down, this mode of operation is intended to be used in applications where slower throughput rates are required, i.e., in the order of 100 kSPS. The timing diagram in Figure 15 shows how to operate the part in this mode. If the AD7810 is powered down, the rising edge of the $\overline{\text{CONVST}}$ pulse causes the part to power up. When the part has powered up (≈ 1.5 μs after the rising edge of $\overline{\text{CONVST}}$), the $\overline{\text{CONVST}}$ signal is brought low, and a conversion is initiated on this falling edge of the $\overline{\text{CONVST}}$ signal. The conversion takes 2.3 μs and after this time, the conversion result is latched into the serial shift register and the part powers down. Therefore, when the part is operated in Mode 2, the effective conversion time is equal to the power-up time (1.5 μs) and the SAR conversion time (2.3 μs).

NOTE: Although the AD7810 takes 1.5 μs to power up after the rising edge of $\overline{\text{CONVST}}$, it is not necessary to leave $\overline{\text{CONVST}}$ high for 1.5 μs after the rising edge before bringing it low to initiate a conversion. If the $\overline{\text{CONVST}}$ signal goes low before 1.5 μs in time has elapsed, then the power-up time is timed out internally and a conversion is then initiated. Hence the AD7810 is guaranteed to have always powered up before a conversion is initiated—even if the $\overline{\text{CONVST}}$ pulsewidth is < 1.5 μs. If the $\overline{\text{CONVST}}$ width is > 1.5 μs, then a conversion is initiated on the falling edge.

As in the case of Mode 1 operation, the rising edge of the $\overline{\text{CONVST}}$ pulse enables the serial port of the AD7810 (see Serial Interface section). If a serial read is initiated soon after this rising edge (Point "A"), i.e., before the end of the conversion, the result of the previous conversion is shifted out on pin D_{OUT}. In order to read the result of the current conversion, the user must wait at least 2.3 μs after the falling edge of $\overline{\text{CONVST}}$ before initiating a serial read. The serial port of the AD7810 is still functional even though the AD7810 has been powered down. NOTE: Serial read should not cross the next rising edge of $\overline{\text{CONVST}}$.

Because it is possible to do a serial read from the part while it is powered down, the AD7810 is powered up only to do the conversion and is immediately powered down at the end of a conversion. This significantly improves the power consumption of the part at slower throughput rates—see Power vs. Throughput Rate section.

SERIAL INTERFACE

The serial interface of the AD7810 consists of three wires, a serial clock input SCLK, serial port enable $\overline{\text{CONVST}}$ and a serial data output D_{OUT} (see Figure 16). The serial interface is designed to allow easy interfacing to most microcontrollers, e.g., PIC16C, PIC17C, QSPI and SPI, without the need for any gluing logic. When interfacing to the 8051, the SCLK must be inverted. The Microprocessor Interface section explains how to interface to some popular microcontrollers.

Figure 16 shows the timing diagram for a serial read from the AD7810. The serial interface works with both a continuous and a noncontinuous serial clock. The rising edge of the $\overline{\text{CONVST}}$ signal *resets* a counter, which counts the number of serial clocks to ensure the correct number of bits are shifted out of the serial shift registers. The SCLK is ignored once the correct number of bits have been shifted out. In order for another serial transfer to take place, the counter must be reset by the falling edge of the 10th SCLK. Data is clocked out from the D_{OUT} line on the first rising SCLK edge after the rising edge of the $\overline{\text{CONVST}}$ signal and on subsequent SCLK rising edges. D_{OUT} enters its high impedance state again on the falling edge of the 10th SCLK. In multipackage applications, the $\overline{\text{CONVST}}$ signal can be used as a chip select signal. The serial interface will not shift data out until it receives a rising edge on the $\overline{\text{CONVST}}$ pin.

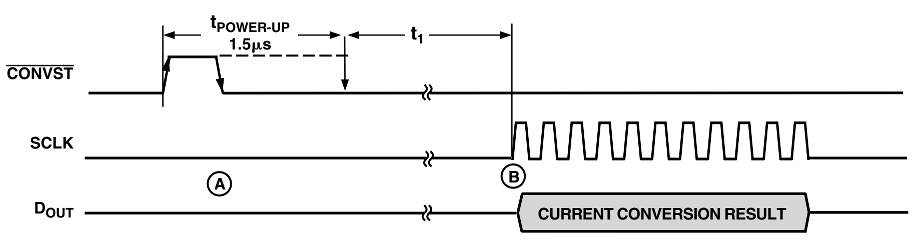


Figure 15. Mode 2 Operation Timing

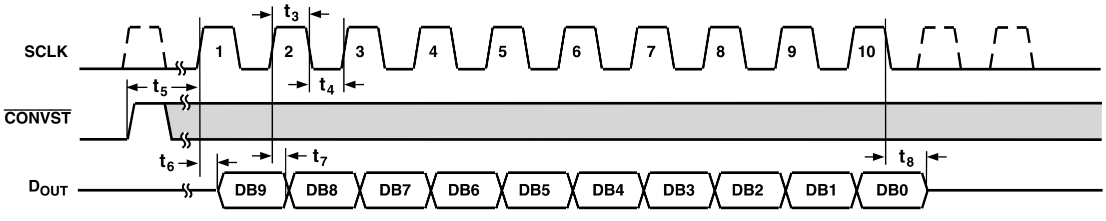


Figure 16. AD7810 Serial Interface Timing

MICROPROCESSOR INTERFACING

The serial interface on the AD7810 allows the parts to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7810 with some of the more common microcontroller serial interface protocols.

AD7810 to PIC16C6x/7x

The PIC16C6x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity Bit = 0. This is done by writing to the Synchronous Serial Port Control Register (SSPCON). See *PIC16/17 Microcontroller User Manual.* Figure 17 shows the hardware connections needed to interface to the PIC16/PIC17. In this example I/O port RA1 is being used to pulse $\overline{\text{CONVST}}$ and enable the serial port of the AD7810. This microcontroller transfers only eight bits of data during each serial transfer operation, therefore, two consecutive read operations are needed.

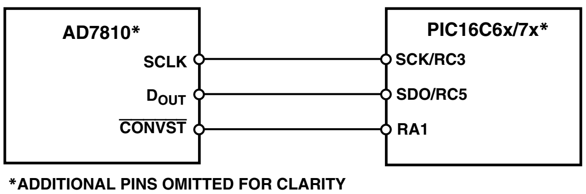


Figure 17. Interfacing to the PIC16/PIC17

AD7810 to MC68HC11

The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 0), Clock Polarity Bit (CPOL) = 0, and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see *68HC11 User Manual.* A connection diagram is shown in Figure 18.

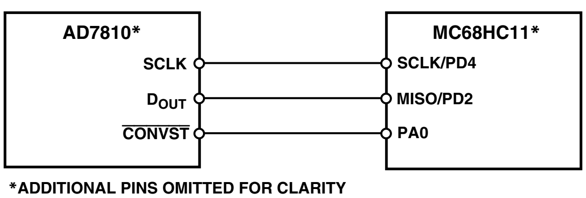


Figure 18. Interfacing to the MC68HC11

AD7810 to 8051

The AD7810 requires a clock synchronized to the serial data; therefore, the 8051 serial interface must be operated in Mode 0. In this mode serial data enters and exits through RXD, and a serial clock is output on TXD (half duplex). Figure 19 shows how the 8051 is connected to the AD7810. However, because the AD7810 shifts data out on the rising edge of the serial clock, the serial clock must be inverted.

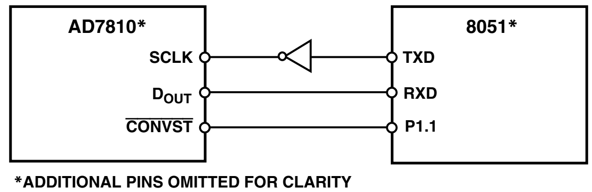


Figure 19. Interfacing to the 8051 Serial Port

It is possible to implement a serial interface using the data ports on the 8051 (or any microcontroller). This would allow direct interfacing between the AD7810 and 8051 to be implemented. The technique involves "bit banging" an I/O port (e.g., P1.0) to generate a serial clock and using another I/O port (e.g., P1.1) to read in data, see Figure 20.

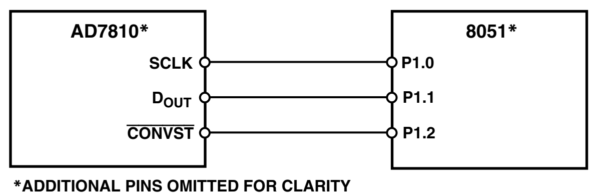
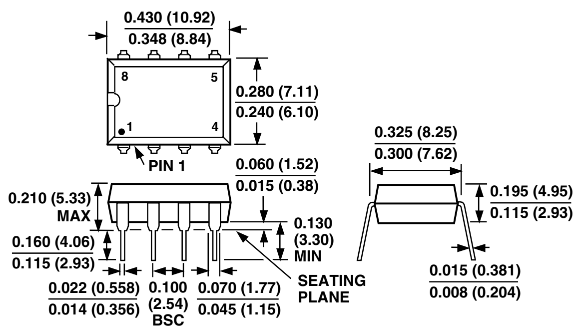


Figure 20. Interfacing to the 8051 Using I/O Ports

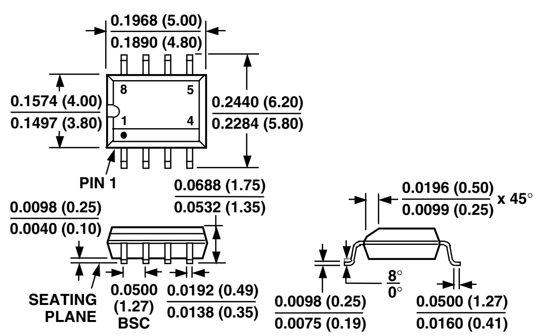
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

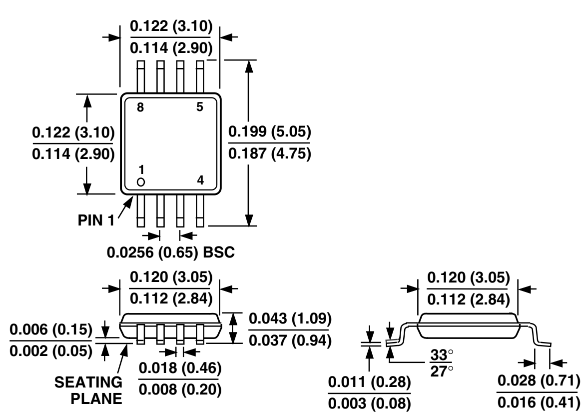
8-Lead Plastic DIP (N-8)



8-Lead Small Outline (SO-8)



8-Lead microSOIC (RM-8)



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