ANALOG DEVICES

CMOS Low Cost, 10-Bit Multiplying DAC

AD7533

FEATURES

Low cost 10-bit DAC
Low cost AD7520 replacement
Linearity: ½ LSB, 1 LSB, or 2 LSB
Low power dissipation
Full 4-quadrant multiplying DAC
CMOS/TTL direct interface
Latch free (protection Schottky not required)
Endpoint linearity

APPLICATIONS

Digitally controlled attenuators
Programmable gain amplifiers
Function generation
Linear automatic gain controls

GENERAL DESCRIPTION

The AD7533 is a low cost, 10-bit, 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the AD7520 industry standard, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on 5 V to 15 V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

FUNCTIONAL BLOCK DIAGRAM

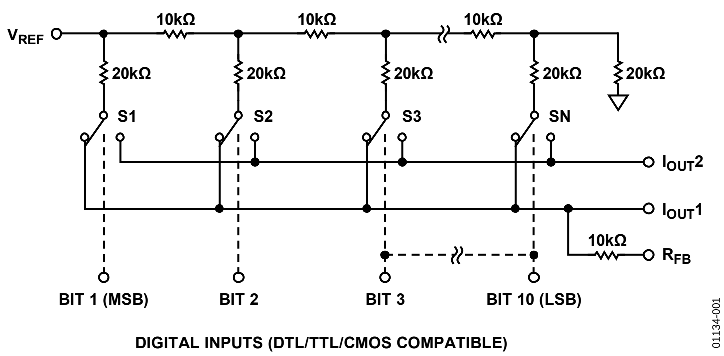


Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

3/07—Rev. B to Rev. C

Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Figure 13, Figure 14, and Figure 17 ... 9
Updated Outline Dimensions ... 10
Changes to Ordering Guide ... 12

1/06—Rev. A to Rev. B

Updated Format ... Universal
Changes to Absolute Maximum Ratings ... 4
Added Pin Configurations and Function Descriptions Section ... 6
Updated Outline Dimensions ... 10
Changes to Ordering Guide ... 12

3/04—Rev. 0 to Rev. A

Changes to Specifications ... 2
Changes to Absolute Maximum Ratings ... 3
Changes to Ordering Guide ... 3
Updated Outline Dimensions ... 7

SPECIFICATIONS

V_{DD} = 15 V, $V_{OUT}1$ = $V_{OUT}2$ = 0 V, V_{REF} = 10 V, unless otherwise noted.

Table 1.

Parameter	T_A = 25°C	T_A = Operating Range	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy[1]			
AD7533JN, AD7533AQ, AD7533SQ, AD7533JP	±0.2% FSR maximum	±0.2% FSR maximum	
AD7533KN, AD7533BQ, AD7533KP, AD7533TE	±0.1% FSR maximum	±0.1% FSR maximum	
AD7533LN, AD7533CQ, AD7533UQ	±0.05% FSR maximum	±0.05% FSR maximum	
DNL	±1 LSB maximum	±1 LSB maximum	
Gain Error[2, 3]	±1% FS maximum	±1% FS maximum	Digital input = V_{INH}
Supply Rejection[4]			
$\Delta Gain/\Delta V_{DD}$	0.001%/% maximum	0.001%/% maximum	Digital inputs = V_{INH}, V_{DD} = 14 V to 17 V
Output Leakage Current			
$I_{OUT}1$	±5 nA maximum	±200 nA maximum	Digital inputs = V_{INL}, V_{REF} = ±10 V
$I_{OUT}2$	±5 nA maximum	±200 nA maximum	Digital inputs = V_{INH}, V_{REF} = ±10 V
DYNAMIC ACCURACY			
Output Current Settling Time	600 ns maximum[4]	800 ns[5]	To 0.05% FSR; R_{LOAD} = 100 Ω, digital inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR maximum[5]	±0.1% FSR maximum[5]	Digital inputs = V_{INL}, V_{REF} = ±10 V, 100 kHz sine wave
Propagation Delay	100 ns typical	100 ns typical	
Glitch Impulse	100 nV-s typical	100 nV-s typical	
REFERENCE INPUT			
Input Resistance (VREF)	5 kΩ min, 20 kΩ maximum	5 kΩ min, 20 kΩ maximum[6]	11 kΩ nominal
ANALOG OUTPUTS			
Output Capacitance			
C_{IOUT1}	50 pF maximum[5]	100 pF maximum[5]	Digital inputs = V_{INH}
C_{IOUT2}	20 pF maximum[5]	35 pF maximum[5]	
C_{IOUT1}	30 pF maximum[5]	35 pF maximum[5]	
C_{IOUT2}	50 pF maximum[5]	100 pF maximum[5]	Digital inputs = V_{INL}
DIGITAL INPUTS			
Input High Voltage (V_{INH})	2.4 V minimum	2.4 V minimum	
Input Low Voltage (V_{INL})	0.8 V maximum	0.8 V maximum	
Input Leakage Current (I_{IN})	±1 μA maximum	±1 μA maximum	V_{IN} = 0 V and V_{DD}
Input Capacitance (C_{IN})	8 pF maximum[5]	8 pF maximum[5]	
POWER REQUIREMENTS			
V_{DD}	15 V ± 10%	15 V ± 10%	Rated accuracy
V_{DD} Ranges[5]	5 V to 16 V	5 V to 16 V	Functionality with degraded performance
I_{DD}	2 mA maximum	2 mA maximum	Digital inputs = V_{INL} or V_{INH} D
	25 μA maximum	50 μA maximum	Digital inputs over V_{IN}

[1] FSR = full-scale range.
[2] Full scale (FS) = V_{REF}.
[3] Maximum gain change from T_A = 25°C to T_{MIN} or T_{MAX} is ±0.1% FSR.
[4] AC parameter, sample tested to ensure specification compliance.
[5] Guaranteed, not tested.
[6] Absolute temperature coefficient is approximately −300 ppm/°C.

ABSOLUTE MAXIMUM RATINGS

T_A = 25 °C unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V, +17 V
R_{FB} to GND	±25 V
V_{REF} to GND	±25 V
Digital Input Voltage Range	−0.3 V to V_{DD} + 0.3 V
$I_{OUT}1$, $I_{OUT}2$ to GND	−0.3 V to V_{DD}
Power Dissipation (Any Package)	
To 75°C	450 mW
Derates above 75°C by	6 mW/°C
Operating Temperature Range	
Plastic (JN, JP, KN, KP, LN Versions)	−40°C to +85°C
Hermetic (AQ, BQ, CQ Versions)	−40°C to +85°C
Hermetic (SQ, TE, UQ Versions)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TERMINOLOGY

Relative Accuracy

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % of full-scale range or (sub) multiples of 1 LSB.

Resolution

Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ (V_{REF}). Resolution in no way implies linearity.

Settling Time

Time required for the output function of the DAC to settle to within ½ LSB for a given digital input stimulus, that is, 0 to full scale.

Gain Error

Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error is adjusted out and is expressed in LSBs. Gain error is adjustable to zero with an external potentiometer.

Feedthrough Error

Error caused by capacitive coupling from V_{REF} to output with all switches off.

Output Capacitance

Capacity from $I_{OUT}1$ and $I_{OUT}2$ terminals to ground.

Output Leakage Current

Current that appears on $I_{OUT}1$ terminal with all digital inputs low or on $I_{OUT}2$ terminal when all inputs are high.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

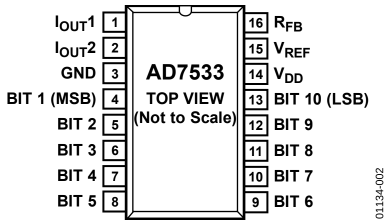


Figure 2. 16-Lead PDIP Pin Configuration

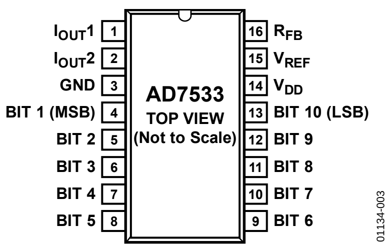


Figure 3. 16-Lead SOIC Pin Configuration

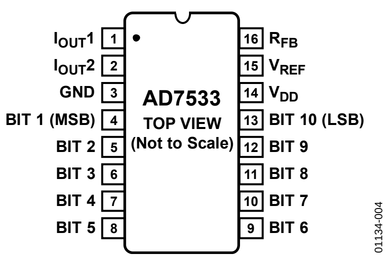


Figure 4. 16-Lead CERDIP Pin Configuration

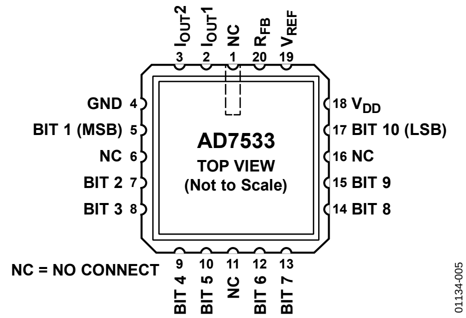


Figure 5. 20-Terminal LCC Pin Configuration

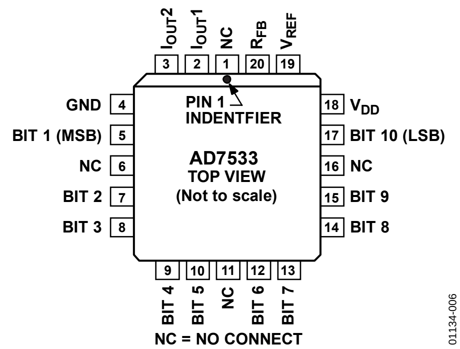


Figure 6. 20-Lead PLCC Pin Configuration

Table 3. Pin Function Descriptions

Pin Number			
16-Lead PDIP, SOIC, CERDIP	**20-Lead LCC, PLCC**	**Mnemonic**	**Description**
1	2	$I_{OUT}1$	DAC Current Output.
2	3	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	4	GND	Ground.
4 to 13	5, 7 to 10, 12 to 15, 17	BIT 1 to BIT 10	MSB to LSB.
14	18	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 5 V to 16 V.
15	19	V_{REF}	DAC Reference Voltage Input Terminal.
16	20	R_{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting R_{FB} to external amplifier output.
NA	1, 6, 11, 16	NC	No Connect.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533 is a 10-bit multiplying DAC that consists of a highly stable thin-film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 7. An inverted R- 2R ladder structure is used, that is, the binarily weighted currents are switched between the $I_{OUT}1$ and $I_{OUT}2$ bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

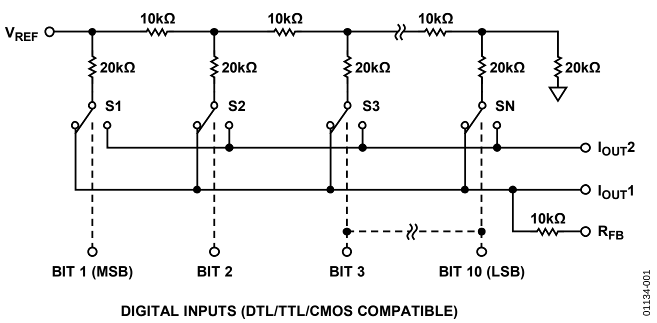


Figure 7. Functional Diagram

One of the CMOS current switches is shown in Figure 8. The geometries of Device 1, Device 2, and Device 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (Device 4, Device 5, Device 6, and Device 7), which in turn drive the two output N channels. The on resistances of the switches are binarily sealed so that the voltage drop across each switch is the same. For example, Switch 1 in Figure 8 is designed for an on resistance of 20 Ω, Switch 2 for 40 Ω, and so on. For a 10 V reference input, the current through Switch 1 is 0.5 mA, the current through Switch 2 is 0.25 mA, and so on, thus maintaining a constant 10 mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

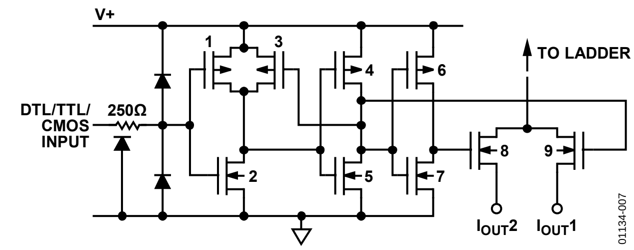


Figure 8. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and digital inputs low are shown in Figure 9 and Figure 10. In Figure 9 with all digital inputs low, the reference current is switched to $I_{OUT}2$. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/1024 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The on capacitance of the output N channel switch is 100 pF, as shown on the $I_{OUT}2$ terminal. The off switch capacitance is 35 pF, as shown on the $I_{OUT}1$ terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 10, is similar to Figure 9; however, the on switches are now on Terminal $I_{OUT}1$. Therefore, there is the 100 pF at that terminal.

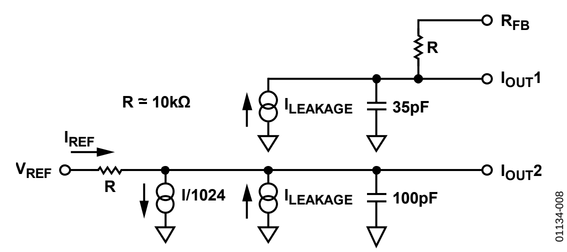


Figure 9. Equivalent Circuit—All Digital Inputs Low

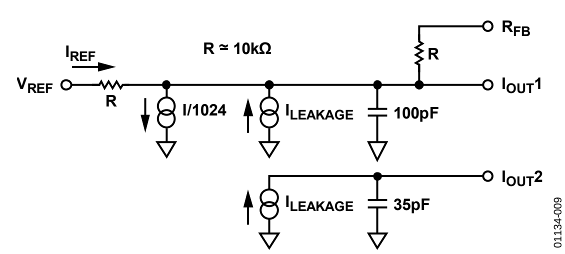


Figure 10. Equivalent Circuit—All Digital Inputs High

OPERATION

UNIPOLAR BINARY CODE

Table 4. Unipolar Binary Operation (2-Quadrant Multiplication)

Digital Input MSB	LSB	Analog Output (V_{OUT} as shown in Figure 11)
1 1 1 1 1 1 1 1 1 1		$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1		$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0		$-V_{REF}\left(\frac{512}{1024}\right)=\left(\frac{V_{REF}}{2}\right)$
0 1 1 1 1 1 1 1 1 1		$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1		$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0		$-V_{REF}\left(\frac{0}{1024}\right)=0$

Nominal LSB magnitude for the circuit of Figure 11 is given by

$$LSB = V_{REF}\left(\frac{1}{1024}\right)$$

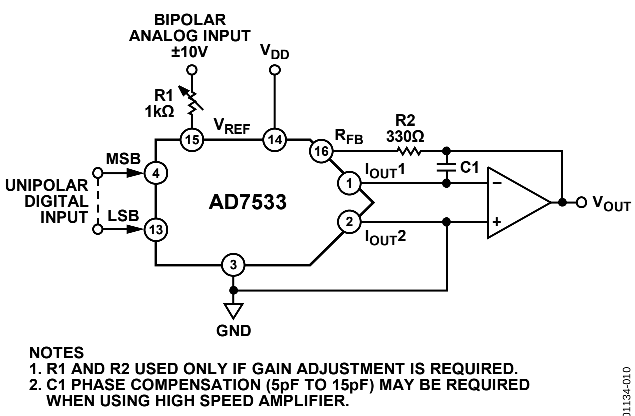


Figure 11. Unipolar Binary Operation (2-Quadrant Multiplication)

BIPOLAR (OFFSET BINARY) CODE

Table 5. Unipolar Binary Operation (4-Quadrant Multiplication)

Digital Input MSB	LSB	Analog Output (V_{OUT} as shown in Figure 12)
1 1 1 1 1 1 1 1 1 1		$+V_{REF}\left(\frac{511}{512}\right)$
1 0 0 0 0 0 0 0 0 1		$+V_{REF}\left(\frac{1}{512}\right)$
1 0 0 0 0 0 0 0 0 0		0
0 1 1 1 1 1 1 1 1 1		$-V_{REF}\left(\frac{1}{512}\right)$
0 0 0 0 0 0 0 0 0 1		$-V_{REF}\left(\frac{511}{512}\right)$
0 0 0 0 0 0 0 0 0 0		$-V_{REF}\left(\frac{512}{512}\right)$

Nominal LSB magnitude for the circuit of Figure 12 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

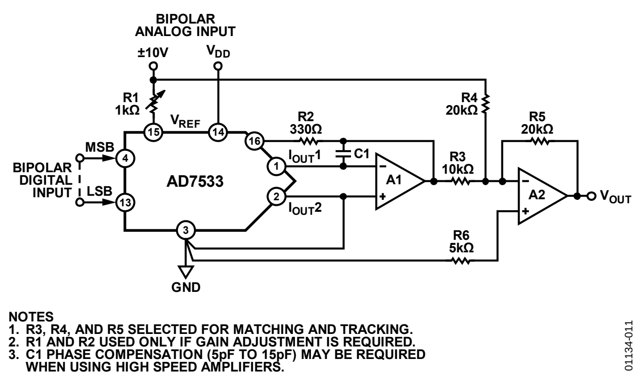


Figure 12. Bipolar Operation (4-Quadrant Multiplication)

APPLICATIONS

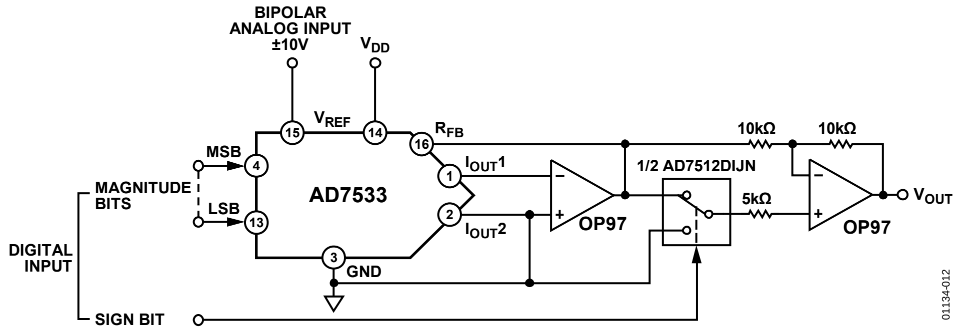


Figure 13. 10-Bit and Sign Multiplying DAC

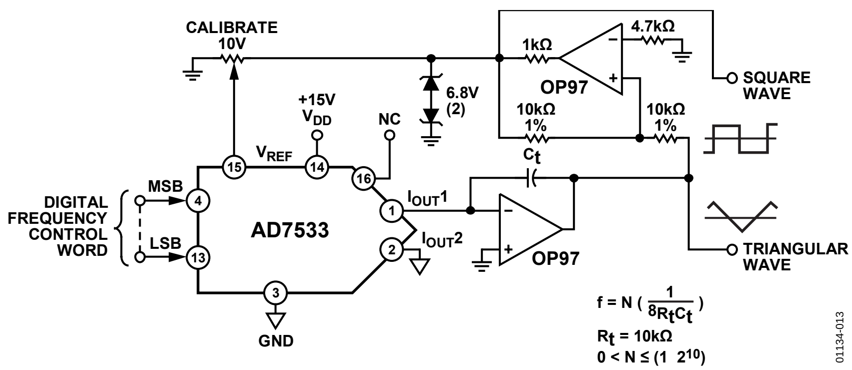


Figure 14. Programmable Function Generator

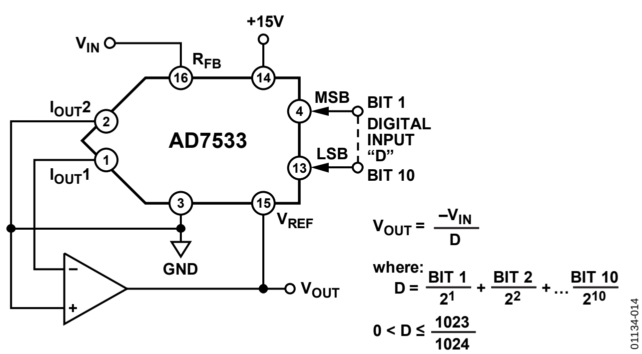


Figure 15. Divider (Digitally Controlled Gain)

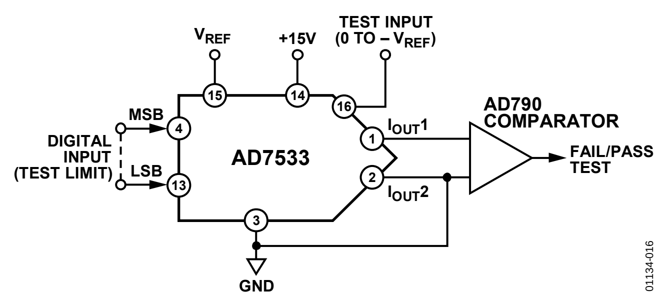


Figure 17. Digitally Programmable Limit Detector

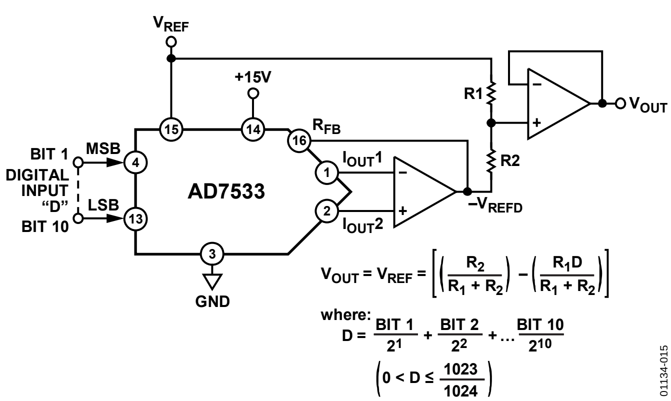


Figure 16. Modified Scale Factor and Offset

OUTLINE DIMENSIONS

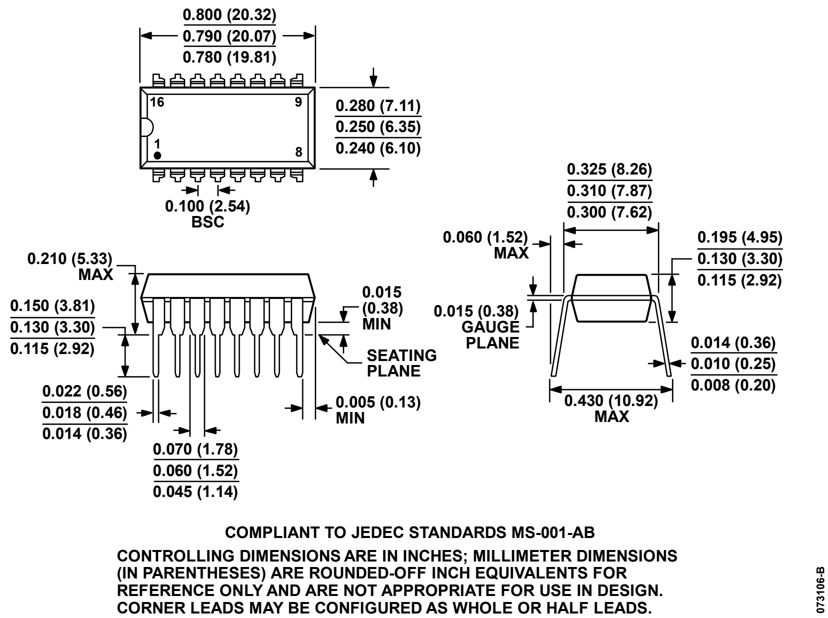


Figure 18. 16-Lead Plastic Dual In-Line Package [PDIP]
(N-16)
Dimensions shown in inches and (millimeters)

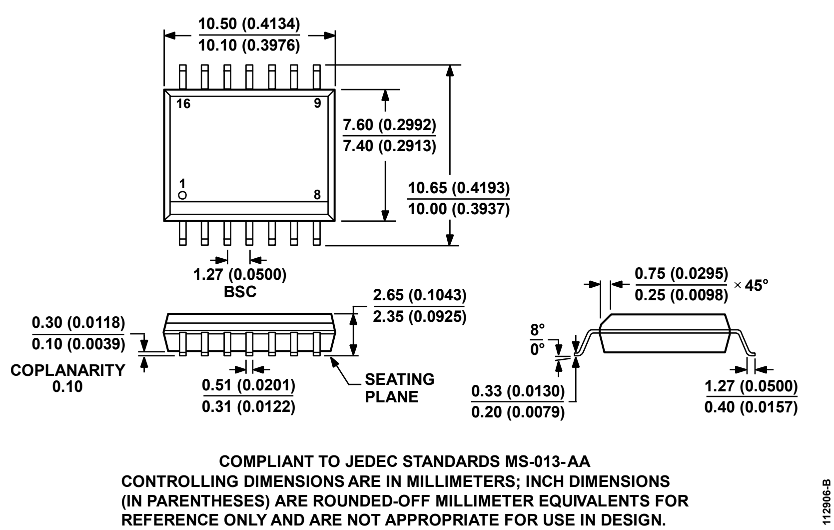
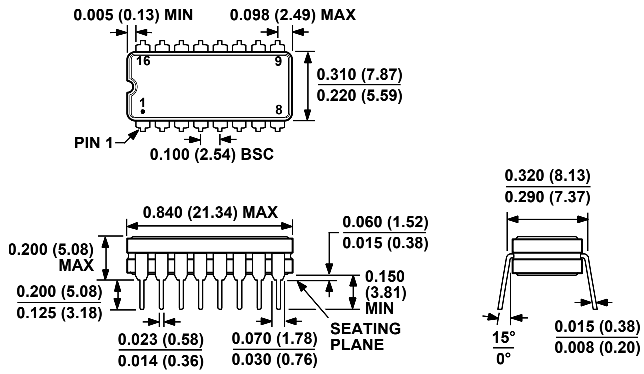
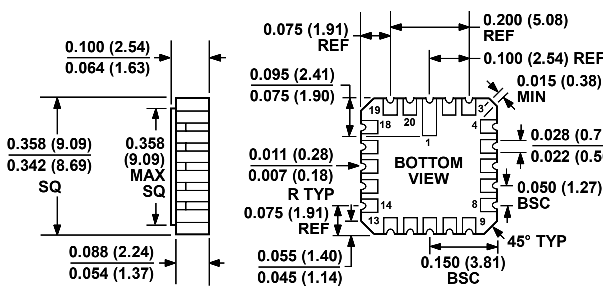


Figure 19. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

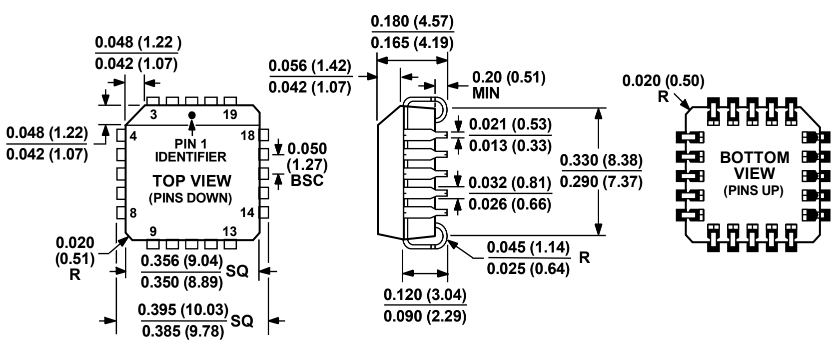
Figure 20. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

022106-A

Figure 21. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20-1)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047-AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 22. 20-Lead Plastic Leaded Chip Carrier [PLCC]
(P-20)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Nonlinearity (% FSR max)
AD7533ACHIPS			DIE	
AD7533JN	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.2
AD7533JNZ[1]	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.2
AD7533KN	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.1
AD7533KNZ[1]	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.1
AD7533LN	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.05
AD7533LNZ[1]	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	±0.05
AD7533JP	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.2
AD7533JP-REEL	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.2
AD7533JPZ[1]	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.2
AD7533JPZ-REEL[1]	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.2
AD7533KP	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.1
AD7533KP-REEL	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.1
AD7533KPZ[1]	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.1
AD7533KPZ-REEL[1]	−40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20	±0.1
AD7533KR	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	±0.1
AD7533KR-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	±0.1
AD7533KRZ[1]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	±0.1
AD7533KRZ-REEL[1]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	±0.1
AD7533AQ	−40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.2
AD7533BQ	−40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.1
AD7533CQ	−40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.05
AD7533SQ	−55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.2
AD7533UQ	−55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.05
AD7533UQ/883B	−55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	±0.05
AD7533TE/883B	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20-1	±0.1

[1]Z = RoHS compliant part.

C01134-0-3/07(C)