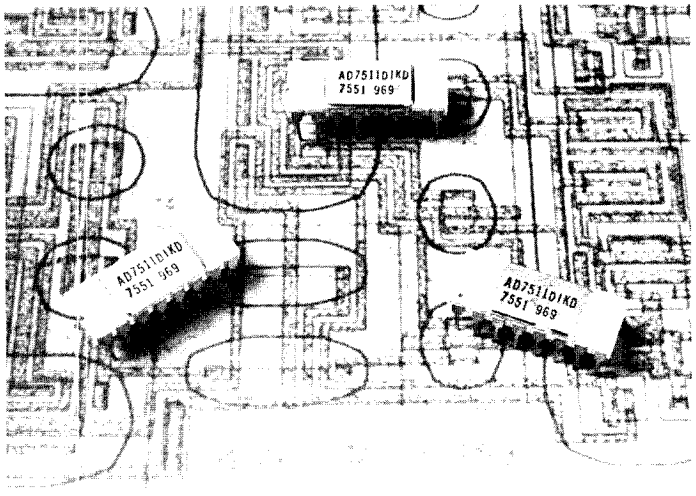
ANALOG DEVICES

DI CMOS Protected Analog Switches

AD7510DI, AD7511DI, AD7512DI

FEATURES

- Latch-Proof
- Overvoltage-Proof: ±25V
- Low R_{ON}: 75Ω
- Low Dissipation: 3mW
- TTL/CMOS Direct Interface
- Silicon-Nitride Passivated
- Monolithic Dielectrically-Isolated CMOS



GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (400pA), the main features of an analog switch.

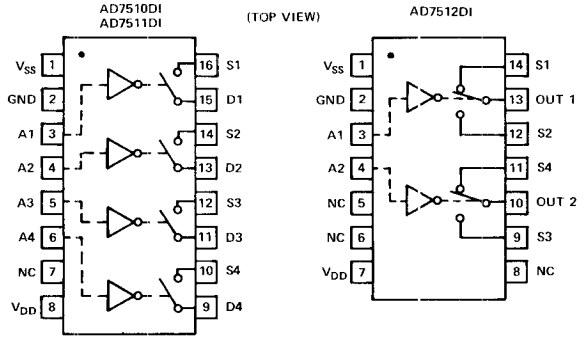
The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged in a 14-pin DIP.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

ORDERING INFORMATION

Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7510DIJN AD7510DIKN AD7511DIJN AD7511DIKN AD7512DIJN AD7512DIKN		0 to +70°C
	AD7510DIJD AD7510DIKD AD7511DIJD AD7511DIKD AD7512DIJD AD7512DIKD	−25°C to +85°C
	AD7510DISD AD7511DISD AD7511DITD AD7512DISD AD7512DITD	−55°C to +125°C

PIN CONFIGURATIONS



CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

COMMERCIAL VERSIONS (J, K)

PARAMETER	MODEL	VERSION	+25°C	0 to +70°C (N) −25°C to +85°C (D)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} [1]	All	J, K	75Ω typ, 100Ω max	175Ω max	−10V ≤ V_D ≤ +10V
R_{ON} vs V_D (V_S)	All	J, K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	J, K	+0.5%/°C typ		
R_{ON} Match	All	J, K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S) OFF[1]	All	J, K	0.5nA typ, 5nA max	500nA max	V_D = −10V, V_S = +10V and V_D = +10V, V_S = −10V
I_D (I_S)$_{ON}$ [2]	All	J, K	10nA max		V_S = V_D = +10V V_S = V_D = −10V
I_{OUT} [1]	AD7512DI	J, K	15nA max	1500nA max	V_{S1} = V_{OUT} = ±10V, V_{S2} = ∓10V and V_{S2} = V_{OUT} = ±10V, V_{S1} = ∓10V
DIGITAL CONTROL					
V_{INL} [1]	All	J, K		0.8V max	
V_{INH} [1]	All	J		3.0V min	
	All	K		2.4V min	
C_{IN}	All	J, K	3pF typ		
I_{INH} [1]	All	J, K	10nA max		V_{IN} = V_{DD}
I_{INL} [1]	All	J, K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		
	AD7511DI	J, K	350ns typ		V_{IN} = 0 to +3.0V
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D)OFF	All	J, K	8pF typ		
C_S (C_D)ON	All	J, K	17pF typ		
C_{DS} (C_{S-OUT})	All	J, K	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to −10V
POWER SUPPLY					
I_{DD} [1]	All	J, K	500μA max		All digital inputs = V_{INH}
I_{SS} [1]	All	J, K	100μA max		
I_{DD} [1]	All	J, K	100μA max		All digital inputs = V_{INL}
I_{SS} [1]	All	J, K	100μA max		

NOTES:
[1] 100% tested.
[2] Guaranteed, not production tested.
[3] A pullup resistor, typically 1-2kΩ is required to make "J" versions TTL compatible.

Specifications subject to change without notice.

MILITARY VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} [1]	All	S, T	100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ I_{DS} = 1mA
I_D $(I_S)_{OFF}$ [1]	All	S, T	3nA max	200nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D $(I_S)_{ON}$ [2]	All	S, T	10		$V_S = V_D$ = +10V and $V_S = V_D$ = -10V
I_{OUT} [1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL} [1]	All	S, T		0.8V max	
V_{INH} [1,3]	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH} [1]	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL}	All	S, T	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON} [2]	AD7510DI	S, T	1.0μs max		V_{IN} = 0 to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF} [2]	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}$ [2]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD} [1]	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS}	All	S, T		800μA max	
I_{DD}	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS}	All	S, T		500μA max	

NOTES:

[1] 100% tested.

[2] Guaranteed, not production tested.

[3] A pullup resistor, typically 1-2kΩ is required to make AD7511DISD and AD7512DISD TTL compatible.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . +17V

V_{SS} to GND . . . . . -17V

Overvoltage at V_D (V_S)

(1 second surge) . . . . . V_{DD} +25V or V_{SS} -25V

(Continuous) . . . . . V_{DD} +20V or V_{SS} -20V

Switch Current (I_{DS}, Continuous) 50mA

Switch Current (I_{DS}, Surge)

1ms Duration, 10% Duty Cycle 150mA

Digital Input Voltage Range . . . . . 0V to V_{DD}

Power Dissipation (Package)

14 & 16 pin Ceramic Dip

Up to +75°C. 450mW

Derates above +75°C by . . . . . 6mW/°C

14 & 16 pin Plastic Dip

Up to +70°C. 670mW

Derates above +75°C by . . . . . 8.3mW/°C

Storage Temperature . . . . . -65°C to +150°C

Operating Temperature

Plastic (J, K Versions) . . . . . 0 to +70°C

Ceramic (J, K Versions) . . . . . -25°C to +85°C

Ceramic (S, T Versions) . . . . . -55°C to +125°C

CAUTION: The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.

CIRCUIT DESCRIPTION

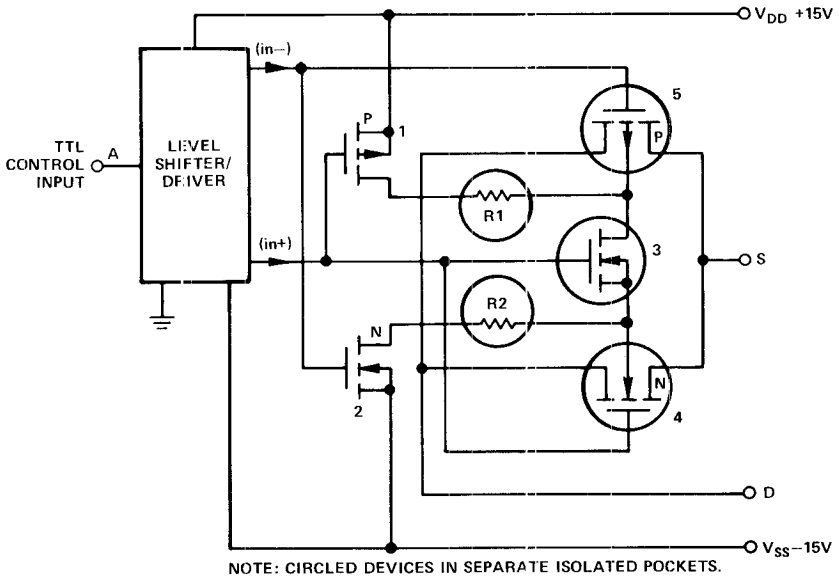


Figure 1. Typical Output Switch Circuitry of AD7510DI Series

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenum necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7510DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in−) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON." Hence, the back-gates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. (The circled devices are located in separate dielectrically isolated pockets.) Floating the output switch back-gates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the back-gates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-back-gate diode is forward biased; however, R1 and R2 provide current limiting action.

Consequently, without external current limiting resistance (or increased R_{ON}), the AD7510DI series switches provide:

1. Latch-proof operation
2. Overvoltage protection 25V beyond the V_{SS} and V_{DD} supply voltage

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices—*not* in series with the signal path between the S and D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor, causing device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or current limiting devices (output of op amps) will prevent damage to the device.

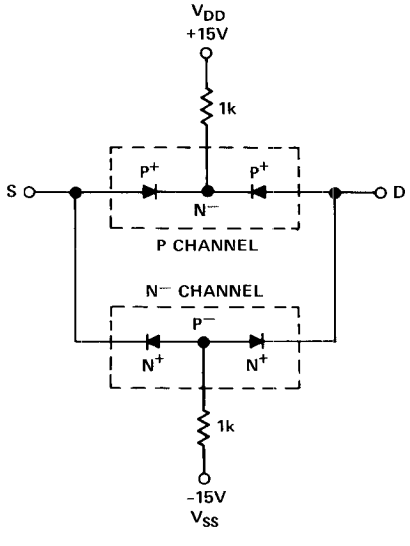
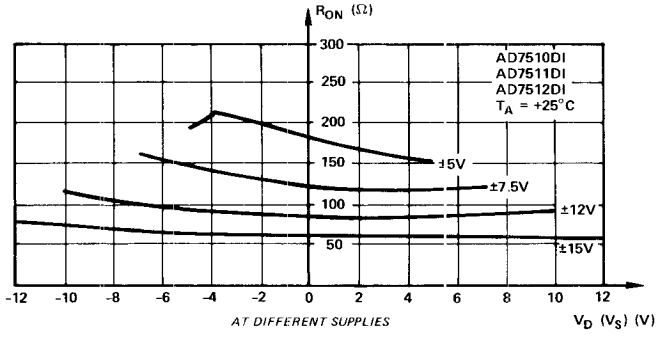
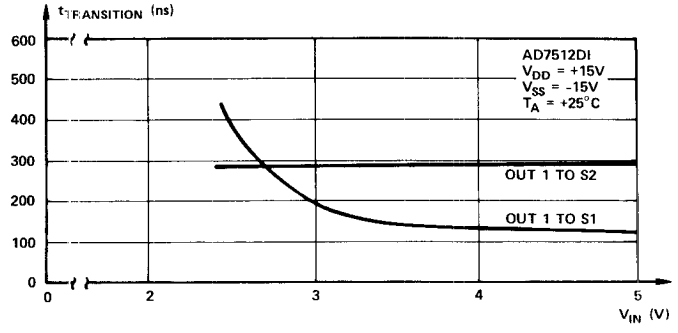


Figure 2. AD7510DI Series Output Switch Diode Equivalent Circuit

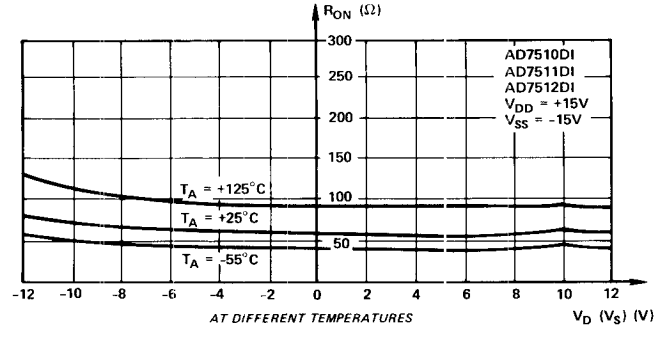
TYPICAL PERFORMANCE CHARACTERISTICS



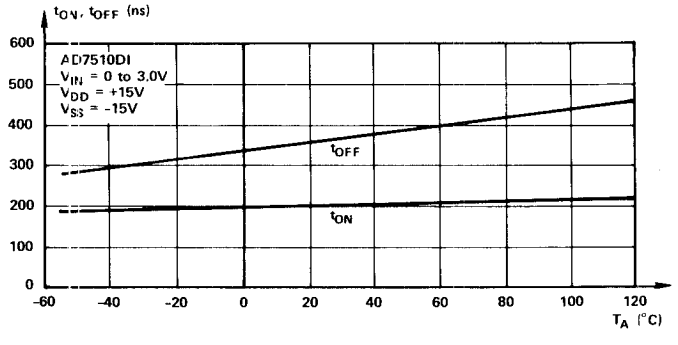
R_{ON} as a Function of V_D (V_S)



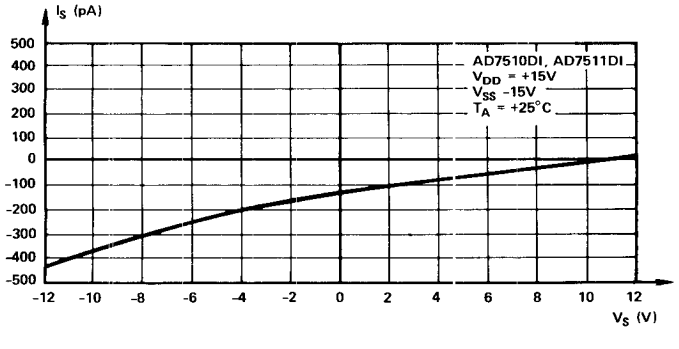
$t_{TRANSITION}$ as a Function of Digital Input Voltage



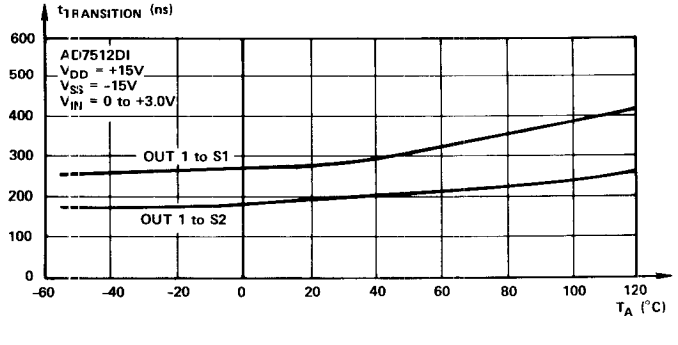
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature

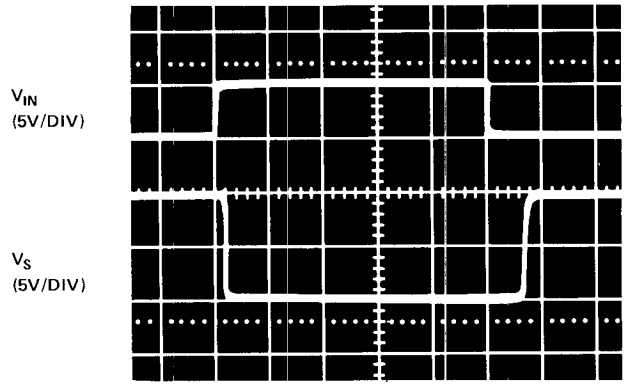


I_S, $(I_D)_{OFF}$ vs V_S



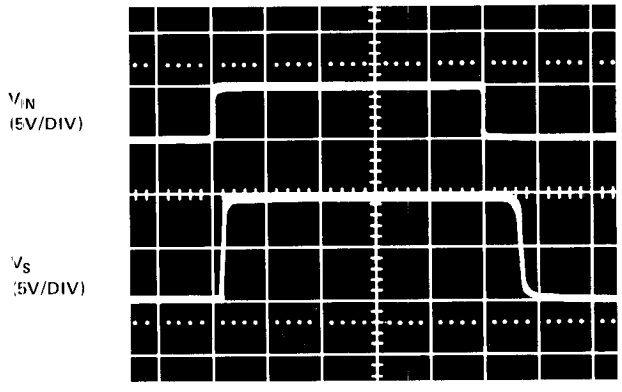
$t_{TRANSITION}$ as a Function of Temperature

0.5μs/DIV



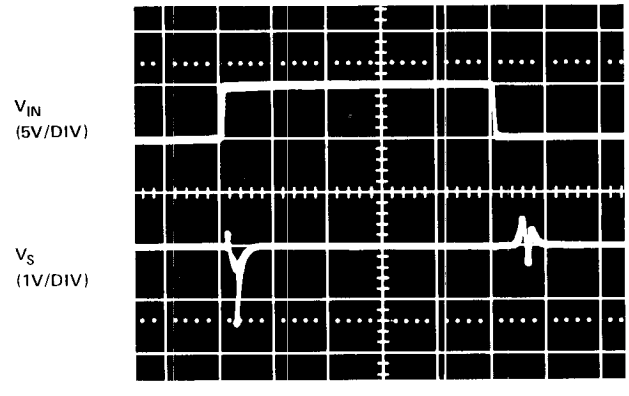
Switching Waveforms for V_D = -10V

0.5μs/DIV



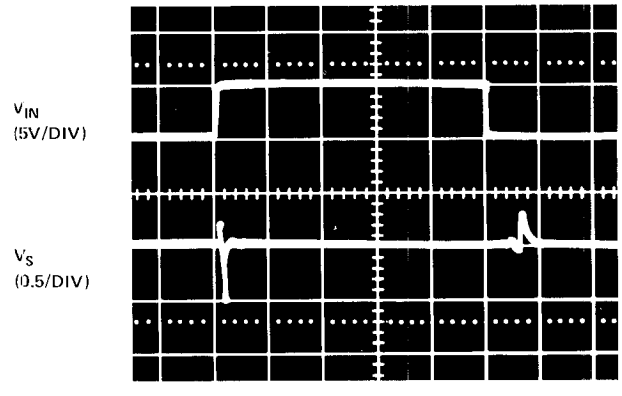
Switching Waveforms for V_D = +10V

0.5μs/DIV



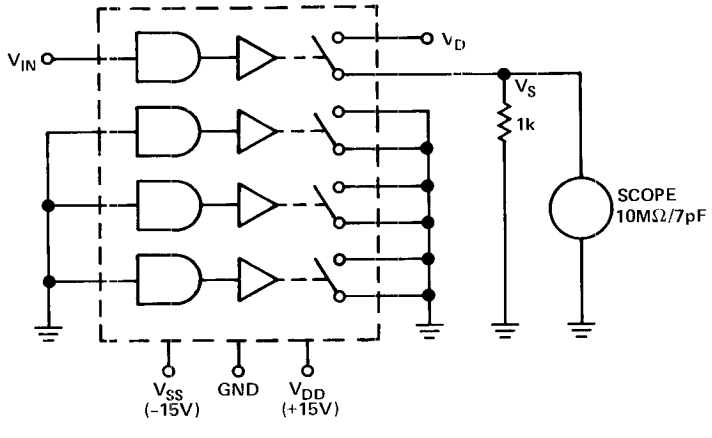
Switching Waveforms for V_D = Open

0.5μs/DIV



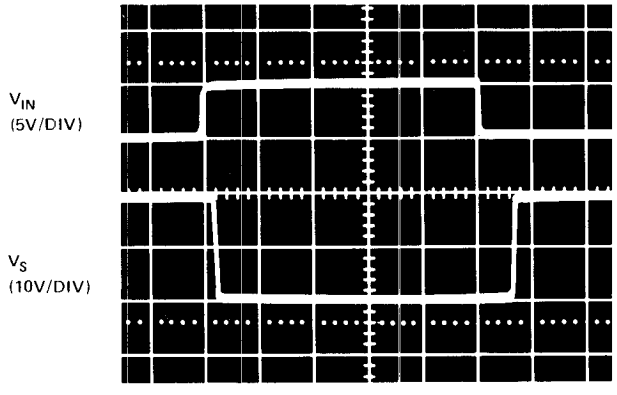
Switching Waveforms for V_D = 0V

AD7510DI, AD7511DI TEST CIRCUIT



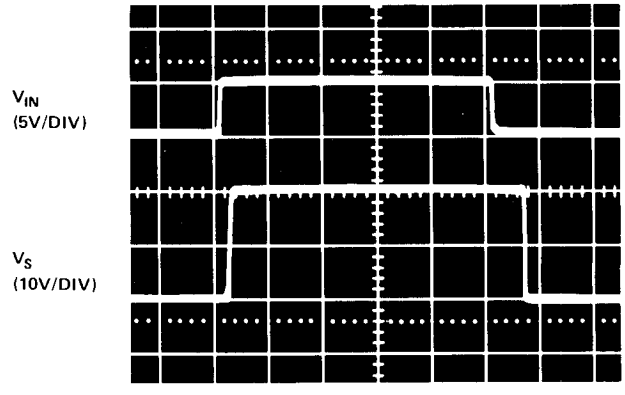
TYPICAL SWITCHING CHARACTERISTICS AD7512DI

0.5μs/DIV



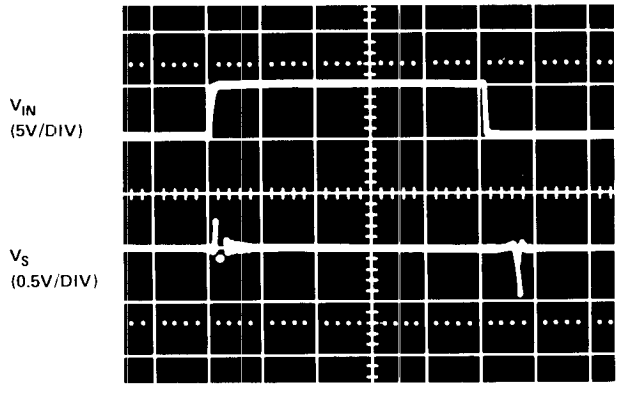
Switching Waveforms for
V_{S1} = -10V, V_{S2} = +10V, R_L = 1k

0.5μs/DIV



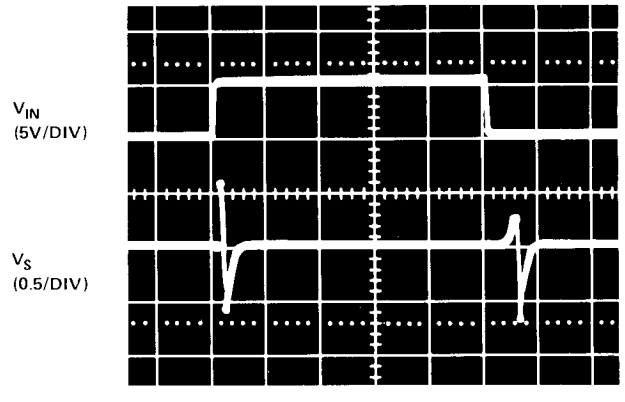
Switching Waveforms for
V_{S1} = +10V, V_{S2} = -10V, R_L = ∞

0.5μs/DIV



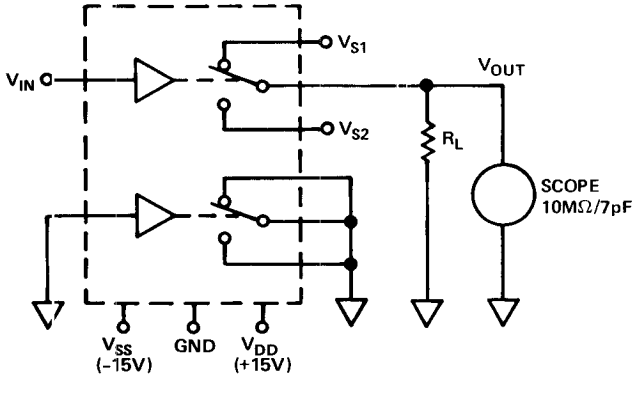
Switching Waveforms for
V_{S1} and V_{S2} = 0V, R_L = ∞

0.5μs/DIV



Switching Waveforms for
V_{S1} and V_{S2} = Open, R_L = 1k

AD7512DI TEST CIRCUIT

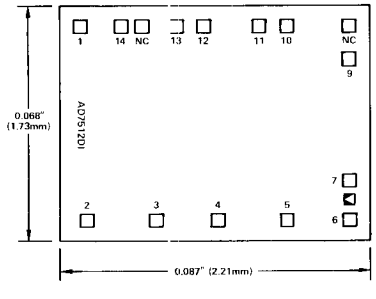


TERMINOLOGY

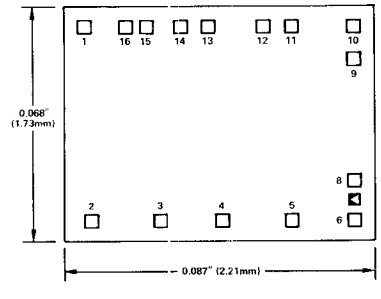
R_{ON}:	Ohmic resistance between terminals D and S.
R_{ON} Drift Match:	Difference between the R_{ON} drift of any two switches.
R_{ON} Match:	Difference between the R_{ON} of any two switches.
I_D (I_S)$_{OFF}$:	Current at terminals D or S. This is a leakage current when the switch is "OFF."
I_D (I_S)$_{ON}$:	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
V_D (V_S):	Analog voltage on terminal D (S).
C_S (CD):	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}:	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
C_{DD} (C_{SS}):	Capacitance between terminals D (S) of any two switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}:	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}:	Delay time between the 50% points of the digital input and switch "OFF" condition.
$t_{transition}$:	Delay time when switching from one address state to another.
V_{INL}:	Threshold voltage for the low state.
V_{INH}:	Threshold voltage for the high state.
I_{INL} (I_{INH}):	Input current of the digital input.
C_{IN}:	Input capacitance to ground of the digital input.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

BONDING DIAGRAMS (TOP VIEW)

AD7512DI



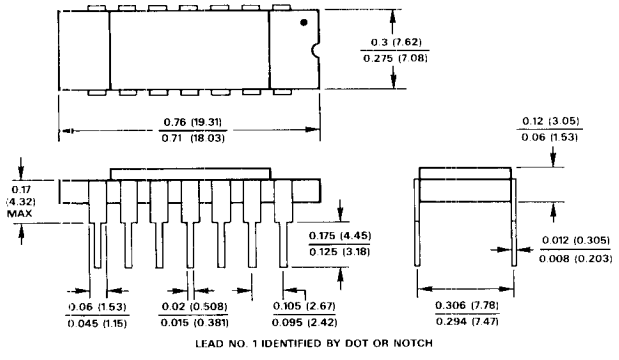
AD7510DI, AD7511DI



OUTLINE DIMENSIONS

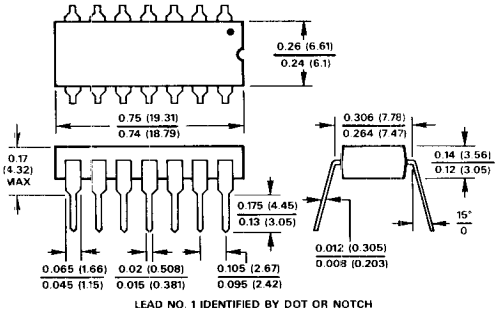
Dimensions shown in inches and (mm).

14-PIN CERAMIC DIP



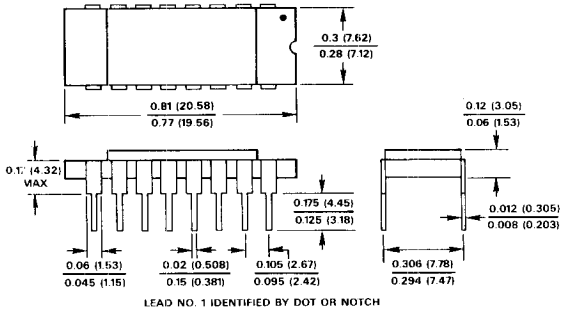
AD7512DI

14-PIN PLASTIC DIP



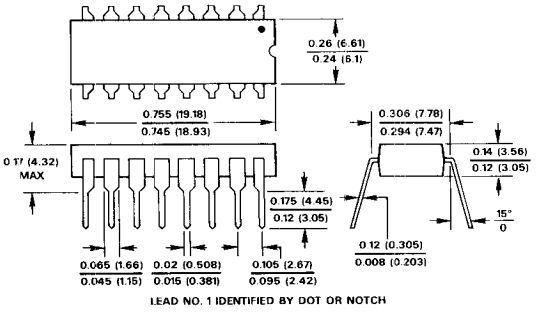
AD7512DI

16-PIN CERAMIC DIP



AD7510DI, AD7511DI

16-PIN PLASTIC DIP



AD7510DI, AD7511DI