±15 V Operation Digital Potentiometer

AD7376*

FEATURES
128 Position
Potentiometer Replacement
10 kΩ, 50 kΩ, 100 kΩ, 1 MΩ
Power Shutdown: Less than 1 μA
3-Wire SPI Compatible Serial Data Input
+5 V to +30 V Single Supply Operation
±5 V to ±15 V Dual Supply Operation
Midscale Preset

APPLICATIONS
Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage-to-Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching
Power Supply Adjustment

GENERAL DESCRIPTION

The AD7376 provides a single channel, 128-position digitally-controlled variable resistor (VR) device. This device performs the same electronic adjustment function as a potentiometer or variable resistor. These products were optimized for instrument and test equipment applications where a combination of high voltage with a choice between bandwidth or power dissipation are available as a result of the wide selection of end-to-end terminal resistance values. The AD7376 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the SPI-compatible serial-input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. The variable resistor offers a completely programmable value of resistance between the A terminal and the wiper or the B terminal and the wiper. The fixed A to B terminal resistance of 10 kΩ, 50 kΩ, 100 kΩ or 1 MΩ has a nominal temperature coefficient of –300 ppm/°C.

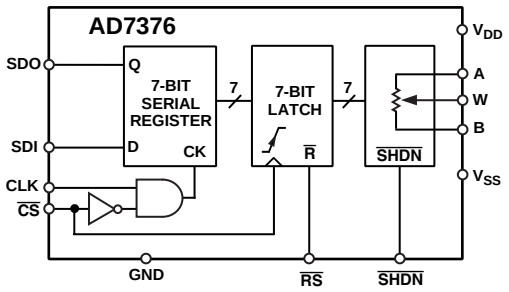
The VR has its own VR latch which holds its programmed resistance value. The VR latch is updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial-input digital interface. Seven data bits make up the data word clocked into the serial data input register (SDI). Only the last seven bits of the data word loaded are transferred into the 7-bit VR latch when the $\overline{CS}$ strobe is returned to logic high. A serial data output pin (SDO) at the opposite end of the serial register allows simple daisy-chaining in multiple VR applications without additional external decoding logic.

The reset ($\overline{RS}$) pin forces the wiper to the midscale position by loading 40_H into the VR latch. The $\overline{SHDN}$ pin forces the resistor

*Patent Number: 5495245

REV. 0

FUNCTIONAL BLOCK DIAGRAM



to an end-to-end open circuit condition on the A terminal and shorts the wiper to the B terminal, achieving a microwatt power shutdown state. When shutdown is returned to logic high, the previous latch settings put the wiper in the same resistance setting prior to shutdown as long as power to V_{DD} is not removed. The digital interface is still active in shutdown so that code changes can be made that will produce a new wiper position when the device is taken out of shutdown.

The AD7376 is available in both surface mount (SOL-16) and the 14-lead plastic DIP package. For ultracompact solutions selected models are available in the thin TSSOP package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C. For operation at lower supply voltages (+3 V to +5 V), see the AD8400/AD8402/AD8403 products.

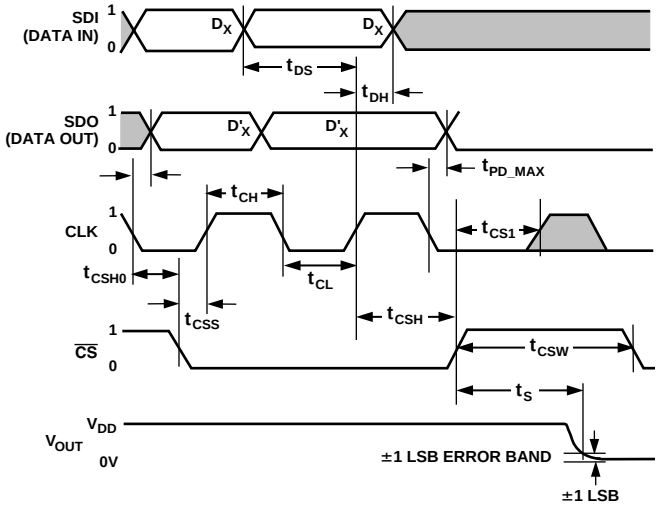


Figure 1. Detail Timing Diagram

The last seven data bits clocked into the serial input register will be transferred to the VR 7-bit latch when $\overline{CS}$ returns to logic high. Extra data bits are ignored.

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AD7376–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD}/V_{SS} = ±15 V ± 10% or ± 5 V ± 10%, $V_A = +V_{DD}$, $V_B = V_{SS}$/0 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE (Specifications Apply to All VRs)						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC	–1	±0.25	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–1	±0.5	+1	LSB
Nominal Resistor Tolerance	ΔR	T_A = +25°C	–30		30	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, Wiper = No Connect		–300		ppm/°C
Wiper Resistance	R_W	I_W = ±15 V/$R_{NOMINAL}$		120	200	Ω
Wiper Resistance	R_W	I_W = ±5 V/$R_{NOMINAL}$		200		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE (Specifications Apply to All VRs)						
Resolution	N		7			Bits
Integral Nonlinearity[3]	INL		–1	±0.5	+1	LSB
Differential Nonlinearity[3]	DNL		–1	±0.1	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 40_H		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = $7F_H$	–2	–0.5	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+0.5	+1	LSB
RESISTOR TERMINALS						
Voltage Range[4]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[5] A, B	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = 40_H		45		pF
Capacitance[5] W	C_W	f = 1 MHz, Measured to GND, Code = 40_H		60		pF
Shutdown Supply Current[6]	I_{A_SD}	$V_A = V_{DD}$, V_B = 0 V, SHDN = 0		0.01	1	μA
Shutdown Wiper Resistance	R_{W_SD}	$V_A = V_{DD}$, V_B = 0 V, SHDN = 0, V_{DD} = +15 V		170	400	Ω
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = +5 V or +15 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = +5 V or +15 V			0.8	V
Output Logic High	V_{OH}	R_L = 2.2 kΩ to +5 V	4.9			V
Output Logic Low[7]	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = +5 V, V_{DD} = +15 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or +15 V			±1	μA
Input Capacitance[5]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}/V_{SS}	Dual Supply Range	±4.5		±16.5	V
Power Supply Range	V_{DD}	Single Supply Range, V_{SS} = 0	4.5		28	V
Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD} = +5 V		0.0001	0.01	mA
Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD} = +15 V		0.75	2	mA
Supply Current	I_{SS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{SS} = –5 V or –15 V		0.02	0.1	mA
Power Dissipation[8]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD} = +15 V, V_{SS} = –15 V		11	30	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, or ΔV_{SS} = –5 V ± 10%		0.05	0.15	%/%
	PSS	ΔV_{DD} = +15 V ± 10% or ΔV_{SS} = –15 V ± 10%		0.01	0.02	%/%
DYNAMIC CHARACTERISTICS[5, 9, 10]						
Bandwidth –3 dB	BW_10K	R_{AB} = 10 kΩ, Code = 40_H		520		kHz
Bandwidth –3 dB	BW_50K	R_{AB} = 50 kΩ, Code = 40_H		125		kHz
Bandwidth –3 dB	BW_100K	R_{AB} = 100 kΩ, Code = 40_H		60		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.005		%
V_W Settling Time	t_S	V_A = 10 V, V_B = 0 V, ±1 LSB Error Band		4		μs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 25 kΩ, f = 1 kHz, $\overline{RS}$ = 0		14		nV√Hz
INTERFACE TIMING CHARACTERISTICS (Applies to All Parts [Notes 5, 11])						
Input Clock Pulsewidth	t_{CH}, t_{CL}	Clock Level High or Low	120			ns
Data Setup Time	t_{DS}		30			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay[12]	t_{PD}	R_L = 2.2 kΩ, C_L < 20 pF	10		100	ns
$\overline{CS}$ Setup Time	t_{CSS}		120			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		150			ns
Reset Pulsewidth	t_{RS}		120			ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		120			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		120			ns

NOTES

[1]Typicals represent average readings at +25°C, V_{DD} = +15 V, and V_{SS} = –15 V.

[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 27. Test Circuit.

[3]INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions. See Figure 26. Test Circuit.

[4]Resistor terminals A, B, W have no limitations on polarity with respect to each other.

[5]Guaranteed by design and not subject to production test.

[6]Measured at the A terminal. A terminal is open circuit in shutdown mode.

[7]I_{OL} = 200 μA for the 50 kΩ version operating at V_{DD} = +5 V.

[8]P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[9]Bandwidth, noise and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

[10]All dynamic characteristics use V_{DD} = +15 V and V_{SS} = –15 V.

[11]See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using both V_{DD} = +5 V or +15 V.

[12]Propagation delay depends on value of V_{DD}, R_L and C_L see Applications section.

Specifications subject to change without notice.

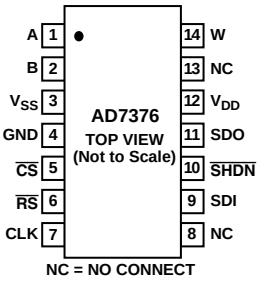
ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

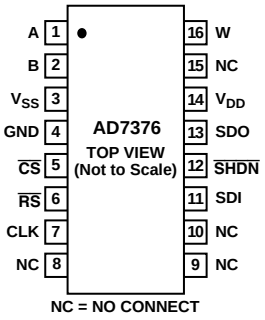
V_{DD} to GND ..... –0.3 V, +30 V
V_{SS} to GND ..... +0.3 V, –16.5 V
V_{DD} to V_{SS} ..... –0.3 V, +44 V
V_A, V_B, V_W to GND ..... V_{SS}, V_{DD}
$A_X – B_X$, $A_X – W_X$, $B_X – W_X$ ..... ±20 mA
Digital Input Voltages to GND ..... 0 V, V_{DD} + 0.3 V
Digital Output Voltage to GND ..... 0 V, +30 V
Operating Temperature Range ..... –40°C to +85°C
Maximum Junction Temperature (T_J MAX) ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_J MAX – T_A)/θ_{JA}
Thermal Resistance θ_{JA}
P-DIP (N-14) ..... 92°C/W
SOIC (SOL-16) ..... 120°C/W
TSSOP-14 ..... 240°C/W

PIN CONFIGURATIONS

PDIP & TSSOP-14



SOL-16



ORDERING GUIDE

Model	kΩ	Temperature Range	Package Description	Package Options
AD7376AN10	10	–40°C to +85°C	PDIP-14	N-14
AD7376AR10	10	–40°C to +85°C	SOL-16	R-16
AD7376ARU10	10	–40°C to +85°C	TSSOP-14	RU-14
AD7376AN50	50	–40°C to +85°C	PDIP-14	N-14
AD7376AR50	50	–40°C to +85°C	SOL-16	R-16
AD7376ARU50	50	–40°C to +85°C	TSSOP-14	RU-14
AD7376AN100	100	–40°C to +85°C	PDIP-14	N-14
AD7376AR100	100	–40°C to +85°C	SOL-16	R-16
AD7376ARU100	100	–40°C to +85°C	TSSOP-14	RU-14
AD7376AN1M	1,000	–40°C to +85°C	PDIP-14	N-14
AD7376AR1M	1,000	–40°C to +85°C	SOL-16	R-16
AD7376ARU1M	1,000	–40°C to +85°C	TSSOP-14	RU-14

Die Size: 101.6 mil × 127.6 mil, 2.58 mm × 3.24 mm
Number Transistors: 840

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7376 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD7376–Typical Performance Characteristics

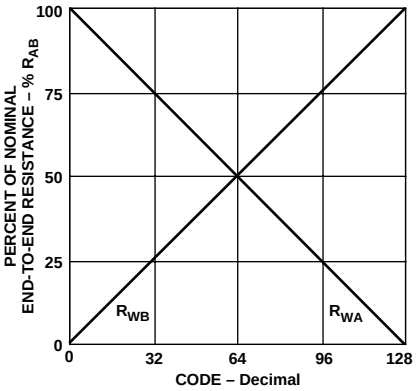


Figure 2. Wiper To End Terminal Percent Resistance vs. Code

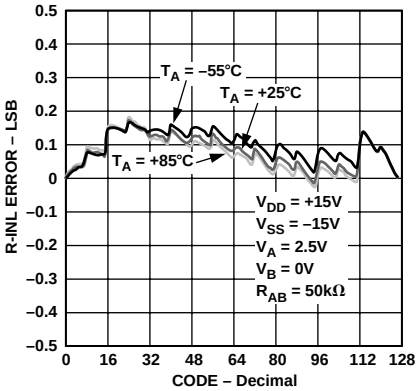


Figure 3. Resistance Step Position Nonlinearity Error vs. Code

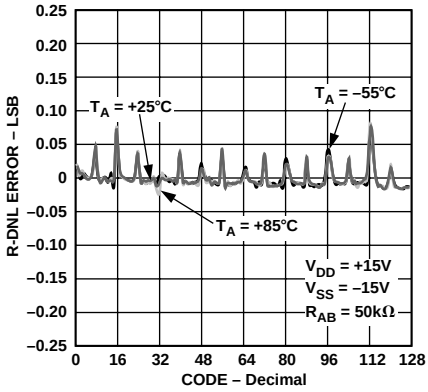


Figure 4. Relative Resistance Step Change from Ideal vs. Code

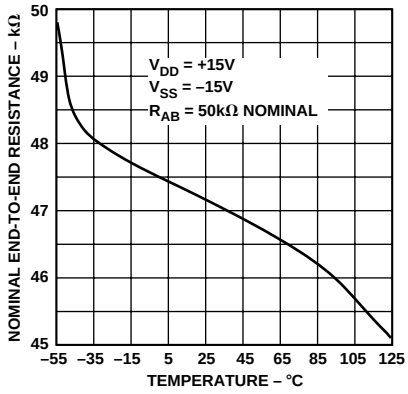


Figure 5. Nominal Resistance vs. Temperature

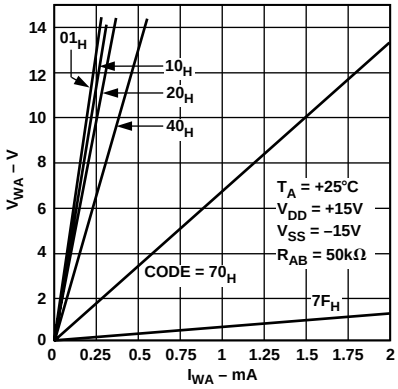


Figure 6. Resistance Linearity vs. Conduction Current

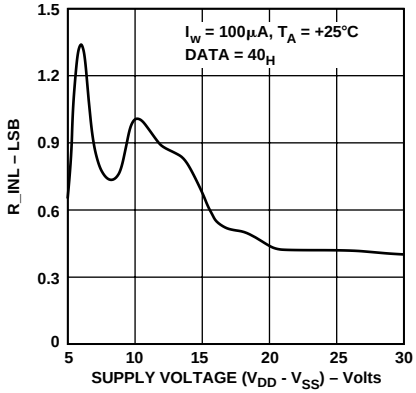


Figure 7. Resistance Nonlinearity Error vs. Supply Voltage

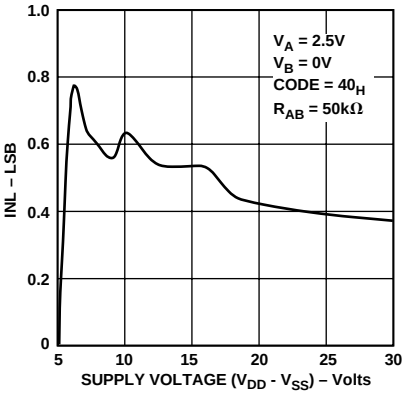


Figure 8. Potentiometer Divider Nonlinearity Error vs. Supply Voltage

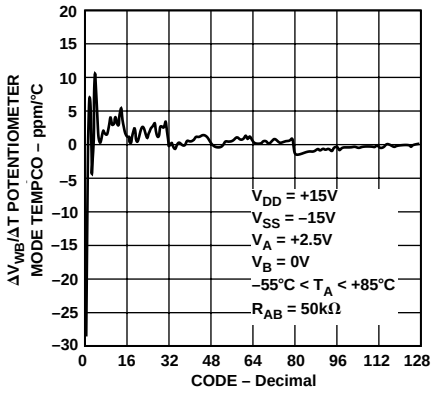


Figure 9. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco

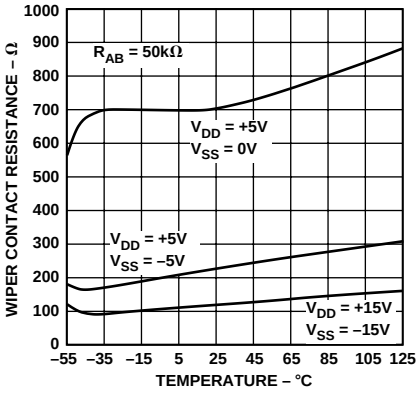


Figure 10. Wiper Contact Resistance vs. Temperature

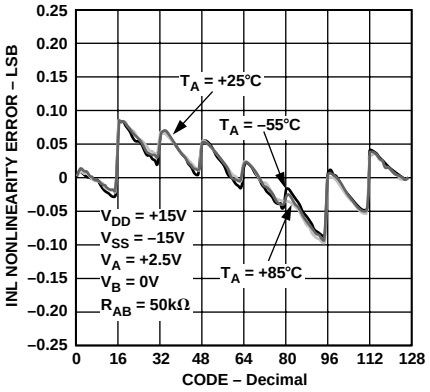


Figure 11. Potentiometer Divider Nonlinearity Error vs. Code

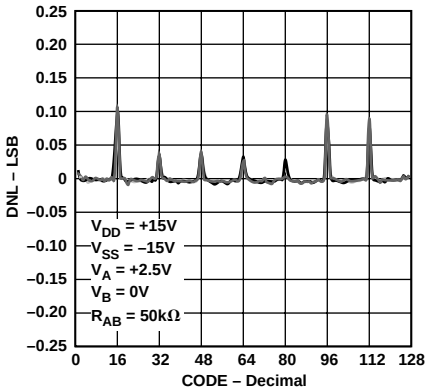


Figure 12. Potentiometer Divider Differential Nonlinearity Error vs. Code

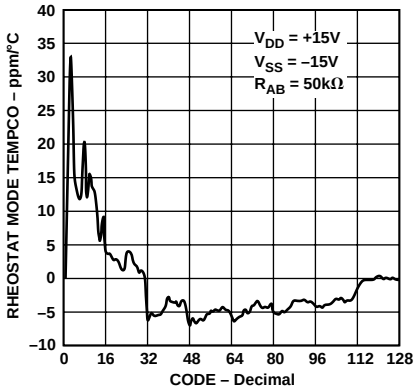


Figure 13. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco

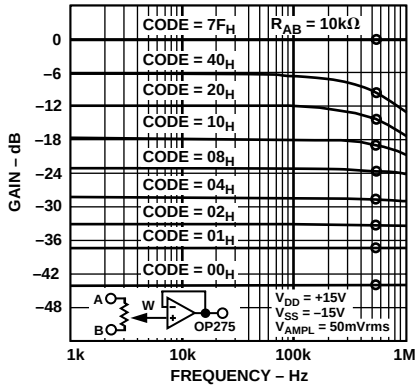


Figure 14. 10 kΩ Gain vs. Frequency vs. Code

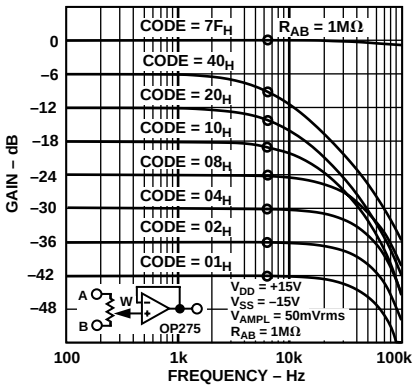


Figure 15. 1 MΩ Gain vs. Frequency vs. Code

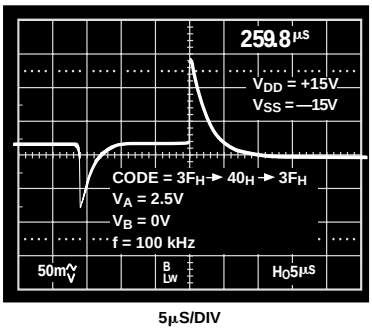


Figure 16. Midscale Transition Glitch

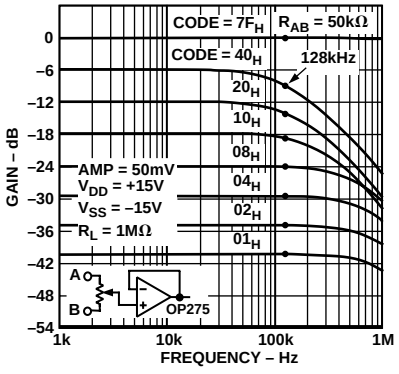


Figure 17. 50 kΩ Gain vs. Frequency vs. Code

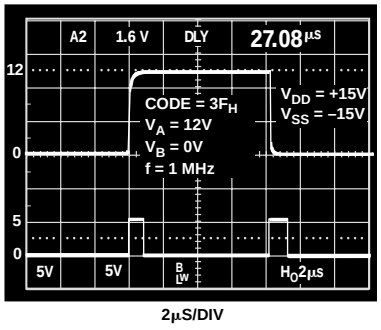


Figure 18. Large Signal Settling Time

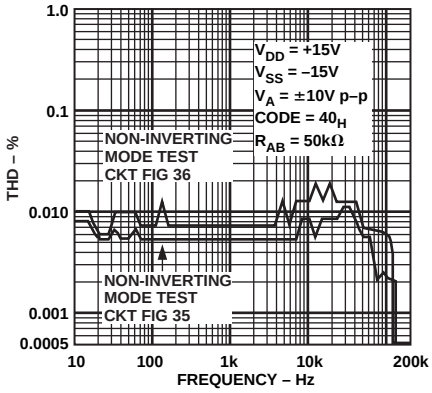


Figure 19. Total Harmonic Distortion Plus Noise vs. Frequency

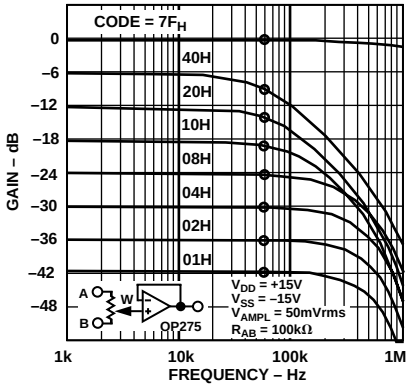


Figure 20. 100 kΩ Gain vs. Frequency vs. Code

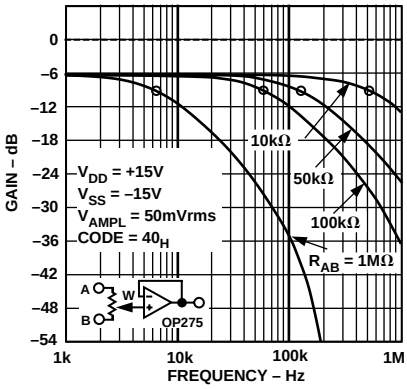


Figure 21. –3 dB Bandwidth vs. Nominal Resistance

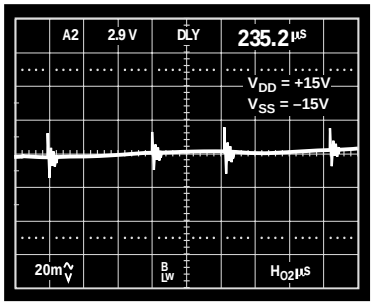


Figure 22. Clock Feedthrough

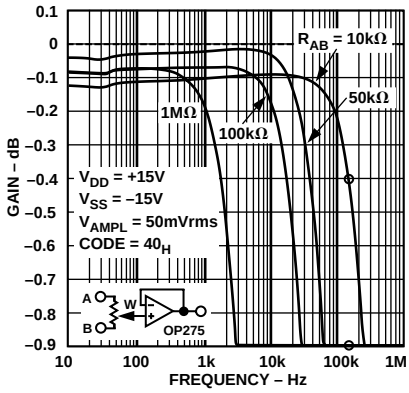


Figure 23. Gain Flatness vs Frequency vs. Nominal Resistance R_{AB}

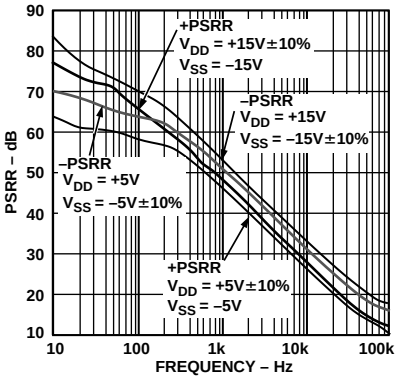


Figure 24. Power Supply Rejection vs. Frequency

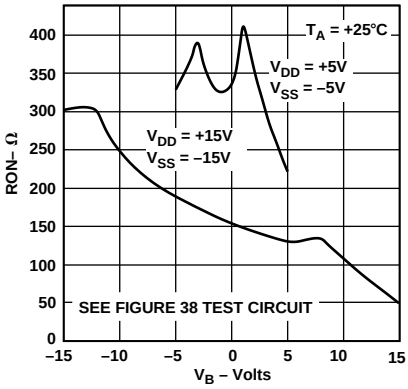


Figure 25. Incremental Wiper Contact Resistance vs. Common-Mode Voltage

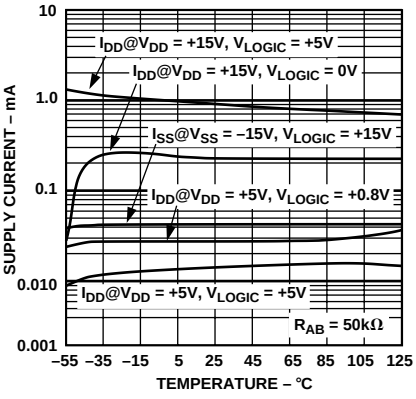


Figure 26. Supply Current (I_{DD}, I_{SS}) vs. Temperature

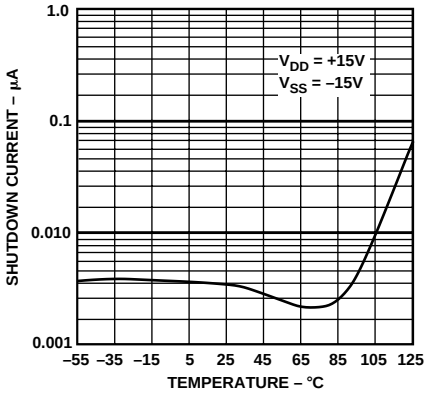


Figure 27. I_{A_SD} Shutdown Current vs. Temperature

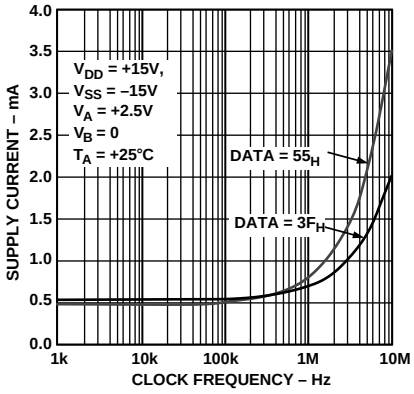


Figure 28. I_{DD} Supply Current vs. Input Clock Frequency

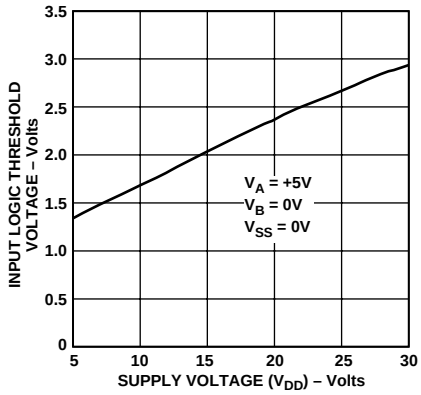


Figure 29. Input Logic Threshold Voltage vs. V_{DD} Supply Voltage

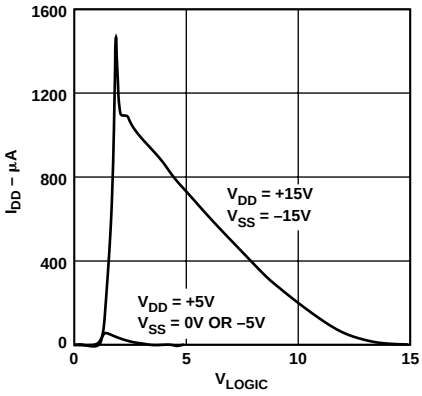


Figure 30. Supply Current (I_{DD}) vs. Logic Voltage

PARAMETRIC TEST CIRCUITS

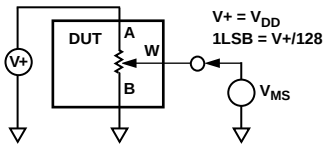


Figure 31. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

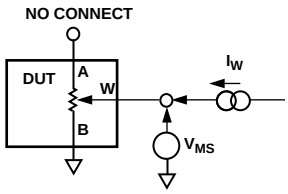


Figure 32. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

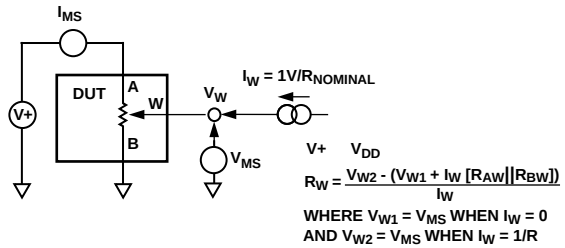


Figure 33. Wiper Resistance Test Circuit

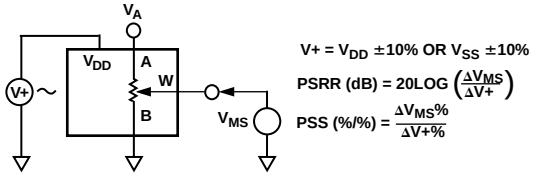


Figure 34. Power Supply Sensitivity Test Circuit (PSS, PSRR)

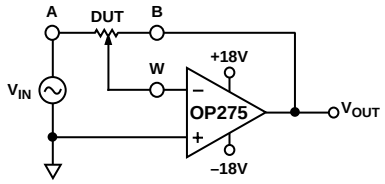


Figure 35. Inverting Programmable Gain Test Circuit

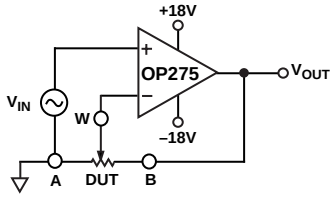


Figure 36. Noninverting Programmable Gain Test Circuit

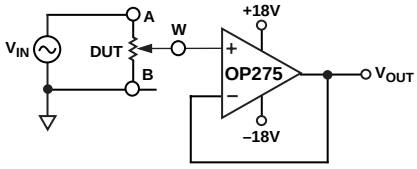


Figure 37. Gain vs. Frequency Test Circuit

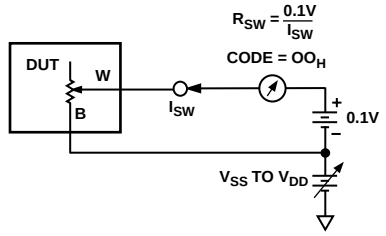


Figure 38. Incremental ON Resistance Test Circuit

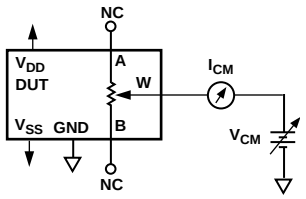


Figure 39. Common-Mode Leakage Current Test Circuit

OPERATION

The AD7376 provides a 128-position digitally-controlled variable resistor (VR) device. Changing the programmed VR settings is accomplished by clocking in a 7-bit serial data word into the SDI (Serial Data Input) pin, while $\overline{CS}$ is active low. When $\overline{CS}$ returns high the last seven bits are transferred into the RDAC latch setting the new wiper position. The exact timing requirements are shown in Figure 1.

The AD7376 resets to a midscale by asserting the $\overline{RS}$ pin, simplifying initial conditions at power-up. Both parts have a power shutdown $\overline{SHDN}$ pin which places the RDAC in a zero power consumption state where terminal A is open circuited and the wiper W is connected to B, resulting in only leakage currents being consumed in the VR structure. In shutdown mode the VR latch settings are maintained so that, returning to operational mode from power shutdown, the VR settings return to their previous resistance values.

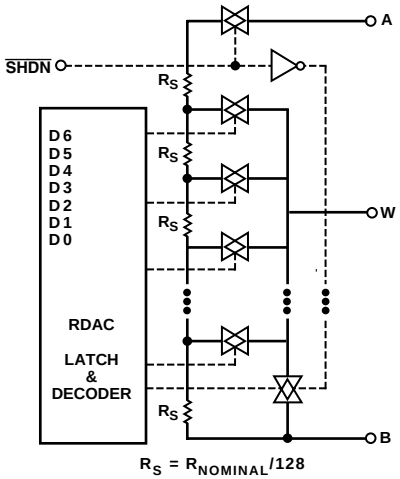


Figure 40. AD7376 Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B are available with values of 10 kΩ, 50 kΩ, 100 kΩ and 1 MΩ. The final three characters of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 50 kΩ = 50; 100 kΩ = 100; 1 MΩ = 1M. The nominal resistance (R_{AB}) of the VR has 128 contact points accessed by the wiper terminal, plus the B terminal contact. The 7-bit data word in the RDAC latch is decoded to select one of the 128 possible settings. The wiper's first connection starts at the B terminal for data 00_H. This B–terminal connection has a wiper contact resistance of 120 Ω. The second connection (10 kΩ part) is the first tap point located at 198 Ω (= R_{BA} [nominal resistance]/128 + R_W = 78 Ω + 120 Ω) for data 01_H. The third connection is the next tap point representing 156 + 120 = 276 Ω for data 02_H. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10041 Ω. The wiper does not directly connect to the B terminal. See Figure 40 for a simplified diagram of the equivalent RDAC circuit.

The general transfer equation that determines the digitally programmed output resistance between W and B is:

$$R_{WB}(D) = (D)/128 \times R_{BA} + R_W \quad (1)$$

where D is the data contained in the 7-bit VR latch, and R_{BA} is the nominal end-to-end resistance.

For example, when V_B = 0 V and A–terminal is open circuit, the following output resistance values will be set for the following VR latch codes (applies to the 10 kΩ potentiometer).

Table I.

D (DEC)	R_{WB} (Ω)	Output State
127	10041	Full-Scale
64	5120	Midscale ($\overline{RS}$ = 0 Condition)
1	276	1 LSB
0	198	Zero-Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 120 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum value of 5 mA to avoid degradation or possible destruction of the internal switch contact.

Like the mechanical potentiometer the RDAC replaces, it is totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled resistance R_{WA}. When these terminals are used the B–terminal should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equation for this operation is:

$$R_{WA}(D) = (128\text{-}D)/128 \times R_{BA} + R_W \quad (2)$$

where D is the data contained in the 7-bit RDAC latch, and R_{BA} is the nominal end-to-end resistance. For example, when V_A = 0 V and B–terminal is tied to the wiper W the following output resistance values will be set for the following RDAC latch codes.

Table II.

D (DEC)	R_{WA} (Ω)	Output State
127	74	Full-Scale
64	5035	Midscale ($\overline{RS}$ = 0 Condition)
1	9996	1 LSB
0	10035	Zero-Scale

The typical distribution of R_{BA} from device to device matching is process lot dependent having a ±30% variation. The change in RBA with temperature has a –300 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example connecting A–terminal to +5 V and B–terminal to ground produces an output voltage at the wiper which can be any value starting at zero volts up to 1 LSB less than +5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 128-position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to terminals AB is:

$$V_W(D) = D/128 \times V_{AB} + V_B$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors, not the absolute value; therefore, the drift improves to 5 ppm/°C.

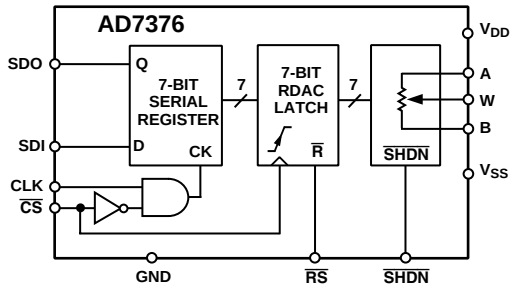


Figure 41. Block Diagram

DIGITAL INTERFACING

The AD7376 contains a standard three-wire serial input control interface. The three inputs are clock (CLK), $\overline{CS}$ and serial data input (SDI). The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation they should be debounced by a flip-flop or other suitable means. When $\overline{CS}$ is taken active low the clock loads data into the serial register on each positive clock edge, see Table III. The last seven bits clocked into the serial register will be transferred to the 7-bit RDAC latch, see Figure 41. Extra data bits are ignored. The serial-data-output (SDO) pin contains an open drain n-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. This allows for daisy chaining several RDACs from a single processor serial data line. Clock period needs to be increased when using a pull-up resistor to the SDI pin of the following device in the series. Capacitive loading at the daisy chain node SDO-SDI between devices must be accounted for to successfully transfer data. When daisy chaining is used, the $\overline{CS}$ should be kept low until all the bits of every package are clocked into their respective serial registers insuring that the data bits are in the proper decoding location. This would require 14 bits of data when two AD7376 RDACs are daisy chained. During shutdown ($\overline{SHDN}$) the SDO output pin is forced to the off (logic high state) to disable power dissipation in the pull up resistor. See Figure 42 for equivalent SDO output circuit schematic.

Table III. Input Logic Control Truth Table

CLK	$\overline{CS}$	$\overline{RS}$	$\overline{SHDN}$	Register Activity
L	L	H	H	Enables SR, enables SDO pin.
P	L	H	H	Shifts one bit in from the SDI pin. The seventh previously entered bit is shifted out of the SDO pin.
X	P	H	H	Loads SR data into 7-bit RDAC latch.
X	H	H	H	No Operation.
X	X	L	H	Sets 7-bit RDAC latch to midscale, wiper centered, and SDO latch cleared.
X	H	P	H	Latches 7-bit RDAC latch to 40_H.
X	H	H	L	Opens circuits resistor A–terminal, connects W to B, turns off SDO output transistor.

NOTE
P = positive edge, X = don't care, SR = shift register.

The data setup and data hold times in the specification table determine the data valid time requirements. The last seven bits of the data word entered into the serial register are held when $\overline{CS}$ returns high. At the same time $\overline{CS}$ goes high it transfers the 7-bit data to the VR latch.

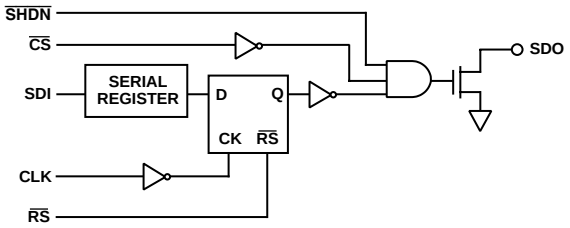


Figure 42. Detail SDO Output Schematic of the AD7376

All digital inputs are protected with a series input resistor and parallel Zener ESD structure shown in Figure 43. Applies to digital input pins $\overline{CS}$, SDI, SDO, $\overline{RS}$, $\overline{SHDN}$, CLK

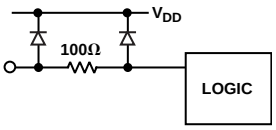


Figure 43. Equivalent ESD Protection Circuit

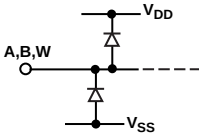
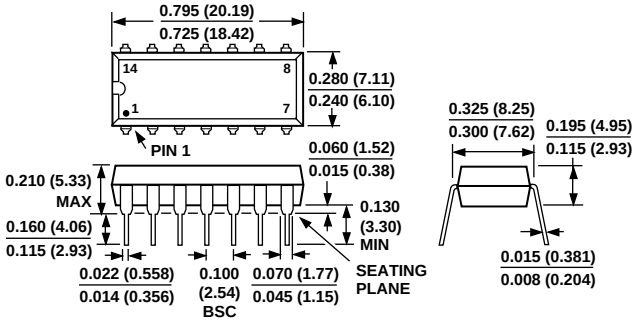


Figure 44. Equivalent ESD Protection Analog Pins

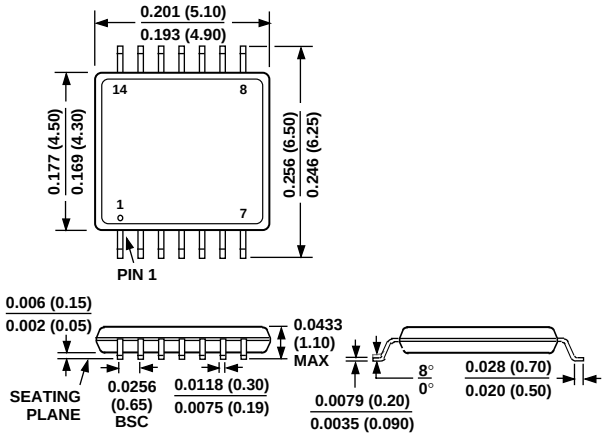
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

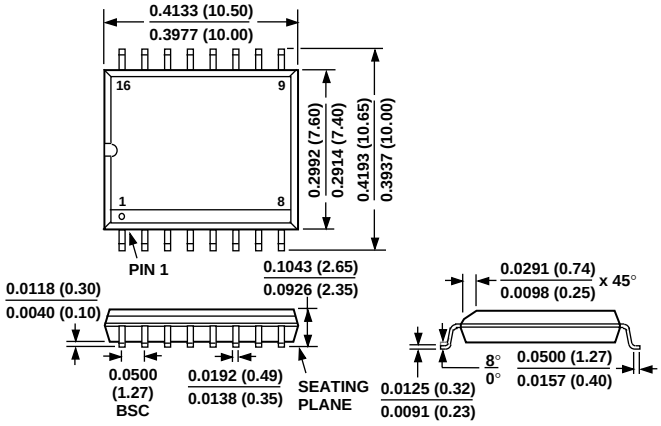
14-Lead Plastic DIP
(N-14)



14-Lead TSSOP
(RU-14)



16-Lead Wide Body SOIC
(R-16)



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