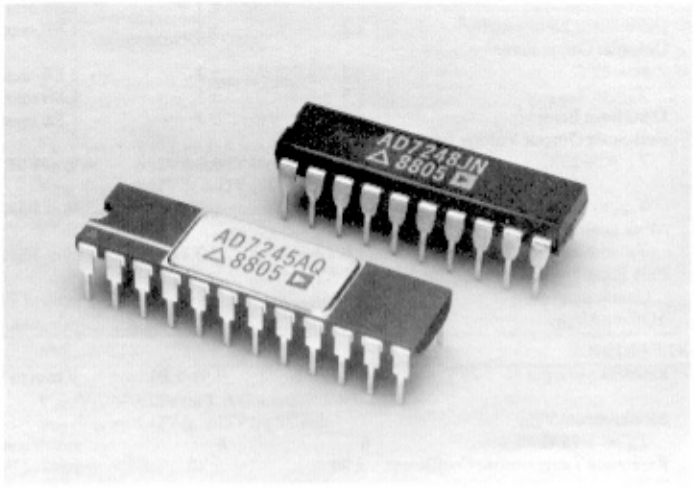
LC²MOS 12-Bit DACPORT

AD7245/AD7248

FEATURES

12-Bit CMOS DAC with Output Amplifier and Reference
Parallel Loading Structure: AD7245
(8+4) Loading Structure: AD7248
Single or Dual Supply Operation
Fast Digital Interface (80ns $\overline{WR}$ Pulse)
Low Power (65mW typ)
0.3", Skinny, 20- and 24-Pin DIP
20- and 28-Terminal Surface Mount Packages



GENERAL DESCRIPTION

The AD7245/AD7248 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The part features double-buffered interface logic with a 12-bit input latch and 12-bit DAC latch. The data held in the DAC latch determines the analog output of the converter. The AD7245 accepts 12-bit parallel data which is latched into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$. The AD7248 has an 8-bit-wide data bus, and data is loaded to the input latch in two write operations, an 8-bit LSB load and a 4-bit MSB load. The input data must be right justified. For both parts, an asynchronous $\overline{LDAC}$ signal transfers data from the input latch to the DAC latch. The AD7245 also has a $\overline{CLR}$ signal on the DAC latch which allows features such as power-on reset to be implemented. All logic inputs are level triggered and are TTL and CMOS (5V) level compatible, while the control logic is speed compatible with most microprocessors.

The on-chip 5V buried Zener diode provides a low-noise, temperature compensated reference for the DAC. The gain setting resistors allow a number of ranges at the output: 0 to +5V, 0 to +10V when using single supply and 0 to +5V, −5V to +5V when operated in dual supplies. The output amplifier is capable of developing +10V across a 2kΩ load to GND.

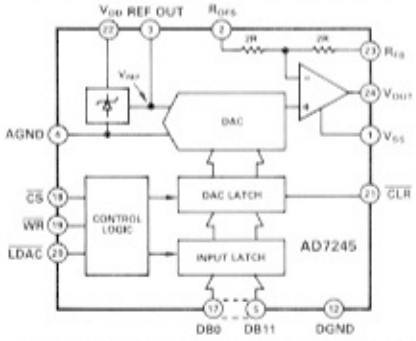
The AD7245/AD7248 is fabricated in an all ion-implanted, high-speed linear, compatible CMOS (LC²MOS) process. The AD7245 is packaged in a small, 0.3"-wide, 24-pin DIP and 28-terminal surface mount packages. The AD7248 is available in a 0.3"-wide, 20-pin DIP and 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

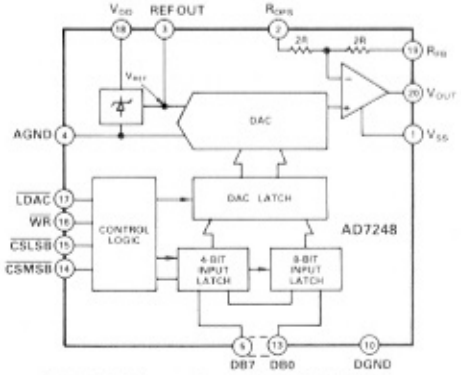
1. Complete 12-Bit DACPORT™
   The AD7245/AD7248 is a complete, voltage output, 12-bit DAC on one chip. This single-chip design of the DAC reference and output amplifier is inherently more reliable than multichip designs.

DACPORT is a trademark of Analog Devices, Inc.

2. Microprocessor Compatibility
   The parallel loading structure of the AD7245 allows connection to microprocessors with a 16-bit-wide data bus. The AD7248 is aimed at microprocessors which have an 8-bit-wide data bus structure. The high-speed logic of both parts allows direct interfacing to most modern microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7245/AD7248 in multiple DAC systems.



AD7245 Functional Block Diagram



AD7248 Functional Block Diagram

One Technology Way; P. O. Box 9106; Norwood, MA 02062-9106
Tel: 617/329-4700 **TWX: 710/394-6577**

West Coast	Central	Atlantic
714/641-9391	214/231-5094	215/643-7790

SPECIFICATIONS

SINGLE SUPPLY

(V_{DD} = +15V ± 5%[1]. V_{SS} = AGND = DGND = 0V; R_L = 2kΩ to GND; C_L = 100pF to GND; REF OUT unloaded unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Version[2]	S Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy	± 1		LSB max	
		± 1	LSB max	V_{DD} = +11.4V to +14.25V
		± 1.5	LSB max	V_{DD} = +14.25V to +15.75V
Differential Nonlinearity[3]	± 1	± 1	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]				
at +25°C	± 3	± 3	LSB max	
T_{min} to T_{max}	± 5	± 5	LSB max	Typical Tempco is ± 3ppm of FSR[4]/°C
DAC Gain Error[3,5]	± 2	± 2	LSB max	
Full-Scale Output Voltage Error[6]				
T_A = +25°C	± 0.2	± 0.2	% of FSR max	V_{DD} = +15V for J, A Grades; V_{DD} = +12V & +15V for S Grade
T_{min} to T_{max}		± 0.6	% of FSR max	V_{DD} = +12V & +15V
ΔFull Scale/ΔV_{DD}				
T_A = +25°C	± 0.12	± 0.12	% of FSR/V max	ΔV_{DD} = +5%
Full-Scale Temperature Coefficient[7]	± 30		ppm of FSR/°C max	
ΔOffset/ΔV_{DD}	± 1	± 2	mV max	ΔV_{DD} = ±5%
REFERENCE				
Reference Output @ +25°C	4.99/5.01	4.99/5.01	V min to V max	V_{DD} = +15V for J, A Grades; V_{DD} = +12V & +15V for S Grade
ΔReference/ΔV_{DD}				
T_A = +25°C	6	6	mV/V max	ΔV_{DD} = ±5%
Reference Temperature Coefficient	± 30	± 40	ppm of FSR/°C typ	FSR = 5V
Reference Load Sensitivity (ΔReference/ΔI)	± 1	± 1.5	mV max	Reference Load Current Change (0-100μA)
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN} (Data Inputs)				V_{IN} = 0V or V_{DD}
at +25°C	± 1	± 1	μA max	
T_{min} to T_{max}	± 10	± 10	μA max	
I_{INH} (Control Inputs)[8]				V_{IN} = V_{DD}
at +25°C	± 1	± 1	μA max	
T_{min} to T_{max}	± 10	± 10	μA max	
I_{INL} (Control Inputs)[8]				V_{IN} = 0V
at +25°C	150	150	μA max	
T_{min} to T_{max}	200	200	μA max	
Input Capacitance[9] (AD7245)	8	8	pF max	
Input Capacitance[9] (AD7248)	16	16	pF max	
ANALOG OUTPUT				
Output Range Resistors	15/30	15/30	kΩ min/kΩ max	
Ranges	+5, +10	+5, +10	V	Pin Strappable. Min Load Resistance is 2kΩ to GND
dc Output Impedance	0.5	0.5	Ω typ	
Short-Circuit Current	40	40	mA typ	
DYNAMIC PERFORMANCE[9]				
Output Voltage Settling Time				Settling Time to ± 1LSB. R_L = 5kΩ, C_L = 100pF
Positive Full-Scale Change	5	8	μs max	DAC Register all 0s to all 1s
Negative Full-Scale Change	10	10	μs typ	DAC Register all 1s to all 0s
Output Voltage Slew Rate	2	1.5	V/μs min	
Digital Feedthrough[1,10]	10	10	nV secs typ	
Digital-to-Analog Glitch Impulse	30	30	nV secs typ	Major Carry Transition
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	11.4/15.75	V min/V max	For Specified Performance
I_{DD}				Output Unloaded
at +25°C	9	9	mA max	Typically 4.5mA
T_{min} to T_{max}	12	12	mA max	

NOTES

[1]For the S Version only: V_{DD} = +12V ± 5% to +15V ± 5%

[2]Temperature ranges are as follows:
J Version, 0 to +70°C
A Version, −25°C to +85°C
S Version, −55°C to +125°C.

[3]See Terminology.

[4]FSR means Full-Scale Range and is 5V with R_{OFS} connected to R_{FB}, V_{OUT} and 10V with R_{OFS} connected to GND and R_{FB} connected to V_{OUT}.

[5]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

[6]This error is calculated w.r.t. an ideal 4.9988V (on the 5V range) or 9.9976V (on the 10V range).
It includes the effects of internal voltage reference, gain and offset errors.

[7]Full-scale T.C. = ΔFS/ΔT, where ΔFS is the full-scale change from T_A = +25°C to T_{min} or T_{max}.

[8]Control inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$ and $\overline{CLR}$ for AD7245 and $\overline{CSMSB}$, $\overline{CSLSB}$, $\overline{WR}$ and $\overline{LDAC}$ for AD7248.

[9]Sample tested at +25°C to ensure compliance.

[10]The metal lid on the AD7245 (only) ceramic (D-24A) package is connected to Pin 12 (DGND).

Specifications subject to change without notice.

SPECIFICATIONS

DUAL SUPPLY (V_{DD} = +15V ±5%[1], V_{SS} = −15V ±5%[1], AGND = DGND = 0V; R_L = 2kΩ to GND; C_L = 100pF to GND; REF OUT unloaded unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Version[2]	S Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1		LSB max	
		±1	LSB max	V_{DD}/V_{SS} = ±11.4V to ±14.25V
		±1.5	LSB max	V_{DD}/V_{SS} = ±14.25V to ±15.75V
Differential Nonlinearity[3]	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Offset Error[3]				R_{OFS} Connected to REF OUT
at +25°C	±3	±3	LSB max	
T_{min} to T_{max}	±5	±5	LSB max	Typical Tempco is ±3ppm of FSR[4]/°C
DAC Gain Error[3,5]	±2	±2	LSB max	
Full-Scale Output Voltage Error[6]				
T_A = +25°C	±0.2	±0.2	% of FSR max	V_{DD}/V_{SS} = ±15V for J, A Grades; V_{DD}/V_{SS} = ±12V & ±15V for S Grade
T_{min} to T_{max}		±0.6	% of FSR max	V_{DD}/V_{SS} = ±12V & ±15V
ΔFull Scale/ΔV_{DD}				
T_A = +25°C	±0.12	±0.12	% of FSR/V max	ΔV_{DD} = ±5%
ΔFull Scale/ΔV_{SS}				
T_A = +25°C	±0.01	±0.01	% of FSR/V max	ΔV_{SS} = ±5%
Full-Scale Temperature Coefficient[7]	±30		ppm of FSR/°C max	
ΔOffset/ΔV_{DD}	±1	±2	mV max	ΔV_{DD} = ±5%
ΔOffset/ΔV_{SS}	±1	±1	mV max	ΔV_{SS} = ±5%
REFERENCE				
Reference Output @ +25°C	4.99/5.01	4.99/5.01	V min to V max	V_{DD}/V_{SS} = ±15V for J, A Grades; V_{DD}/V_{SS} = ±12V & ±15V for S Grade
ΔReference/ΔV_{DD}				
T_A = +25°C	6	6	mV/V max	ΔV_{DD} = ±5%
Reference Temperature Coefficient	±30	±40	ppm of FSR/°C typ	FSR = 5V
Reference Load Sensitivity (ΔReference/ΔI)	±1	±1.5	mV max	Reference Load Current Change (0-100μA) (Not Including R_{OFS} Current)
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN} (Data Inputs)				V_{IN} = 0V or V_{DD}
at +25°C	±1	±1	μA max	
T_{min} to T_{max}	±10	±10	μA max	
I_{INH} (Control Inputs)[8]				V_{IN} = V_{DD}
at +25°C	±1	±1	μA max	
T_{min} to T_{max}	±10	±10	μA max	
I_{INL} (Control Inputs)[8]				V_{IN} = 0V
at +25°C	150	150	μA max	
T_{min} to T_{max}	200	200	μA max	
Input Capacitance[9] (AD7245)	8	8	pF max	
Input Capacitance[9] (AD7248)	16	16	pF max	
ANALOG OUTPUT				
Output Range Resistors	15/30	15/30	kΩ min/kΩ max	
Ranges	±5, +5	±5, +5	V	Pin Strappable. Min Load Resistance is 2kΩ to GND
dc Output Impedance	0.5	0.5	Ω typ	
Short-Circuit Current	40	40	mA typ	
DYNAMIC PERFORMANCE[9]				
Output Voltage Settling Time				Settling Time to ±1LSB. R_L = 5kΩ, C_L = 100pF
Positive Full-Scale Change	5	10	μs max	DAC Register all 0s to all 1s
Negative Full-Scale Change	10	10	μs max	DAC Register all 1s to all 0s
Output Voltage Slew Rate	2	1.5	V/μs min	
Digital Feedthrough[3,10]	10	10	nV secs typ	
Digital-to-Analog Glitch Impulse	30	30	nV secs typ	Major Carry Transition
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	11.4/15.75	V min/V max	For Specified Performance
V_{SS} Range	−14.25/−15.75	−11.4/−15.75	V min/V max	For Specified Performance
I_{DD}				Output Unloaded
at +25°C	9	9	mA max	Typically 5mA
T_{min} to T_{max}	12	12	mA max	
I_{SS}				Output Unloaded
at +25°C	3	3	mA max	Typically 2mA
T_{min} to T_{max}	5	5	mA max	

NOTES

[1]For the S Version only: V_{DD} = +12V ±5% to +15V ±5%; V_{SS} = −12V ±5% to −15V ±5%.

[2]Temperature ranges are as follows:
J Version, 0 to +70°C
A Version, −25°C to +85°C
S Version, −55°C to +125°C.

[3]See Terminology.

[4]FSR means Full-Scale Range and is 5V with R_{OFS} connected to R_{FB}, V_{OUT} and 10V with R_{OFS} connected to GND and R_{FB} connected to V_{OUT}.

[5]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

[6]This error is calculated w.r.t. an ideal 4.9988V (on the 5V range) or 9.9976V (on the 10V range).
It includes the effects of internal voltage reference, gain and offset errors.

[7]Full-scale T.C. = $\Delta FS/\Delta T$, where ΔFS is the full-scale change from T_A = +25°C to T_{min} or T_{max}.

[8]Control inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$ and $\overline{CLR}$ for AD7245 and $\overline{CSMSB}$, $\overline{CSLSB}$, $\overline{WR}$ and $\overline{LDAC}$ for AD7248.

[9]Sample tested at +25°C to ensure compliance.

[10]The metal lid on the AD7245 (only) ceramic (D-24A) package is connected to Pin 12 (DGND).

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1] (V_{DD} = +15V ±5%[2]; V_{SS} = 0V or −15V ±5%[2]; See Figures 5 and 7)

Parameter	J Grade	A Grade	S Grade	Units	Conditions
t_1					
@ +25°C	80	80	105	ns min	Chip Select Pulse Width
T_{min} to T_{max}	100	100	135	ns min	
t_2					
@ +25°C	80	80	105	ns min	Write Pulse Width
T_{min} to T_{max}	100	100	135	ns min	
t_3					
@ +25°C	0	0	0	ns min	Chip Select to Write Setup Time
T_{min} to T_{max}	0	0	0	ns min	
t_4					
@ +25°C	0	0	0	ns min	Chip Select to Write Hold Time
T_{min} to T_{max}	0	0	0	ns min	
t_5 (AD7245 Only)					
@ +25°C	100	100	155	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	110	130	250	ns min	
t_5 (AD7248 Only)					
@ +25°C	110	110	180	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	130	130	270	ns min	
t_6					
@ +25°C	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	ns min	
t_7					
@ +25°C	80	80	90	ns min	Load DAC Pulse Width
T_{min} to T_{max}	100	100	120	ns min	
t_8 (AD7245 Only)					
@ +25°C	80	80	140	ns min	Clear Pulse Width
T_{min} to T_{max}	100	100	200	ns min	

NOTE
[1]Sample tested at +25°C to ensure compliance.
[2]For the S Version only: V_{DD} = +12V ±5% to +15V ±5%; V_{SS} = 0V or −12V ±5% to −15V ±5%. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V, +17V
V_{DD} to DGND . . . . . −0.3V, +17V
V_{DD} to V_{SS} . . . . . −0.3V, +34V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
V_{OUT} to V_{SS}[1] . . . . . 0V, +24V
V_{OUT} to V_{DD}[1] . . . . . −32V, 0V
REF OUT[1] to AGND . . . . . 0V, V_{DD}
Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature
Commercial . . . . . 0 to +70°C
Industrial . . . . . −25°C to +85°C
Extended . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTE
[1]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic-discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

AD7245 ORDERING INFORMATION

Relative Accuracy (LSB)	Temperature Range and Package		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP	Hermetic DIP[1]	Hermetic DIP[1,2]
±1	AD7245JN	AD7245AQ	AD7245SQ
	PLCC[3]		LCCC[4]
±1	AD7245JP		AD7245SE

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

AD7248 ORDERING INFORMATION

Relative Accuracy (LSB)	Temperature Range and Package		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP	Hermetic DIP[1]	Hermetic DIP[1,2]
±1	AD7248JN	AD7248AQ	AD7248SQ
	PLCC[3]		LCCC[4]
±1	AD7248JP		AD7248SE

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-20) or cerdip (Q-20) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

AD7245 PRICING (100s)

AD7245JN	$ 9.85	AD7245SQ	$38.55
AD7245JP	$11.35	AD7245SE	$67.50
AD7245AQ	$12.85		

AD7248 PRICING (100s)

AD7248JN	$ 9.85	AD7248SQ	$38.55
AD7248JP	$11.35	AD7248SE	$67.50
AD7248AQ	$12.85		

TERMINOLOGY

RELATIVE ACCURACY
Relative Accuracy, or end-point nonlinearity, is a measure of the actual deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY
Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH
Digital Feedthrough is the glitch impulse injected from the digital inputs to the analog output when the inputs change state. It is measured with $\overline{LDAC}$ high and is specified in nV secs.

DAC GAIN ERROR
DAC Gain Error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been allowed for. It is therefore defined as:

Measured Value – Offset – Ideal Value

where the ideal value is calculated relative to the actual reference value.

UNIPOLAR OFFSET ERROR
Unipolar Offset Error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured when the part is configured for unipolar outputs. It is present for all codes and is measured with all 0s in the DAC register.

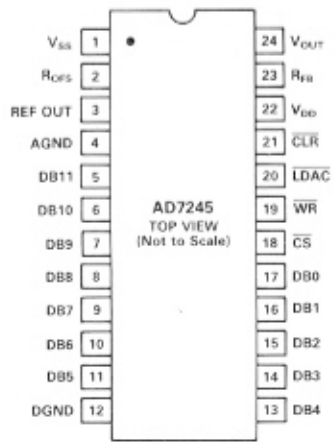
BIPOLAR ZERO OFFSET ERROR
Bipolar Zero Offset Error is measured when the part is configured for bipolar output and is a combination of errors from the DAC and output amplifier. It is present for all codes and is measured with a code of 2048 (decimal) in the DAC register.

AD7245 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

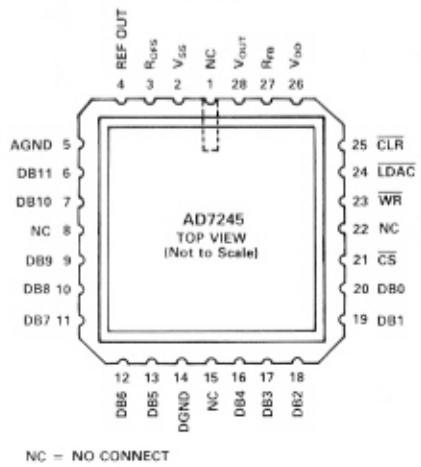
Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB11	Data Bit 11. Most Significant Bit (MSB).
6–11	DB10–DB5	Data Bit 10 to Data Bit 5.
12	DGND	Digital Ground.
13–16	DB4–DB1	Data Bit 4 to Data Bit 1.
17	DB0	Data Bit 0. Least Significant Bit (LSB).
18	$\overline{CS}$	Chip Select Input (Active LOW). The device is selected when this input is active.
19	$\overline{WR}$	Write Input (Active LOW). This is used in conjunction with $\overline{CS}$ to write data into the input latch of the AD7245.
20	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
21	$\overline{CLR}$	Clear Input (Active LOW). When this input is active the contents of the DAC latch are reset to all 0s.
22	V_{DD}	Positive Supply Voltage.
23	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
24	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 to +5V, 0 to +10V or −5V to +5V.

AD7245 PIN CONFIGURATIONS

DIP

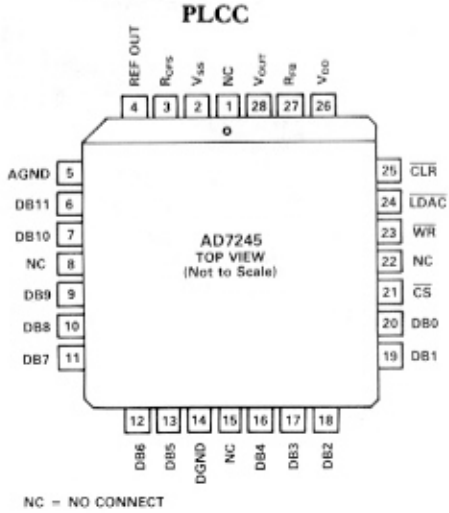


LCCC



NC = NO CONNECT

PLCC



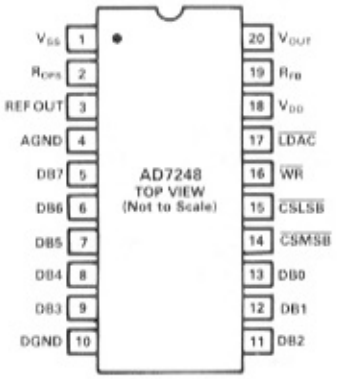
NC = NO CONNECT

AD7248 PIN FUNCTION DESCRIPTION
(ANY PACKAGE)

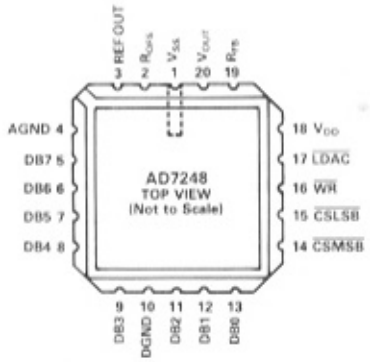
Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB7	Data Bit 7.
6	DB6	Data Bit 6.
7	DB5	Data Bit 5.
8	DB4	Data Bit 4.
9	DB3	Data Bit 3/Data Bit 11 (MSB).
10	DGND	Digital Ground.
11	DB2	Data Bit 2/Data Bit 10.
12	DB1	Data Bit 1/Data Bit 9.
13	DB0	Data Bit 0 (LSB)/Data Bit 8.
14	$\overline{CSMSB}$	Chip Select Input for MS Nibble. (Active LOW). This selects the upper 4 bits of the input latch. Input data is right-justified.
15	$\overline{CSLSB}$	Chip Select Input for LS byte. (Active LOW). This selects the lower 8 bits of the input latch.
16	$\overline{WR}$	Write Input. This is used in conjunction with $\overline{CSMSB}$ and $\overline{CSLSB}$ to load data into the input latch of the AD7248.
17	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
18	V_{DD}	Positive Supply Voltage.
19	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
20	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 to + 5V, 0 to + 10V or − 5V to + 5V.

AD7248 PIN CONFIGURATIONS

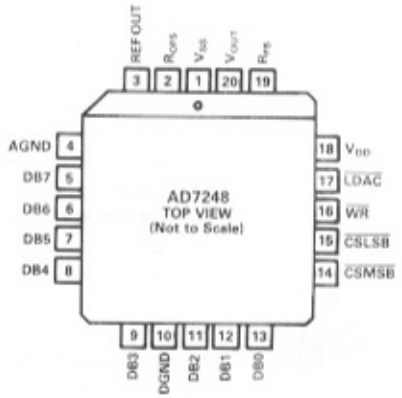
DIP



LCCC

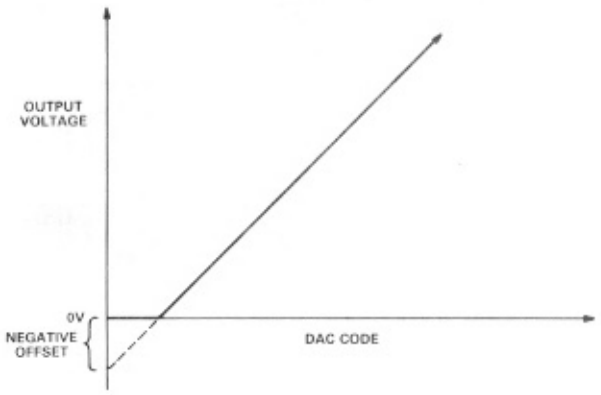


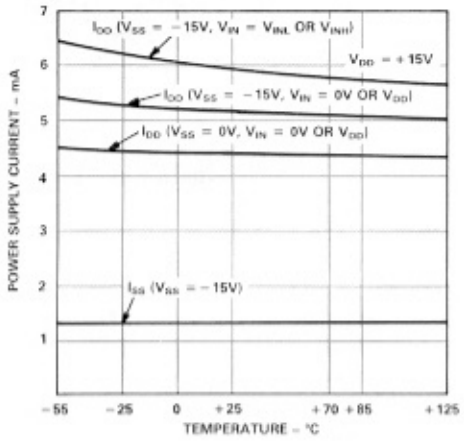
PLCC



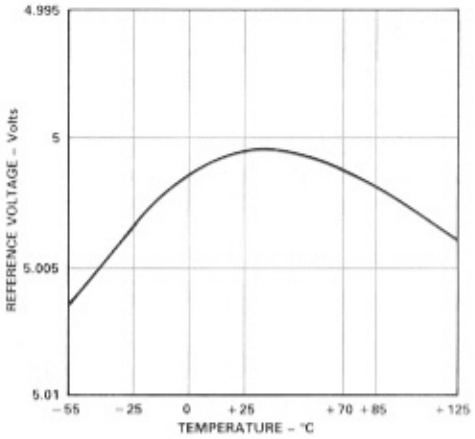
SINGLE SUPPLY LINEARITY AND GAIN ERROR

The output amplifier of the AD7245/AD7248 can have a true negative offset even when the part is operated from a single positive power supply. However, because the lower supply rail to the part is 0V, the output voltage cannot actually go negative. Instead the output voltage sits on the lower rail and this results in the transfer function shown across. This is an offset effect and the transfer function would have followed the dotted line if the output voltage could have gone negative. Normally, linearity is measured after offset and full scale have been adjusted or allowed for. On the AD7245/AD7248 the negative offset is allowed for by calculating the linearity from the code which the amplifier comes off the lower rail. This code is given by the negative offset specification. For example, the single supply linearity specification applies between Code 3 and Code 4095 for the 25°C specification and between Code 5 and Code 4095 over the T_{min} to T_{max} temperature range. Since gain error is also measured after offset has been allowed for, it is calculated between the same codes as the linearity error. Bipolar linearity and gain error are measured between Code 0 and Code 4095.

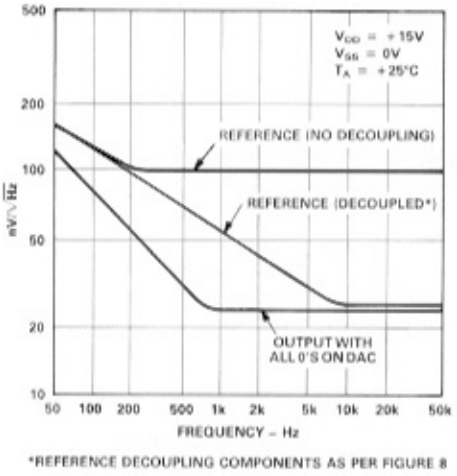




Power Supply Current vs. Temperature

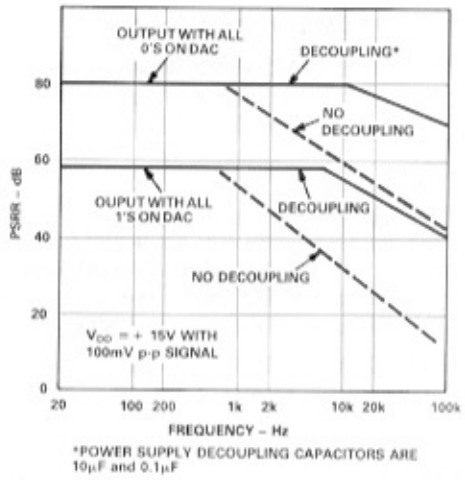


Reference Voltage vs. Temperature



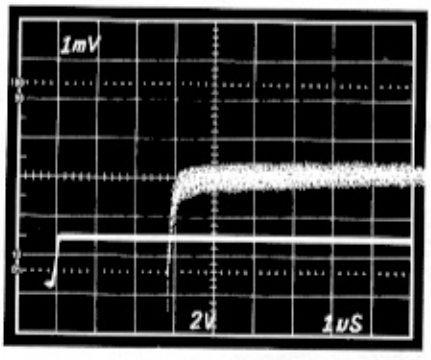
*REFERENCE DECOUPLING COMPONENTS AS PER FIGURE 8

Noise Spectral Density vs. Frequency

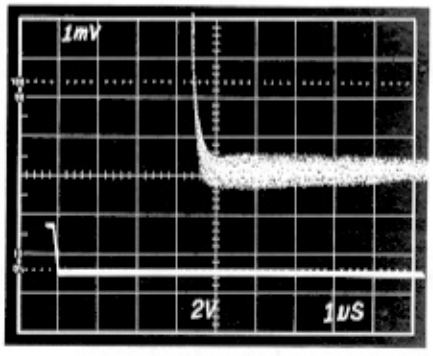


*POWER SUPPLY DECOUPLING CAPACITORS ARE 10μF and 0.1μF

Power Supply Rejection Ratio vs. Frequency



Positive-Going Settling Time (V_{DD} = +15V, V_{SS} = −15V)



Negative-Going Settling Time (V_{DD} = +15V, V_{SS} = −15V)

CIRCUIT INFORMATION

D/A SECTION

The AD7245/AD7248 contains a 12-bit voltage-mode digital-to-analog converter. The output voltage from the converter has the same positive polarity as the reference voltage allowing single supply operation. The reference voltage for the DAC is provided by an on-chip buried-Zener diode.

The DAC consists of a highly stable, thin-film, R-2R ladder and twelve high-speed NMOS single-pole, double-throw switches. The simplified circuit diagram for this DAC is shown in Figure 1.

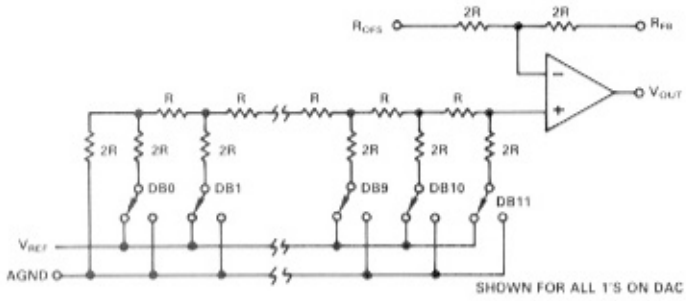


Figure 1. D/A Simplified Circuit Diagram

The input impedance of the DAC is code dependent and can vary from 8kΩ to infinity. The input capacitance also varies with code, typically from 50pF to 200pF.

OP AMP SECTION

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The user has access to two gain setting resistors which can be connected to allow different output voltage ranges (discussed later). The buffer amplifier is capable of developing up to 10V across a 2kΩ load to GND.

The output amplifier can be operated from a single positive power supply by tying V_{SS} = AGND = 0V. The amplifier can also be operated from dual supplies to allow a bipolar output range of −5V to +5V. *The amplifier should not be configured for the 0 to +10V output range when V_{SS} is more negative than −5V.* For dual supply operation on this range a V_{SS} of −5V should be applied to the part. The advantage of having dual supplies for the unipolar output ranges are faster settling time to voltages near 0V, full-sink capability of 2.5mA maintained over the entire output range and elimination of the effects of negative offset on the transfer characteristic (outlined previously). Figure 2 shows the sink capability of the amplifier for single supply operation.

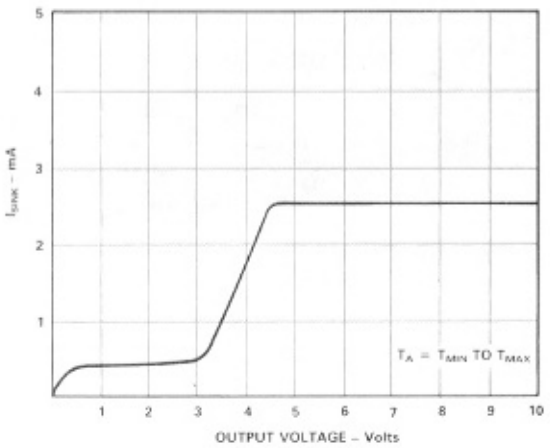


Figure 2. Typical Single Supply Sink Current vs. Output Voltage

The small-signal (200mV p-p) bandwidth of the output buffer amplifier is typically 1MHz. The output noise from the amplifier is low with a figure of 25nV/$\sqrt{Hz}$ at a frequency of 1kHz. The broadband noise from the amplifier has a typical peak-to-peak figure of 150μV for a 1MHz output bandwidth. There is no significant difference in the output noise between single and dual supply operation.

VOLTAGE REFERENCE

The AD7245/AD7248 contains an internal low-noise buried-Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. The reference is internally connected to the DAC. Since the DAC has a variable input impedance at its reference input the Zener diode reference is buffered. This buffered reference is available to the user to drive the circuitry required for bipolar output ranges. It can be used as a reference for other parts in the system provided it is externally buffered. The reference will give long-term stability comparable with the best discrete Zener reference diodes. The performance of the AD7245/AD7248 is specified with internal reference, and all the testing and trimming is done with this reference. The reference should be decoupled at the REF OUT pin and recommended decoupling components are 10μF and 0.1μF capacitors in series with a 10Ω resistor. A simplified schematic of the reference circuitry is shown in Figure 3.

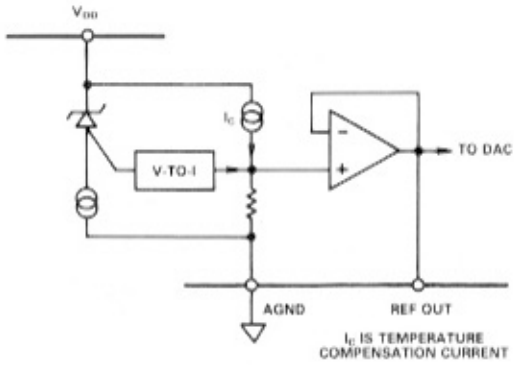


Figure 3. Internal Reference

DIGITAL SECTION

The AD7245/AD7248 digital inputs are compatible with either TTL or 5V CMOS levels. All data inputs are static-protected MOS gates with typical input currents of less than 1nA. The control inputs sink higher currents (150μA max) as a result of the fast digital interfacing. Internal input protection of all logic inputs is achieved by on-chip distributed diodes.

The AD7245/AD7248 features a very low digital feedthrough figure of 10nV secs in a 5V output range. This is due to the voltage-mode configuration of the DAC. Most of the impulse is actually as a result of feedthrough across the package. Normally, ceramic packages show more feedthrough than the other packages because of the metal lid. However, on the AD7245, the lid of the ceramic package is connected to DGND (Pin 12), and this reduces the feedthrough. The AD7248 metal lid is not connected to DGND on the package, but this can be done externally to reduce the feedthrough.

INTERFACE LOGIC INFORMATION – AD7245

Table I shows the truth table for AD7245 operation. The part contains two 12-bit latches, an input latch and a DAC latch. $\overline{CS}$ and $\overline{WR}$ control the loading of the input latch while $\overline{LDAC}$ controls the transfer of information from the input latch to the DAC latch. All control signals are level-triggered; and therefore either or both latches may be made transparent, the input latch by keeping $\overline{CS}$ and $\overline{WR}$ "LOW", the DAC latch by keeping $\overline{LDAC}$ "LOW". Input data is latched on the rising edge of $\overline{WR}$.

The data held in the DAC latch determines the analog output of the converter. Data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. This $\overline{LDAC}$ signal is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. For example, if $\overline{LDAC}$ goes LOW while $\overline{WR}$ is "LOW", then the $\overline{LDAC}$ signal must stay LOW for t_7 or longer after $\overline{WR}$ goes high to ensure correct data is latched through to the output.

$\overline{CLR}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Latches are Transparent
H	H	H	X	Both Latches are Latched
H	H	X	H	Both Latches are Latched
H	H	L	L	Input Latches Transparent
H	H	↓	L	Input Latches Latched
H	L	H	H	DAC Latches Transparent
H	↓	H	H	DAC Latches Latched
L	X	X	X	DAC Latches Loaded with all 0s
↓	H	H	H	DAC Latches Latched with All 0s and Output Remains at 0V or −5V
↓	L	L	L	Both Latches are Transparent and Output Follows Input Data

H = High State L = Low State X = Don't Care

Table I. AD7245 Truth Table

The contents of the DAC latch are reset to all 0s by a low level on the $\overline{CLR}$ line. With both latches transparent, the $\overline{CLR}$ line functions like a zero override with the output brought to 0V in the unipolar mode and −5V in the bipolar mode for the duration of the $\overline{CLR}$ pulse. If both latches are latched, a "LOW" pulse on the $\overline{CLR}$ input latches all 0s into the DAC latch and the output remains at 0V (or −5V) after the $\overline{CLR}$ line has returned "HIGH". The $\overline{CLR}$ line can be used to ensure powerup to 0V on the AD7245 output in unipolar operation and is also useful, when used as a zero override, in system calibration cycles.

Figure 4 shows the input control logic for the AD7245 and the write cycle timing for the part is shown in Figure 5.

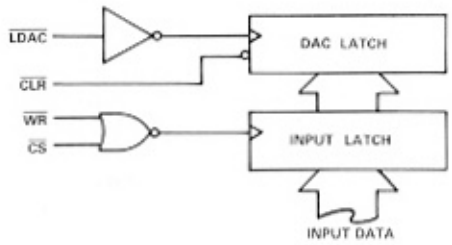


Figure 4. AD7245 Input Control Logic

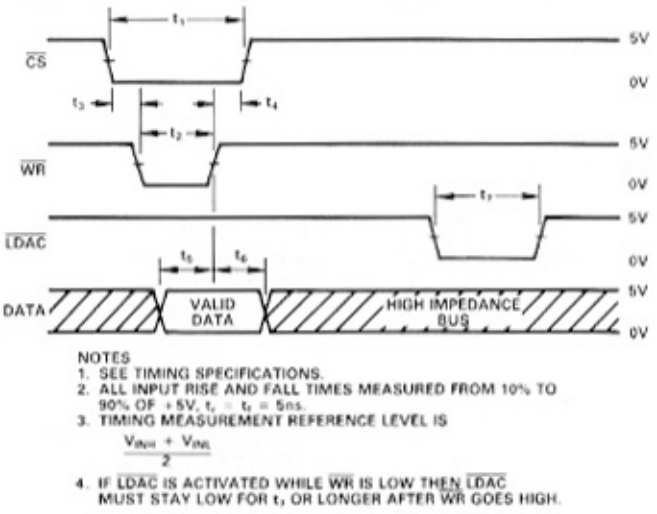


Figure 5. AD7245 Write-Cycle Timing Diagram

INTERFACE LOGIC INFORMATION – AD7248

The input loading structure on the AD7248 is configured for interfacing to microprocessors with an 8-bit-wide data bus. The part contains two 12-bit latches – an input latch and a DAC latch. Only the data held in the DAC latch determines the analog output from the converter. The truth table for AD7248 operation is shown in Table II, while the input control logic diagram is shown in Figure 6.

$\overline{CSMSB}$, $\overline{CSLSB}$ and $\overline{WR}$ control the loading of data from the external data bus to the input latch. The eight data inputs on the AD7248 accept right-justified data. This data is loaded to the input latch in two separate write operations. $\overline{CSLSB}$ and $\overline{WR}$ control the loading of the lower 8-bits into the 12-bit-wide latch. The loading of the upper 4-bit nibble is controlled by $\overline{CSMSB}$ and $\overline{WR}$. All control inputs are level triggered, and input data for either the lower byte or upper 4-bit nibble is latched into the input latches on the rising edge of $\overline{WR}$ (or either $\overline{CSMSB}$ or $\overline{CSLSB}$). The order in which the data is loaded to the input latch (i.e., lower byte or upper 4-bit nibble first) is not important.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latch to the DAC latch. This $\overline{LDAC}$ signal is also level triggered, and data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in the simultaneous updating of multiple AD7248 outputs. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that

incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ goes low while $\overline{WR}$ and either $\overline{CS}$ input are low (or $\overline{WR}$ and either $\overline{CS}$ go low while $\overline{LDAC}$ is low), then the $\overline{LDAC}$ signal must stay low for t_7 or longer after $\overline{WR}$ returns high to ensure correct data is latched through to the output. The write cycle timing diagram for the AD7248 is shown in Figure 7.

An alternate scheme for writing data to the AD7248 is to tie the $\overline{CSMSB}$ and $\overline{LDAC}$ inputs together. In this case exercising $\overline{CSLSB}$ and $\overline{WR}$ latches the lower 8 bits into the input latch. The second write, which exercises $\overline{CSMSB}$, $\overline{WR}$ and $\overline{LDAC}$ loads the upper 4-bit nibble to the input latch and at the same time transfers the 12-bit data to the DAC latch. This automatic transfer mode updates the output of the AD7248 in two write operations. This scheme works equally well for $\overline{CSLSB}$ and $\overline{LDAC}$ tied together provided the upper 4-bit nibble is loaded to the input latch followed by a write to the lower 8 bits of the input latch.

$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	Function
L	H	L	H	Loads LS Byte into Input Latch
L	H	↓	H	Latches LS Byte into Input Latch
↓	H	L	H	Latches LS Byte into Input Latch
H	L	L	H	Loads MS Nibble into Input Latch
H	L	↓	H	Latches MS Nibble into Input Latch
H	↓	L	H	Latches MS Nibble into Input Latch
H	H	H	L	Loads Input Latch into DAC Latch
H	H	H	↓	Latches Input Latch into DAC Latch
H	L	L	L	Loads MS Nibble into Input Latch and Loads Input Latch into DAC Latch
H	H	H	H	No Data Transfer Operation

H = High State L = Low State

Table II. AD7248 Truth Table

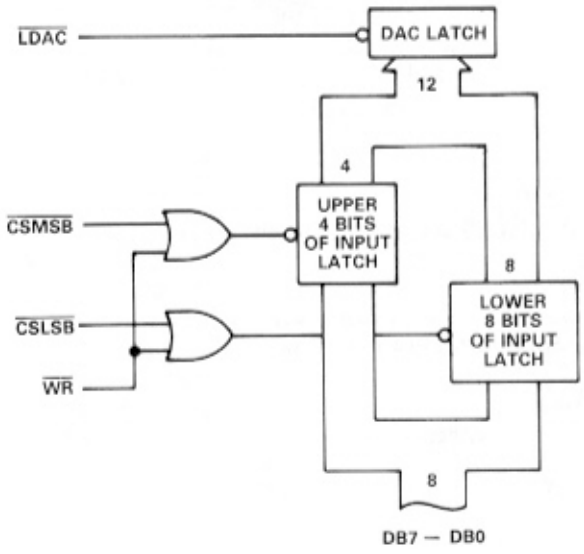


Figure 6. AD7248 Input Control Logic

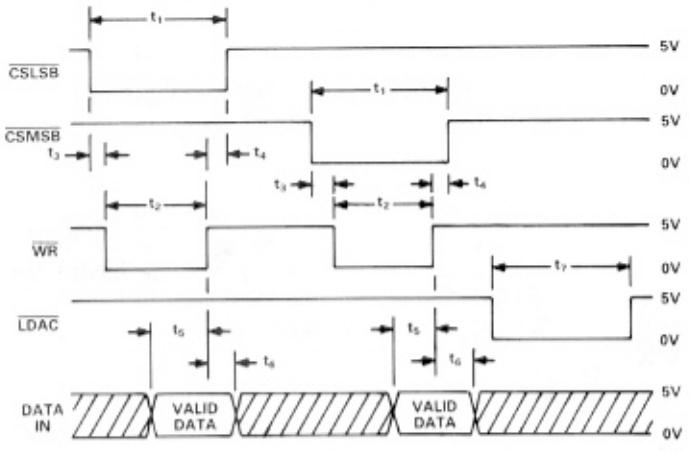


Figure 7. AD7248 Write Cycle Timing Diagram

APPLYING THE AD7245/AD7248

The internal scaling resistors provided on the AD7245/AD7248 allow several output voltage ranges. The part can produce unipolar output ranges of 0V to +5V or 0V to +10V and a bipolar output range of −5V to +5V. Connections for the various ranges are outlined below.

UNIPOLAR (0V to +10V) CONFIGURATION

The first of the configurations provides an output voltage range of 0V to +10V. This is achieved by connecting the bipolar offset resistor, R_{OFS}, to AGND and connecting R_{FB} to V_{OUT}. In this configuration the AD7245/AD7248 can be operated single supply (V_{SS} = 0V = AGND). If dual supply performance is required, a V_{SS} of −5V should be applied. Note that a V_{SS} supply more negative than −5V should not be applied to the AD7245/AD7248 when it is configured for a 0 to +10V output range. Figure 8 shows the connection diagram for unipolar operation while the table for output voltage versus the digital code in the DAC latch is shown in Table III.

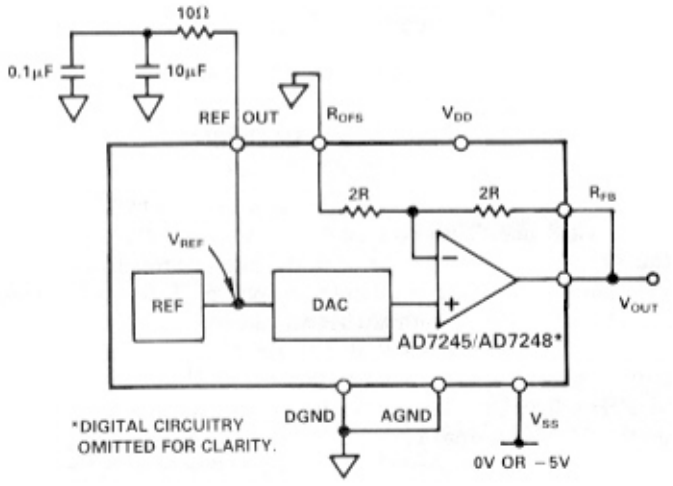


Figure 8. Unipolar (0 to +10V) Configuration

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+2 \cdot V_{REF} \cdot \left(\frac{4095}{4096}\right)$
1000 0000 0001	$+2 \cdot V_{REF} \cdot \left(\frac{2049}{4096}\right)$
1000 0000 0000	$+2 \cdot V_{REF} \cdot \left(\frac{2048}{4096}\right) = +V_{REF}$
0111 1111 1111	$+2 \cdot V_{REF} \cdot \left(\frac{2047}{4096}\right)$
0000 0000 0001	$+2 \cdot V_{REF} \cdot \left(\frac{1}{4096}\right)$
0000 0000 0000	0V

NOTE: $1LSB = 2 \cdot V_{REF}(2^{-12}) = V_{REF}\left(\frac{1}{2048}\right)$

Table III. Unipolar Code Table (0V to +10V Range)

UNIPOLAR (0V to +5V) CONFIGURATION

The 0V to +5V output voltage range is achieved by tying R_{OFS}, R_{FB} and V_{OUT} together. For this output range the AD7245/AD7248 can be operated single supply (V_{SS} = 0V) or dual supply. The table for output voltage versus digital code is as in Table III, with $2 \cdot V_{REF}$ replaced by V_{REF}. Note that for this range

$$1LSB = V_{REF}(2^{-12}) = V_{REF} \cdot \frac{1}{4096}.$$

BIPOLAR CONFIGURATION

The bipolar configuration for the AD7245/AD7248, which gives an output voltage range from −5V to +5V, is achieved by connecting the R_{OFS} input to REF OUT and connecting R_{FB} and V_{OUT}. The AD7245/AD7248 must be operated from dual supplies to achieve this output voltage range. The code table for bipolar operation is shown in Table IV.

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{REF} \cdot \left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF} \cdot \left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF} \cdot \left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF} \cdot \left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF} \cdot \left(\frac{2048}{2048}\right) = -V_{REF}$

NOTE: $1LSB = 2 \cdot V_{REF}(2^{-11}) = V_{REF}\left(\frac{1}{2048}\right)$

Table IV. Bipolar Code Table

AGND BIAS

The AD7245/AD7248 AGND pin can be biased above system GND (AD7245/AD7248 DGND) to provide an offset "zero" analog output voltage level. With unity gain on the amplifier (R_{OFS} = V_{OUT} = R_{FB}) the output voltage, V_{OUT} is expressed as:

$$V_{OUT} = V_{BIAS} + D \cdot V_{REF}$$

where D is a fractional representation of the digital word in the DAC latch and V_{BIAS} is the voltage applied to the AD7245/AD7248 AGND pin.

Because the current flowing out of the AGND pin varies with digital code, the AGND pin should be driven from a low impedance source. A circuit configuration is outlined for AGND bias in Figure 9 using the AD589, a +1.23V bandgap reference.

If a gain of 2 is used on the buffer amplifier the output voltage, V_{OUT} is expressed as

$$V_{OUT} = 2(V_{BIAS} + D \cdot V_{REF})$$

In this case care must be taken to ensure that the maximum output voltage is not greater than V_{DD} − 3V. The $V_{DD} - V_{OUT}$ overhead must be greater than 3V to ensure correct operation of the part. Note that V_{DD} and V_{SS} for the AD7245/AD7248 must be referenced to DGND (system GND). The entire circuit can be operated in single supply with the V_{SS} pin of the AD7245/AD7248 connected to system GND.

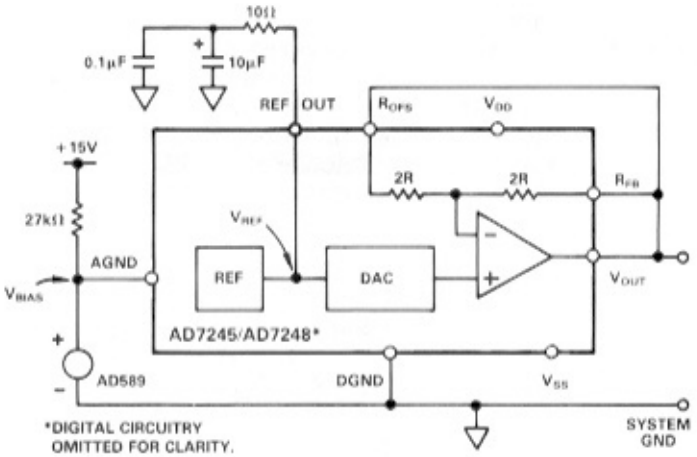


Figure 9. AGND Bias Current

PROGRAMMABLE CURRENT SINK

Figure 10 shows how the AD7245/AD7248 can be configured with a power MOSFET transistor, the VN0300M, to provide a

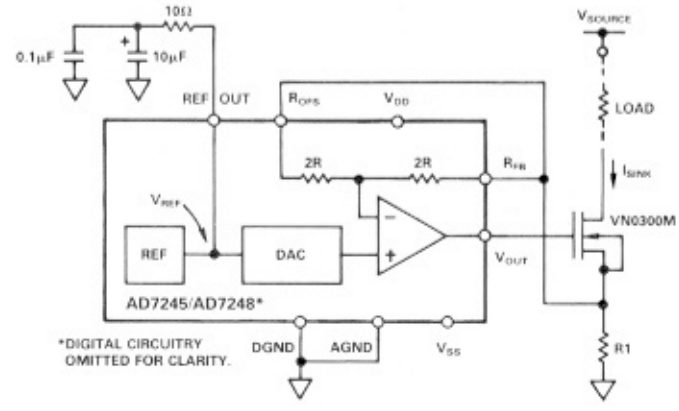


Figure 10. Programmable Current Sink

programmable current sink from V_{DD} or V_{SOURCE}. The VN0300M is placed in the feedback of the AD7245/AD7248 amplifier. The entire circuit can be operated in single supply by tying the V_{SS} of the AD7245/AD7248 to AGND. The sink current, I_{SINK}, can be expressed as:

$$I_{SINK} = \frac{D \cdot V_{REF}}{R1}$$

Using the VN0300M, the voltage drop across the load can typically be as large as (V_{SOURCE} −6V) with V_{OUT} of the DAC at +5V. Therefore, for a current of 50mA flowing in the R1 (with all 1s in the DAC register) the maximum load is 200Ω with V_{SOURCE} = +15V. The VN0300M can actually handle currents up to 500mA and still function correctly in the circuit, but in practice the circuit must be used with larger values of V_{SOURCE} otherwise it requires a very small load.

Since the tolerance value on the reference voltage of the AD7245/AD7248 is ±0.2%, then the absolute value of I_{SINK} can vary by ±0.2% from device to device for a fixed value of R1.

Because the input bias current of the AD7245/AD7248's op amp is only of the order of pA's, its effect on the sink current is negligible. Tying the R_{OFS} input to the R_{FB} input reduces this effect even further and prevents noise pickup which could occur if the R_{OFS} pin was left unconnected.

The circuit of Figure 10 can be modified to provide a programmable current source to AGND or $-V_{SINK}$ (for $-V_{SINK}$, dual supplies are required on the AD7245/AD7248). The AD7245/AD7248 is configured as before. The current through R1 is mirrored with a current mirror circuit to provide the programmable source current (see CMOS DAC Application Guide, Publication No. G872-30-10/84, for suitable current mirror circuit). As before the absolute value of the source current will be affected by the ±0.2% tolerance on V_{REF}. In this case the performance of the current mirror will also affect the value of the source current.

FUNCTION GENERATOR WITH PROGRAMMABLE FREQUENCY

Figure 11 shows how the AD7245/AD7248 can be configured with the AD537, voltage-to-frequency converter and the AD639, trigonometric function generator to provide a complete function generator with programmable frequency. The circuit provides square-wave, triwave and sinewave outputs, each output of ±10V amplitude.

The AD7245/AD7248 provides a programmable voltage to the AD537 input. Since both the AD7245/AD7248 and AD537 are guaranteed monotonic, the output frequency will always increase with increasing digital code. The AD537 provides a square-wave output which is conditioned for ±10V by amplifier A1. The AD537 also provides a differential triwave output. This is conditioned by amplifiers A2 and A3 to provide the ±1.8V triwave required at the input of the AD639. The triwave is further scaled by amplifier A4 to provide a ±10V output.

Adjusting the triwave applied to the AD639 adjusts the distortion performance of the sine wave output, (+10V in configuration shown). Amplitude, offset and symmetry of the triwave can affect the distortion. By adjusting these, via VR1 and VR2, an output sine wave with harmonic distortion of better than −50dB can be achieved at low and intermediate frequencies.

Using the capacitor value shown in Figure 11 for C_F (i.e. 680pF) the output frequency range is 0 to 100kHz over the digital input code range. The step size for frequency increments is 25Hz. The accuracy of the output frequency is limited to 8 or 9 bits by the AD537, but it is guaranteed monotonic to 12 bits.

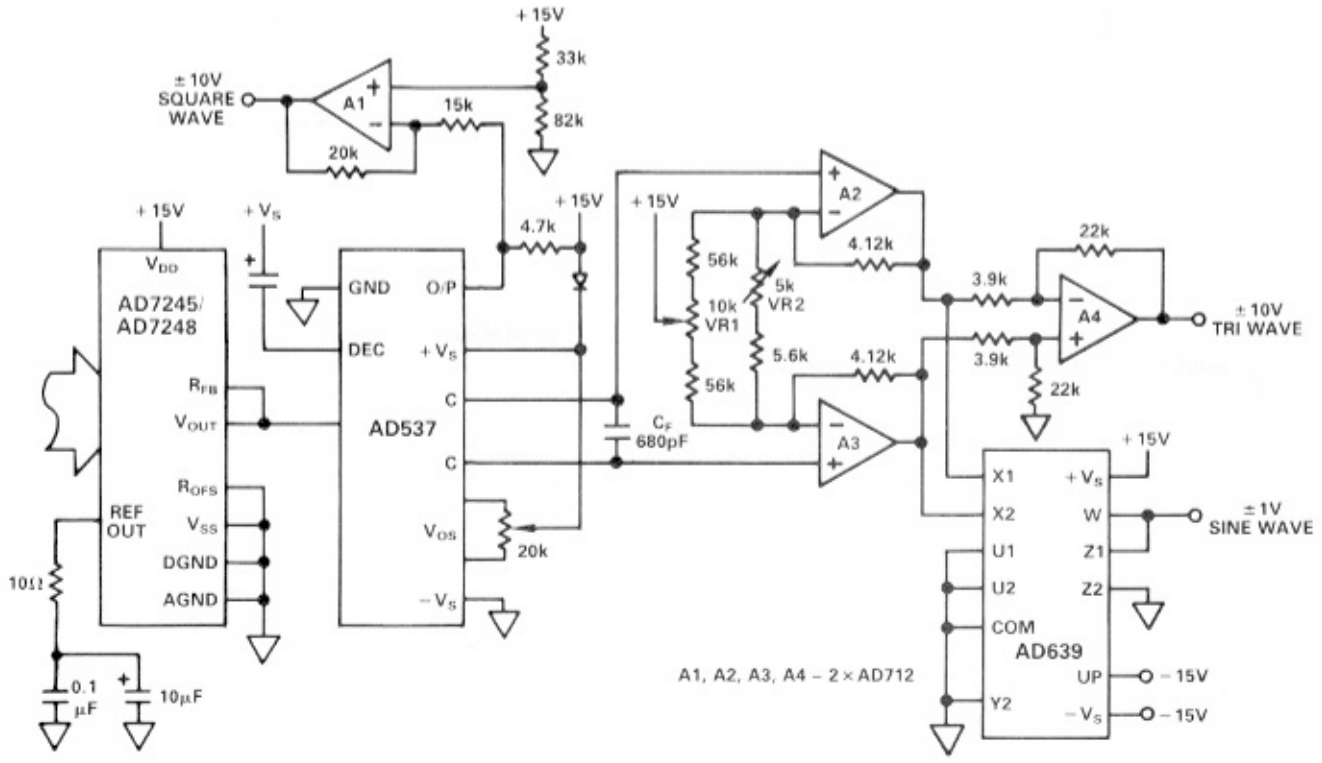


Figure 11. Programmable Function Generator

MICROPROCESSOR INTERFACING – AD7245

AD7245 – 8086A INTERFACE

Figure 12 shows the 8086 16-bit processor interfacing to the AD7245. In the setup shown the double-buffering feature of the DAC is not used and the $\overline{LDAC}$ input is tied LOW. AD0-AD11 of the 16-bit data bus are connected to the AD7245 data bus (DB0-DB11). The 12-bit word is written to the AD7245 in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 12 is given in Table V.

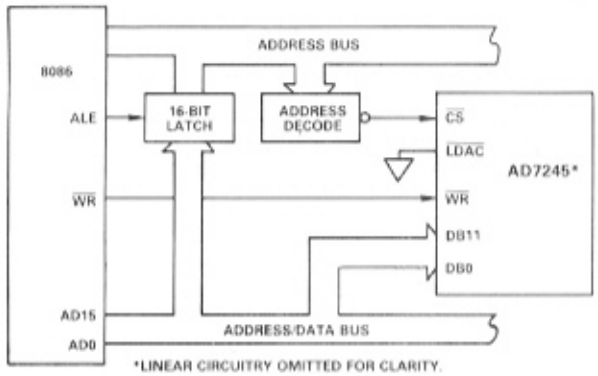


Figure 12. AD7245 to 8086 Interface

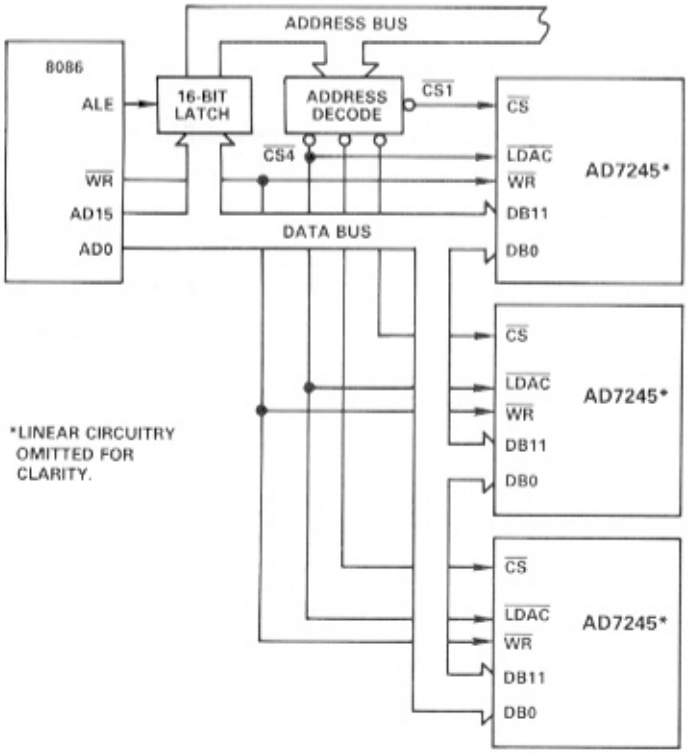


Figure 13. AD7245 to 8086 Multiple DAC Interface

```
                ASSUME DS : DACLOAD, CS : DACLOAD
                DACLOAD SEGMENT AT 000
00  8CC9        MOV CX,     : DEFINE DATA SEGMENT
                CS            REGISTER
02  8ED9        MOV DS,     : EQUAL TO CODE
                CX            SEGMENT REGISTER
04  BF00D0      MOV DI,     : LOAD DI WITH D000
                #D000
07  C705        MOV MEM,    : DAC LOADED WITH WXYZ
    "YZWX"      #YZWX
0B  EA00 00                 : CONTROL IS RETURNED TO
0E  00 FF                     THE MONITOR PROGRAM
```

Table V. Sample Program for Loading AD7245 from 8086

In a multiple DAC system the double-buffering of the AD7245 allows the user to simultaneously update all DACs. In Figure 13, a 12-bit word is loaded to the input latches of each of the DACs in sequence. Then, with one instruction to the appropriate address, $\overline{CS4}$ (i.e., $\overline{LDAC}$) is brought LOW, updating all the DACs simultaneously.

AD7245 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7245 is accomplished using the circuit of Figure 14. Once again the AD7245 is used in the single-buffered mode. A software routine for loading data to the AD7245 is given in Table VI. In this example the AD7245 is located at address E000, and the 12-bit word is written to the DAC in one MOVE instruction.

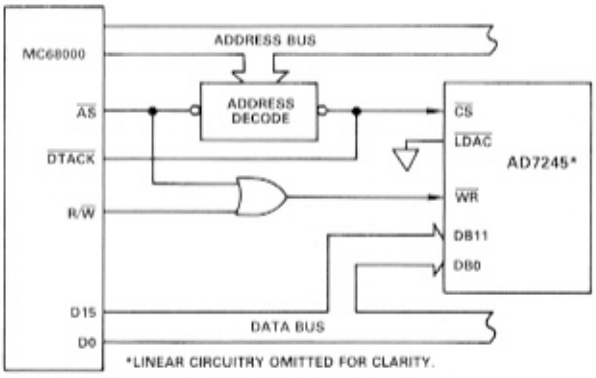


Figure 14. AD7245 to 68000 Interface

01000	MOVE.W	#X,D0	The desired DAC data, X, is loaded into Data Register 0. X may be any value between 0 and 4095 (decimal) or 0 and OFFF (hexadecimal).
	MOVE.W	D0,$E000	The Data X is transferred between D0 and the DAC Latch.
	MOVE.B	#228,D7	Control is returned to the System Monitor Program using these two instructions.
	TRAP	#14	

Table VI. Sample Routine for Loading AD7245 from 68000

MICROPROCESSOR INTERFACING – AD7248

Figure 15 shows the connection diagram for interfacing the AD7248 to both the 8085A and 8088 microprocessors. This scheme is also suited to the Z80 microprocessor, but the Z80 address/data bus does not have to be demutiplexed. Data to be loaded to the AD7248 is right-justified. The AD7248 is memory mapped with a separate memory address for the input latch high byte, the input latch low byte and the DAC latch. Data is first written to the AD7248 input latch in two write operations. Either the high byte or the low byte data can be written first to the AD7248 input latch. A write to the AD7248 DAC latch address transfers the input latch data to the DAC latch and updates the output voltage. Alternatively, the $\overline{LDAC}$ input can be asynchronous or can be common to a number of AD7248s for simultaneous updating of a number of voltage channels.

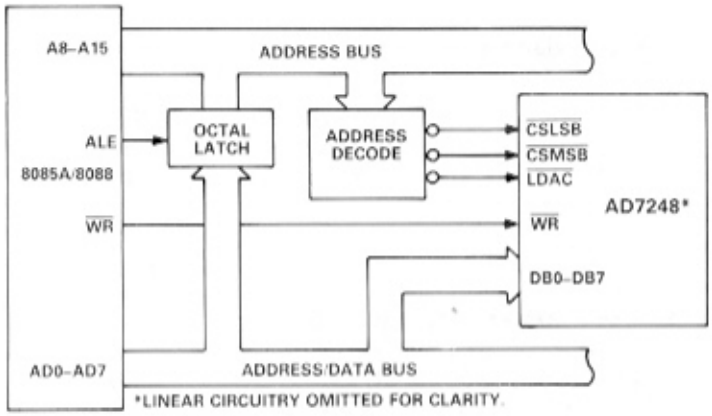


Figure 15. AD7248 to 8085A/8088 Interface

A connection diagram for the interface between the AD7248 and 68008 microprocessor is shown in Figure 16. Once again, the AD7248 acts as a memory mapped device and data is right-justified. In this case the AD7248 is configured in the automatic transfer mode which means that the high byte of the input latch has the same address as the DAC latch. Data is written to the AD7248 by first writing data to the AD7248 low byte. Writing data to the high byte of the input latch also transfers the input latch contents to the DAC latch and updates the output.

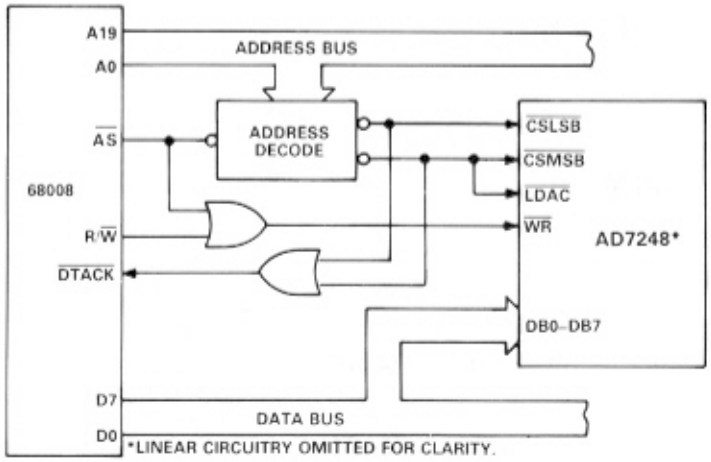


Figure 16. AD7248 to 68008 Interface

An interface circuit for connections to the 6502 or 6809 microprocessors is shown in Figure 17. Once again, the AD7248 is memory mapped and data is right-justified. The procedure for writing data to the AD7248 is as outlined for the 8085A/8088. For the 6502 microprocessor the $\phi 2$ clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

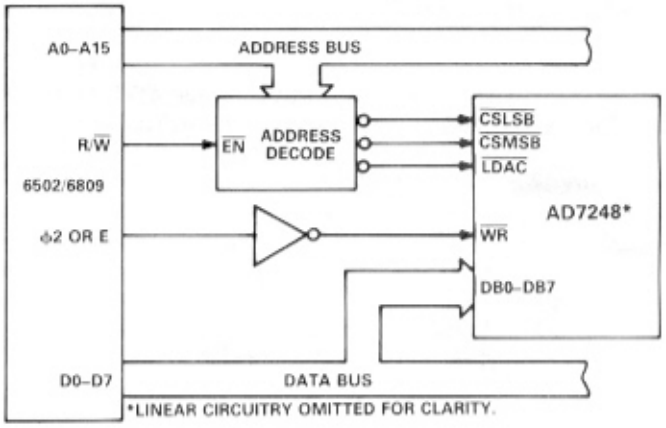


Figure 17. AD7248 to 6502/6809 Interface

Figure 18 shows a connection diagram between the AD7248 and the 8051 microprocessor. The AD7248 is port mapped in this interface and is configured in the automatic transfer mode. Data to be loaded to the input latch low byte is output to Port 1. Output Line P3.0, which is connected to $\overline{CSLSB}$ of the AD7248, is pulsed to load data into the low byte of the input latch. Pulsing the P3.1 line, after the high byte data has been set up on Port 1, updates the output of the AD7248. The $\overline{WR}$ input of the AD7248 can be hardwired low in this application because spurious address strobes on $\overline{CSLSB}$ and $\overline{CSMSB}$ do not occur.

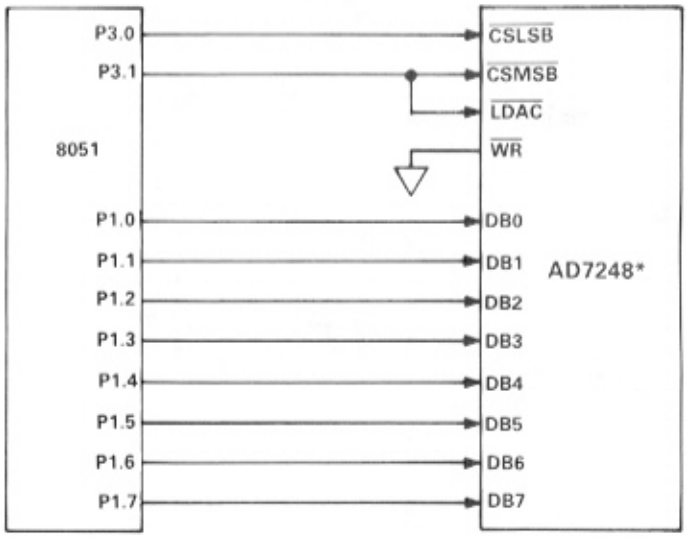


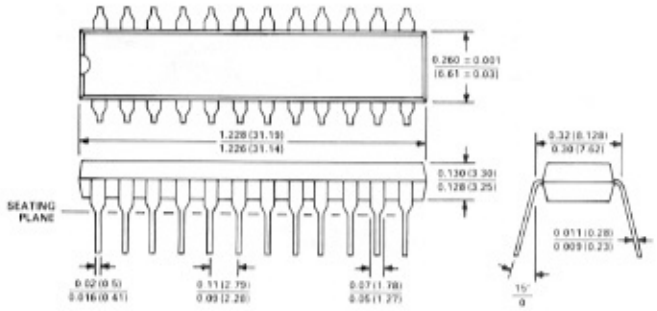
Figure 18. AD7248 to MCS-51 Interface

MECHANICAL INFORMATION – AD7245

OUTLINE DIMENSION

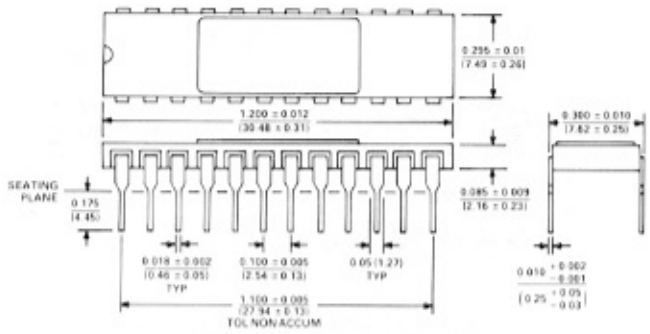
Dimensions shown in inches and (mm).

24-Pin Plastic DIP (N-24)



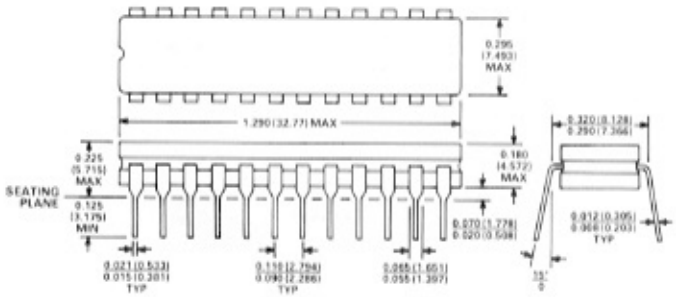
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Ceramic DIP (D-24A)



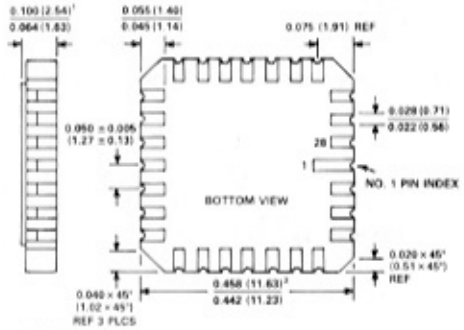
LEAD NO 1 IDENTIFIED BY DOT OR NOTCH.
CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.
METAL LID IS CONNECTED TO DGND.

24-Pin Cerdip (Q-24)



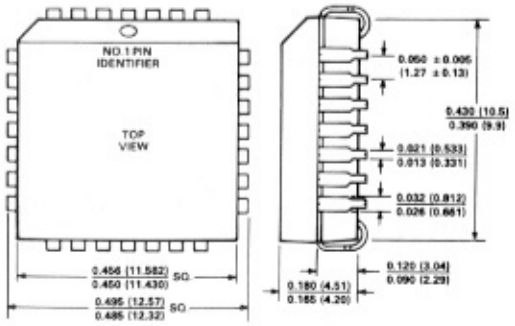
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Terminal Leadless Ceramic Chip Carrier (E-28A)



NOTES
¹THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
²APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED.

28-Terminal Plastic Leaded Chip Carrier (P-28A)

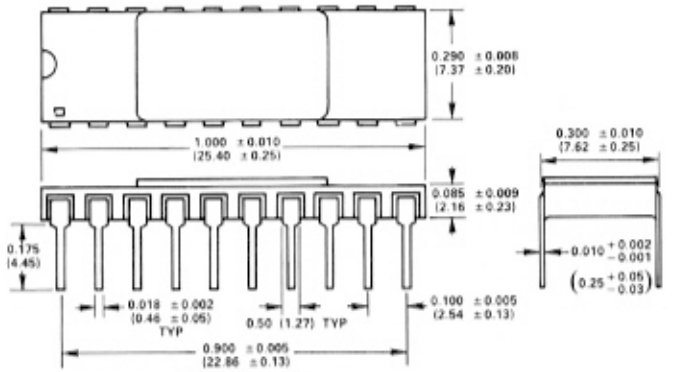


MECHANICAL INFORMATION – AD7248

OUTLINE DIMENSIONS

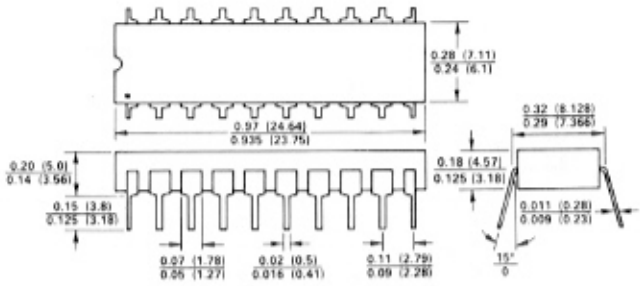
Dimensions shown in inches and (mm).

20-Pin Ceramic DIP (D-20)



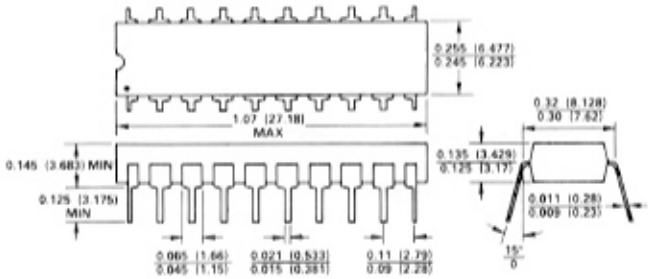
LEAD NUMBER 1 IDENTIFIED BY DOT OR NOTCH.
LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

20-Pin Cerdip (Q-20)



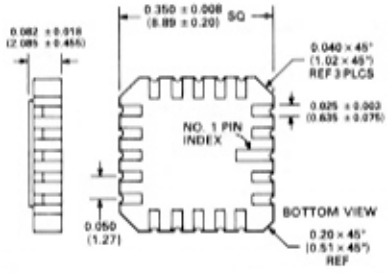
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

20-Pin Plastic DIP (N-20)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

20-Terminal Leadless Ceramic Chip Carrier (E-20A)



20-Terminal Plastic Leaded Chip Carrier (P-20A)