2.7 V to 5.5 V, Serial-Input, Voltage-Output, 16-/12-Bit *nano*DACs in LFCSP

Preliminary Technical Data

AD5541A/AD5542A/AD5512A

FEATURES

Low power, 1 LSB INL *nano*DACs
AD5541A: 16 bits
AD5542A: 16 bits
AD5512A: 12 bits
2.7 V to 5.5 V single-supply operation
Low glitch: 0.5 nV-s
Unbuffered voltage output capable of driving 60 kΩ loads directly
V_{LOGIC} pin provides 1.8 V digital interface capability
Hardware CLR and LDAC functions
50 MHz SPI-/QSPI-/MICROWIRE-/DSP-compatible interface standards
Power-on reset clears DAC output to zeroscale and midscale
Schmitt trigger inputs
Available in 3 mm × 3 mm 16-LFCSP, 10-LFCSP, and 8-LFCSP
Also available in10-MSOP and 16-TSSOP

APPLICATIONS

Automatic test equipment
Precision Source-measure Instruments
Data Acquisition Systems
Medical Instrumentation
Aerospace Instrumentation
Communications Infrastructure equipment
Industrial Control

GENERAL DESCRIPTION

The AD5541A/AD5542A/AD5512A[1] are single, 16-/16-/12-bit, serial input, unbuffered voltage output digital-to-analog converters (DACs) that operate from a single 2.7 V to 5.5 V supply.

The AD5541A/AD5542A/AD5512A utilize a versatile 3-wire interface that is compatible with a 50 MHz SPI, QSPI™, MICROWIRE™, and DSP interface standards.

These DACs provide 16-/12-bit performance without any adjustments. The DAC output is unbuffered, which reduces power consumption and offset errors contributed to by an output buffer.

The AD5542A/AD5512A can be operated in bipolar mode, which generates a $\pm V_{REF}$ output swing. The AD5542A/AD5512A also includes Kelvin sense connections for the reference and analog ground pins to reduce layout sensitivity.

The AD5541A is available in 10-lead 3 mm × 3 mm LFCSP and 10-lead MSSOP. The AD5541A-1 is available in 8-lead 3 mm × 3 mm LFCSP. The AD5542A/AD5512A are available in 16-lead 3 mm × 3 mm LFCSP and the AD5542A is also available in 16-lead TSSOP. The AD5542A-1 is available in 10-lead LFCSP. The AD5541A and AD5542A are specified over a temperature range of −40°C to 105°C.

FUNCTIONAL BLOCK DIAGRAMS

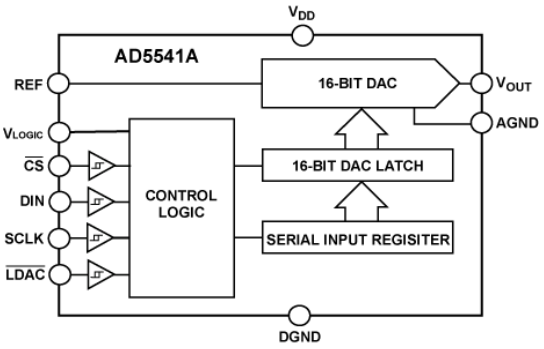

Figure 1. AD5541A

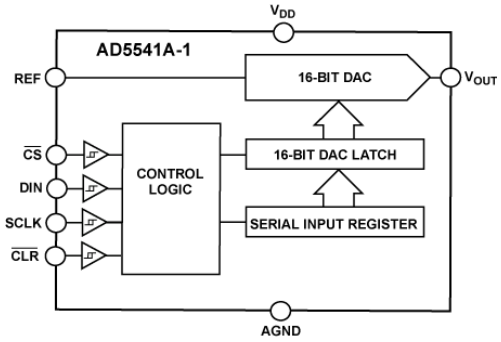

Figure 2. AD5541A-1

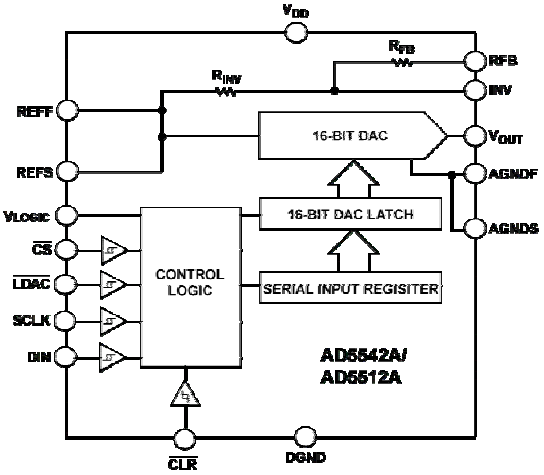

Figure 3. AD5542A

Rev. PrA

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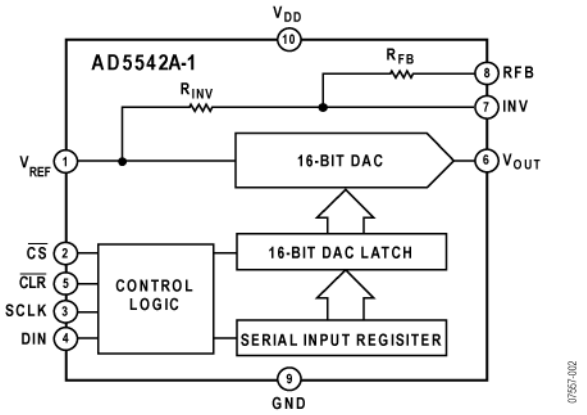

Figure 4.

[1] All references to the AD5541A/AD5542A/AD5512A incorporate all models (see Ordering Guide) including the AD5541A-1/AD5542A-1 unless specified.

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REVISION HISTORY

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5V, V_{REF} = 2.5 V, AGND = DGND = 0 V. −40°C < T_A < +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Condition
STATIC PERFORMANCE					
AD5541A/AD5542A					
Resolution	16			Bits	
Relative Accuracy (INL)		±0.5	±1.0	LSB	L, C grades
		±0.5	±2.0	LSB	B, J grades
		±0.5	±4.0	LSB	A grade
Differential Nonlinearity (DNL)		±0.5	±1.0	LSB	Guaranteed monotonic
			±1.5	LSB	J grade
AD5512A					
Resolution	12			Bits	
Relative Accuracy (INL)			±1.0	LSB	
Differential Nonlinearity (DNL)			±1.0	LSB	
Gain Error		−1.5	±5	LSB	T_A = 25°C
			±7	LSB	
Gain Error Temperature Coefficient		±0.1		ppm/°C	
Zero Code Error		0.3	±1	LSB	T_A = 25°C
			±2	LSB	
Zero Code Temperature Coefficient		±0.05		ppm/°C	
AD5542A/AD5512A					
Bipolar Resistor Matching		1.000		Ω/Ω	R_{FB}/R_{INV}, typically $R_{FB} = R_{INV}$ = 28 kΩ
		±0.0015	TBD	%	Ratio error
Bipolar Zero Offset Error		±1	±5	LSB	T_A = 25°C
			±7	LSB	
Bipolar Zero Temperature Coefficient		±0.2		ppm/°C	
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		V_{REF} − 1 LSB	V	Unipolar operation
	$-V_{REF}$		$+V_{REF}$ − 1 LSB	V	AD5542 bipolar operation
Output Voltage Settling Time		1		µs	To 1/2 LSB of FS, C_L = 10 pF
Slew Rate		25		V/µs	C_L = 10 pF, measured from 0% to 63%
Digital-to-Analog Glitch Impulse		0.5		nV-sec	1 LSB change around the major carry
Digital Feedthrough		0.2		nV-sec	All 1s loaded to DAC, V_{REF} = 2.5 V
DAC Output Impedance		6.25		kΩ	Tolerance typically 20%
Power Supply Rejection Ratio			±1.0	LSB	ΔV_{DD} ± 10%
DAC REFERENCE INPUT					
Reference Input Range	2.0		V_{DD}	V	
Reference Input Resistance[1]	9			kΩ	Unipolar operation
	7.5			kΩ	AD5542, bipolar operation
LOGIC INPUTS					
Input Current			±1	µA	
Input Low Voltage, V_{INL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
Input High Voltage, V_{INH}	2.0			V	V_{DD} = 4.5 V to 5.5 V
Input High Voltage, V_{INH}	1.8			V	V_{DD} = 2.7 V to 3.6 V
Input Capacitance[2]			10	pF	
Hysteresis Voltage[2]		0.15		V	
REFERENCE					
Reference −3 dB Bandwidth		1.3		MHz	All 1s loaded
Reference Feedthrough		1		mV p-p	All 0s loaded, V_{REF} = 1 V p-p at 100 kHz
THD		TBD		dB	
Signal-to-Noise Ratio		92		dB	
Reference Input Capacitance		75		pF	Code 0x0000
		120		pF	Code 0xFFFF

Parameter	Min	Typ	Max	Unit	Test Condition
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD}		200	TBD	µA	
V_{LOGIC}	1.8		5.5	V	
I_{LOGIC}		200	TBD	µA	
Power Dissipation		1.5	TBD	mW	

[1] Reference input resistance is code-dependent, minimum at 0x8555.
[2] Guaranteed by design, not subject to production test.

TIMING CHARACTERISTICS

V_{LOGIC} = 1.8 V to 5.5 V V, V_{DD} = 5V, V_{REF} = 2.5 V, V_{INH} = 90% of V_{LOGIC}, V_{INL} = 10% of V_{LOGIC}, AGND = DGND = 0 V; −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit	Unit	Description
f_{SCLK}	50	MHz max	SCLK cycle frequency
t_1	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	5	ns min	$\overline{CS}$ low to SCLK high setup
t_5	7	ns min	$\overline{CS}$ high to SCLK high setup
t_6	15	ns min	SCLK high to $\overline{CS}$ low hold time
t_7	10	ns min	SCLK high to $\overline{CS}$ high hold time
t_8	7	ns min	Data setup time
t_9	5	ns min	Data hold time (V_{INH} = 90% of V_{DD}, V_{INL} = 10% of V_{DD})
t_9	5	ns min	Data hold time (V_{INH} = 3V, V_{INL} = 0 V)
t_{10}	15	ns min	$\overline{LDAC}$ pulsewidth
t_{11}	15	ns min	$\overline{CS}$ high to $\overline{LDAC}$ low setup
t_{12}	15	ns min	$\overline{CS}$ high time between active periods
t_{13}	15	ns min	$\overline{CLR}$ pulsewidth

[1] Guaranteed by design and characterization. Not production tested
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V and timed from a voltage level of (V_{INL} + V_{INH})/2.

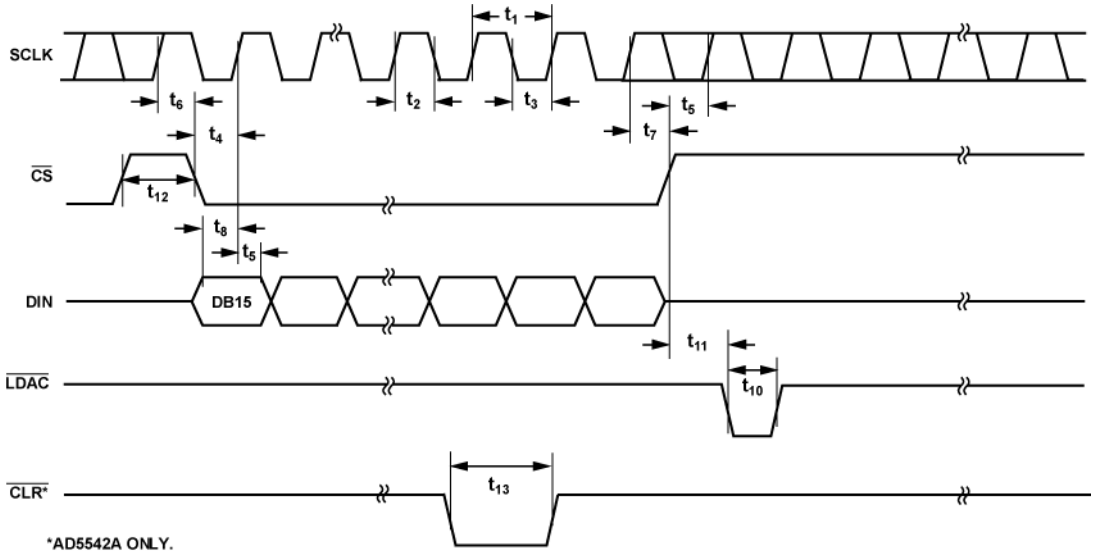


Figure 5. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
AGND, AGNDF, AGNDS to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Operating Temperature Range	
Industrial (A, B, C Versions)	−40°C to +85°C
Commercial (J, L Versions)	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_J max)	150°C
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
Thermal Impedance, θ_{JA}	
SOIC (R-8)	149.5°C/W
SOIC (R-14)	104.5°C/W
Lead Temperature, Soldering	
Peak Temperature[1]	260°C

[1] As per JEDEC Standard 20.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

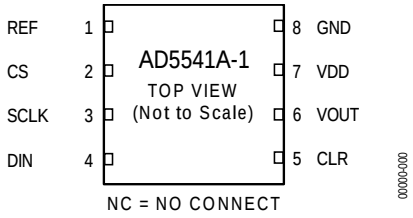


Figure 6. AD5541A-1 8-Lead LFCSP Pin Configuration

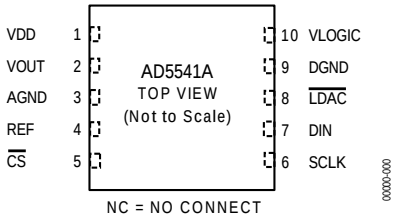


Figure 8. AD5541A 10-Lead LFCSP Pin Configuration

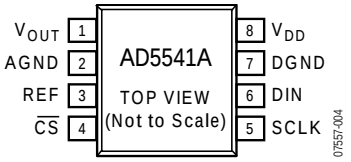


Figure 7. AD5541A 8-Lead SOIC Pin Configuration

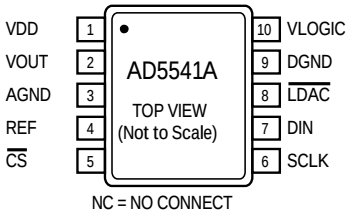


Figure 9. AD5541A 10-Lead MSOP Pin Configuration

Table 4. AD5541A Pin Function Descriptions

Pin No.					
8-Lead LFCSP	**8-Lead SOIC**	**10-Lead LFCSP**	**10-Lead MSOP**	**Mnemonic**	**Description**
6	1	2	2	VOUT	Analog Output Voltage from the DAC.
	2	3	3	AGND	Ground Reference Point for Analog Circuitry.
1	3	4	4	REF	Voltage Reference Input for the DAC. Connect to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
2	4	5	5	$\overline{CS}$	Logic Input Signal. The chip select signal is used to frame the serial data input.
3	5	6	6	SCLK	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
4	6	7	7	DIN	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
	7	9	9	DGND	Digital Ground. Ground reference for digital circuitry.
7	8	1	1	VDD	Analog Supply Voltage, 5 V ± 10%.
5				$\overline{CLR}$	Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the input register and the DAC register are cleared to the model selectable midscale or zeroscale .
		10	10	VLOGIC	Logic Power Supply.
		8	8	$\overline{LDAC}$	$\overline{LDAC}$ Input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register.

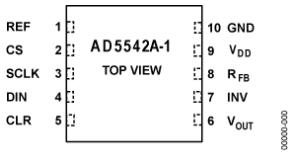


Figure 10. AD5542A-1 10-Lead LFCSP Pin Configuration

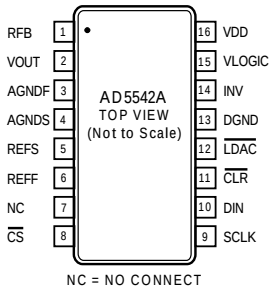


Figure 12. AD5542A 16-Lead TSSOP Pin Configuration

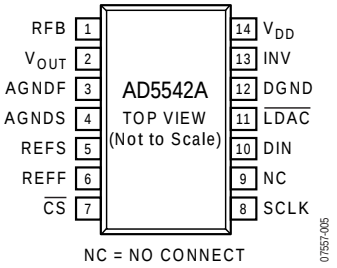


Figure 11. AD5542 14-Lead SOIC Pin Configuration

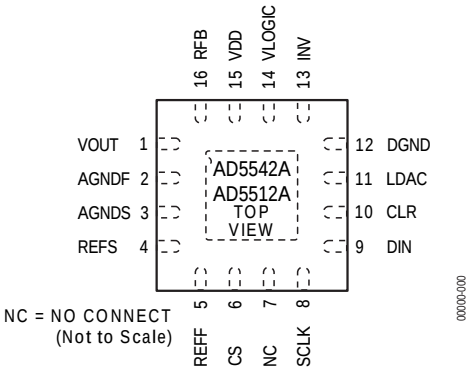


Figure 13. AD5542A 16-Lead LFCSP Pin Configuration

Table 5. AD5542A/AD5512A Pin Function Descriptions

Pin No.					
10-Lead LFCSP	**14-Lead SOIC**	**16-Lead TSSOP**	**16-Lead LFCSP**	**Mnemonic**	**Description**
8	1	1	16	RFB	Feedback Resistor Pin. In bipolar mode, connect this pin to the external op amp output.
6	2	2	1	VOUT	Analog Output Voltage from the DAC.
	3	3	2	AGNDF	Ground Reference Point for Analog Circuitry (Force).
	4	4	3	AGNDS	Ground Reference Point for Analog Circuitry (Sense).
	5	5	4	REFS	Voltage Reference Input (Sense) for the DAC. Connect to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
	6	6	5	REFF	Voltage Reference Input (Force) for the DAC. Connect to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
2	7	8	6	$\overline{CS}$	Logic Input Signal. The chip select signal is used to frame the serial data input.
3	8	9	8	SCLK	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
5		11	10	$\overline{CLR}$	Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the input register and the DAC register are cleared to the model selectable midscale or zeroscale .
4	10	10	9	DIN	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
	11	12	11	$\overline{LDAC}$	$\overline{LDAC}$ Input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register.
	12	13	12	DGND	Digital Ground. Ground reference for digital circuitry.
7	13	14	13	INV	Connected to the Internal Scaling Resistors of the DAC. Connect the INV pin to external op amps inverting input in bipolar mode.
9	14	16	15	VDD	Analog Supply Voltage, 5 V ± 10%.
		15	14	VLOGIC	Logic Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

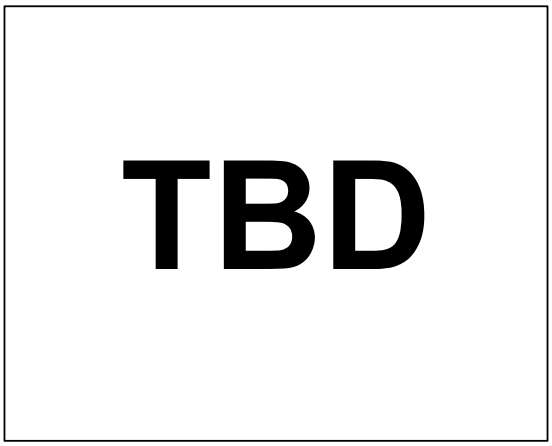


Figure 14. Integral Nonlinearity vs. Code

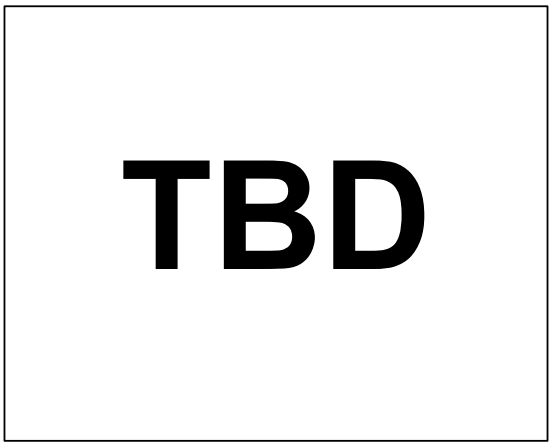


Figure 17. Differential Nonlinearity vs. Code

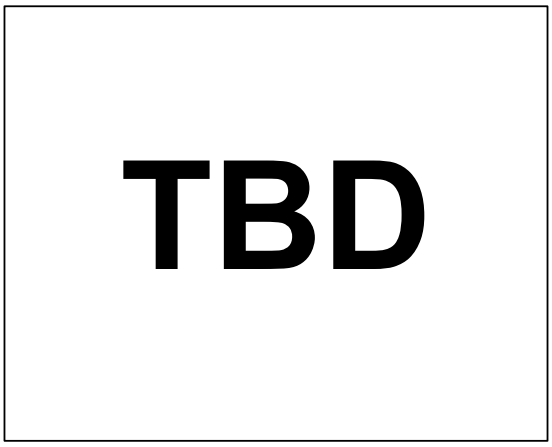


Figure 15. Integral Nonlinearity vs. Temperature

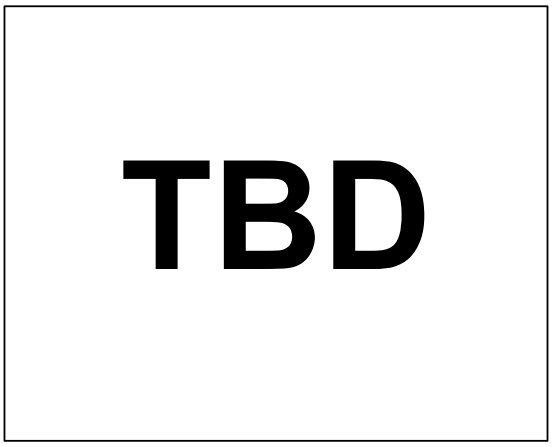


Figure 18. Differential Nonlinearity vs. Temperature

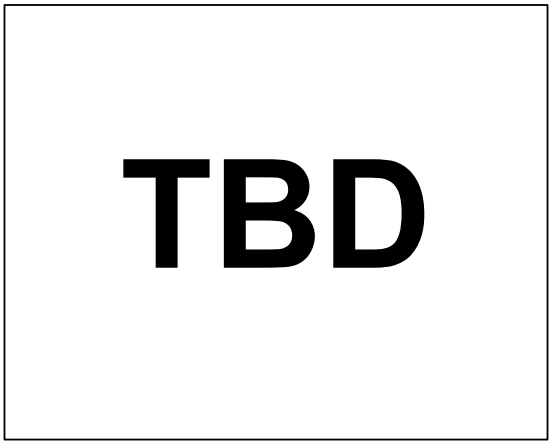


Figure 16. Linearity Error vs. Supply Voltage

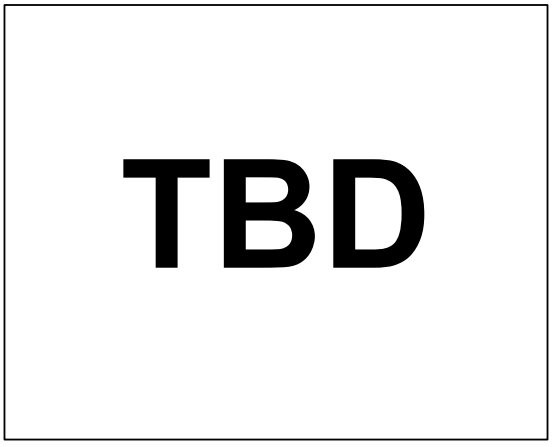


Figure 19. Linearity Error vs. Reference Voltage

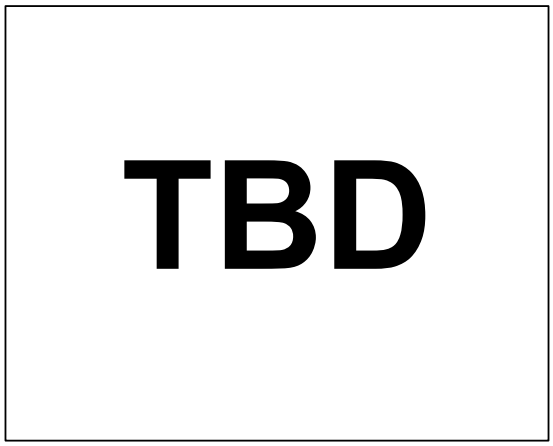


Figure 20. Gain Error vs. Temperature

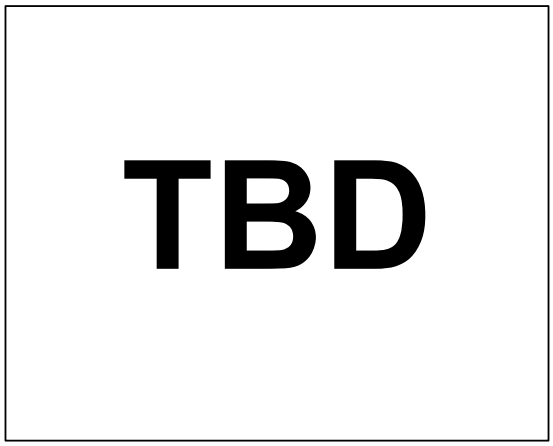


Figure 23. Zero-Code Error vs. Temperature

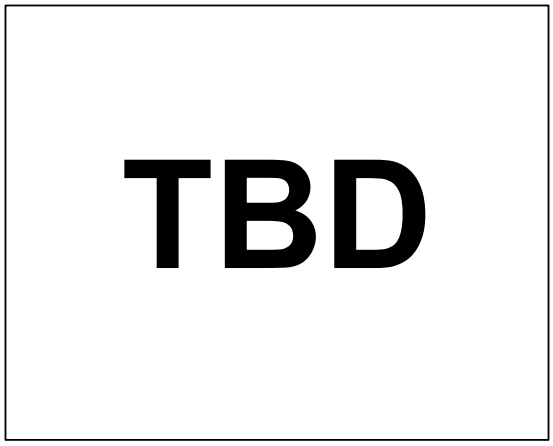


Figure 21. Supply Current vs. Temperature

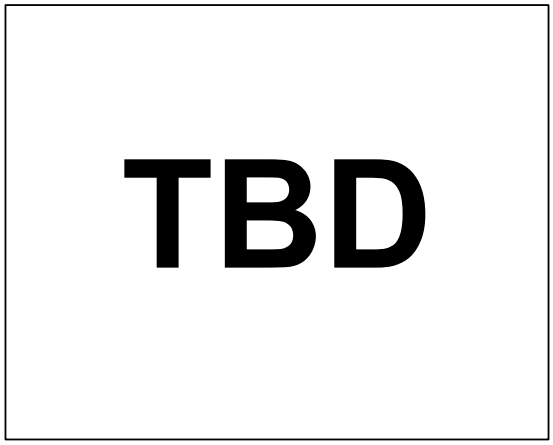


Figure 24. Supply Current vs. Reference Voltage or Supply Voltage

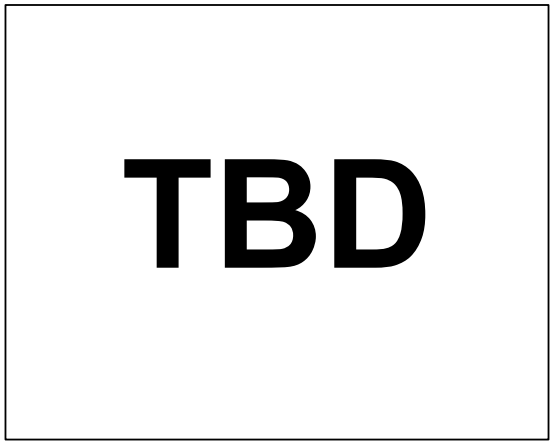


Figure 22. Supply Current vs. Digital Input Voltage

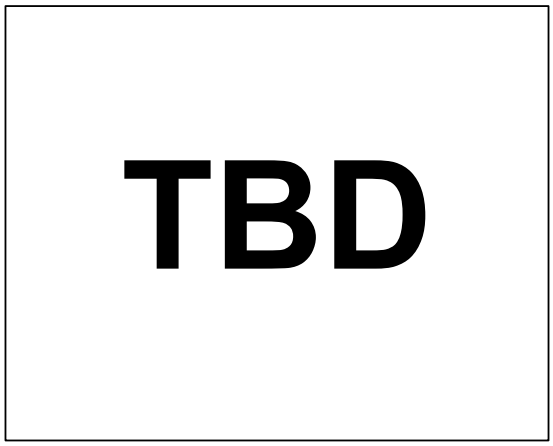


Figure 25. Reference Current vs. Code

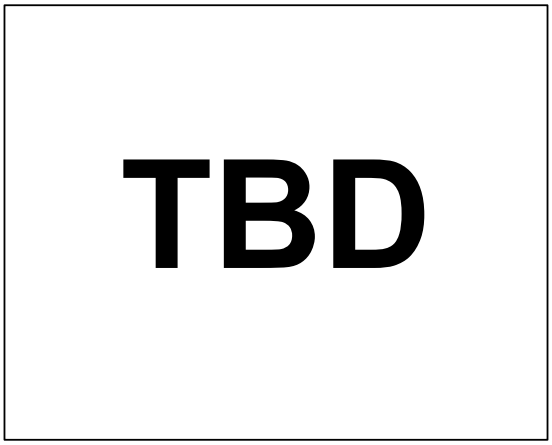


Figure 26. Digital Feedthrough

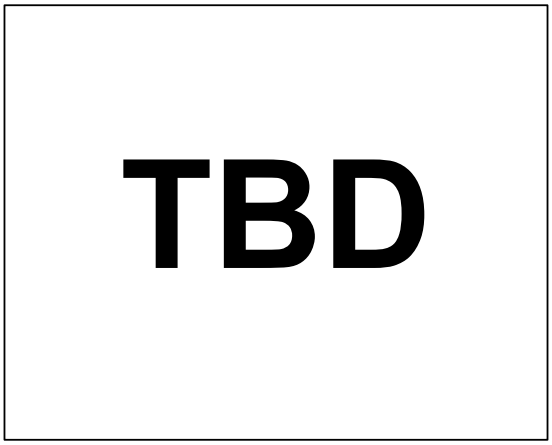


Figure 28. Large Signal Settling Time

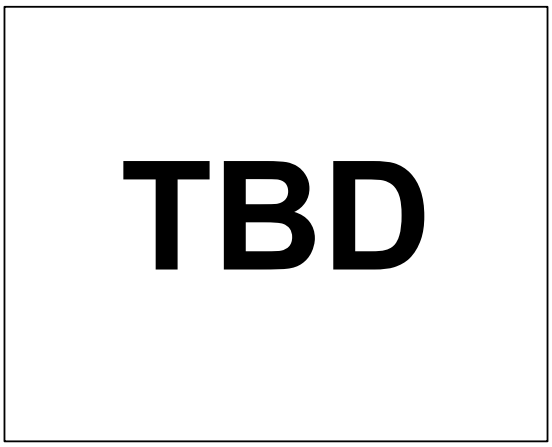


Figure 27. Digital-to-Analog Glitch Impulse

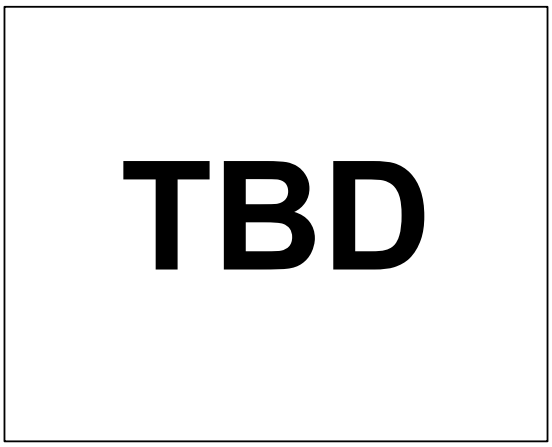


Figure 29. Small Signal Settling Time

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or INL is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 14.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. A typical DNL vs. code plot is shown in Figure 17.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Temperature Coefficient
Gain error temperature coefficient is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero Code Error
Zero code error is a measure of the output error when zero code is loaded to the DAC register.

Zero Code Temperature Coefficient
This is a measure of the change in zero code error with a change in temperature. It is expressed in mV/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition. A digital-to-analog glitch impulse plot is shown in Figure 27.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. $\overline{CS}$ is held high while the CLK and DIN signals are toggled. It is specified in nV-sec and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa. A typical digital feedthrough plot is shown in Figure 26.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage. Power-supply rejection ratio is quoted in terms of percent change in output per percent change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
Reference feedthrough is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in mV p-p.

THEORY OF OPERATION

The AD5541A/AD5542A/AD5512A are single, 16-bit, serial input, voltage output DACs. They operate from a single supply ranging from 2.7 V to 5 V and consume typically 300 μA with a supply of 5 V. Data is written to these devices in a 16-bit word format,
via a 3- or 4-wire serial interface. To ensure a known power-up state, these parts are designed with a power-on reset function. In unipolar mode, the output is reset to 0 V; in bipolar mode, the AD5542 output is set to $-V_{REF}$. Kelvin sense connections for the reference and analog ground are included on the AD5542.

DIGITAL-TO-ANALOG SECTION

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 30. The DAC architecture of the AD5541/AD5542 is segmented. The four MSBs of the 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each switch connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data-word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

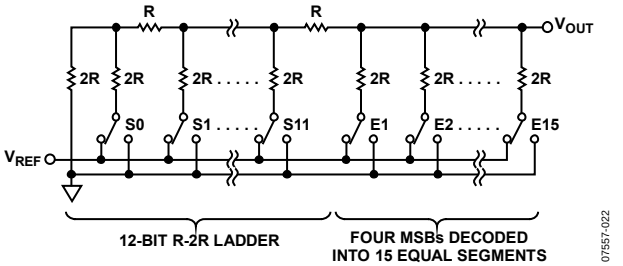


Figure 30. DAC Architecture

With this type of DAC configuration, the output impedance is independent of code, while the input impedance seen by the reference is heavily code dependent. The output voltage is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal data-word loaded to the DAC register.
N is the resolution of the DAC.

For a reference of 2.5 V, the equation simplifies to the following:

$$V_{OUT} = \frac{2.5 \times D}{65{,}536}$$

This gives a V_{OUT} of 1.25 V with midscale loaded, and 2.5 V with full-scale loaded to the DAC.

The LSB size is V_{REF}/65,536.

SERIAL INTERFACE

The AD5541/AD5542 are controlled by a versatile 3- or 4-wire serial interface that operates at clock rates up to 25 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The timing diagram is shown in Figure 5. Input data is framed by the chip select input, $\overline{CS}$. After a high-to-low transition on $\overline{CS}$, data is shifted synchronously and latched into the input register on the rising edge of the serial clock, SCLK. Data is loaded MSB first in 16-bit words. After 16 data bits have been loaded into the serial input register, a low-to-high transition on $\overline{CS}$ transfers the contents of the shift register to the DAC. Data can be loaded to the part only while $\overline{CS}$ is low.

The AD5542 has an $\overline{LDAC}$ function that allows the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. $\overline{LDAC}$ should be maintained high while data is written to the shift register. Alternatively, $\overline{LDAC}$ can be tied permanently low to update the DAC synchronously. With $\overline{LDAC}$ tied permanently low, the rising edge of $\overline{CS}$ loads the data to the DAC.

UNIPOLAR OUTPUT OPERATION

These DACs are capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low supply current, typically 300 μA, and a low offset error. The AD5541 provides a unipolar output swing ranging from 0 V to V_{REF}. The AD5542 can be configured to output both unipolar and bipolar voltages. Figure 31 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 6.

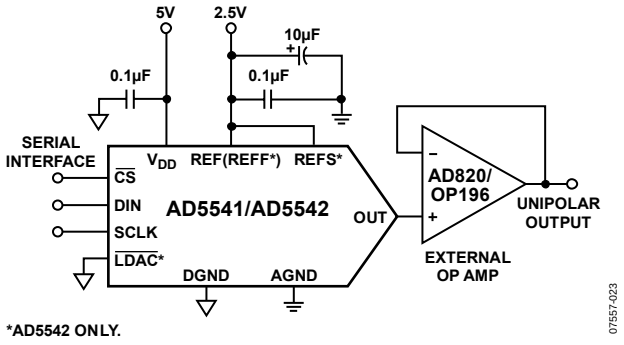


Figure 31. Unipolar Output

Table 6. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$V_{REF} \times (65{,}535/65{,}536)$
1000 0000 0000 0000	$V_{REF} \times (32{,}768/65{,}536) = ½ V_{REF}$
0000 0000 0000 0001	$V_{REF} \times (1/65{,}536)$
0000 0000 0000 0000	0 V

Assuming a perfect reference, the unipolar worst-case output voltage can be calculated from the following equation:

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times \left(V_{REF} + V_{GE}\right) + V_{ZSE} + INL$$

where:
$V_{OUT-UNI}$ is unipolar mode worst-case output.
D is code loaded to DAC.
V_{REF} is reference voltage applied to the part.
V_{GE} is gain error in volts.
V_{ZSE} is zero scale error in volts.
INL is integral nonlinearity in volts.

BIPOLAR OUTPUT OPERATION

With the aid of an external op amp, the AD5542 can be configured to provide a bipolar voltage output. A typical circuit of such operation is shown in Figure 32. The matched bipolar offset resistors, R_{FB} and R_{INV}, are connected to an external op amp to achieve this bipolar output swing, typically $R_{FB} = R_{INV} = 28\ k\Omega$. Table 7 shows the transfer function for this output operating mode. Also provided on the AD5542 are a set of Kelvin connections to the analog ground inputs.

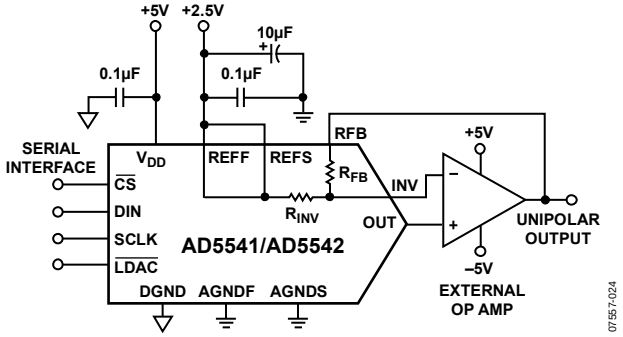


Figure 32. Bipolar Output (AD5542 Only)

Table 7. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$+V_{REF} \times (32{,}767/32{,}768)$
1000 0000 0000 0001	$+V_{REF} \times (1/32{,}768)$
1000 0000 0000 0000	0 V
0111 1111 1111 1111	$-V_{REF} \times (1/32{,}768)$
0000 0000 0000 0000	$-V_{REF} \times (32{,}768/32{,}768) = -V_{REF}$

Assuming a perfect reference, the worst-case bipolar output voltage can be calculated from the following equation:

$$V_{OUT-BIP} = \frac{\left[\left(V_{OUT-UNI} + V_{OS}\right)\left(2 + RD\right) - V_{REF}\left(1 + RD\right)\right]}{1 + \left(2 + RD\right)/A}$$

where:
$V_{OUT-BIP}$ is the bipolar mode worst-case output
$V_{OUT-UNI}$ is the unipolar mode worst-case output.
V_{OS} is the external op amp input offset voltage.
RD is the R_{FB} and R_{INV} resistor matching error.
A is the op amp open-loop gain.

OUTPUT AMPLIFIER SELECTION

For bipolar mode, a precision amplifier should be used and supplied from a dual power supply. This provides the $\pm V_{REF}$ output. In a single-supply application, selection of a suitable op amp may be more difficult as the output swing of the amplifier does not usually include the negative rail, in this case, AGND. This can result in some degradation of the specified performance unless the application does not use codes near zero.

The selected op amp needs to have a very low-offset voltage (the DAC LSB is 38 µV with a 2.5 V reference) to eliminate the need for output offset trims. Input bias current should also be very low because the bias current, multiplied by the DAC output impedance (approximately 6 kΩ), adds to the zero code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

FORCE SENSE AMPLIFIER SELECTION

Use single-supply, low-noise amplifiers. A low-output impedance at high frequencies is preferred because the amplifiers need to be able to handle dynamic currents of up to ±20 mA.

REFERENCE AND GROUND

Because the input impedance is code-dependent, the reference pin should be driven from a low impedance source. The AD5541/AD5542 operate with a voltage reference ranging from 2 V to V_{DD}. References below 2 V result in reduced accuracy. The full-scale output voltage of the DAC is determined by the reference. Table 6 and Table 7 outline the analog output voltage or particular digital codes. For optimum performance, Kelvin sense connections are provided on the AD5542.

If the application doesn't require separate force and sense lines, tie the lines close to the package to minimize voltage drops between the package leads and the internal die.

POWER-ON RESET

The AD5541/AD5542 have a power-on reset function to ensure that the output is at a known state on power-up. On power-up, the DAC register contains all 0s until the data is loaded from the serial register. However, the serial register is not cleared on power-up, so its contents are undefined. When loading data initially to the DAC, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept, and if less than 16 bits are loaded, bits remain from the previous word. If the AD5541/ AD5542 need to be interfaced with data shorter than 16 bits, the data should be padded with 0s at the LSBs.

POWER SUPPLY AND REFERENCE BYPASSING

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5541/AD5542 is via a serial bus that uses standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 3- or 4-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD5541/AD5542 require a 16-bit data-word with data valid on the rising edge of SCLK. The DAC update can be done automatically when all the data is clocked in or it can be done under control of the $\overline{\text{LDAC}}$ (AD5542 only).

AD5541/AD5542 TO ADSP-2101/ADSP-2103 INTERFACE

Figure 33 shows a serial interface between the AD5541/AD5542 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set to operate in the SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 are programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out on each rising edge of the serial clock, an inverter is required between the DSP and the DAC, because the AD5541/AD5542 clock data in on the falling edge of the SCLK.

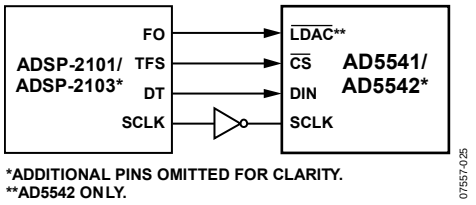


Figure 33. AD5541/AD5542 to ADSP-2101/ADSP-2103 Interface

AD5541/AD5542 TO 68HC11/68L11 INTERFACE

Figure 34 shows a serial interface between the AD5541/AD5542 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the DAC, and the MOSI output drives the serial data line serial DIN. The $\overline{\text{CS}}$ signal is driven from one of the port lines. The 68HC11/68L11 is configured for master mode: MSTR = 1, CPOL = 0, and CPHA = 0. Data appearing on the MOSI output is valid on the rising edge of SCK.

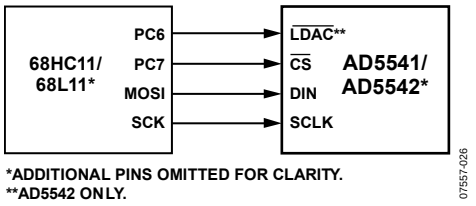


Figure 34. AD5541/AD5542 to 68HC11/68L11 Interface

AD5541/AD5542 TO MICROWIRE INTERFACE

Figure 35 shows an interface between the AD5541/AD5542 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and into the AD5541/AD5542 on the rising edge of the serial clock. No glue logic is required because the DAC clocks data into the input shift register on the rising edge.

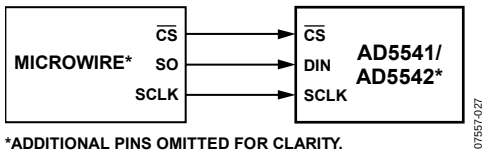


Figure 35. AD5541/AD5542 to MICROWIRE Interface

AD5541/AD5542 TO 80C51/80L51 INTERFACE

A serial interface between the AD5541/AD5542 and the 80C51/80L51 microcontroller is shown in Figure 36. TxD of the microcontroller drives the SCLK of the AD5541/AD5542, and RxD drives the serial data line of the DAC. P3.3 is a bit programmable pin on the serial port that is used to drive $\overline{\text{CS}}$.

The 80C51/80L51 provide the LSB first, whereas the AD5541/AD5542 expects the MSB of the 16-bit word first. Care should be taken to ensure the transmit routine takes this into account.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is valid on the falling edge of TxD, so the clock must be inverted as the DAC clocks data into the input shift register on the rising edge of the serial clock. The 80C51/80L51 transmit data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. As the DAC requires a 16-bit word, P3.3 must be left low after the first eight bits are transferred, and brought high after the second byte is transferred. $\overline{\text{LDAC}}$ on the AD5542 can also be controlled by the 80C51/ 80L51 serial port output by using another bit programmable pin, P3.4.

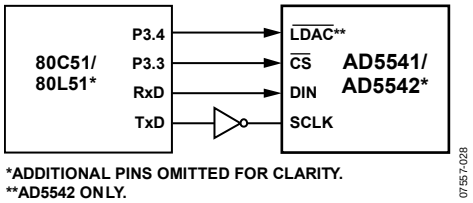


Figure 36. AD5541/AD5542 to 80C51/80L51 Interface

APPLICATIONS INFORMATION

OPTOCOUPLER INTERFACE

The digital inputs of the AD5541A/AD5542A/AD5512A are Schmitt-triggered so that they can accept slow transitions on the digital input lines. This makes these parts ideal for industrial applications where it may be necessary to isolate the DAC from the controller via optocouplers. Figure 37 illustrates such an interface.

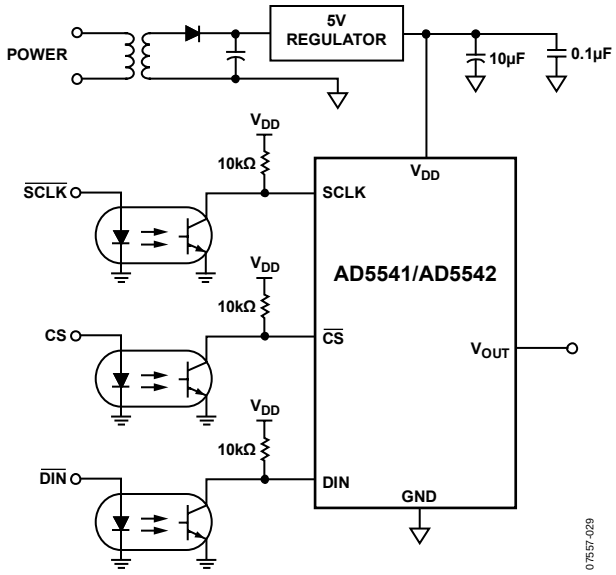


Figure 37. AD5541/AD5542 in an Optocoupler Interface

DECODING MULTIPLE AD5541/AD5542s

The $\overline{CS}$ pin of the AD5541/AD5542 can be used to select one of a number of DACs. All devices receive the same serial clock and serial data, but only one device receives the $\overline{CS}$ signal at any one time. The DAC addressed is determined by the decoder. There is some digital feedthrough from the digital input lines. Using a burst clock minimizes the effects of digital feedthrough on the analog signal channels. Figure 38 shows a typical circuit.

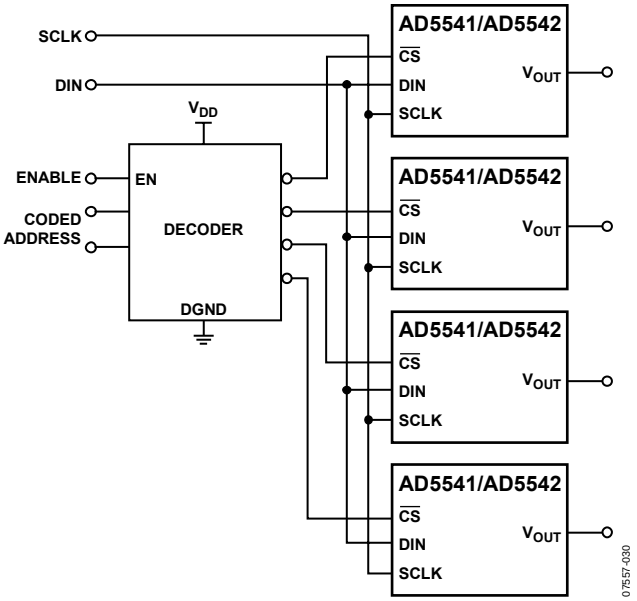
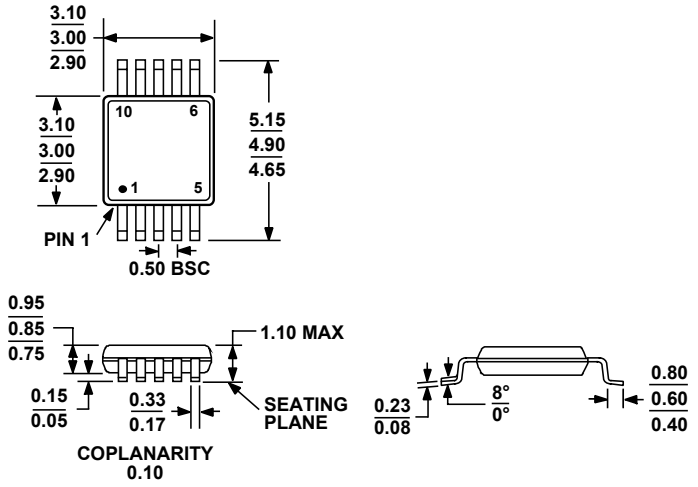


Figure 38. Addressing Multiple AD5541/AD5542s

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 39. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters.

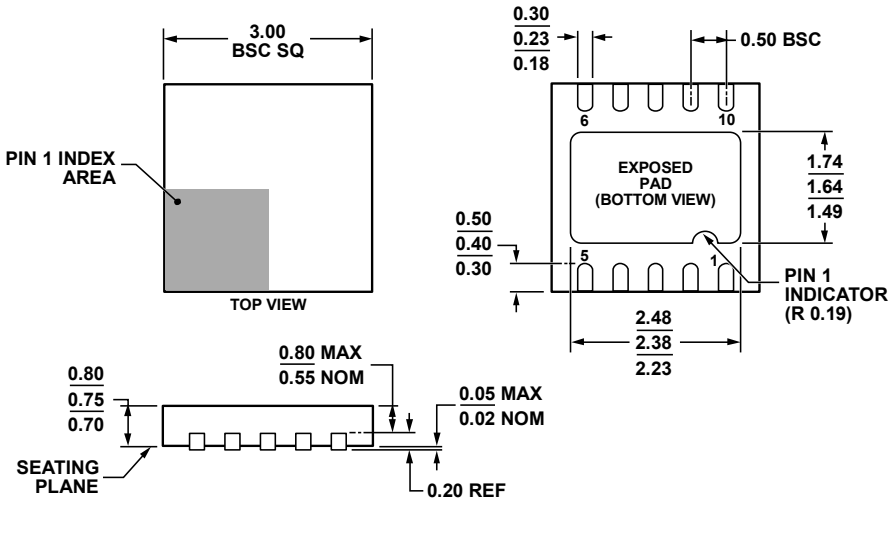


Figure 40. 10-Lead Lead Frame Chip Scale Package [LFCSP]

(CP-10-9)

Dimensions shown in millimeters.

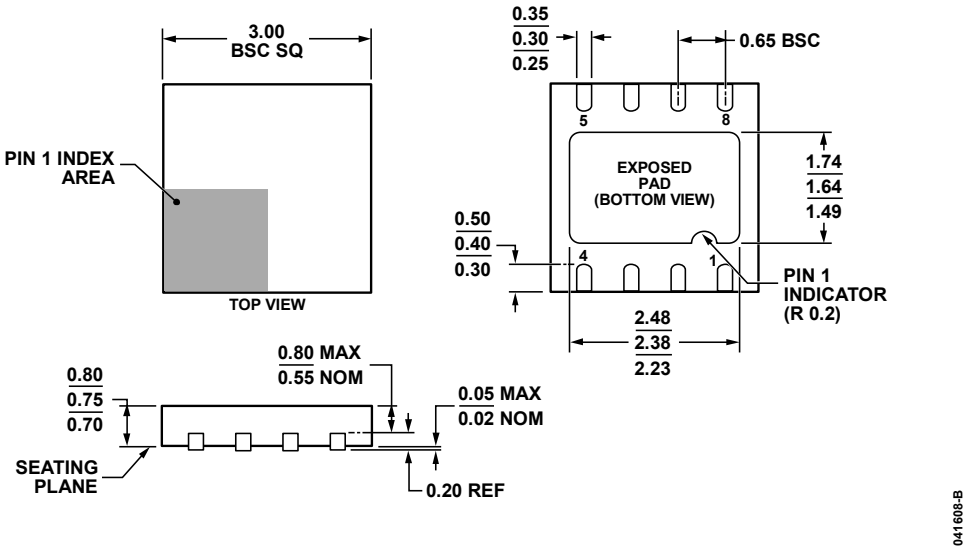
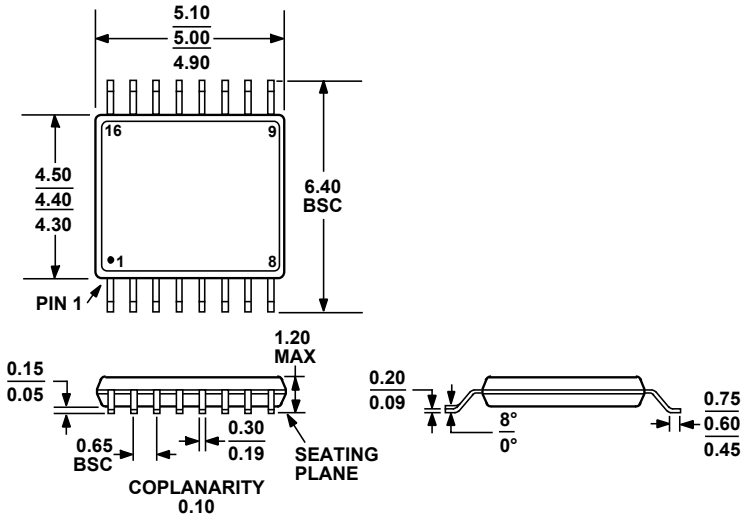


Figure 41. 8-Lead Lead Frame Chip Scale Package [LFCSP]

(CP-8-3)

Dimensions shown in millimeters.

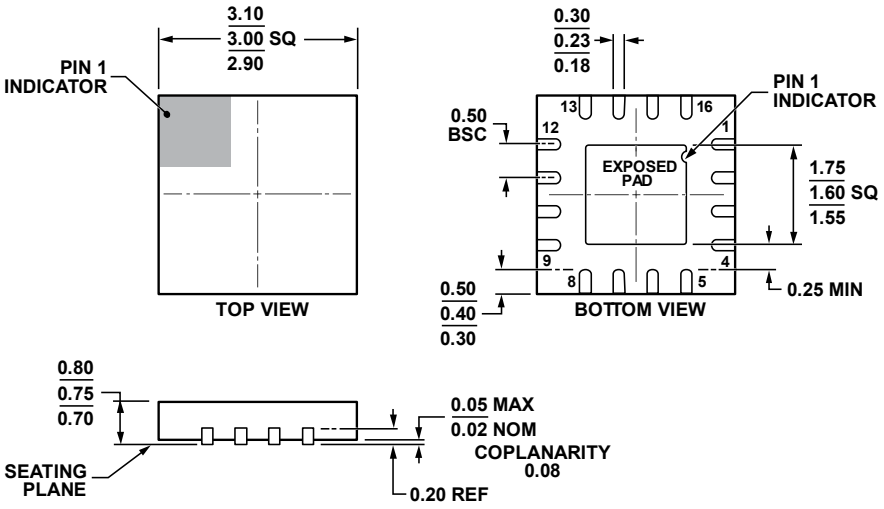


COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 42. 16-Lead Thin Shrink Small Outline Package [TSSOP]

(RU-16)

Dimensions shown in millimeters.



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.

Figure 43. 16-Lead Lead Frame Chip Scale Package [LFCSP]

(CP-16-22)

Dimensions shown in millimeters.

ORDERING GUIDE

Model	INL	DNL	Clear to Code	Temperature Range	Package Description	Package Option
AD5541ABRMZ	±1 LSB	±1 LSB	Midscale	−40°C to +105°C	10-Lead MSOP	RM-10
AD5541AARMZ	±2 LSB	±1 LSB	Midscale	−40°C to +105°C	10-Lead MSOP	RM-10
AD5541ABCPZ	±1 LSB	±1 LSB	Midscale	−40°C to +105°C	10-Lead LFCSP	CP-10-9
AD5541AACPZ	±2 LSB	±1 LSB	Midscale	−40°C to +105°C	10-Lead LFCSP	CP-10-9
AD5541ABCPZ-1	±1 LSB	±1 LSB	Zero-scale	−40°C to +105°C	8-Lead LFCSP	CP_8-3
AD5542ABRUZ	±1 LSB	±1 LSB	Midscale	−40°C to +105°C	16-Lead TSSOP	RU-16
AD5542AARUZ	±2 LSB	±1 LSB	Midscale	−40°C to +105°C	16-Lead TSSOP	RU-16
AD5542ASRUZ	±1 LSB	±1 LSB	Midscale	−55°C to +125°C	16-Lead TSSOP	RU-16
AD5542ABCPZ	±1 LSB	±1 LSB	Midscale	−40°C to +105°C	16-Lead LFCSP	CP-16-22
AD5542AACPZ	±2 LSB	±1 LSB	Midscale	−40°C to +105°C	16-Lead LFCSP	CP-16-22
AD5442ABCPZ-1	±1 LSB	±1 LSB	Midscale	−40°C to +105°C	10-Lead LFCSP	CP-10-9
AD5512AACPZ	±1 LSB	±1 LSB	Midscale	−40°C to +105°C	16-Lead LFCSP	CP-16-22

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PR08516-0-12/09(PrA)