40-Channel, 14-Bit Serial Input, Voltage-Output DAC

Preliminary Technical Data

AD5371

FEATURES

- 40-channel DAC in 80 Lead LQFP and 100 Ball CSPBGA
- Guaranteed monotonic to 14 bits
- Maximum output voltage span of 4 × V_{REF} (20 V)
- Nominal output voltage range of -4 V to +8 V
- Multiple, Independent output spans available
- System calibration function allowing user-programmable offset and gain
- Channel grouping and addressing features
- Thermal Monitor Function
- DSP/microcontroller-compatible serial interface
- LVDS serial interface
- 2.5 V to 5.5 V JEDEC-compliant digital levels
- Power-on reset
- Digital reset ($\overline{RESET}$)
- Clear function to user-defined SIGGND ($\overline{CLR}$ pin)
- Simultaneous update of DAC outputs ($\overline{LDAC}$ pin)

APPLICATIONS

- Level setting in automatic test equipment (ATE)
- Variable optical attenuators (VOA)
- Optical switches
- Industrial control systems
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

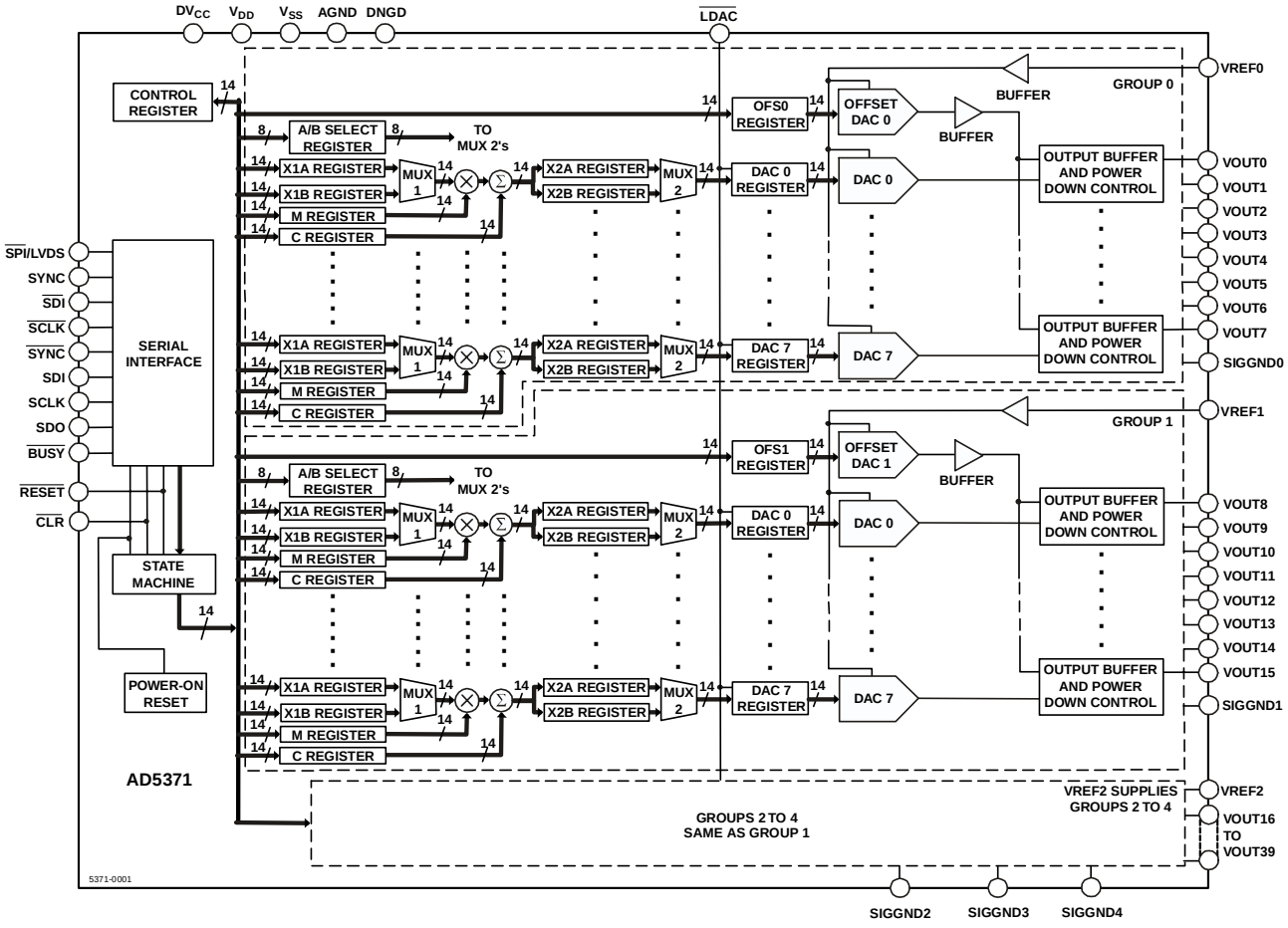

Figure 1.

Rev. PrF

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REVISION HISTORY

The AD5371 contains 40, 14-bit DACs in a single, 80-lead, LQFP package. It provides buffered voltage outputs with a span 4 times the reference voltage. The gain and offset of each DAC can be independently trimmed to remove errors. For even greater flexibility, the device is divided into blocks of 8 DACs, and the output range of each block can be independently adjusted by an offset DAC. Group 0 can be adjusted by Offset DAC 0, group 1 can be adjusted by Offset DAC 1 and group 2 to group 4 can be adjusted by Offset DAC 2.

The AD5371 offers guaranteed operation over a wide supply range with V_{SS} from -4.5 V to -16.5 V and V_{DD} from +8 V to +16.5 V. The output amplifier headroom requirement is 1.4 V operating with a load current of 1 mA.

The AD5371 has a high-speed serial interface, which is compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards and can handle clock speeds of up to 50 MHz. It also has a 100 MHz Low Voltage Differential Signaling (LVDS) serial interface compliant with EIA-644 specification.

The DAC outputs are updated on reception of new data into the DAC registers. All the outputs can be updated simultaneously by taking the $\overline{\text{LDAC}}$ input low. Each channel has a programmable gain and an offset adjust register.

Each DAC output is amplified and buffered on-chip with respect to an external SIGGND input. The DAC outputs can also be switched to SIGGND via the $\overline{\text{CLR}}$ pin.

Table 1. High Channel Count Bipolar DACs

Model	Resolution	Nominal Output Span	Output Channels	Linearity Error (LSB)	Package Description	Package Option
AD5360BCPZ	16 Bits	4 × V_{REF} (20 V)	16	±4	56-Lead LFCSP	CP-56
AD5360BSTZ	16 Bits	4 × V_{REF} (20 V)	16	±4	52-Lead LQFP	ST-52
AD5361BCPZ	14 Bits	4 × V_{REF} (20 V)	16	±1	56-Lead LFCSP	CP-56
AD5361BSTZ	14 Bits	4 × V_{REF} (20 V)	16	±1	52-Lead LQFP	ST-52
AD5362BCPZ	16 Bits	4 × V_{REF} (20 V)	8	±4	56-Lead LFCSP	CP-56
AD5362BSTZ	16 Bits	4 × V_{REF} (20 V)	8	±4	52-Lead LQFP	ST-52
AD5363BCPZ	14 Bits	4 × V_{REF} (20 V)	8	±1	56-Lead LFCSP	CP-56
AD5363BSTZ	14 Bits	4 × V_{REF} (20 V)	8	±1	52-Lead LQFP	ST-52
AD5370BCPZ	16 Bits	4 × V_{REF} (12 V)	40	±4	64-Lead LFCSP	CP-64
AD5370BSTZ	16 Bits	4 × V_{REF} (12 V)	40	±4	64-Lead LQFP	ST-64
AD5371BCPZ	14 Bits	4 × V_{REF} (12 V)	40	±1	100-Ball CSPBGA	BC-100-2
AD5371BSTZ	14 Bits	4 × V_{REF} (12 V)	40	±1	80-Lead LQFP	ST-80
AD5372BCPZ	16 Bits	4 × V_{REF} (12 V)	32	±4	56-Lead LFCSP	CP-56
AD5372BSTZ	16 Bits	4 × V_{REF} (12 V)	32	±4	64-Lead LQFP	ST-64
AD5373BCPZ	14 Bits	4 × V_{REF} (12 V)	32	±1	56-Lead LFCSP	CP-56
AD5373BSTZ	14 Bits	4 × V_{REF} (12 V)	32	±1	64-Lead LQFP	ST-64

SPECIFICATIONS

DV_{CC} = 2.3 V to 5.5 V; V_{DD} = 8 V to 16.5 V; V_{SS} = −4.5 V to −16.5 V; V_{REF} = 3 V; AGND = DGND = SIGGND = 0 V; R_L = Open Circuit; Gain (m), Offset (c) and DAC Offset registers at default values; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.Performance Specifications

Parameter	B Version[1]	Unit	Test Conditions/Comments[2]
ACCURACY			
Resolution	14	Bits	
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed monotonic by design over temperature.
Offset Error	±20	mV max	Before Calibration
Gain Error	±20	mV max	Before Calibration
Offset Error[2]	100	µV max	After Calibration
Gain Error[2]	100	µV max	After Calibration
Gain Error of Offset DAC	±35	mV max	Positive or Negative Full Scale. See Offset DACs section for details
VOUT Temperature Coefficient	5	ppm FSR/°C typ	Includes linearity, offset, and gain drift.
DC Crosstalk[2]	1.5	mV max	Typically 100 µV. Measured channel at mid-scale, full-scale change on any other channel
REFERENCE INPUTS (VREF0, VREF1, VREF2)[2]			
V_{REF} Input Current	60	nA max	Per input. Typically ±30 nA.
V_{REF} Range	2/5	V min/max	±2% for specified operation.
SIGGND INPUT (SIGGND0 TO SIGGND4)[2]			
DC Input Impedance	55	kΩ min	Typically 60 kΩ.
Input Range	±0.5	V min/max	
OUTPUT CHARACTERISTICS[2]			
Output Voltage Range	V_{SS} + 1.4	V min	I_{LOAD} = 1 mA.
	V_{DD} − 1.4	V max	I_{LOAD} = 1 mA.
Nominal Output Voltage Range	-4 to +8	V	
Short Circuit Current	10	mA max	
Load Current	±1	mA max	
Capacitive Load Stability	2	nF max	
DC Output Impedance	0.5	Ω max	
DIGITAL INPUTS			JEDEC compliant.
Input High Voltage	1.7	V min	DV_{CC} = 2.3 V to 3.6 V.
	2.0	V min	DV_{CC} = 3.6 V to 5.5 V.
Input Low Voltage	0.8	V max	DV_{CC} = 2.5 V to 5.5 V.
	0.7	V	DV_{CC} = 2.3 V to 2.7 V.
Input Current	±1	µA max	Except $\overline{CLR}$ and $\overline{RESET}$
Input Capacitance[2]	10	pF max	
DIGITAL OUTPUTS (SDO, $\overline{BUSY}$)			
Output Low Voltage	0.5	V max	Sinking 200 µA.
Output High Voltage (SDO)	DV_{CC} − 0.5	V min	Sourcing 200 µA.
High Impedance Leakage Current	±5	µA max	SDO only.
High Impedance Output Capacitance	10	pF typ	

Parameter	B Version[1]	Unit	Test Conditions/Comments[2]
LVDS INTERFACE – Reduced Range Link			
Digital Inputs[2]			
Input Voltage Range	875/1575	mV min/max	
Input Differential Threshold	−0.1/0.1	V min/max	
External Termination Resistance	80/120	Ω min/max	
	100	Ω typ	
	132	Ω max	
Differential Input Voltage	100	mV min	
POWER REQUIREMENTS			
DV_{CC}	2.3/5.5	V min/max	
V_{DD}	8/16.5	V min/max	
V_{SS}	−4.5/−16.5	V min/max	
Power Supply Sensitivity[2]			
Δ Full Scale/Δ V_{DD}	−75	dB typ	
Δ Full Scale/Δ V_{SS}	−75	dB typ	
Δ Full Scale/Δ V_{CC}	−90	dB typ	
DI_{CC}	2	mA max	V_{CC} = 5.5 V, $V_{IH} = V_{CC}$, V_{IL} = GND.
I_{DD}	14	mA max	Outputs unloaded.
I_{SS}	14	mA max	Outputs unloaded.
Power Dissipation			
Power Dissipation Unloaded (P)	250	mW	V_{SS} = -5.5 V, V_{DD} = +9.5 V, DV_{CC} = 2.5 V
Junction Temperature[3]	130	°C max	$T_J = T_A + P_{TOTAL} \times \theta_J$.

AC CHARACTERISTICS

DV_{CC} = 2.5; V_{DD} = 15 V; V_{SS} = −15 V; V_{REF} = 3 V; AGND = DGND = SIGGND = 0 V; C_L = 200 pF to GND; R_L = 10 kΩ to GND; Gain (m), Offset (c) and DAC Offset registers at default values; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3. AC Characteristics

Parameter	b Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	TBD	µs typ	Full-scale change
	30	µs max	
Slew Rate	1	V/µs typ	
Digital-to-Analog Glitch Energy	20	nV-s typ	
Glitch Impulse Peak Amplitude	10	mV max	
Channel-to-Channel Isolation	100	dB typ	V_{REF}(+) = 2 V p-p, 1 kHz.
DAC-to-DAC Crosstalk	40	nV-s typ	Between DACs inside a group.
	10	nV-s typ	Between DACs from different groups.
Digital Crosstalk	0.1	nV-s typ	
Digital Feedthrough	1	nV-s typ	Effect of input bus activity on DAC output under test.
Output Noise Spectral Density @ 10 kHz	250	nV/(Hz)$^{1/2}$ typ	V_{REF} = 0 V.

TIMING CHARACTERISTICS

DV_{CC} = 2.3 V to 5.5 V; V_{DD} = 8 V to 16.5 V; V_{SS} = −4.5 V to −16.5 V; V_{REF} = 3 V; AGND = DGND = SIGGND = 0 V; R_L = Open Circuit; Gain (m), Offset (c) and DAC Offset registers at default values; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

SPI INTERFACE (Figure 4 and Figure 5)

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	20	ns min	SCLK Cycle Time.
t_2	8	ns min	SCLK High Time.
t_3	8	ns min	SCLK Low Time.
t_4	11	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time.
t_5	20	ns min	Minimum $\overline{SYNC}$ High Time.
t_6	10	ns min	24th SCLK Falling Edge to $\overline{SYNC}$ Rising Edge.
t_7	5	ns min	Data Setup Time.
t_8	5	ns min	Data Hold Time.
t_9[3]	42	ns max	$\overline{SYNC}$ Rising Edge to $\overline{BUSY}$ Falling Edge.
t_{10}	1.25	µs max	$\overline{BUSY}$ Pulse Width Low (Single-Channel Update.) See Table 7
t_{11}	500	ns max	Single-Channel Update Cycle Time
t_{12}	20	ns min	24th SCLK Falling Edge to $\overline{LDAC}$ Falling Edge.
t_{13}	10	ns min	$\overline{LDAC}$ Pulse Width Low.
t_{14}	3	µs max	$\overline{BUSY}$ Rising Edge to DAC Output Response Time.
t_{15}	0	ns min	$\overline{BUSY}$ Rising Edge to $\overline{LDAC}$ Falling Edge.
t_{16}	3	µs max	$\overline{LDAC}$ Falling Edge to DAC Output Response Time.
t_{17}	20/30	µs typ/max	DAC Output Settling Time.
t_{18}	125	ns max	$\overline{CLR}$/$\overline{RESET}$ Pulse Activation Time.
t_{19}	30	ns min	$\overline{RESET}$ Pulse Width Low.
t_{20}	400	µs max	$\overline{RESET}$ Time Indicated by $\overline{BUSY}$ Low.
t_{21}	270	ns min	Minimum $\overline{SYNC}$ High Time in Readback Mode.
t_{22}[5]	25	ns max	SCLK Rising Edge to SDO Valid.

LVDS INTERFACE (Figure 6)

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	10	ns min	SCLK Cycle Time.
t_2	4	ns min	SCLK Pulse Width High and Low Time.
t_3	2	ns min	$\overline{SYNC}$ to SCLK Setup Time.
t_4	2	ns min	Data Setup Time.
t_5	2	ns min	Data Hold Time.
t_6	2	ns min	SCLK to $\overline{SYNC}$ Hold Time.

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_r = t_f$ = 2 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.

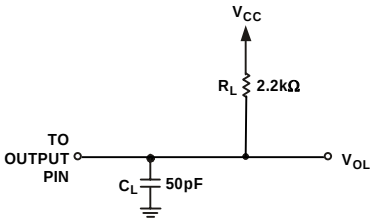


Figure 2. Load Circuit for $\overline{BUSY}$ Timing Diagram

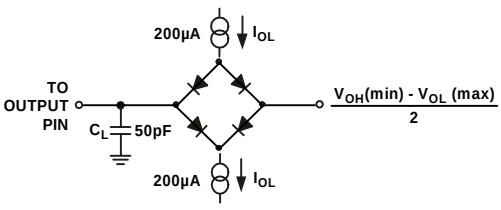
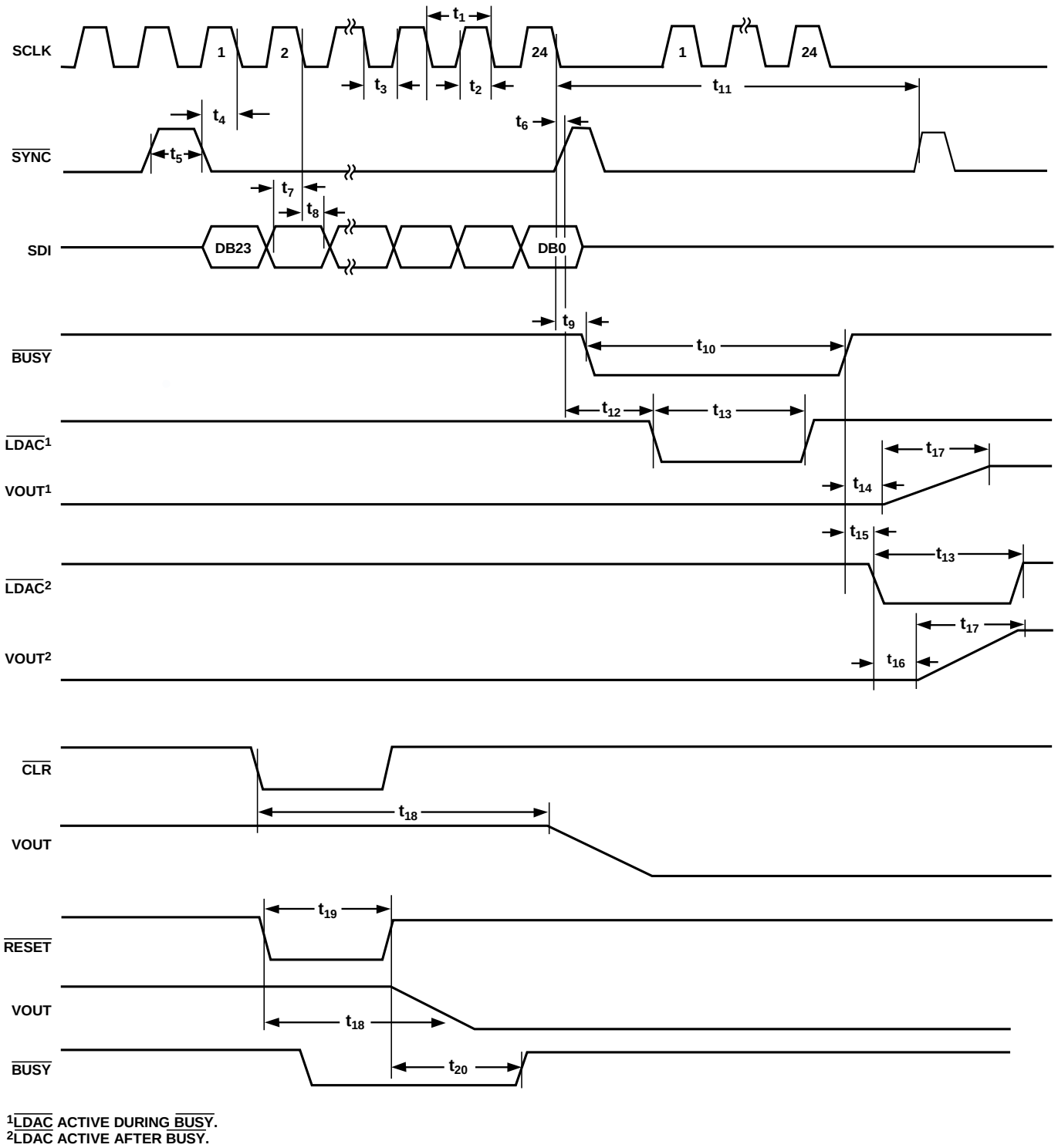


Figure 3. Load Circuit for SDO Timing Diagram



[1]LDAC ACTIVE DURING BUSY.
[2]LDAC ACTIVE AFTER BUSY.

Figure 4. SPI Write Timing

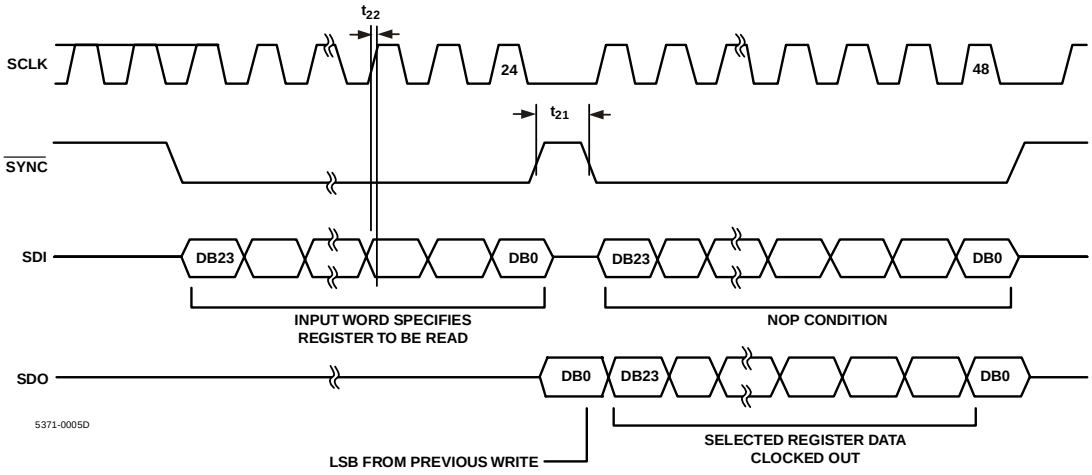


Figure 5. SPI Read Timing

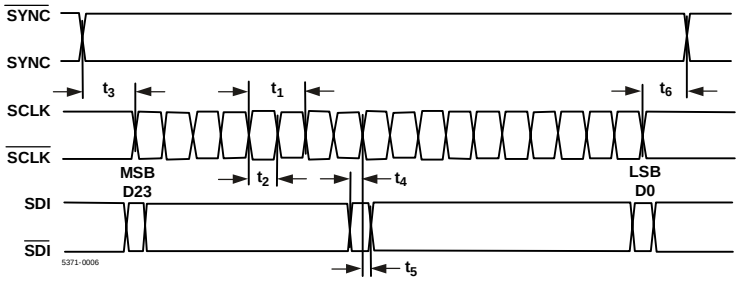


Figure 6.LVDS Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to AGND	−0.3 V to +17 V
V_{SS} to AGND	−17 V to +0.3 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to V_{CC} + 0.3 V
Digital Outputs to DGND	−0.3 V to V_{CC} + 0.3 V
$V_{REF}1$, $V_{REF}2$ to AGND	−0.3 V to +7 V
VOUT0–VOUT39 to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
SIGGND to AGND	± 1 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	130°C
θ_{JA} Thermal Impedance	
80-LQFP	38.72°C/w
100-CSPBGA	40°C/w
Reflow Soldering	
Peak Temperature	230°C
Time at Peak Temperature	10 s to 40 s

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

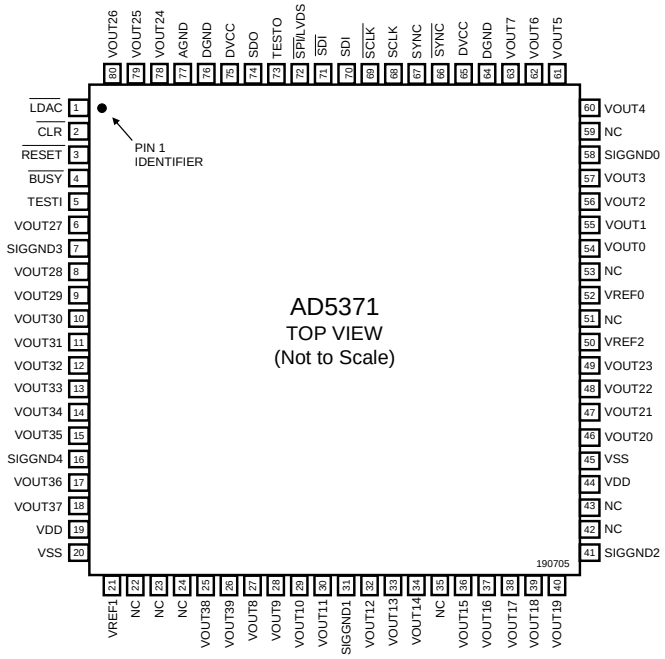


Figure 7.80-Lead LQFP Pin Configuration

12	11	10	9	8	7	6	5	4	3	2	1	
DGND	DGND	DVCC	SYNC	SCLK	DIN	SPI/ LVDS	NC	LDAC	CLR	NC	AGND2	A
VOUT6	VOUT7	DVCC	SYNC	SCLK	DIN	NC	SDO	RESET	BUSY	TESTI	AGND2	B
VOUT4	VOUT5	NC	NC	NC	NC	NC	NC	NC	NC	AGND1	AGND1	C
VOUT3	SIGGND 0	NC	AGND2	AGND1	AGND1	AGND1	AGND1	AGND1	NC	VOUT25	VOUT26	D
VOUT1	VOUT2	NC	AGND2	NC	NC	NC	NC	VSS	NC	VOUT24	VOUT27	E
VOUT0	NC	NC	AGND2	NC	NC	NC	NC	VSS	NC	NC	SIGGND 3	F
VREF0	NC	NC	AGND2	NC	NC	NC	NC	VSS	NC	VOUT28	NC	G
VOUT23	VREF2	NC	AGND2	NC	NC	NC	NC	VSS	NC	VOUT30	VOUT29	H
VOUT21	VOUT22	NC	VDD	VDD	VDD	VDD	VDD	VSS	NC	VOUT32	VOUT31	J
VOUT20	VOUT19	NC	NC	NC	NC	NC	NC	NC	NC	VOUT34	VOUT33	K
SIGGND 2	VDD	VOUT17	VOUT15	VOUT13	SIGGND 1	VOUT10	VOUT8	VOUT38	SIGGND 4	VSS	VOUT35	L
VDD	VOUT18	VOUT16	VOUT14	VOUT12	VOUT11	VOUT9	VOUT39	VREF1	VOUT37	VOUT36	VSS	M

NC = NO CONNECT

5371-0100A

Figure 8.144-Ball Grid Array Pin Configuration – Bottom View

Table 5. Pin Function Descriptions

Pin	Function
DV_{CC}	Logic Power Supply; 2.5 V to 5.5 V. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
V_{SS}	Negative Analog Power Supply; −4.5 V to −16.5 V for specified performance. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
V_{DD}	Positive Analog Power Supply; +8 V to +16.5 V for specified performance. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
AGND	Ground for All Analog Circuitry. All AGND pins should be connected to the AGND plane.
DGND	Ground for All Digital Circuitry. All DGND pins should be connected to the DGND plane.
$V_{REF}0$	Reference Input for DACs 0 to 7. This reference voltage is referred to AGND.
$V_{REF}1$	Reference Input for DACs 8 to 15. reference This voltage is referred to AGND.
$V_{REF}2$	Reference Input for DACs 16 to 39. This reference voltage is referred to AGND.
VOUT0 to VOUT39	DAC Outputs. Buffered analog outputs for each of the 40 DAC channels. Each analog output is capable of driving an output load of 10 kΩ to ground. Typical output impedance of these amplifiers is 0.5 Ω.
$\overline{SYNC}$	Active Low or Differential $\overline{SYNC}$ Input (Complement) for SPI or LVDS Interface. This is the frame synchronization signal for the SPI or LVDS serial interface. See SPI and LVDS timing diagrams and descriptions for more details.
SCLK	Serial Clock Input for SPI or LVDS Interface. See SPI and LVDS timing diagrams and descriptions for more details.
SDI	Serial Data Input for SPI or LVDS Interface. See SPI and LVDS timing diagrams and descriptions for more details.
SDO	Serial Data Output for SPI Interface. CMOS output. SDO can be used for readback. Data is clocked out on SDO on the rising edge of SCLK and is valid on the falling edge of SCLK.
SYNC	Differential SYNC Input for LVDS Interface . This is the frame synchronization signal for the LVDS serial interface. See LVDS timing diagram and description for more details.
$\overline{SCLK}$	Differential Serial Clock Input (Complement) for LVDS Interface. See LVDS timing diagrams and descriptions for more details.
$\overline{SDI}$	Differential Serial Data Input (Complement) for LVDS Interface. See LVDS timing diagrams and descriptions for more details.
$\overline{CLR}$	Asynchronous Clear Input (level sensitive, active low). See the Clear Function section for more information
$\overline{SPI}$/LVDS	Selects between SPI (low) or LVDS (high) serial interface.
$\overline{LDAC}$	Load DAC Logic Input (active low). See the $\overline{BUSY}$ AND $\overline{LDAC}$ FUNCTIONS section for more information
$\overline{BUSY}$	Digital Input/Open-Drain Output. $\overline{BUSY}$ is open-drain when an output. See the $\overline{BUSY}$ AND $\overline{LDAC}$ FUNCTIONS section for more information
$\overline{RESET}$	Asynchronous Digital Reset Input.
SIGGND0	Reference Ground for DACs 0 to 7. VOUT0 to VOUT7 are referenced to this voltage.
SIGGND1	Reference Ground for DACs 8 to 15. VOUT8 to VOUT15 are referenced to this voltage.
SIGGND1	Reference Ground for DACs 16 to 23. VOUT16 to VOUT23 are referenced to this voltage.
SIGGND3	Reference Ground for DACs 24 and 31. VOUT24 to VOUT31 are referenced to this voltage.
SIGGND4	Reference Ground for DACs 32 to 39. VOUT32 to VOUT39 are referenced to this voltage.
TESTI	Test Input Pin. This pin should be connected to DGND
TESTO	Test Output Pin. This pin should be left unconnected

TERMINOLOGY

Relative Accuracy
Relative accuracy, or endpoint linearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in least significant bits (LSB).

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register.
Zero-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV. Zero-scale error is mainly due to offsets in the output amplifier.

Full-Scale Error
Full-scale error is the error in DAC output voltage when all 1s are loaded into the DAC register.
Full-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV. It does not include zero-scale error.

Gain Error Gain error is the difference between full-scale error and zero-scale error. It is expressed in mV.

Gain Error = Full-Scale Error − Zero-Scale Error

VOUT Temperature Coefficient
This includes output error contributions from linearity, offset, and gain drift.

DC Output Impedance
DC output impedance is the effective output source resistance. It is dominated by package lead resistance.

DC Crosstalk
The DAC outputs are buffered by op amps that share common V_{DD} and V_{SS} power supplies. If the dc load current changes in one channel (due to an update), this can result in a further dc change in one or more channel outputs. This effect is more significant at high load currents and reduces as the load currents are reduced. With high impedance loads, the effect is virtually immeasurable. Multiple V_{DD} and V_{SS} terminals are provided to minimize dc crosstalk.

Output Voltage Settling Time
The amount of time it takes for the output of a DAC to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Energy
The amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input that appears at the output of another DAC operating from another reference. It is expressed in dB and measured at midscale.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog output change at another converter. It is specified in nV-s.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the VOUT pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density

Output noise spectral density is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in $nV/(Hz)^{1/2}$

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE—GENERAL

The AD5371 contains 40 DAC channels and 40 output amplifiers in a single package. The architecture of a single DAC channel consists of a 14-bit resistor-string DAC followed by an output buffer amplifier. The resistor-string section is simply a string of resistors, each of value R, from V_{REF} to AGND. This type of architecture guarantees DAC monotonicity. The 14-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier multiplies the DAC out voltage by 4. The output span is 12 V with a 3 V reference and 20 V with a 5 V reference.

CHANNEL GROUPS

The 40 DAC channels of the AD5371 are arranged into five groups of 8 channels. The eight DACs of Group 0 derive their reference voltage from VREF0, those of Group 1 from VREF1, while the remaining groups derive their reference voltage from VREF2. Each group has its own signal ground pin.

Table 6. AD5371 Registers

Register Name	Word Length (Bits)	Description
X1A (group)(channel)	14	Input data register A, one for each DAC channel.
X1B (group) (channel)	14	Input data register B, one for each DAC channel.
M (group) (channel)	14	Gain trim registers, one for each DAC channel.
C (group) (channel)	14	Offset trim registers, one for each DAC channel.
X2A (group)(channel)	14	Output data register A, one for each DAC channel. These registers store the final, calibrated DAC data after gain and offset trimming. They are not readable, nor directly writable.
X2B (group) (channel)	14	Output data register B, one for each DAC channel. These registers store the final, calibrated DAC data after gain and offset trimming. They are not readable, nor directly writable.
DAC (group) (channel)		Data registers from which the DACs take their final input data. The DAC registers are updated from the X2A or X2B registers. They are not readable, nor directly writable.
OFS0	14	Offset DAC 0 data register, sets offset for Group 0.
OFS1	14	Offset DAC 1 data register, sets offset for Group 1.
OFS2	14	Offset DAC 2 data register, sets offset for Groups 2 to 4.
Control	3	Bit 2 = $\overline{A}$/B. 0 = global selection of X1A input data registers. 1 = X1B registers. Bit 1 = Enable Temp Shutdown. 0 = disable temp shutdown. 1 = enable. Bit 0 = Soft Power Down. 0 = soft power up. 1 = soft power down.
A/B Select 0	8	Each bit in this register determines if a DAC in Group 0 takes its data from register X2A or X2B (0 = X2A, 1 = X2B)
A/B Select 1	8	Each bit in this register determines if a DAC in Group 1 takes its data from register X2A or X2B (0 = X2A, 1 = X2B)
A/B Select 2	8	Each bit in this register determines if a DAC in Group 2 takes its data from register X2A or X2B (0 = X2A, 1 = X2B)
A/B Select 3	8	Each bit in this register determines if a DAC in Group 3 takes its data from register X2A or X2B (0 = X2A, 1 = X2B)
A/B Select 4	8	Each bit in this register determines if a DAC in Group 4 takes its data from register X2A or X2B (0 = X2A, 1 = X2B)

A/ B REGISTERS AND GAIN/OFFSET ADJUSTMENT

Each DAC channel has seven data registers. The actual DAC data word can be written to either the X1A or X1B input register, depending on the setting of the $\overline{A}$/B bit in the Control Register. If the $\overline{A}$/B bit is 0, data will be written to the X1A register. If the $\overline{A}$/B bit is 1, data will be written to the X1B register. Note that this single bit is a global control and affects every DAC channel in the device. It is not possible to set up the device on a per-channel basis so that some writes are to X1A registers and some writes are to X1B registers.

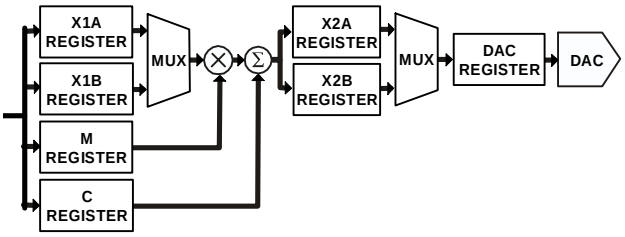


Figure 9. Data Registers Associated With Each DAC Channel

Each DAC channel also has a gain (M) and offset (C) register, which allow trimming out of the gain and offset errors of the entire signal chain. Data from the X1A register is operated on by a digital multiplier and adder controlled by the contents of the M and C registers. The calibrated DAC data is then stored in the X2A register. Similarly, data from the X1B register is operated on by the multiplier and adder and stored in the X2B register.

Although a multiplier and adder symbol are shown for each channel, there is only one multiplier and one adder in the device, which are shared between all channels. This has implications for the update speed when several channels are updated at once, as described later.

Each time data is written to the X1A register, or to the M or C register with the $\overline{A}$/B control bit set to 0, the X2A data is recalculated and the X2A register is automatically updated. Similarly, X2B is updated each time data is written to X1B, or to M or C with $\overline{A}$/B set to 1. The X2A and X2B registers are not readable, nor directly writable by the user.

Data output from the X2A and X2B registers is routed to the final DAC register by a multiplexer. Whether each individual DAC takes its data from the X2A or X2B register is controlled by an 8-bit A/B Select Register associated with each group of 8 DACs. If a bit in this register is 0, the DAC takes its data from the X2A register; if 1 the DAC takes its data from the X2B register (bit 0 controls DAC 0 through bit 7 controls DAC 7).

Note that, since there are 40 bits in 5 registers, it is possible to set up, on a per-channel basis, whether each DAC takes its data from the X2A or X2B register. A global command is also provided that sets all bits in the A/B Select Registers to 0 or to 1.

LOAD DAC

All DACs in the AD5371 can be updated simultaneously by taking $\overline{LDAC}$ low, when each DAC register will be updated from either its X2A or X2B register, depending on the setting of the A/B select registers. The DAC register is not readable, nor directly writable by the user.

OFFSET DACS

In addition to the gain and offset trim for each DAC, there are three 14-bit Offset DACs, one for Group 0, one for group 1, and one for groups 2 to 4. These allow the output range of all DACs connected to them to be offset within a defined range. Thus, subject to the limitations of headroom, it is possible to set the output range of Group 0, Group 1 or Groups 2 to 4 to be unipolar positive, unipolar negative, or bipolar, either symmetrical or asymmetrical about zero volts. The DACs in the AD5371 are factory trimmed with the Offset DACs set at their default values. This gives the best offset and gain performance for the default output range and span.

When the output range is adjusted by changing the value of the Offset DAC an extra offset is introduced due to the gain error of the Offset DAC. The amount of offset is dependent on the magnitude of the reference and how much the Offset DAC moves from its default value. This offset is quoted on the specification page. The worst case offset occurs when the Offset DAC is at positive or negative full-scale. This value can be added to the offset present in the main DAC of a channel to give an indication of the overall offset for that channel. In most cases the offset can be removed by programming the channels C register with an appropriate value. The extra offset cause by the Offset DACs only needs to be taken into account when the Offset DAC is changed from its default value. Figure 10 shows the allowable code range which may be loaded to the Offset DAC and this is dependant on the reference value used. Thus, for a 5V reference, the Offset DAC should not be programmed with a value greater than 8192 (0x2000).

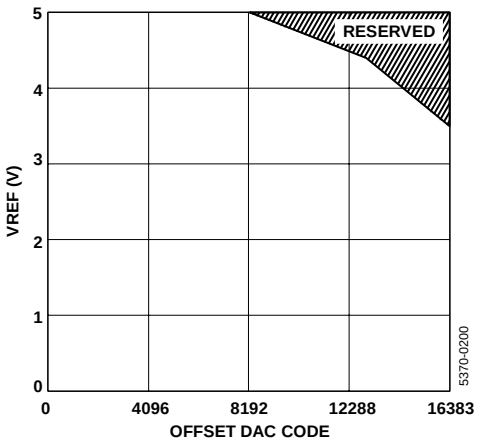


Figure 10. Offset DAC Code Range

OUTPUT AMPLIFIER

As the output amplifiers can swing to 1.4 V below the positive supply and 1.4 V above the negative supply, this limits how much the output can be offset for a given reference voltage. For example, it is not possible to have a unipolar output range of 20V, since the maximum supply voltage is ±16.5 V.

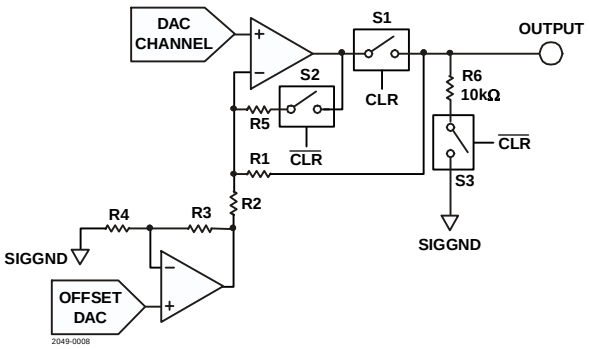


Figure 11. Output Amplifier and Offset DAC

Figure 11 shows details of a DAC output amplifier and its connections to the Offset DAC. On power up, S1 is open, disconnecting the amplifier from the output. S3 is closed, so the output is pulled to SIGGND (R1 and R2 are very much greater than R6). S2 is also closed to prevent the output amplifier being open-loop. If $\overline{\text{CLR}}$ is low at power-up, the output will remain in this condition until $\overline{\text{CLR}}$ is taken high. The DAC registers can be programmed, and the outputs will assume the programmed values when $\overline{\text{CLR}}$ is taken high. Even if $\overline{\text{CLR}}$ is high at power-up, the output will remain in the above condition until V_{DD} > 6 V and V_{SS} < -4 V and the initialization sequence has finished. The outputs will then go to their power-on default value.

TRANSFER FUNCTION

From the previous text, it can be seen that the output voltage of a DAC in the AD5371 depends on the value in the input register, the value of the M and C registers, and the offset from the Offset DAC. The transfer function is given by:

Code applied to DAC from X1A or X1B register:-

$$DAC\_CODE = INPUT\_CODE \times (m+1)/2^{14} + c - 2^{13}$$

DAC output voltage:-

$$V_{OUT} = 4 \times V_{REF} \times (DAC\_CODE - OFFSET\_CODE)/2^{14} + V_{SIGGND}$$

Notes
DAC_CODE should be within the range of 0 to 16383.
For 12 V span V_{REF} = 3.0 V.
For 20 V span V_{REF} = 5.0 V.
X1A, X1B default code = 5461
m = code in gain register - default code = $2^{14} - 1$.
c = code in offset register - default code = 2^{13}.
OFFSET_CODE is the code loaded to the offset DAC. It is multiplied by 4 in the transfer function as this DAC is a 14 bit device. On power up the default code loaded to the offset DAC is 5461 (0x1555). With a 3V reference this gives a span of -4 V to +8 V.

REFERENCE SELECTION

The AD5371 has three reference input pins. The voltage applied to the reference pins determines the output voltage span on VOUT0 to VOUT31. VREF0 determines the voltage span for VOUT0 to VOUT7 (Group 0) and VREF1 determines the voltage span for VOUT8 to VOUT15 (Group 1) and VREF2 determines the voltage span for VOUT16 to VOUT31 (Group 2 to Group 3). The reference voltage applied to each VREF pin can be different, if required, allowing the groups to have a different voltage spans. The output voltage range and span can be adjusted further by programming the offset and gain registers for each channel as well as programming the offset DACs. If the offset and gain features are not used (i.e. the m and c registers are left at their default values) the required reference levels can be calculated as follows:

$$VREF = (VOUT_{max} - VOUT_{min})/4$$

If the offset and gain features of the AD5371 are used, then the required output range is slightly different. The chosen output range should take into account the system offset and gain errors that need to be trimmed out. Therefore, the chosen output range should be larger than the actual, required range.

The required reference levels can be calculated as follows:

1. Identify the nominal output range on VOUT.
2. Identify the maximum offset span and the maximum gain required on the full output signal range.
3. Calculate the new maximum output range on VOUT including the expected maximum offset and gain errors.
4. Choose the new required $VOUT_{max}$ and $VOUT_{min}$, keeping the VOUT limits centered on the nominal values. Note that V_{DD} and V_{SS} must provide sufficient headroom.
5. Calculate the value of VREF as follows:
   VREF = (VOUTMAX – VOUTMIN)/4

Reference Selection Example

Nominal Output Range = 12V (-4V to +8V)
Offset Error = ±70mV
Gain Error = ±3%
SIGGND = AGND = 0V

1) *Gain Error* = ±3%
   => *Maximum Positive Gain Error* = +3%
   => *Output Range incl. Gain Error* = 12 + 0.03(12)=12.36V

2) *Offset Error* = ±70mV
=> *Maximum Offset Error Span* = 2(70mV)=0.14V
=> *Output Range including Gain Error and Offset Error* = 12.36V + 0.14V = 12.5V

3) *VREF Calculation*
Actual Output Range = 12.5V, that is -4.25V to +8.25V *(centered);*
VREF = (8.25V + 4.25V)/4 = 3.125V

If the solution yields an inconvenient reference level, the user can adopt one of the following approaches:

1. Use a resistor divider to divide down a convenient, higher reference level to the required level.
2. Select a convenient reference level above VREF and modify the Gain and Offset registers to digitally downsize the reference. In this way the user can use almost any convenient reference level but may reduce the performance by overcompaction of the transfer function.
3. Use a combination of these two approaches

CALIBRATION

The user can perform a system calibration on the AD5371 to reduce gain and offset errors to below 1 LSB. This is achieved by calculating new values for the m and c registers and reprogramming them.

Reducing Offset and Gain Error

Offset Error is reduced as follows:
1. Set the output to the lowest possible value.
2. Measure the actual output voltage and compare it to the required value. This gives the offset error.
3. Calculate the number of LSBs equivalent to the offset error and add or subtract this from the default value of the c register.

Gain Error is reduced as follows:
1. Reduce the offset error.
2. Set the output to the highest possible value
3. Measure the actual output voltage and compare it to the required value. This gives the gain error.
4. Calculate the number of LSBs equivalent to the gain error and subtract it from the default value of the m register. Note that only positive gain error can be reduced.

CALIBRATION EXAMPLE

This example assumes that a -4V to +8V output is required. The DAC output is set to -4V but is measured at -4.03V. This gives an offset of
-30mV.
1) 1 LSB = 12V/16384 = 732.42µV
2) 30mV = 41 LSBs
3) 41 LSBs should be added to the default c register value: (8192 + 41) = 8151
4) 8151 should be programmed to the c register

The gain error can now be removed. The output is set to +8V and a value of +8.02V is measured. This is a gain error of +20mV

1) 20mV = 27 LSBs
2) 27 LSBs should be subtracted from the default m register value: (16383-27) = 16356.
3) 16356 should be programmed to the m register

RESET FUNCTION

When the $\overline{\text{RESET}}$ pin is taken low, the DAC buffers are disconnected and the DAC outputs VOUT0 to VOUT39 are tied to their associated SIGGND signals via a 10 kΩ resistor. On the rising edge of $\overline{\text{RESET}}$ the AD5371 state machine initiates a reset sequence to reset the X, M and C registers to their default values. This sequence typically takes 300µs and the user should not write to the part during this time. When the reset sequence is complete, and provided that $\overline{\text{CLR}}$ is high, the DAC output will be at a potential specified by the default register settings which will be equivalent to SIGGGND. The DAC outputs will remain at SIGGND until the X, M or C registers are updated and $\overline{\text{LDAC}}$ is taken low.

CLEAR FUNCTION

$\overline{\text{CLR}}$ is an active low input which should be high for normal operation. The $\overline{\text{CLR}}$ pin has in internal 500kΩ pull-down resistor. When $\overline{\text{CLR}}$ is low, the input to each of the DAC output buffer stages, VOUT0 to VOUT39, is switched to the externally set potential on the relevant SIGGND pin. While $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is taken high again, the DAC outputs remain cleared until $\overline{\text{LDAC}}$ is taken low. The contents of input registers and DAC registers 0 to 39 are not affected by taking $\overline{\text{CLR}}$ low. To prevent glitches appearing on the outputs $\overline{\text{CLR}}$ should be brought low whenever the output span is adjusted by writing to the offset DAC.

$\overline{\text{BUSY}}$ AND $\overline{\text{LDAC}}$ FUNCTIONS

The value of an X2 (A or B) register is calculated each time the user writes new data to the corresponding X1, C, or M registers. During the calculation of X2, the $\overline{\text{BUSY}}$ output goes low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the X1, M, or C registers (see the Register Update Rates section for more details), but no DAC output updates can take place. The DAC outputs are updated by taking the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored and the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. A user can also hold the $\overline{\text{LDAC}}$ input permanently low. In this case, the DAC outputs update immediately after $\overline{\text{BUSY}}$

goes high. $\overline{\text{BUSY}}$ also goes low, for approximately 500ns, whenever the A/B Select Registers are written to.

The $\overline{\text{BUSY}}$ pin is bidirectional and has a 50 kΩ internal pullup resistor. Where multiple AD5371 devices may be used in one system the $\overline{\text{BUSY}}$ pins can be tied together. This is useful where it is required that no DAC in any device is updated until all other DACs are ready. When each device has finished updating the X2 (A or B) registers it will release the $\overline{\text{BUSY}}$ pin. If another device hasn't finished updating its X2 registers it will hold $\overline{\text{BUSY}}$ low, thus delaying the effect of $\overline{\text{LDAC}}$ going low.

The DAC outputs are updated by taking the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored and the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. A user can also hold the $\overline{\text{LDAC}}$ input permanently low. In this case, the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high.

As described later, the AD5371 has flexible addressing that allows writing of data to a single channel, all channels in a group, the same channel in groups 0 to 4 or groups 1 to 4, or all channels in the device. This means that 1, 5, 8 or 40 X2 register values may need to be calculated and updated. As there is only one multiplier shared between 40 channels, this task must be done sequentially, so the length of the $\overline{\text{BUSY}}$ pulse will vary according to the number of channels being updated.

Table 7. $\overline{\text{BUSY}}$ Pulse Widths

Action	$\overline{\text{BUSY}}$ Pulse Width (µs max)
Loading X1A, X1B, C, or M to 1 channel	1.25
Loading X1A, X1B, C, or M to 5 channels	3.25
Loading X1A, X1B, C, or M to 8 channels	4.75
Loading X1A, X1B, C, or M to 40 channels	20.75

$\overline{\text{BUSY}}$ Pulse Width = ((Number of Channels +1) × 500ns) +250ns

The AD5371 contains an extra feature whereby a DAC register is not updated unless its X2A or X2B register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the X2A or X2B registers, depending on the setting of the A/B Select Registers. However the AD5371 updates the DAC register only if the X2 data has changed, thereby removing unnecessary digital crosstalk.

POWER-DOWN MODE

The AD5371 can be powered down by setting Bit 0 in the control register. This will turn off the DACs thus reducing the current consumption. The DAC outputs will be connected to their respective SIGGND potentials. The power-down mode doesn't change the contents of the registers and the DACs will return to their previous voltage when the power-down bit is cleared.

THERMAL MONITOR FUNCTION

The AD5371 can be programmed to power down the DACs if the temperature on the die exceeds 130°C. Setting Bit 1 in the control register (see Table 12) will enable this function. If the die temperature exceeds 130°C the AD5371 will enter a temperature power-down mode, which is equivalent to setting the power-down bit in the control register. To indicate that the AD5371 has entered temperature shutdown mode Bit 4 of the control register is set. The AD5371 will remain in temperature shutdown mode, even if the die temperature falls, until Bit 1 in the control register is cleared.

TOGGLE MODE

The AD5371 has two X2 registers per channel, X2A and X2B, which can be used to switch the DAC output between two levels with ease. This approach greatly reduces the overhead required by a micro-processor which would otherwise have to write to each channel individually. When the user writes to either the X1A ,X2A, M or C registers the calculation engine will take a certain amount of time to calculate the appropriate X2A or X2B values. If the application only requires that the DAC output switch between two levels, such as a data generator, any method which reduces the amount of calculation time encountered is advantageous. For the data generator example the user need only set the high and low levels for each channel once, by writing to the X1A and X1B registers. The values of X2A and X2B will be calculated and stored in their respective registers. The calculation delay therefore only happens during the setup phase, i.e. when programming the initial values. To toggle a DAC output between the two levels it is only required to write to the relevant A/B Select Register to set the MUX2 register bit. Furthermore, since there are 8 MUX2 control bits per register it is possible to update eight channels with a single write. Table 14 shows the bits that correspond to each DAC output.

SERIAL INTERFACE

The AD5371 contains two high-speed serial interfaces, an SPI-compatible, interface operating at clock frequencies up to 50MHz (20MHz for read operations), and an LVDS interface. To minimize both the power consumption of the device and on-chip digital noise, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{SYNC}}$.

SPI INTERFACE

The serial interface is 2.5 V LVTTL compatible when operating from a 2.7 V to 3.6 V DV_{CC} supply. The SPI interface is selected when the $\overline{\text{SPI}}$/LVDS pin is held low.It is controlled by four pins, as follows.

$\overline{\text{SYNC}}$
Frame synchronization input.

SDI
Serial data input pin.

SCLK
Clocks data in and out of the device.

SDO
Serial data output pin for data readback.

When the SPI mode is used the SYNC, $\overline{\text{SDI}}$ and $\overline{\text{SCLK}}$ pins should be connected to DGND either directly or by using pull-down resistors.

LVDS INTERFACE

The LVDS interface is selected when the $\overline{\text{SPI}}$/LVDS pin is held high. The LVDS interface uses the same input pins as the SPI interface with the same designations. SDO is not used. In addition, three other pins are provided for the complementary signals needed for differential operation, thus:

SYNC/$\overline{\text{SYNC}}$
Differential frame synchronization signal.

SDI/$\overline{\text{SDI}}$
Differential serial data input.

SCLK/$\overline{\text{SCLK}}$
Differential clock input.

SPI WRITE MODE

The AD5371 allows writing of data via the serial interface to every register directly accessible to the serial interface, which is all registers except the X2A and X2B registers and the DAC registers. The X2A and X2B registers are updated when writing to the X1A, X1B, M and C registers, and the DAC registers are updated by $\overline{\text{LDAC}}$.

The serial word (see Table 8) is 24 bits long. 14 of these bits are data bits, six bits are address bits, and two bits are mode bits that determine what is done with the data. Two bits are reserved.

The serial interface works with both a continuous and a burst (gated) serial clock. Serial data applied to SDI is clocked into the AD5371 by clock pulses applied to SCLK. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. At least 24 falling clock edges must be applied to SCLK to clock in 24 bits of data, before $\overline{\text{SYNC}}$ is taken high again. If $\overline{\text{SYNC}}$ is taken high before the 24th falling clock edge, the write operation will be aborted.

If a continuous clock is used, $\overline{\text{SYNC}}$ must be taken high before the 25th falling clock edge. This inhibits the clock within the AD5371. If more than 24 falling clock edges are applied before $\overline{\text{SYNC}}$ is taken high again, the input data will be corrupted. If an externally gated clock of exactly 24 pulses is used, $\overline{\text{SYNC}}$ may be taken high any time after the 24th falling clock edge.

The input register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. In order for another serial transfer to take place, $\overline{\text{SYNC}}$ must be taken low again.

Table 8. Serial Word Bit Assignation

I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1*	I0*
M1	M0	A5	A4	A3	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0

*Bits I1 and I0 are reserved for future use. Set to 0 when writing. Read back as 0.

SPI READBACK MODE

The AD5371 allows data readback via the serial interface from every register directly accessible to the serial interface, which is all registers except the X2A, X2B and DAC registers. In order to read back a register, it is first necessary to tell the AD5371 which register is to be read. This is achieved by writing to the device a word whose first two bits are the special function code 00. The remaining bits then determine if the operation is a readback, and the register which is to be read back, or if it is a write to of the special function registers such as the control register.

After the special function write has been performed, if it is a readback command then data from the selected register will be clocked out of the SDO pin during the next SPI operation. The SDO pin is normally three-state but becomes driven as soon as a read command has been issued. The pin will remain driven until the registers data has been clocked out. Figure 5 for the read timing diagram. Note that due to the timing requirements of t_5 (25ns) the maximum speed of the SPI interface during a read operation should not exceed 20MHz.

LVDS OPERATION

The LVDS interface operates as follows (note that, since the LVDS signals are differential, when a signal goes high its complementary signal goes low, and vice versa).

The $\overline{\text{SYNC}}$ signal frames the data. SCLK is initially high. After $\overline{\text{SYNC}}$ goes low and the $\overline{\text{SYNC}}$ to SCLK setup time has elapsed, SCLK can start to clock in the data. Data is clocked into the AD5371 on the high to low transition of SCLK and must be stable at this time (observe setup and hold time specs). $\overline{\text{SYNC}}$ may then be taken high after the SCLK to $\overline{\text{SYNC}}$ hold time to latch the data.

The same comments about burst and continuous clocks apply to the LVDS interface as to the SPI interface. Readback is not available when using the LVDS interface.

REGISTER UPDATE RATES

As mentioned previously the value of the X2 (A or B) register is calculated each time the user writes new data to the corresponding X1, C or M registers. The calculation is performed by a three stage process. The first two stages take 500ns each and the third stage takes 250ns. When the write to one of the X1, C or M registers is complete the calculation process begins. If the write operation involves the update of a single DAC channel the user is free to write to another register provided that the write operation doesn't finish until the first stage calculation is complete, i.e. 500ns after the completion of the first write operation. If a group of channels is being updated by a single write operation the first stage calculation will be repeated for each channel, taking 500ns per channel. In this case the user should not complete the next write operation until this time has elapsed.

CHANNEL ADDRESSING AND SPECIAL MODES

If the mode bits are not 00, then the data word D13 to D0 is written to the device. Address bits A5 to A0 determine which channel or channels is/are written to, while the mode bits determine to which register (X1A, X1B, C or M) the data is written, as shown in Table 8. If data is to be written to the X1A or X1B register, the setting of the $\overline{\text{A}}$/B bit in the Control Register determines which (0 → X1A, 1 → X1B).

Table 9. Mode Bits

M1	M0	Action
1	1	Write DAC input data (X1A or X1B) register, depending on Control Register $\overline{\text{A}}$/B bit.
1	0	Write DAC offset (C) register
0	1	Write DAC gain (M) register
0	0	Special function, used in combination with other bits of word

The AD5371 has very flexible addressing that allows writing of data to a single channel, all channels in a group, the same channel in groups 0 to 4 or groups 1 to 4, or all channels in the device Table 10 shows all these address modes.

Table 10. Group and Channel Addressing

This table shows which group(s) and which channel(s) is/are addressed for every combination of address bits A5 to A0.

		ADDRESS BITS A5 TO A3							
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
ADDRESS BITS A2 TO A0	**000**	All groups, all channels	Group 0, channel 0	Group 1, channel 0	Group 2, channel 0	Group 3, channel 0	Group 4, channel 0	Groups 0,1,2,3,4 channel 0	Groups 1,2,3,4 channel 0
	001	Group 0, all channels	Group 0, channel 1	Group 1, channel 1	Group 2, channel 1	Group 3, channel 1	Group 4, channel 1	Groups 0,1,2,3,4 channel 1	Groups 1,2,3,4 channel 1
	010	Group 1, all channels	Group 0, channel 2	Group 1, channel 2	Group 2, channel 2	Group 3, channel 2	Group 4, channel 2	Groups 0,1,2,3,4 channel 2	Groups 1,2,3,4 channel 2
	011	Group 2, all channels	Group 0, channel 3	Group 1, channel 3	Group 2, channel 3	Group 3, channel 3	Group 4, channel 3	Groups 0,1,2,3,4 channel 3	Groups 1,2,3,4 channel 3
	100	Group 3, all channels	Group 0, channel 4	Group 1, channel 4	Group 2, channel 4	Group 3, channel 4	Group 4, channel 4	Groups 0,1,2,3,4 channel 4	Groups 1,2,3,4 channel 4
	101	Group 4, all channels	Group 0, channel 5	Group 1, channel 5	Group 2, channel 5	Group 3, channel 5	Group 4, channel 5	Groups 0,1,2,3,4 channel 5	Groups 1,2,3,4 channel 5
	110	Reserved	Group 0, channel 6	Group 1, channel 6	Group 2, channel 6	Group 3, channel 6	Group 4, channel 6	Groups 0,1,2,3,4 channel 6	Groups 1,2,3,4 channel 6
	111	Reserved	Group 0, channel 7	Group 1, channel 7	Group 2, channel 7	Group 3, channel 7	Group 4, channel 7	Groups 0,1,2,3,4 channel 7	Groups 1,2,3,4 channel 7

SPECIAL FUNCTION MODE

If the mode bits are 00, then the special function mode is selected, as shown in Table 11. Bits I21 to I16 of the serial data word select the special function, while the remaining bits are data required for execution of the special function, for example the channel address for data readback.

The codes for the special functions are shown in Table 12. Table 13 shows the addresses for data readback.

Table 11. Special Function Mode

I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
0	**0**	S5	S4	S3	S2	S1	S0	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

Table 12. Special Function Codes

SPECIAL FUNCTION CODE						DATA	ACTION
S5	S4	S3	S2	S1	S0	F15-F0	
0	0	0	0	0	0	0000 0000 0000 0000	NOP
0	0	0	0	0	1	XXXX XXXX XXXX X[F2:F0]	Write control register F2 = 1 → Select B reg for input; F2 = 0 → Select A reg for input F1 = 1 → En temp shutdown; F1 = 0 → Disable temp shutdown F0 = 1 → Soft power down; F0 = 0 → soft power up
0	0	0	0	1	0	XX[F13:F0]	Write data in F13:F0 to OFS0 register
0	0	0	0	1	1	XX[F13:F0]	Write data in F13:F0 to OFS1 register
0	0	0	1	0	0	XX[F13:F0]	Write data in F13:F0 to OFS2 register
0	0	0	1	0	1	See Table 13	Select register for readback
0	0	0	1	1	0	XXXX XXXX[F7:F0]	Write data in F7:F0 to A/B Select Register 0
0	0	0	1	1	1	XXXX XXXX[F7:F0]	Write data in F7:F0 to A/B Select Register 1
0	0	1	0	0	0	XXXX XXXX[F7:F0]	Write data in F7:F0 to A/B Select Register 2
0	0	1	0	0	1	XXXX XXXX[F7:F0]	Write data in F7:F0 to A/B Select Register 3
0	0	1	0	1	0	XXXX XXXX[F7:F0]	Write data in F7:F0 to A/B Select Register 4
0	0	1	0	1	1	XXXX XXXX[F7:F0]	Block write A/B Select Registers F7:F0 = 0, write all 0's (all channels use X2A register) F7:F0 = 1, wrote all 1's (all channels use X2B register)

Table 13. Address Codes for Data Readback

F15	F14	F13	F12	F11	F10	F9	F8	F7	REGISTER READ
0	0	0	Bits F12 to F7 select channel to be read back, from Channel 0 = 001000 to Channel 39 = 101111						A Register
0	0	1							B Register
0	1	0							C Register
0	1	1							M Register
1	0	0	0	0	0	0	0	1	Control Register
1	0	0	0	0	0	0	1	0	OFS0 Data Register
1	0	0	0	0	0	0	1	1	OFS1 Data Register
1	0	0	0	0	0	1	0	0	OFS2 Data Register
1	0	0	0	0	0	1	1	0	A/B Select Register 0
1	0	0	0	0	0	1	1	1	A/B Select Register 1
1	0	0	0	0	1	0	0	0	A/B Select Register 2
1	0	0	0	0	1	0	0	1	A/B Select Register 3
1	0	0	0	0	1	0	1	0	A/B Select Register 4

Table 14. DACs Select by A/B Select Registers

A/B Select Register	Bits							
	F7	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**
0	VOUT7	VOUT6	VOUT5	VOUT4	VOUT3	VOUT2	VOUT1	VOUT0
1	VOUT15	VOUT14	VOUT13	VOUT12	VOUT11	VOUT10	VOUT9	VOUT8
2	VOUT23	VOUT22	VOUT21	VOUT20	VOUT19	VOUT18	VOUT17	VOUT16
3	VOUT31	VOUT30	VOUT29	VOUT28	VOUT27	VOUT26	VOUT25	VOUT24
4	VOUT39	VOUT38	VOUT37	VOUT36	VOUT35	VOUT34	VOUT33	VOUT32

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5371 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5371 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (V_{SS}, V_{DD}, V_{CC}), it is recommended to tie these pins together and to decouple each supply once.

The AD5371 should have ample supply decoupling of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types that provide a low impedance path to ground at high frequent cies, to handle transient currents due to internal logic switching.

Digital lines running under the device should be avoided, because these couple noise onto the device. The analog ground plane should be allowed to run under the AD5371 to avoid noise coupling. The power supply lines of the AD5371 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. It is essential to minimize noise on all V_{REF} lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of this package during the assembly process.

POWER SUPPLY SEQUENCING

When the supplies are connected to the AD5371 it is important that the AGND and DGND pins are connected to the relevant ground plane before the positive or negative supplies are applied. In most applications this is not an issue as the ground pins for the power supplies will be connected to the ground pins of the AD5371 via ground planes. Where the AD5371 is to be used in a hot-swap card care should be taken to ensure that the ground pins are connected to the supply grounds before the positive or negative supplies are connected. This is required to prevent currents flowing in directions other than towards an analog or digital ground.

INTERFACING EXAMPLES

The SPI interface of the AD5371 is designed to allow the parts to be easily connected to industry standard DSPs and micro-controllers. Figure 12 shows how the AD5371 could be connected to the Analog Devices Blackfin® DSP. The Blackfin has an integrated SPI port which can be connected directly to the SPI pins of the AD5371 and programmable I/O pins which can be used to set or read the state of the digital input or output pins associated with the interface.

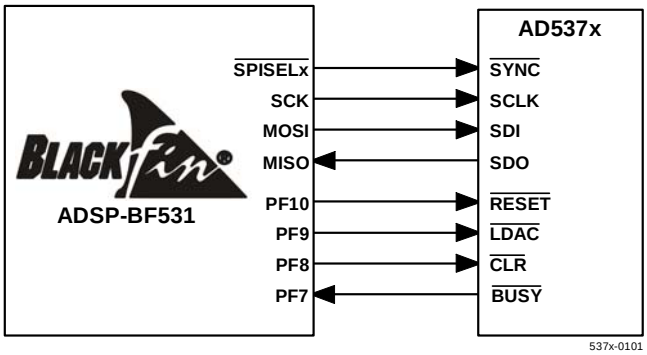


Figure 12. Interfacing to a Blackfin DSP

The Analog Devices ADSP-21065L is a floating point DSP with two serial ports (SPORTS). Figure 13 shows how one SPORT can be used to control the AD5371. In this example the Transmit Frame Synchronization (TFS) pin is connected to the Receive Frame Synchronization (RFS) pin. Similarly the transmit and receive clocks (TCLK and RCLK) are also connected together. The user can write to the AD5371 by writing to the transmit register. A read operation can be accomplished by first writing to the AD5371 to tell the part that a read operation is required. A second write operation with a NOP instruction will cause the data to be read from the AD5371. The DSPs receive interrupt can be used to indicate when the read operation is complete.

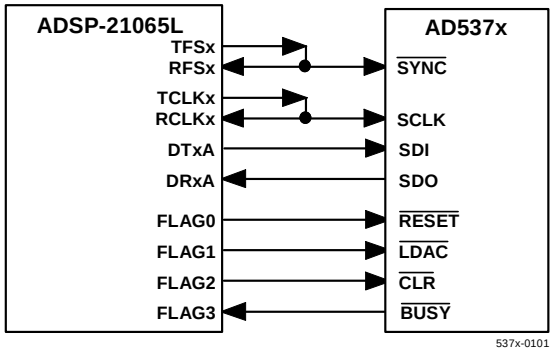


Figure 13. Interfacing to an ADSP-21065L DSP

OUTLINE DIMENSIONS

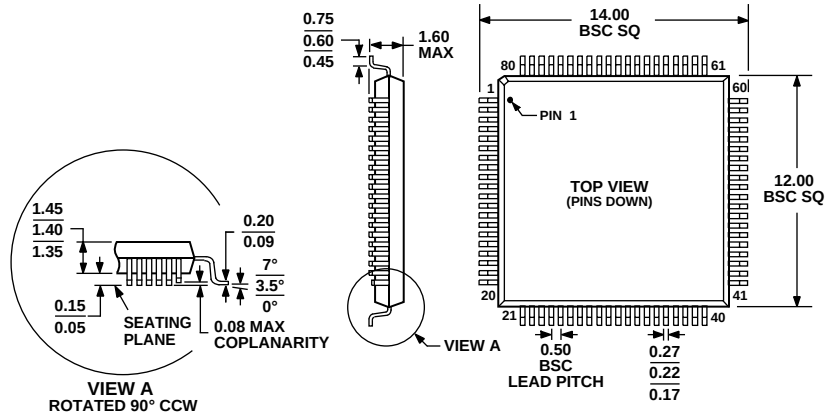


Figure 14. 80 Lead Quad Flat Package
(ST-80-1)
Dimensions shown in millimeters

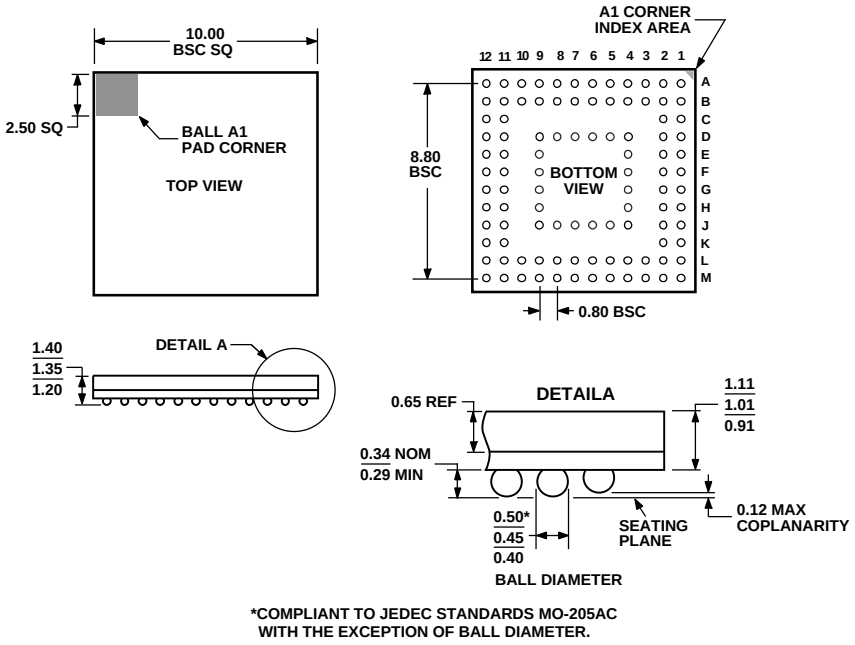


Figure 15. 100-Lead Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-100-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5371BSTZ	-40°C to +85°C	80-Lead Quad Flat Pack (LQFP)	ST-80
AD5371BBCZ	-40°C to +85°C	100 Ball Chip Scale Package (CSPBGA)	BC-100-2

NOTES

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