64-Position Up/Down Control Digital Potentiometer

AD5227

FEATURES

64-position digital potentiometer
10 kΩ, 50 kΩ, 100 kΩ end-to-end terminal resistance
Simple up/down digital or manual configurable control
Midscale preset
Low potentiometer mode tempco = 10 ppm/°C
Low rheostat mode tempco = 35 ppm/°C
Ultralow power, I_{DD} = 0.4 µA typ and 3 µA max
Fast adjustment time, ts = 1 µs
Chip select enable multiple device operation
Low operating voltage, 2.7 V to 5.5 V
Automotive temperature range, −40°C to +105°C
Compact thin SOT-23-8 (2.9 mm × 3 mm) Pb-free package

APPLICATIONS

Mechanical potentiometer and trimmer replacements
LCD backlight, contrast, and brightness controls
Portable electronics level adjustment
Programmable power supply
Digital trimmer replacements
Automatic closed-loop control

FUNCTIONAL BLOCK DIAGRAM

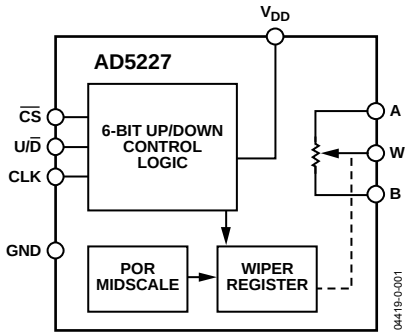

Figure 1.

GENERAL DESCRIPTION

The AD5227 is Analog Devices' latest 64-step up/down control digital potentiometer[1]. This device performs the same electronic adjustment function as a 5 V potentiometer or variable resistor. Its simple 3-wire up/down interface allows manual switching or high speed digital control. The AD5227 presets to midscale at power-up. When $\overline{CS}$ is enabled, the devices changes step at every clock pulse. The direction is determined by the state of the U/$\overline{D}$ pin (see Table 1). The interface is simple to activate by any host controller, discrete logic, or manually with a rotary encoder or pushbuttons. The AD5227's 64-step resolution, small footprint, and simple interface enable it to replace mechanical potentiometers and trimmers with typically 6× improved resolution, solid-state reliability, and design layout flexibility, resulting in a considerable cost savings in end users' systems.

The AD5227 is available in a compact thin SOT-23-8 (TSOT-8) Pb-free package. The part is guaranteed to operate over the automotive temperature range of −40°C to +105°C.

Users who consider EEMEM potentiometers should refer to some recommendations in the Applications section.

Table 1. Truth Table

$\overline{CS}$	CLK	U/$\overline{D}$	Operation[1]
0	↓	0	R_{WB} Decrement
0	↓	1	R_{WB} Increment
1	X	X	No Operation

[1] R_{WA} increments if R_{WB} decrements and vice versa.

[1] The terms *digital potentiometer* and *RDAC* are used interchangeably.

Rev. B

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REVISION HISTORY

5/09—Rev. A to Rev. B

Changes to Table 2 3

4/09—Rev. 0 to Rev. A

Changes to Table 2 3
Changes to Ordering Guide 15

3/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

10 kΩ, 50 kΩ, 100 kΩ versions: V_{DD} = 3 V ± 10% or 5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, A = no connect	−0.5	±0.15	+0.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, A = no connect	−1	±0.3	+1	LSB
Nominal Resistor Tolerance[3]	$\Delta R_{AB}/R_{AB}$		−20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 2.7 V		100	250	Ω
		V_{DD} = 2.8 V to 5.5 V		50	200	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Resolution	N				6	Bits
Integral Nonlinearity[3]	INL		−1	±0.1	+1	LSB
Differential Nonlinearity[3, 4]	DNL		−0.5	±0.1	+0.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Midscale		5		ppm/°C
Full-Scale Error	V_{WFSE}	≥+31 steps from midscale	−1.2	−0.5	0	LSB
		−40°C < T_A < +60°C, V_{DD} = 2.8 V to 5.5 V	−1	−0.5	0	LSB
Zero-Scale Error	V_{WZSE}	≤−32 steps from midscale	0	0.5	1.2	LSB
		−40°C < T_A < +60°C, V_{DD} = 2.8 V to 5.5 V	0	0.5	1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$	With respect to GND	0		V_{DD}	V
Capacitance A, B[6]	$C_{A, B}$	f = 1 MHz, measured to GND		140		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND		150		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS ($\overline{CS}$, CLK, U/$\overline{D}$)						
Input Logic High	V_{IH}		2.4		5.5	V
Input Logic Low	V_{IL}		0		0.8	V
Input Current	I_I	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_I			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		0.4	3	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			17	µW
Power Supply Sensitivity	PSSR	V_{DD} = 5 V ± 10%		0.01	0.05	%/%
DYNAMIC CHARACTERISTICS[6, 8, 9]						
Bandwidth −3 dB	BW_10 k	R_{AB} = 10 kΩ, midscale		460		kHz
	BW_50 k	R_{AB} = 50 kΩ, midscale		100		kHz
	BW_100 k	R_{AB} = 100 kΩ, midscale		50		kHz
Total Harmonic Distortion	THD	V_A = 1 V rms, R_{AB} = 10 kΩ, V_B = 0 V dc, f = 1 kHz		0.05		%
Adjustment Settling Time	t_S	V_A = 5 V ± 1 LSB error band, V_B = 0, measured at V_W		1		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		14		nV/√Hz

Footnotes on the next page.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS (applies to all parts[6, 10])						
Clock Frequency	f_{CLK}				50	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	10			ns
$\overline{CS}$ to CLK Setup Time	t_{CSS}		10			ns
$\overline{CS}$ Rise to CLK Hold Time	t_{CSH}		10			ns
U/$\overline{D}$ to Clock Fall Setup Time	t_{UDS}		10			ns

[1] Typicals represent average readings at 25°C, V_{DD} = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] NL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V.
[4] DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[9] All dynamic characteristics use V_{DD} = V.
[10] All input control voltages are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using V_{DD} = 5 V.

INTERFACE TIMING DIAGRAMS

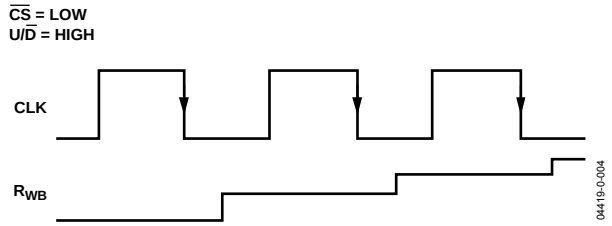

Figure 2. Increment R_{WB}

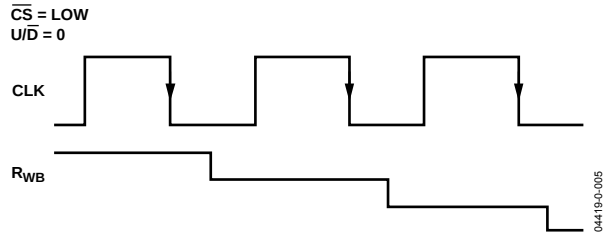

Figure 3. Decrement R_{WB}

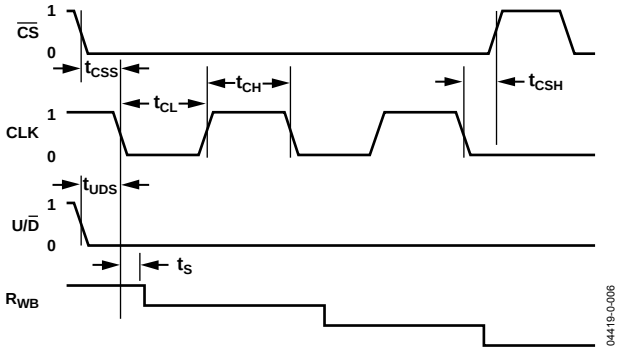

Figure 4. Detailed Timing Diagram (Only R_{WB} Decrement Shown)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V, +7 V
V_A, V_B, V_W to GND	0 V, V_{DD}
Digital Input Voltage to GND ($\overline{CS}$, CLK, U/$\overline{D}$)	0 V, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous ($R_{WB} \leq 5$ kΩ, A open)[1]	±1 mA
I_{WA} Continuous ($R_{WA} \leq 5$ kΩ, B open)[1]	±1 mA
I_{AB} Continuous (R_{AB} = 10 kΩ/50 kΩ/100 kΩ)[1]	±500 µA/ ±100 µA/±50 µA
Operating Temperature Range	−40°C to +105°C
Maximum Junction Temperature ($T_J$max)	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 s – 30 s)	245°C
Thermal Resistance[2] θ_{JA}	230°C/W

[1] Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package. V_{DD} = 5 V.

[2] Package power dissipation = ($T_J$max – T_A) / θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

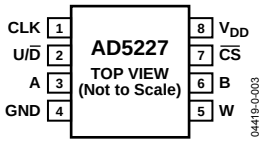

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Clock Input. Each clock pulse executes the step-up or step-down of the resistance. The direction is determined by the state of the U/$\overline{D}$ pin. CLK is a negative-edge trigger. Logic high signal can be higher than V_{DD}, but lower than 5.5 V.
2	U/$\overline{D}$	Up/Down Selections. Logic 1 selects up and Logic 0 selects down. U can be higher than V_{DD}, but lower than 5.5 V.
3	A	Resistor Terminal A. GND ≤ V_A ≤ V_{DD}.
4	GND	Common Ground.
5	W	Wiper Terminal W. GND ≤ V_W ≤ V_{DD}.
6	B	Resistor Terminal B. GND ≤ V_B ≤ V_{DD}.
7	$\overline{CS}$	Chip Select. Active Low. Logic high signal can be higher than V_{DD}, but lower than 5.5 V.
8	V_{DD}	Positive Power Supply, 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

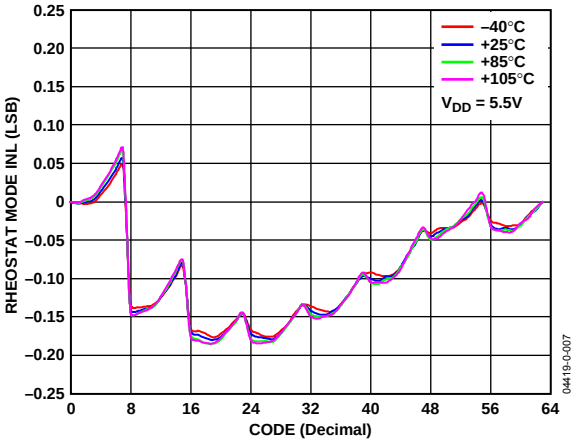

Figure 6. R-INL vs. Code vs. Temperature, V_{DD} = 5 V

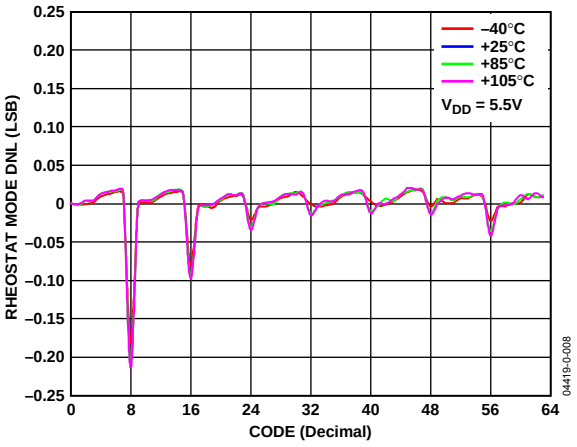

Figure 7. R-DNL vs. Code vs. Temperature, V_{DD} = 5 V

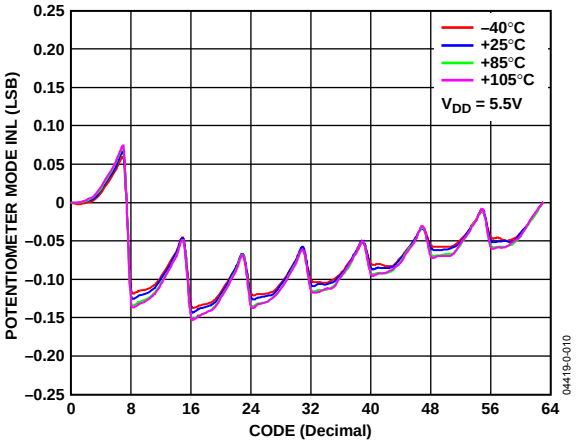

Figure 8. INL vs. Code, V_{DD} = 5 V

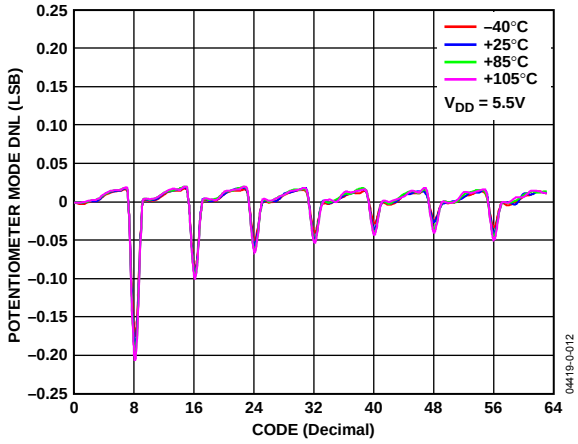

Figure 9. DNL vs. Code vs. Temperature, V_{DD} = 5 V

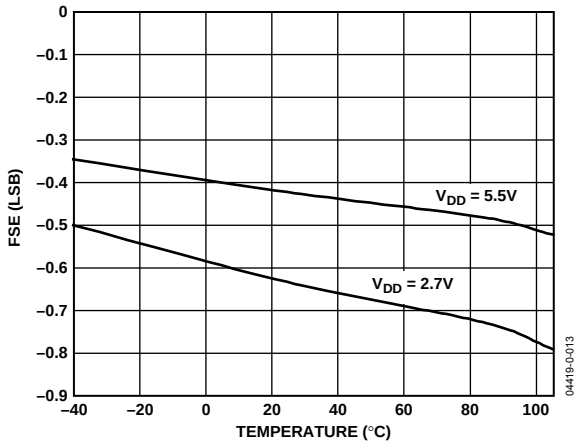

Figure 10. Full-Scale Error vs. Temperature

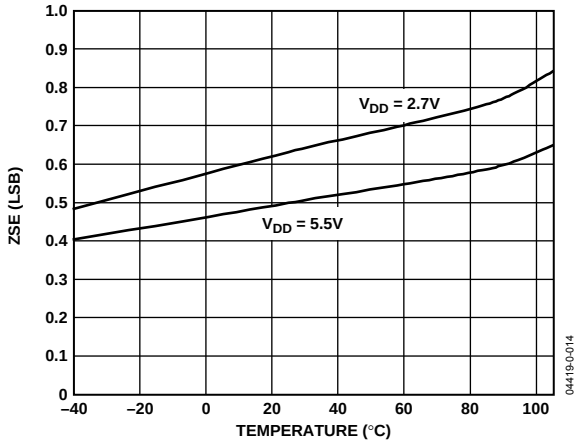

Figure 11. Zero-Scale Error vs. Temperature

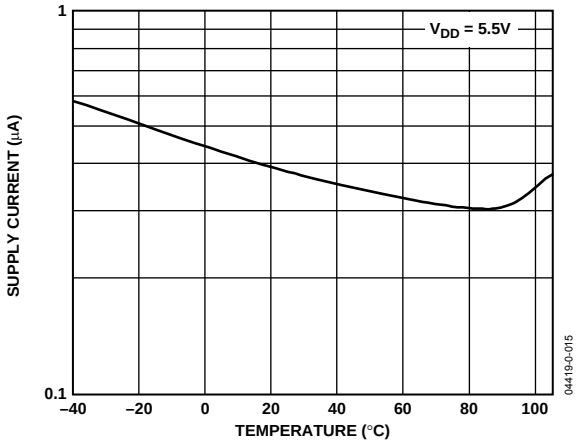

Figure 12. Supply Current vs. Temperature

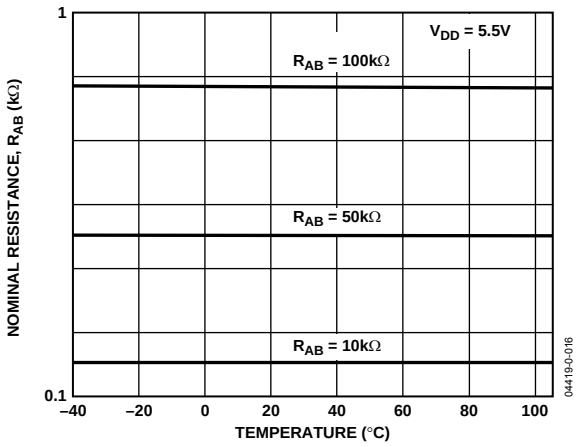

Figure 13. Nominal Resistance vs. Temperature

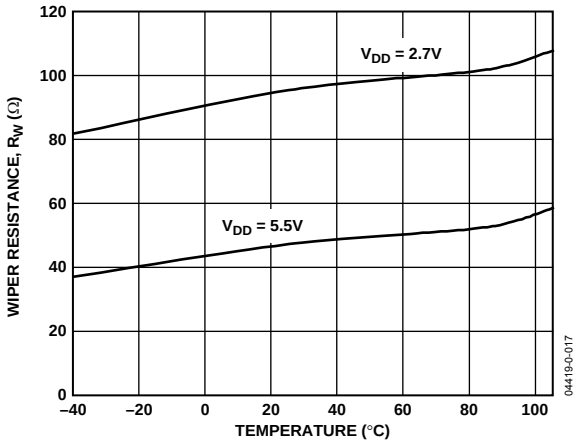

Figure 14. Wiper Resistance vs. Temperature

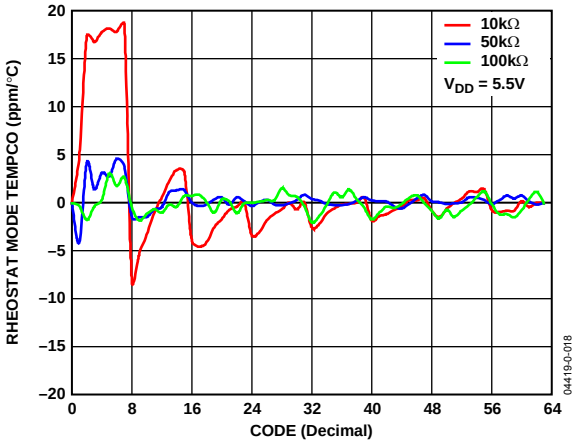

Figure 15. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

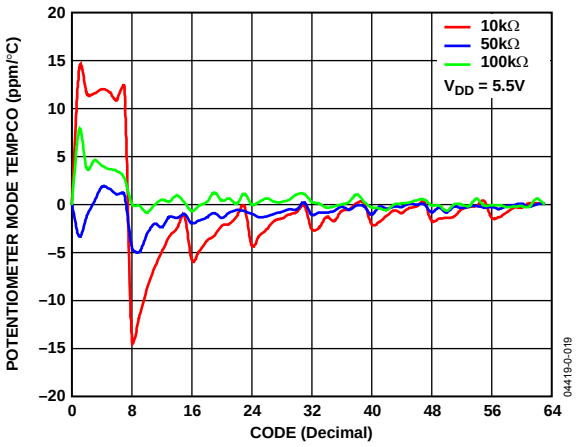

Figure 16. Potentiometer Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

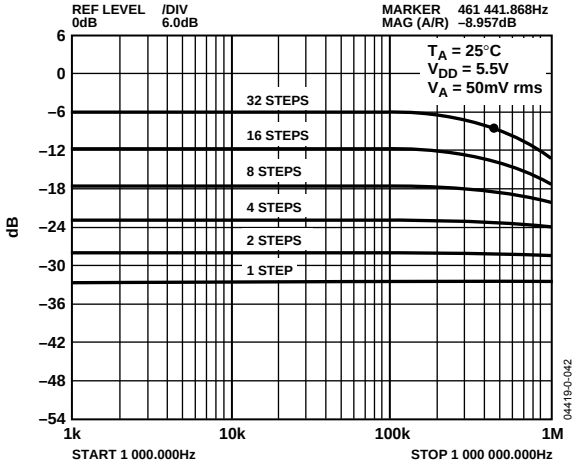

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

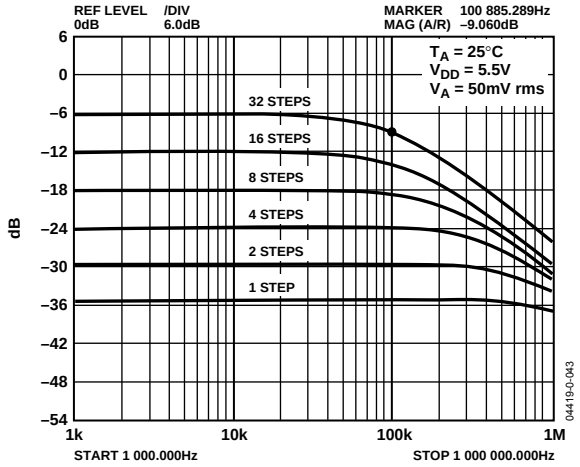

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

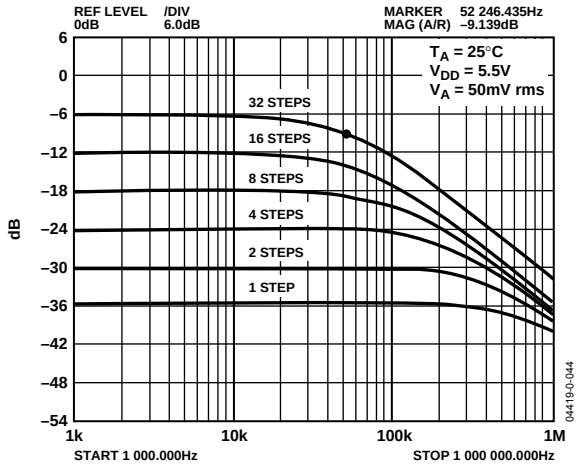

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

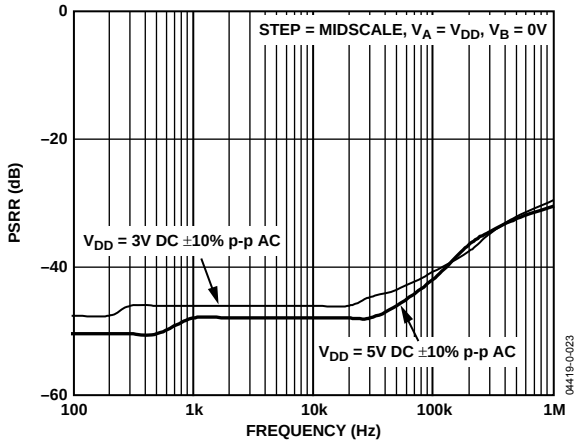

Figure 20. PSRR

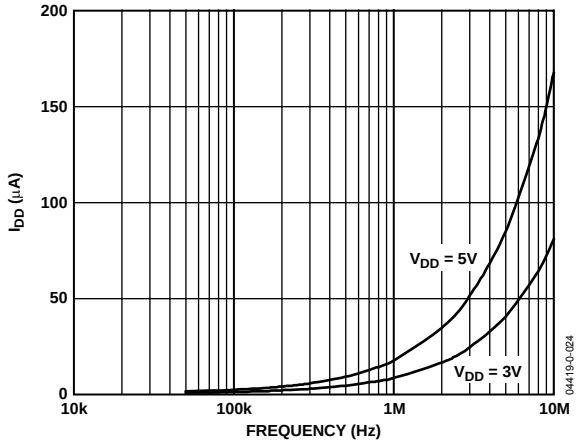

Figure 21. I_{DD} vs. CLK Frequency

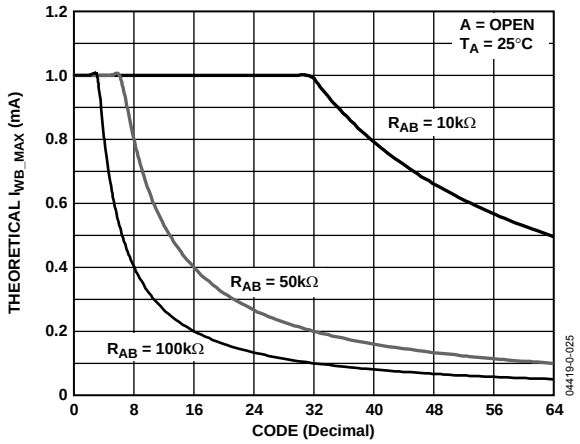

Figure 22. Maximum I_{WB} vs. Code

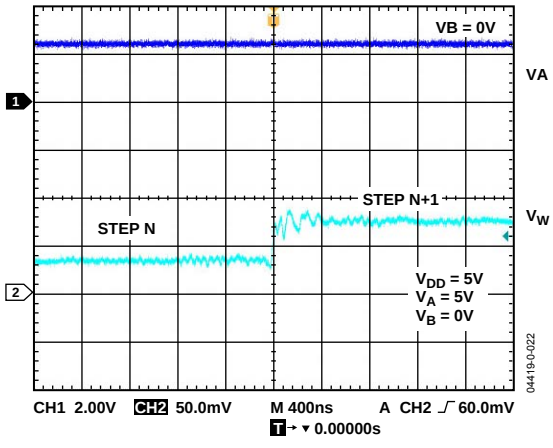

Figure 23. Step Change Settling Time

THEORY OF OPERATION

The AD5227 is a 64-position 3-terminal digitally controlled potentiometer device. It presets to a midscale at system power-on. When $\overline{CS}$ is enabled, changing the resistance settings is achieved by clocking the CLK pin. It is negative-edge triggered, and the direction of stepping is determined by the state of the U/$\overline{D}$ input. When the wiper reaches the maximum or the minimum setting, additional CLK pulses do not change the wiper setting.

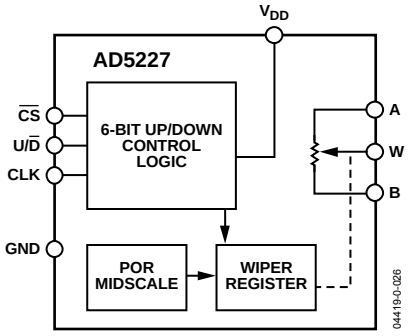

Figure 24. Functional Block Diagram

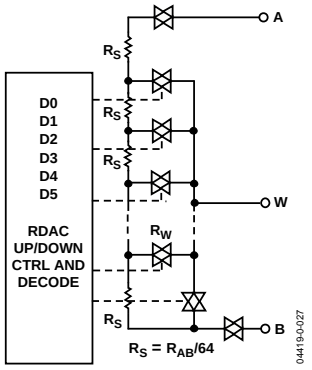

Figure 25. AD5227 Equivalent RDAC Circuit

PROGRAMMING THE DIGITAL POTENTIOMETERS

Rheostat Operation

If only the W-to-B or W-to-A terminals are used as variable resistors, the unused terminal can be opened or shorted with W. This operation is called *rheostat mode* and is shown in Figure 26.

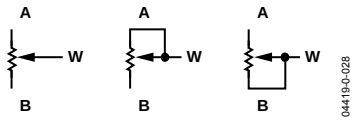

Figure 26. Rheostat Mode Configuration

The end-to-end resistance, R_{AB}, has 64 contact points accessed by the wiper terminal, plus the B terminal contact, assuming that R_{WB} is used (see Figure 25). Clocking the CLK input steps, R_{WB} by one step. The direction is determined by the state of U/$\overline{D}$ pin. The change of R_{WB} can be determined by the number of clock pulses, provided that the AD5227 has not reached its maximum or minimum scale. ΔR_{WB} can, therefore, be approximated as

$$\Delta R_{WB} = \pm\left(CP \times \frac{R_{AB}}{64} + R_W \right) \quad (1)$$

where:

CP is the number of clock pulses.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on-resistance of the internal switch.

Since in the lowest end of the resistor string a finite wiper resistance is present, care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switches can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened or shorted to W. Similarly, ΔR_{WA} can be approximated as

$$\Delta R_{WA} = \pm\left((64 - CP)\frac{R_{AB}}{64} + R_W \right) \quad (2)$$

Equations 1 and 2 do not apply when CP = 0.

The typical distribution of the resistance tolerance from device to device is process lot dependent. It is possible to have ±20% tolerance.

Potentiometer Mode Operation

If all three terminals are used, the operation is called *potentiometer mode*. The most common configuration is the voltage divider operation as shown in Figure 27.

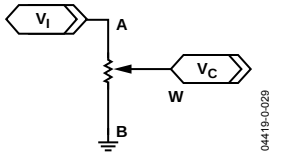

Figure 27. Potentiometer Mode Configuration

The change of V_{WB} is known provided that the AD5227 has not reached the maximum or minimum scale. If one ignores the effect of the wiper resistance, the transfer functions can be simplified as

$$\Delta V_{WB} = +\frac{CP}{64} V_A \Big| \ U/\overline{D} = 1 \quad (3)$$

$$\Delta V_{WB} = -\frac{CP}{64} V_A \Big| \ U/\overline{D} = 0 \quad (4)$$

Unlike rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratiometric function of CP/64 with a relatively small error contributed by the R_W term. The tolerance effect is, therefore, almost canceled. Although the thin film step resistor, R_S, and CMOS switches resistance, R_W, have very different temperature coefficients, the ratiometric adjustment also reduces the overall temperature coefficient to 5 ppm/°C except at low value codes where R_W dominates.

Potentiometer mode operation includes an op amp gain configuration among others. The A, W, and B terminals can be input or output terminals and have no polarity constraint provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed V_{DD}-to-GND.

DIGITAL INTERFACE

The AD5227 contains a 3-wire serial input interface. The three inputs are clock (CLK), chip select ($\overline{CS}$), and up/down control ($U/\overline{D}$). These inputs can be controlled digitally for optimum speed and flexibility

When $\overline{CS}$ is pulled low, a clock pulse increments or decrements the up/down counter. The direction is determined by the state of the $U/\overline{D}$ pin. When a specific state of the $U/\overline{D}$ remains, the device continues to change in the same direction under consecutive clocks until it comes to the end of the resistance setting. All digital inputs, $\overline{CS}$, CLK, and $U/\overline{D}$ pins, are protected with a series input resistor and a parallel Zener ESD structure as shown in Figure 28.

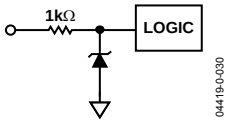

Figure 28. Equivalent ESD Protection Digital Pins

TERMINAL VOLTAGE OPERATION RANGE

The AD5227 is designed with internal ESD protection diodes (Figure 29), but the diodes also set the boundary of the terminal operating voltages. Voltage present on Terminal A, B, or W that exceeds V_{DD} by more than 0.5 V is clamped by the diode and, therefore, elevates V_{DD}. There is no polarity constraint between V_{AB}, V_{WA}, and V_{WB}, but they cannot be higher than V_{DD}-to-GND.

POWER-UP AND POWER-DOWN SEQUENCES

Because of the ESD protection diodes, it is important to power on V_{DD} before applying any voltage to Terminals A, B, and W. Otherwise, the diodes are forward-biased such that V_{DD} can be powered unintentionally and can affect the rest of the system circuit. Similarly, V_{DD} should be powered down last. The ideal power-on sequence is in the following order: GND, V_{DD}, $V_{A/B/W}$, and digital inputs.

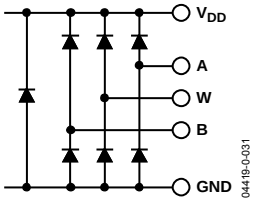

Figure 29. Maximum Terminal Voltages Set by V_{DD} and GND

LAYOUT AND POWER SUPPLY BIASING

It is a good practice to use compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Low ESR (equivalent series resistance) 1 µF to 10 µF tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and filter low frequency ripple.

Figure 30 illustrates the basic supply bypassing configuration for the AD5227. The ground pin of the AD5227 is a digital ground reference that should be joined to the common ground at a single point to minimize the digital ground bounce.

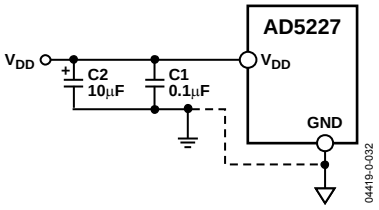

Figure 30. Power Supply Bypassing

APPLICATIONS

MANUAL CONTROL WITH TOGGLE AND PUSHBUTTON SWITCHES

The AD5227's simple interface allows it to be used with mechanical switches for simple manual operation. The states of the $\overline{CS}$ and U/$\overline{D}$ can be selected by toggle switches and the CLK input can be controlled by a pushbutton switch. Because of the numerous bounces due to contact closure, the pushbutton switch should be debounced by flip-flops or by the ADM812 as shown in Figure 31.

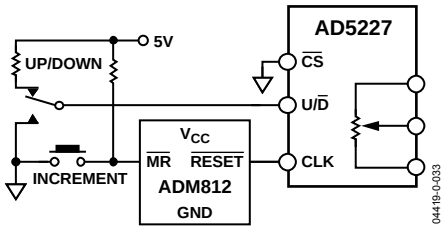

Figure 31. Manual Push Button Up/Down Control

MANUAL CONTROL WITH ROTARY ENCODER

Figure 32 shows another way of using AD5227 to emulate mechanical potentiometer in a rotary knob operation. The rotary encoder U1 has a C ground terminal and two out-of-phase signals, A and B. When U1 is turned clockwise, a pulse generated from the B terminal leads a pulse generated from the A terminal and vice versa. Signals A and B of U1 pass through a quadrature decoder U2 that translates the phase difference between A and B of U1 into compatible inputs for U3 AD5227. Therefore, when B leads A (clockwise), U2 provides the AD5227 with a logic high U/$\overline{D}$ signal, and vice versa. U2 also filters noise, jitter, and other transients as well as debouncing the contact bounces generated by U1.

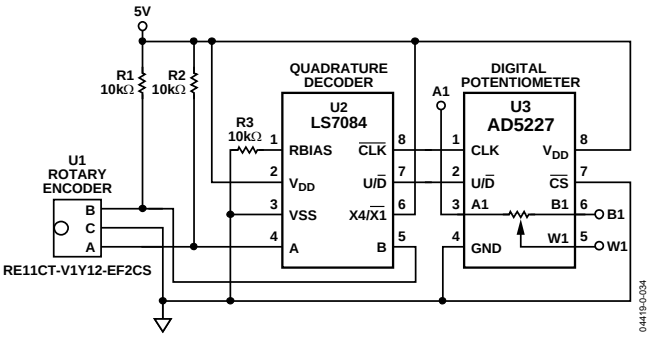

Figure 32. Manual Rotary Control

ADJUSTABLE LED DRIVER

The AD5227 can be used in many electronics-level adjustments such as LED drivers for LCD panel backlight control. Figure 33 shows an adjustable LED driver. The AD5227 sets the voltage across the white LED D1 for the brightness control. Since U2 handles up to 250 mA, a typical white LED with V_F of 3.5 V requires a resistor, R1, to limit the U2 current. This circuit is simple but not power-efficient, therefore the U2 shutdown pin can be toggled with a PWM signal to conserve power.

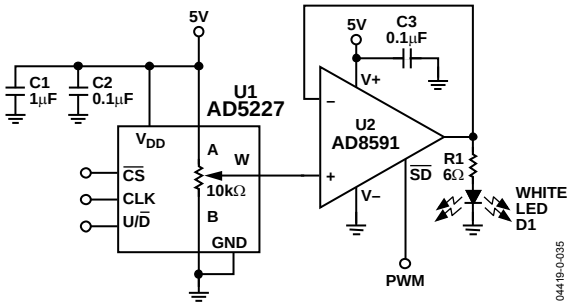

Figure 33. Low Cost Adjustable LED Driver

ADJUSTABLE CURRENT SOURCE FOR LED DRIVER

Since LED brightness is a function of current rather than forward voltage, an adjustable current source is preferred over a voltage source as shown in Figure 34.

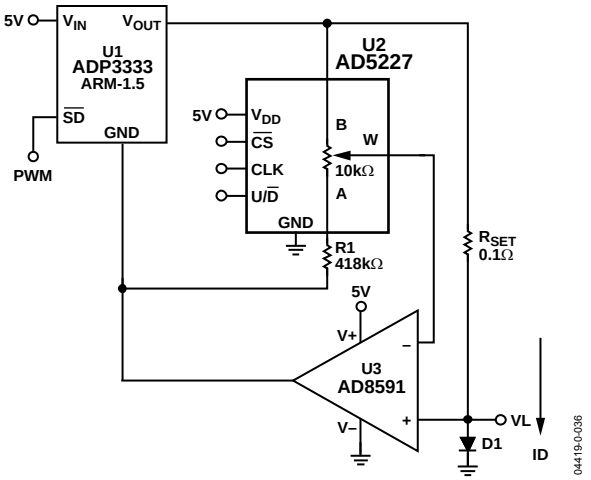

Figure 34. Adjustable Current Source for LED Driver

The load current can be found as the V_{WB} of the AD5227 divided by R_{SET}.

$$I_D = \frac{V_{WB}}{R_{SET}} \quad (5)$$

The U1 ADP3333ARM-1.5 is a 1.5 V LDO that is lifted above or lowered below 0 V. When V_{WB} of the AD5227 is at minimum, there is no current through D1, so the GND pin of U1 would be at −1.5 V if U3 were biased with the dual supplies. As a result, some of the U2 low resistance steps have no effect on the output until the U1 GND pin is lifted above 0 V. When V_{WB} of the AD5227 is at its maximum, V_{OUT} becomes $V_L + V_{AB}$, so the U1 supply voltage must be biased with adequate headroom. Similarly, a PWM signal can be applied at the U1 shutdown pin for power efficiency. This circuit works well for a single LED.

ADJUSTABLE HIGH POWER LED DRIVER

Figure 35 shows a circuit that can drive three to four high power LEDs. ADP1610 is an adjustable boost regulator that provides the voltage headroom and current for the LEDs. The AD5227 and the op amp form an average gain of 12 feedback network that servos the R_{SET} voltage and ADP1610's FB pin 1.2 V band gap reference voltage. As the loop is set, the voltage across R_{SET} is regulated around 0.1 V and adjusted by the digital potentiometer.

$$I_{LED} = \frac{V_{R_{SET}}}{R_{SET}} \quad (6)$$

R_{SET} should be small enough to conserve power but large enough to limit maximum LED current. R3 should also be used in parallel with AD5227 to limit the LED current within an achievable range. A wider current adjustment range is possible by lowering the R2 to R1 ratio, as well as changing R3 accordingly.

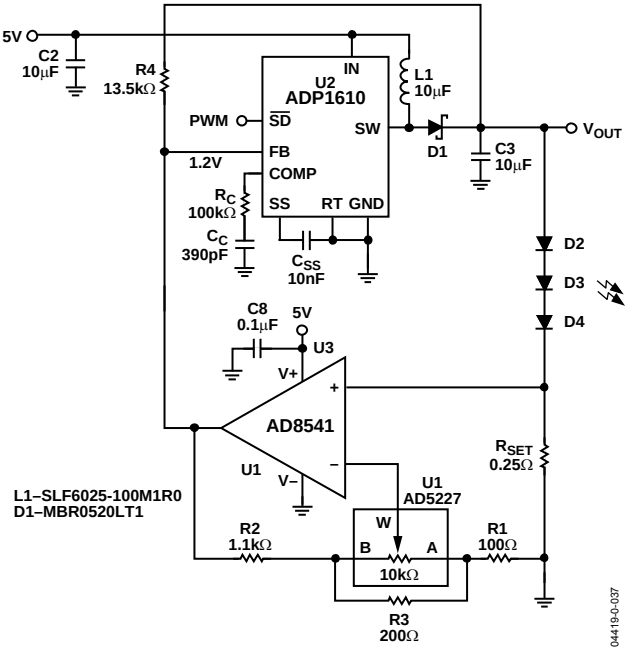

Figure 35. Adjustable Current Source for LEDs in Series

AUTOMATIC LCD PANEL BACKLIGHT CONTROL

With the addition of a photocell sensor, an automatic brightness control can be achieved. As shown in Figure 36, the resistance of the photocell changes linearly but inversely with the light output. The brighter the light output, the lower the photocell resistance and vice versa. The AD5227 sets the voltage level that is gained up by U2 to drive N1 to a desirable brightness. With the photocell acting as the variable feedback resistor, the change in the light output changes the R2 resistance, therefore causing U2 to drive N1 accordingly to regulate the output. This simple low cost implementation of the LED controller can compensate for the temperature and aging effects typically found in high power LEDs. Similarly, for power efficiency, a PWM signal can be applied at the gate of N2 to switch the LED on and off without any noticeable effect.

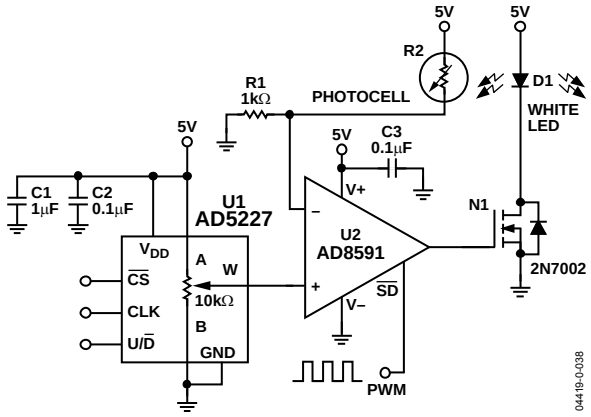

Figure 36. Automatic LCD Panel Backlight Control

6-BIT CONTROLLER

The AD5227 can form a simple 6-bit controller with a clock generator, a comparator, and some output components. Figure 37 shows a generic 6-bit controller with a comparator that first compares the sampling output with the reference level and outputs either a high or low level to the AD5227 U/$\overline{D}$ pin. The AD5227 then changes step at every clock cycle in the direction indicated by the U/$\overline{D}$ state. Although this circuit is not as elegant as the one shown in Figure 36, it is self-contained, very easy to design, and can adapt to various applications.

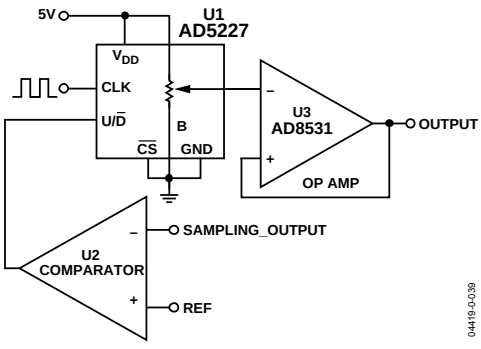

Figure 37. 6-Bit Controller

CONSTANT BIAS WITH SUPPLY TO RETAIN RESISTANCE SETTING

Users who consider EEMEM potentiometers but cannot justify the additional cost and programming for their designs can consider constantly biasing the AD5227 with the supply to retain the resistance setting as shown in Figure 38. The AD5227 is designed specifically with low power to allow power conservation even in battery-operated systems. As shown in Figure 39, a similar low power digital potentiometer is biased with a 3.4 V 450 mA/hour Li-Ion cell phone battery. The measurement shows that the device drains negligible power. Constantly biasing the potentiometer is a practical approach because most portable devices do not require detachable batteries for charging. Although the resistance setting of the AD5227 is lost when the battery needs to be replaced, this event occurs so infrequently that the inconvenience is minimal for most applications.

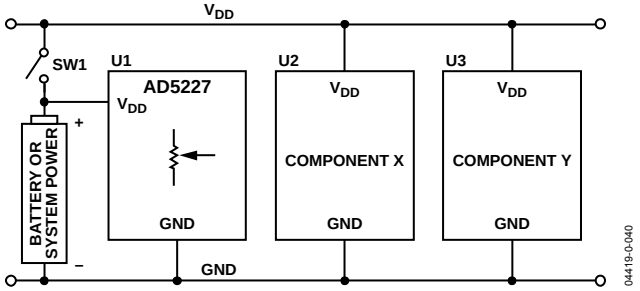

Figure 38. Constant Bias AD5227 for Resistance Retention

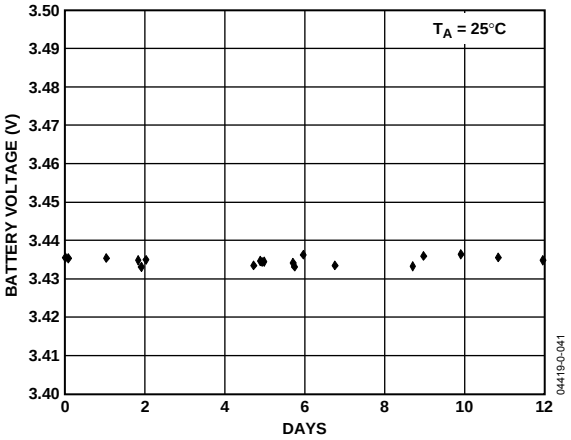

Figure 39. Battery Consumption Measurement

OUTLINE DIMENSIONS

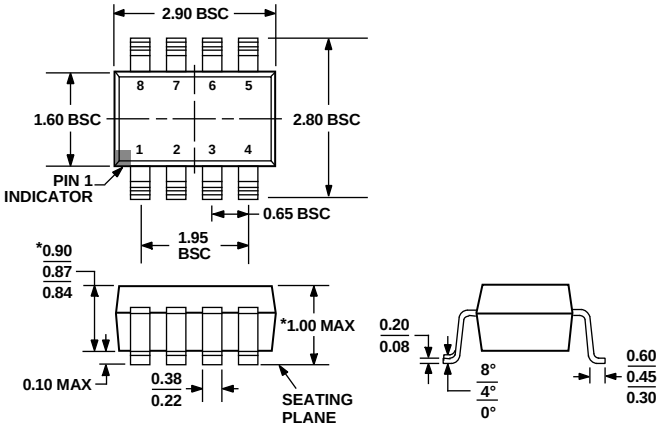

Figure 40. 8-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB}[1] (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
AD5227BUJZ10-RL7[2]	10	−40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3G
AD5227BUJZ10-R2[2]	10	−40°C to +105°C	8-Lead TSOT	UJ-8	250	D3G
AD5227BUJZ50-RL7[2]	50	−40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3H
AD5227BUJZ50-R2[2]	50	−40°C to +105°C	8-Lead TSOT	UJ-8	250	D3H
AD5227BUJZ100-RL7[2]	100	−40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3J
AD5227BUJZ100-R2[2]	100	−40°C to +105°C	8-Lead TSOT	UJ-8	250	D3J
AD5227EVAL	10		Evaluation Board		1	

[1] The end-to-end resistance R_{AB} is available in 10 kΩ, 50 kΩ, and 100 kΩ versions. The final three characters of the part number determine the nominal resistance value, for example, 10 kΩ = 10.
[2] Z = RoHS Compliant Part.

NOTES

D04419–0–5/09(B)