256-Position Two-Time Programmable I²C Digital Potentiometer

AD5170

FEATURES

- 256-position
- TTP (two-time programmable) set-and-forget resistance setting allows second-chance permanent programming
- Unlimited adjustments prior to OTP (one-time programming) activation
- OTP overwrite allows dynamic adjustments with user defined preset
- End-to-end resistance: 2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
- Compact MSOP-10 (3 mm × 4.9 mm) package
- Fast settling time: t_S = 5 µs typ in power-up
- Full read/write of wiper register
- Power-on preset to midscale
- Extra package address decode pins AD0 and AD1
- Single-supply 2.7 V to 5.5 V
- Low temperature coefficient: 35 ppm/°C
- Low power, I_{DD} = 6 µA maximum
- Wide operating temperature: –40°C to +125°C
- Evaluation board and software are available
- Software replaces µC in factory programming applications

APPLICATIONS

- Systems calibration
- Electronics level setting
- Mechanical Trimmers® replacement in new designs
- Permanent factory PCB setting
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier biasing
- Automotive electronics adjustment
- Gain control and offset adjustment

GENERAL OVERVIEW

The AD5170 is a 256-position, two-time programmable (TTP) digital potentiometer[1] that employs fuse link technology to enable two opportunities at permanently programming the resistance setting. OTP is a cost-effective alternative to EEMEM for users who do not need to program the digital potentiometer setting in memory more than once. This device performs the same electronic adjustment function as mechanical potentiometers or variable resistors with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

FUNCTIONAL BLOCK DIAGRAM

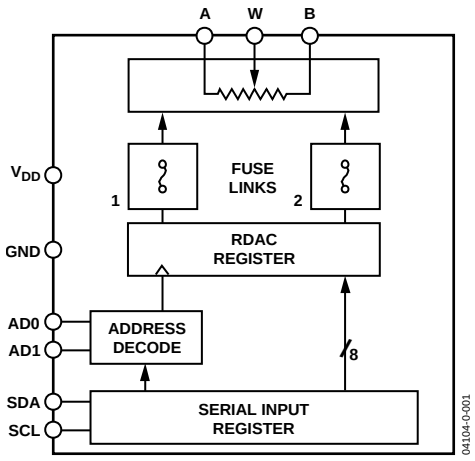

Figure 1.

The AD5170 is programmed using a 2-wire, I²C® compatible digital interface. Unlimited adjustments are allowed before permanently (there are actually two opportunities) setting the resistance value. During OTP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

Unlike traditional OTP digital potentiometers, the AD5170 has a unique temporary OTP overwrite feature that allows for new adjustments even after the fuse has been blown. However, the OTP setting is restored during subsequent power-up conditions. This feature allows users to treat these digital potentiometers as volatile potentiometers with a programmable preset.

For applications that program the AD5170 at the factory, Analog Devices offers device programming software running on Windows NT®, 2000, and XP® operating systems. This software effectively replaces any external I²C controllers, thus enhancing the time-to-market of the user's systems.

[1] The terms digital potentiometer, VR, and RDAC are used interchangeably.

Rev. A

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11/03—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS — 2.5 kΩ

V_{DD} = 5 V ± 10% or 3 V ±10%, V_A = +V_{DD}, V_B = 0 V, –40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	–2	±0.1	+2	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	–6	±0.75	+6	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	–20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	V_{AB} = V_{DD}, Wiper = no connect		35		ppm/°C
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS — POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Differential Nonlinearity[4]	DNL		–1.5	±0.1	+1.5	LSB
Integral Nonlinearity[4]	INL		–2	±0.6	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	–10	–2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	2	10	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A,V_B,V_W		GND		V_{DD}	V
Capacitance[6] A, B	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Shutdown Supply Current[7]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[5]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
OTP Supply Voltage	V_{DD_OTP}	T_A = 25°C	5.25		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
OTP Supply Current	I_{DD_OTP}	V_{DD_OTP} = 5.5 V, T_A = 25°C	100			mA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, Code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[9]						
Bandwidth –3 dB	BW_2.5K	Code = 0x80		4.8		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 1.25 kΩ, R_S = 0		3.2		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] V_{AB} = V_{DD}, Wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.
[9] All dynamic characteristics use V_{DD} = 5 V.

ELECTRICAL CHARACTERISTICS — 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$; V_B = 0 V, –40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	–1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	–2.5	±0.25	+2.5	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	–20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS — POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Differential Nonlinearity[4]	DNL		–1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		–1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	–2.5	–1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2.5	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A,V_B,V_W		GND		V_{DD}	V
Capacitance[6] A, B	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Shutdown Supply Current[7]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
OTP Supply Voltage[8]	V_{DD_OTP}		5.25		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
OTP Supply Current[9]	I_{DD_OTP}	V_{DD_OTP} = 5.5 V, T_A = 25°C	100			mA
Power Dissipation[10]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[11]						
Bandwidth –3 dB	BW	R_{AB} = 10 kΩ, code = 0x80		600		kHz
		R_{AB} = 50 kΩ, code = 0x80		100		kHz
		R_{AB} = 100 kΩ, code = 0x80		40		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.1		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8] Different from operating power supply, power supply OTP is used one time only.
[9] Different from operating current, supply current for OTP lasts approximately 400 ms for one time only.
[10] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[11] All dynamic characteristics use V_{DD} = 5 V.

TIMING CHARACTERISTICS — 2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$; V_B = 0 V, –40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I^2C INTERFACE TIMING CHARACTERISTICS[1] (Specifications apply to all parts)						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6			µs
$t_{SU;STA}$ Setup Time for Repeated START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time[2]	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

[1] See timing diagrams for locations of measured values.
[2] The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Value
V_{DD} to GND	–0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
Terminal Current, Ax–Bx, Ax–Wx, Bx–Wx[1]	
Pulsed	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	–40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2] θ_{JA}: MSOP-10	230°C/W

[1] Maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_{JMAX} – T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

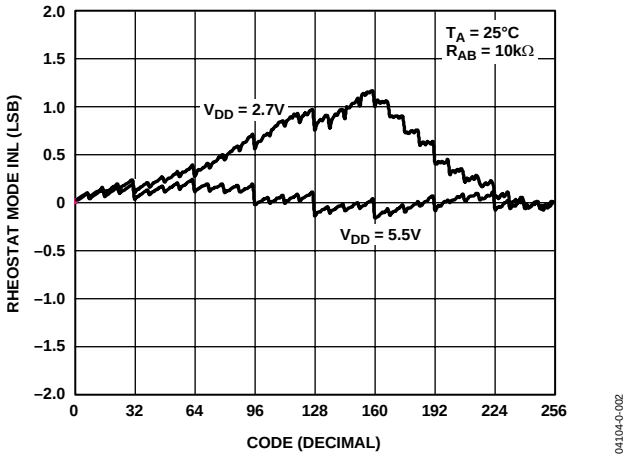

Figure 2. R-INL vs. Code vs. Supply Voltages

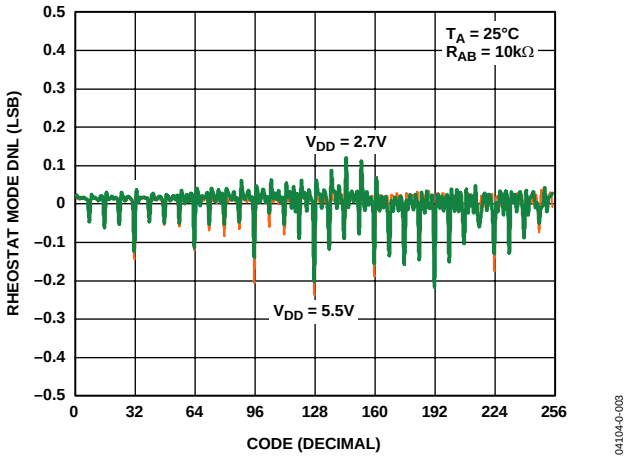

Figure 3. R-DNL vs. Code vs. Supply Voltages

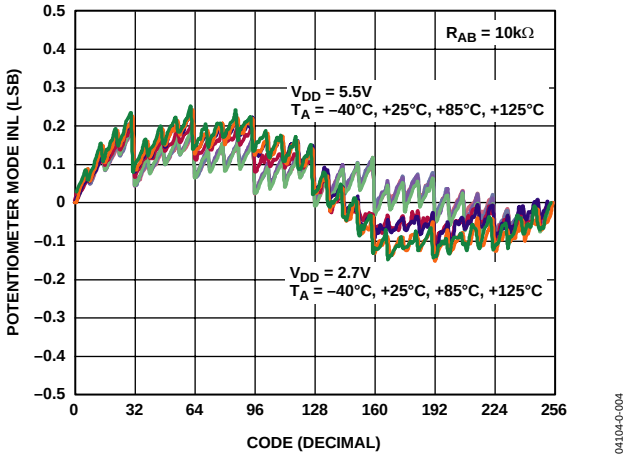

Figure 4. INL vs. Code vs. Temperature

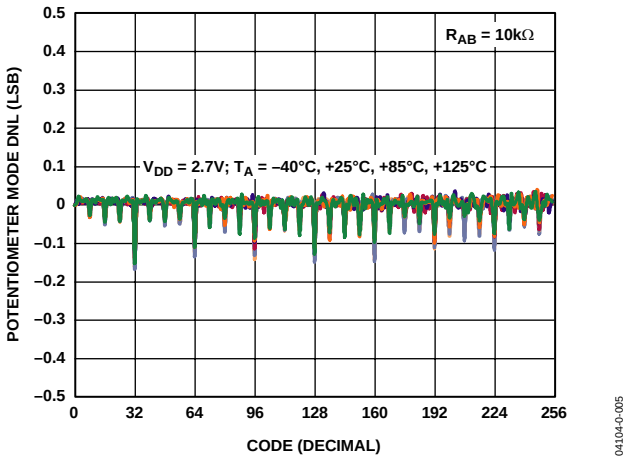

Figure 5. DNL vs. Code vs. Temperature

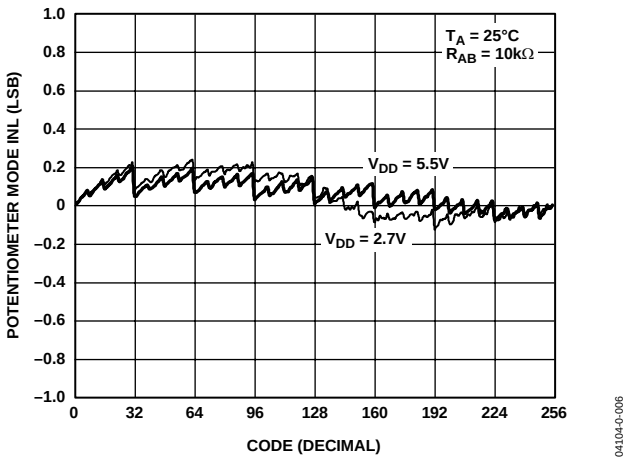

Figure 6. INL vs. Code vs. Supply Voltages

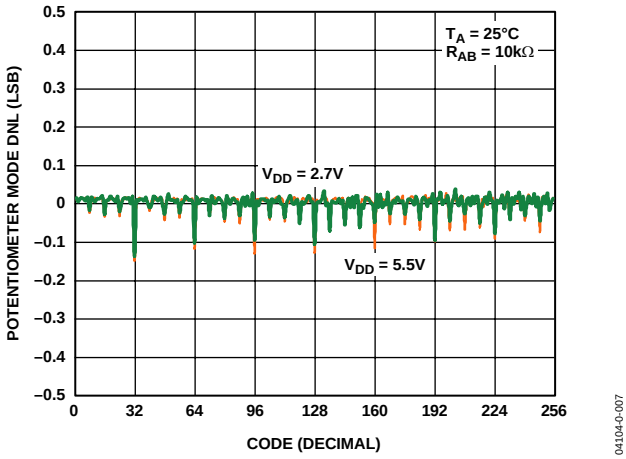

Figure 7. DNL vs. Code vs. Supply Voltages

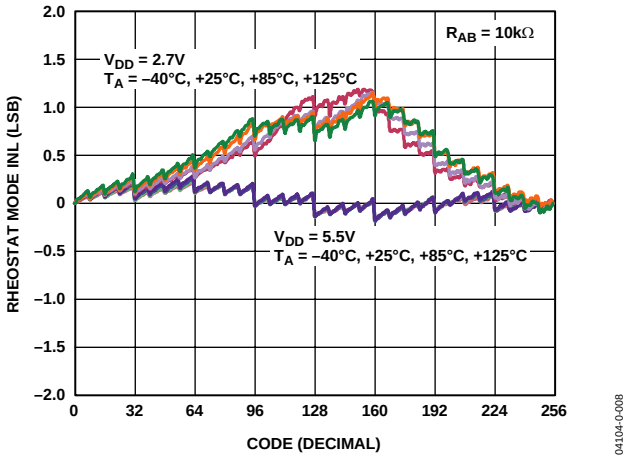

Figure 8. R-INL vs. Code vs. Temperature

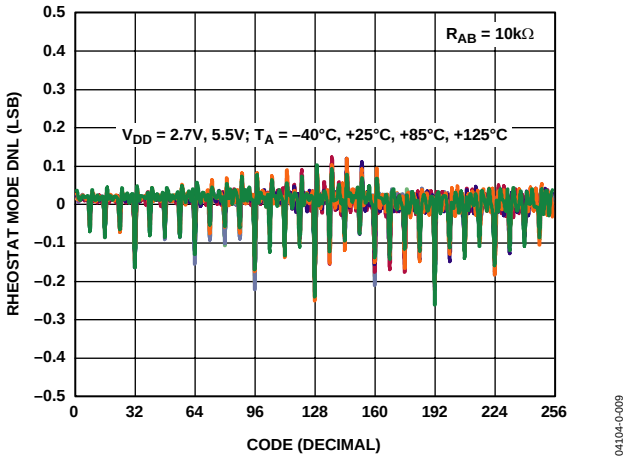

Figure 9. R-DNL vs. Code vs. Temperature

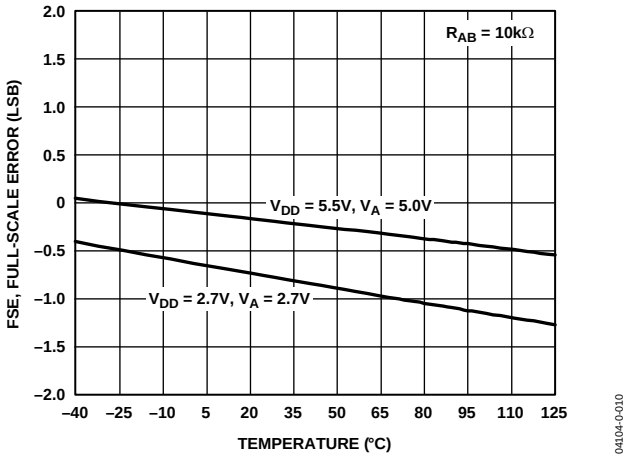

Figure 10. Full-Scale Error vs. Temperature

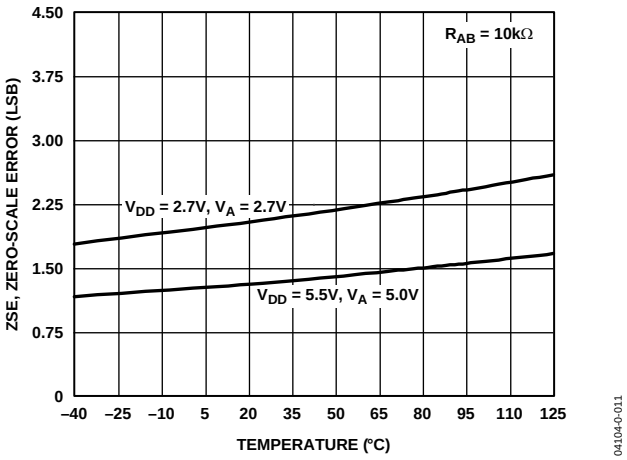

Figure 11. Zero-Scale Error vs. Temperature

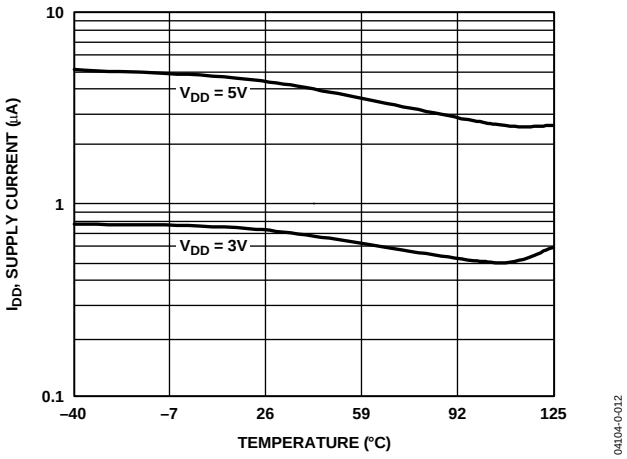

Figure 12. Supply Current vs. Temperature

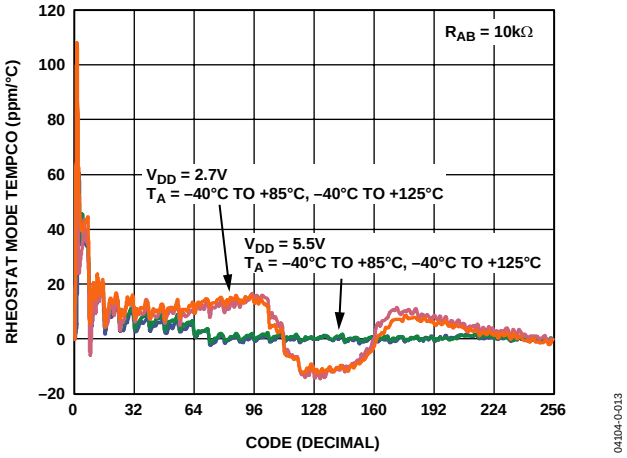

Figure 13. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

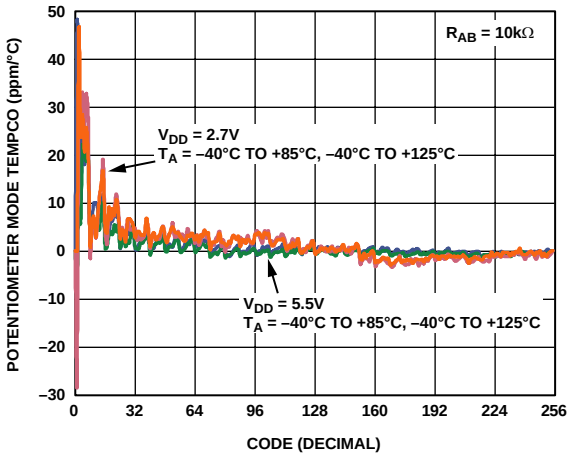

Figure 14. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

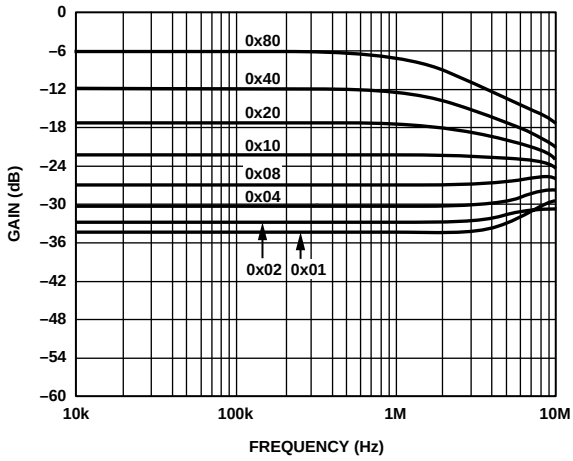

Figure 15. Gain vs. Frequency vs. Code, R_{AB} = 2.5 kΩ

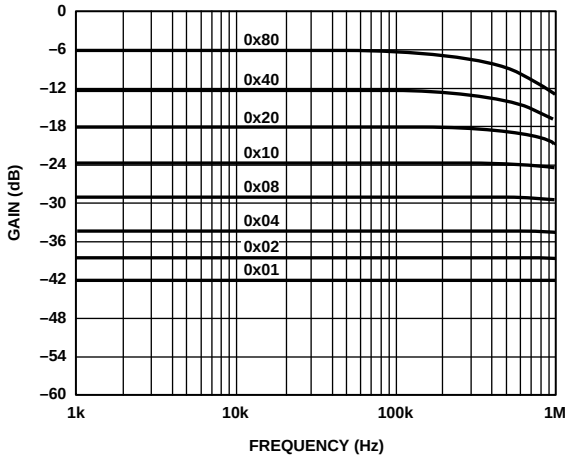

Figure 16. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

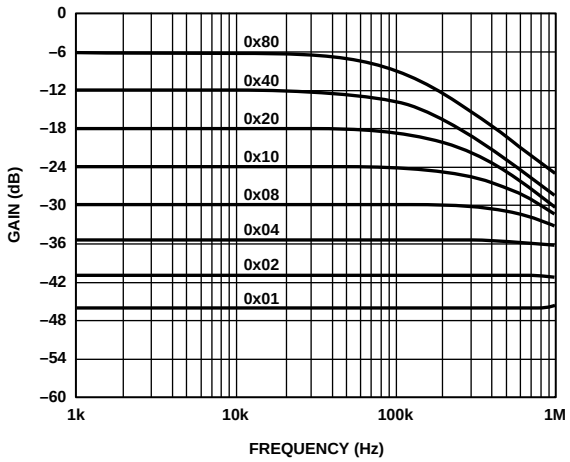

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

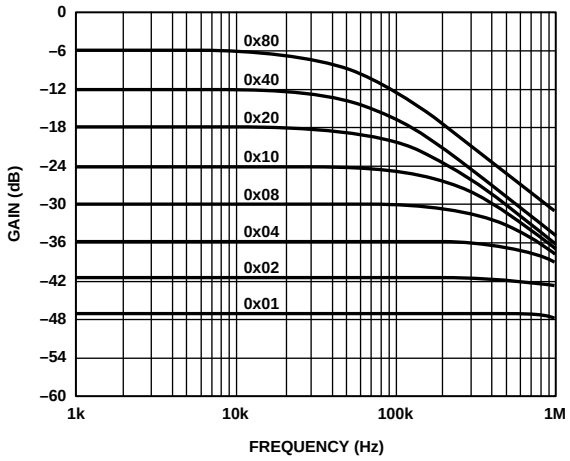

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

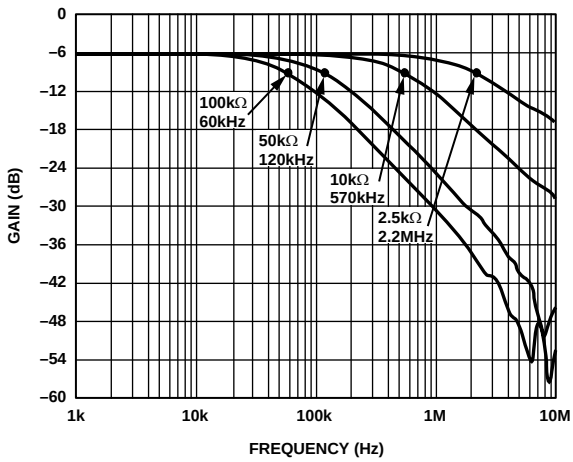

Figure 19. –3 dB Bandwidth at Code = 0x80

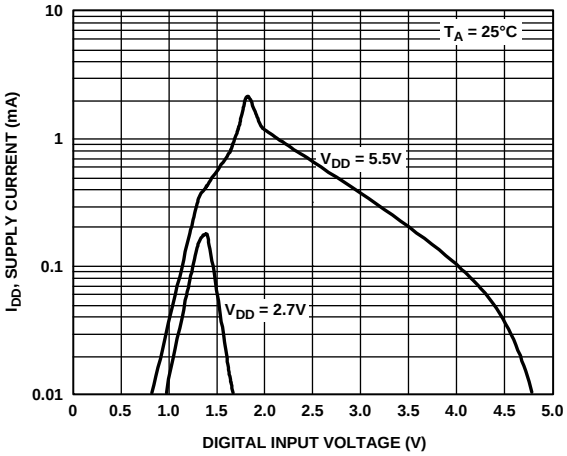

Figure 20. I_{DD} vs. Input Voltage

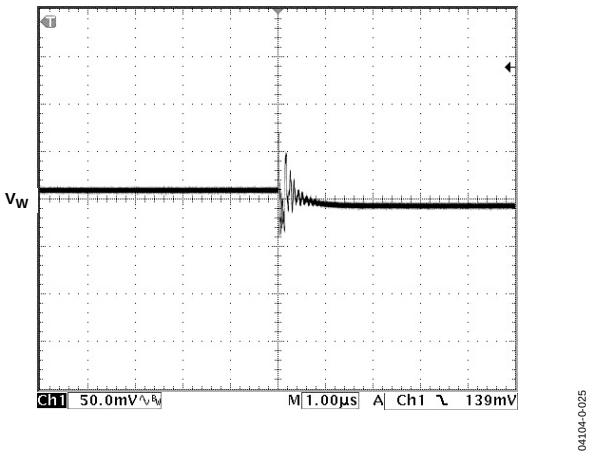

Figure 22. Midscale Glitch, Code 0x80 to 0x7F

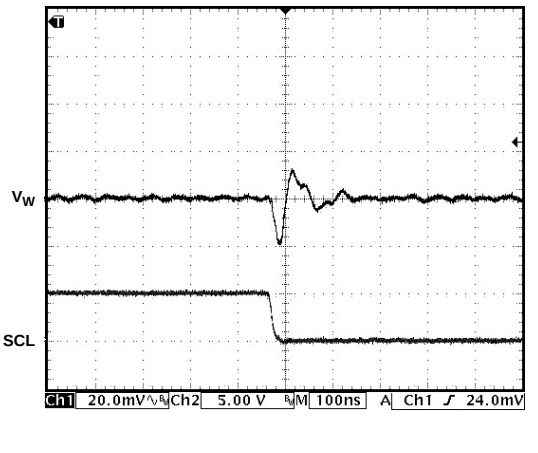

Figure 21. Digital Feedthrough

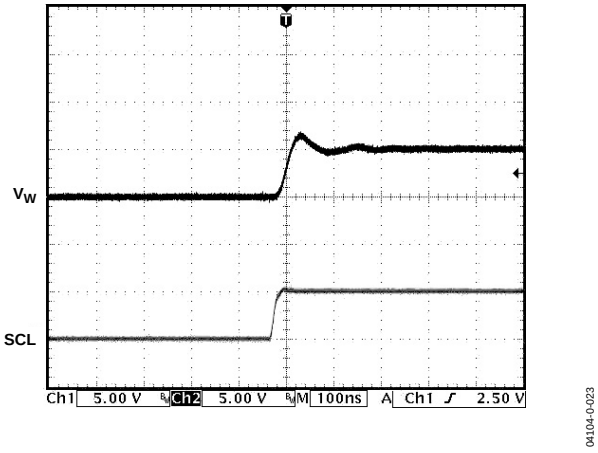

Figure 23. Large Signal Settling Time

TEST CIRCUITS

Figure 24 to Figure 29 illustrate the test circuits that define the test conditions used in the product specification tables.

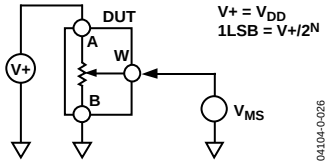

Figure 24. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

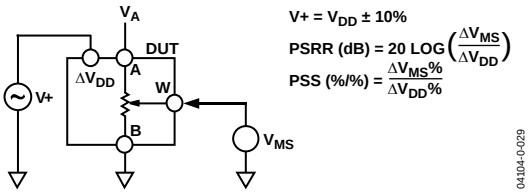

Figure 27. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

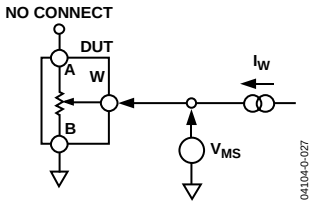

Figure 25. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

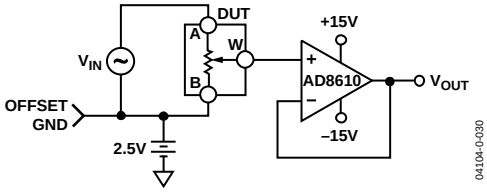

Figure 28. Test Circuit for Gain vs. Frequency

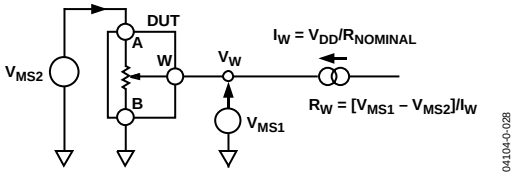

Figure 26. Test Circuit for Wiper Resistance

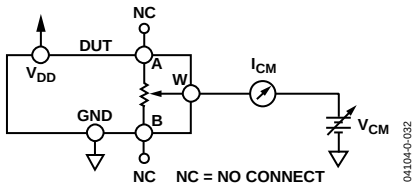

Figure 29. Test Circuit for Common-Mode Leakage Current

THEORY OF OPERATION

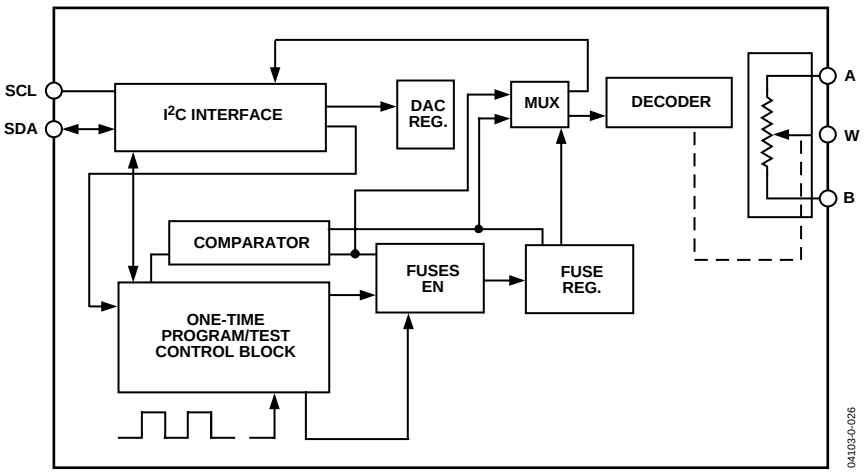

Figure 30. Detailed Functional Block Diagram

The AD5170 is a 256-position, digitally controlled variable resistor (VR) that employs fuse link technology to achieve memory retention of resistance setting.

An internal power-on preset places the wiper at midscale during power-on. If the OTP function has been activated, the device powers up at the user-defined permanent setting.

ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5170 presets to midscale during initial power-on. After the wiper is set at the desired position, the resistance can be permanently set by programming the T bit high along with the proper coding (see Table 7 and Table 8) and one time V_{DD_OTP}. Note that fuse link technology of the AD517x family of digital pots requires V_{DD_OTP} between 5.25 V and 5.5 V to blow the fuses to achieve a given nonvolatile setting. On the other hand, V_{DD} can be 2.7 V to 5.5 V during operation. As a result, system supply that is lower than 5.25 V requires external supply for one-time programming. Note that the user is allowed only one attempt in blowing the fuses. If the user fails to blow the fuses at the first attempt, the fuses' structures may have changed such that they may never be blown regardless of the energy applied at subsequent events. For details, see the Power Supply Considerations section.

The device control circuit has two validation bits, E1 and E0, that can be read back to check the programming status (see Table 7). Users should always read back the validation bits to ensure that the fuses are properly blown. After the fuses have been blown, all fuse latches are enabled upon subsequent power-on; therefore, the output corresponds to the stored setting. Figure 30 shows a detailed functional block diagram.

PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of 256 possible settings.

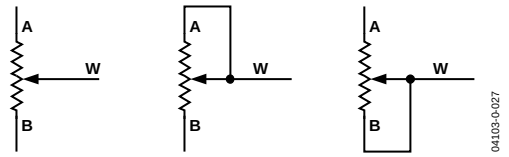

Figure 31. Rheostat Mode Configuration

Assuming a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between Terminal W and Terminal B. The second connection is the first tap point, which corresponds to 139 Ω ($R_{WB} = R_{AB}/256 + 2 \times R_W = 39\ \Omega + 2 \times 50\ \Omega$) for data 0x01. The third connection is the next tap point, representing 178 Ω (2 × 39 Ω + 2 × 50 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100 Ω ($R_{AB} + 2 \times R_W$).

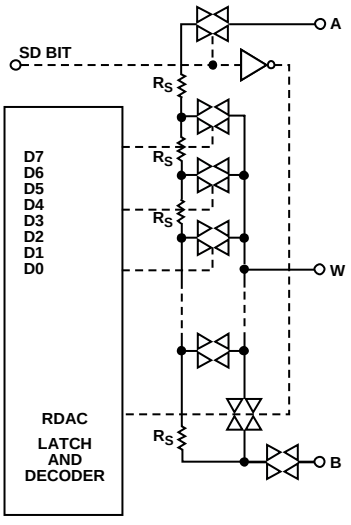

Figure 32. AD5170 Equivalent RDAC Circuit

The general equation that determines the digitally programmed output resistance between Terminal W and Terminal B is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + 2 \times R_W \quad (1)$$

where D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register, R_{AB} is the end-to-end resistance, and R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and the A terminal is open-circuited, the output resistance R_{WB} is set for the RDAC latch codes, as shown in Table 5.

Table 5. Codes and Corresponding R_{WB} Resistance

D (Dec.)	R_{WB} (Ω)	Output State
255	9,961	Full Scale (R_{AB} – 1 LSB + R_W)
128	5,060	Midscale
1	139	1 LSB
0	100	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition, a finite wiper resistance of 100 Ω is present. Care should be taken to limit the current flow between Terminal W and Terminal B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper, Terminal W, and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{128} \times R_{AB} + 2 \times R_W \quad (2)$$

For R_{AB} = 10 kΩ and the B terminal open-circuited, the following output resistance, $R_{WA,}$ is set for the RDAC latch codes, as shown in Table 6.

Table 6. Codes and Corresponding R_{WA} Resistance

D (Dec.)	R_{WA} (Ω)	Output State
255	139	Full Scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero Scale

Typical device-to-device matching is process lot dependent and may vary by up to ±30%. Since the resistance element is processed using thin film technology, the change in R_{AB} with temperature has a very low 35 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A–B, W–A, and W–B can be at either polarity.

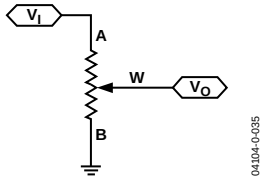

Figure 33. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB}, and not the absolute values. Thus, the temperature drift reduces to 15 ppm/°C.

ESD PROTECTION

All digital inputs—SDA, SCL, AD0, and AD1—are protected with a series input resistor and parallel Zener ESD structures, as shown in Figure 34 and Figure 35.

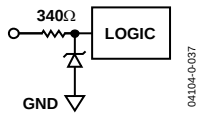

Figure 34. ESD Protection of Digital Pins

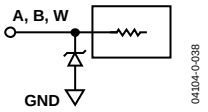

Figure 35. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5170 V_{DD} to GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} or GND will be clamped by the internal forward-biased diodes (see Figure 36).

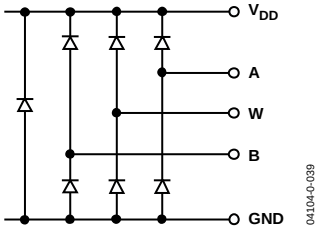

Figure 36. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 36), it is important to power V_{DD}/GND before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode will be forward biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is GND, V_{DD}, the digital inputs, and then V_A/V_B/V_W. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltage supplies share the same V_{DD} terminal of the AD5170. The AD5170 employs fuse link technology that requires 5.25 V to 5.5 V for blowing the internal fuses to achieve a given setting, but normal V_{DD} can be anywhere between 2.7 V and 5.5 V after the fuse programming process. As a result, dual voltage supplies and isolation are needed if system V_{DD} is lower than the required V_{DD_OTP}. The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 5.25 V to 5.5 V and able to provide a 100 mA current for 400 ms for successful one-time programming. Once fuse programming is completed, the V_{DD_OTP} supply must be removed to allow normal operation at 2.7 V to 5.5 V and the device will consume current in μA range. Figure 37 shows the simplest implementation of a dual supply requirement by using a jumper. This approach saves one voltage supply, but draws additional current and requires manual configuration.

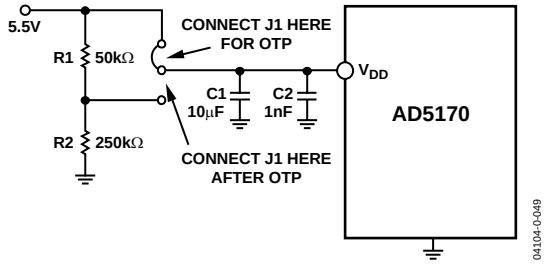

Figure 37. Power Supply Requirement

An alternate approach in 3.5 V to 5.25 V systems adds a signal diode between the system supply and the OTP supply for isolation, as shown in Figure 38.

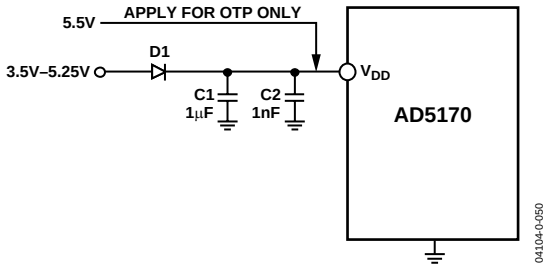

Figure 38. Isolate 5.5 V OTP Supply from 3.5 V to 5.25 V Normal Operating Supply. The V_{DD_OTP} must be removed once OTP is completed.

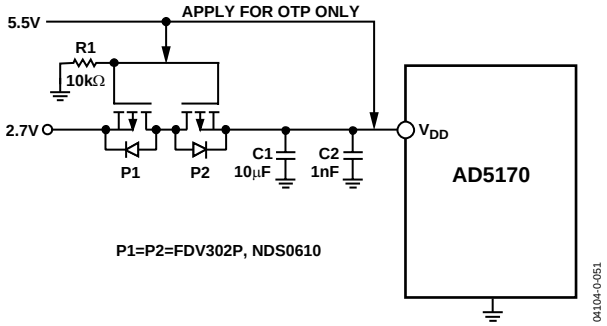

Figure 39. Isolate 5.5 V OTP Supply from 2.7 V Normal Operating Supply. The V_{DD_OTP} supply must be removed once OTP is completed.

For users who operate their systems at 2.7 V, use of the bidirectional low threshold P-Ch MOSFETs is recommended for the supply's isolation. As shown in Figure 39, this assumes

the 2.7 V system voltage is applied first, and the P1 and P2 gates are pulled to ground, thus turning on P1 and subsequently P2. As a result, V_{DD} of the AD5170 approaches 2.7 V. When the AD5170 setting is found, the factory tester applies the V_{DD_OTP} to both the V_{DD} and the MOSFETs gates turning off P1 and P2. The OTP command is executed at this time to program the AD5170 while the 2.7 V source is protected. Once the fuse programming is completed, the tester withdraws the V_{DD_OTP} and the setting for AD5170 is permanently fixed.

AD5170 achieves the OTP function through blowing internal fuses. Users should always apply the 5.25 V to 5.5 V one-time program voltage requirement at the first fuse programming attempt. Failure to comply with this requirement may lead to a change in the fuse structures, rendering programming inoperable.

Poor PCB layout introduces parasitics that may affect the fuse programming. Therefore, it is recommended to add a 10 µF tantalum capacitor in parallel with a 1 nF ceramic capacitor as close as possible to the V_{DD} pin. The type and value chosen for both capacitors are important. This combination of capacitor values provides both a fast response and larger supply current handling with minimum supply droop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple while C2 reduces high frequency noise during normal operation.

LAYOUT CONSIDERATIONS

It is good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

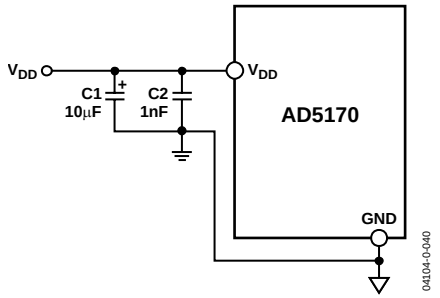

Figure 40. Power Supply Bypassing

EVALUATION SOFTWARE/HARDWARE

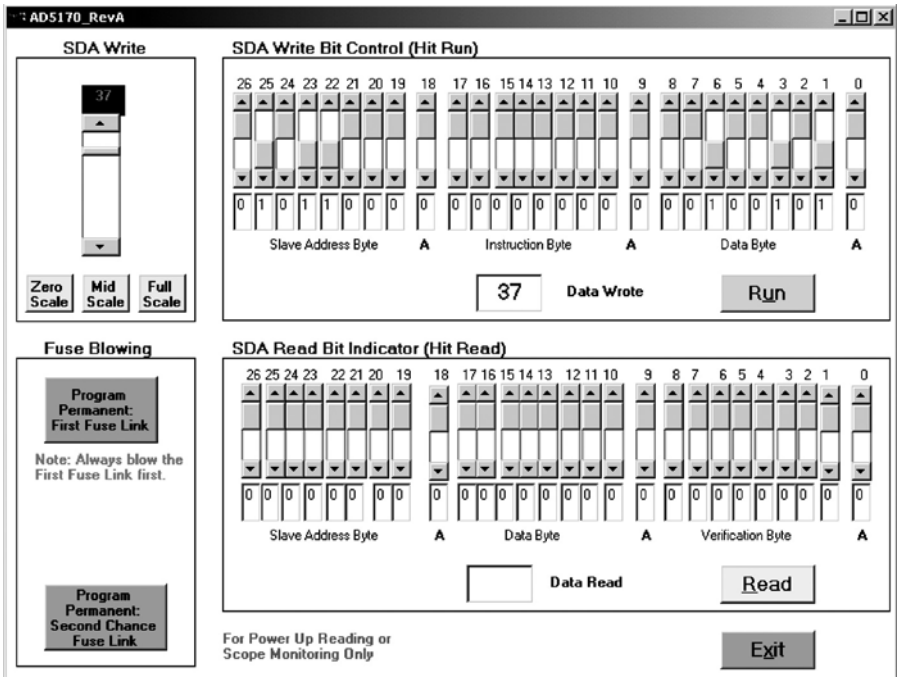

Figure 41. AD5170 Computer Software Interface

There are two ways of controlling the AD5170. Users can either program the devices with computer software or external I²C controllers.

SOFTWARE PROGRAMMING

Due to the advantages of the one-time programmable feature, users may consider programming the device in the factory before shipping the final product to end-users. ADI offers device programming software that can be implemented in the factory on PCs running Windows® 95 or later. As a result, external controllers are not required, which significantly reduces development time. The program is an executable file that does not require knowledge of any programming languages or programming skills. It is easy to set up and to use. Figure 41 shows the software interface. The software can be downloaded from www.analog.com.

The AD5170 starts at midscale after power-up prior to OTP programming. To increment or decrement the resistance, the user may simply move the scrollbars on the left. To write any specific value, the user should use the bit pattern in the upper screen and press the Run button. The format of writing data to the device is shown in Table 7. Once the desired setting is found, the user presses the Program Permanent button to blow the internal fuse links.

To read the validation bits and data from the device, the user simply presses the Read button. The format of the read bits is shown in Table 8.

To apply the device programming software in the factory, users must modify a parallel port cable and configure Pin 2, Pin 3, Pin 15, and Pin 25 for SDA_write, SCL, SDA_read, and DGND, respectively, for the control signals (Figure 42). Users should also lay out the PCB of the AD5170 with SCL and SDA pads, as shown in Figure 43, such that pogo pins can be inserted for factory programming.

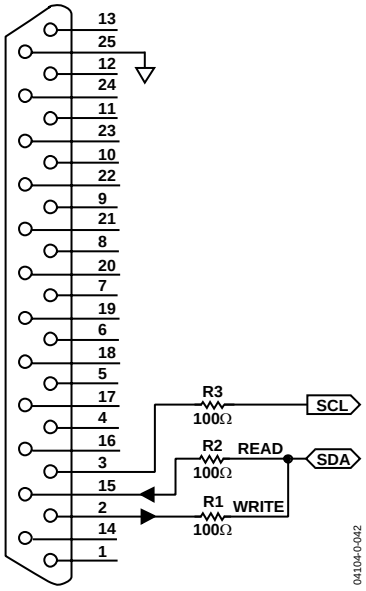

Figure 42. Parallel Port Connection. Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND.

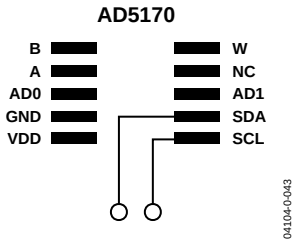

Figure 43. Recommended AD5170 PCB Layout. The SCL and SDA pads allow pogo pins to be inserted so that signals can be communicated through the parallel port for programming (Figure 42).

I²C INTERFACE

Table 7. Write Mode

S	0	1	0	1	1	AD1	AD0	$\overline{W}$	A	2T	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 8. Read Mode

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

S = Start Condition.

P = Stop Condition.

A = Acknowledge.

AD0, AD1 = Package Pin Programmable Address Bits.

X = Don't Care.

$\overline{W}$ = Write.

R = Read.

2T = Second fuse link array for two-time programming. Logic 0 corresponds to first trim. Logic 1 corresponds to second trim. Note that blowing trim #2 before trim #1 effectively disables trim #1 and in turn only allows one-time programming.

SD = Shutdown connects wiper to B terminal and open circuits the A terminal. It does not change the contents of the wiper register.

T = OTP Programming Bit. Logic 1 permanently programs the wiper.

OW = Overwrite the fuse setting and program the digital potentiometer to a different setting. Note that upon power-up, the digital potentiometer presets to either midscale or fuse setting depending on whether the fuse link has been blown.

D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits.

E1, E0 = OTP Validation Bits.

0, 0 = Ready to Program.

1, 0 = Fatal Error. Some fuses not blown. Do not retry. Discard this unit.

1, 1 = Programmed Successfully. No further adjustments are possible.

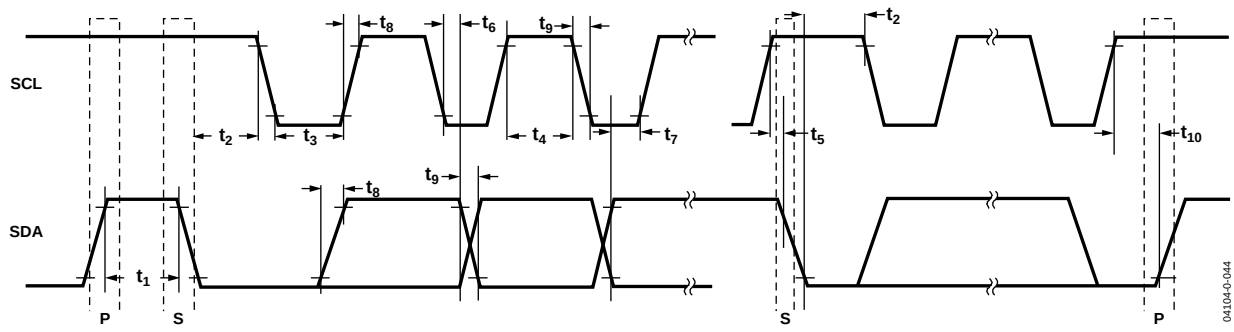

Figure 44. I²C Interface Detailed Timing Diagram

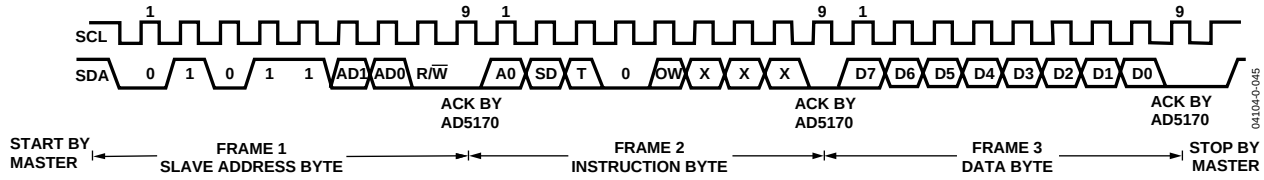

Figure 45. Writing to the RDAC Register

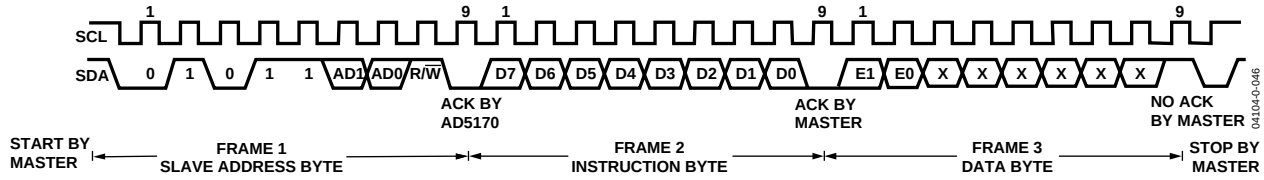

Figure 46. Reading Data from the RDAC Register

I²C COMPATIBLE 2-WIRE SERIAL BUS

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 45). The following byte is the slave address byte, which consists of the slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from, or written to, the slave device). AD0 and AD1 are configurable address bits which allow up to four devices on one bus (see Table 7).

   The slave address corresponding to the transmitted address bits responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. If the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. In the write mode, the second byte is the instruction byte. The first bit (MSB), 2T, of the instruction byte is the second trim enable bit. A logic low selects the first array of fuses, and a logic high selects the second array. This means that after blowing the fuses with trim#1, the user still has another chance to blow them again with trim#2. Note that using trim#2 before trim#1 effectively disables trim#1 and, in turn, only allows one-time programming.

   The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC. Also, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

   The third MSB, T, is the OTP (one-time programmable) programming bit. A logic high blows the poly fuses and programs the resistor setting permanently. For example, if the user wanted to blow the first array of fuses, the instruction byte would be 00100XXX. To blow the second array of fuses, the instruction byte would be 10100XXX. A logic low of the T bit simply allows the device to act as a typical volatile digital potentiometer.

   The fourth MSB must always be at Logic 0.

   The fifth MSB, OW, is an overwrite bit. When raised to a logic high, OW allows the RDAC setting to be changed even after the internal fuses have been blown. However, once OW is returned to a logic zero, the position of the RDAC returns to the setting prior to overwrite. Because OW is not static, if the device is powered off and on, the RDAC presets to midscale or to the setting at which the fuses were blown, depending on whether the fuses have been permanently set.

   The remainder of the bits in the instruction byte are Don't Care bits (see Figure 45).

   After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 44).

3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference from the write mode, with eight data bits followed by an Acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 46).

   Following the data byte, the validation byte contains two validation bits, E0 and E1. These bits signify the status of the one-time programming (see Figure 46).

4. After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a STOP condition (see Figure 45). In read mode, the master issues a No Acknowledge for the 9th clock pulse (i.e., the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, which goes high to establish a STOP condition (see Figure 46).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output updates on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

Table 9. Validation Status

E1	E0	Status
0	0	Ready for Programming.
1	0	Fatal Error. Some fuses not blown. Do not retry. Discard this unit.
1	1	Successful. No further programming is possible.

Multiple Devices on One Bus

Figure 47 shows four AD5170s on the same serial bus. Each has a different slave address because the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to, or read from, independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C compatible interface.

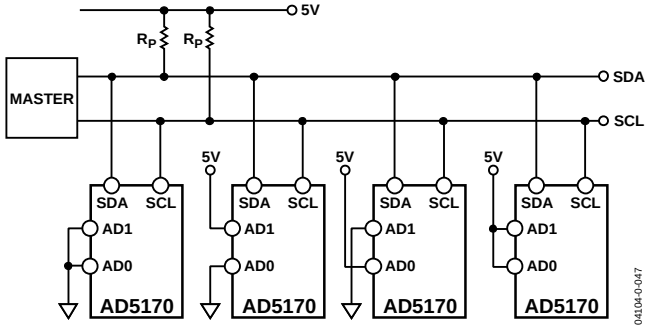

Figure 47. Multiple AD5170s on One I²C Bus

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

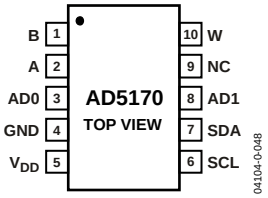

Figure 48. Pin Configuration

Table 10. Pin Function Descriptions

Pin	Mnemonic	Description
1	B	B Terminal.
2	A	A Terminal.
3	AD0	Programmable Address Bit 0 for Multiple Package Decoding.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply.
6	SCL	Serial Clock Input. Positive Edge Triggered.
7	SDA	Serial Data Input/Output.
8	AD1	Programmable Address Bit 1 for Multiple Package Decoding.
9	NC	No Connect.
10	W	W Terminal.

OUTLINE DIMENSIONS

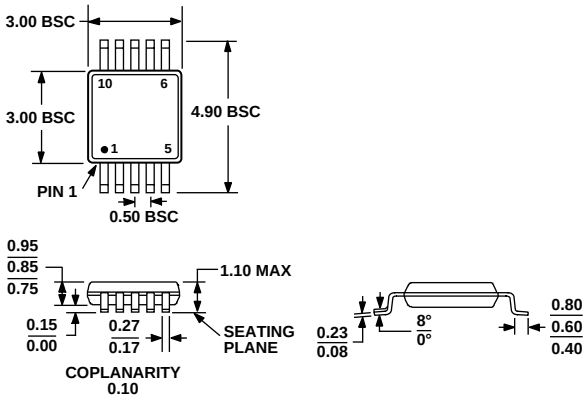

Figure 49. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (kΩ)	Temperature	Package Description	Package Option	Branding
AD5170BRM2.5	2.5	–40°C to +125°C	MSOP-10	RM-10	D0Y
AD5170BRM2.5-RL7	2.5	–40°C to +125°C	MSOP-10	RM-10	D0Y
AD5170BRM10	10	–40°C to +125°C	MSOP-10	RM-10	D0Z
AD5170BRM10-RL7	10	–40°C to +125°C	MSOP-10	RM-10	D0Z
AD5170BRM50	50	–40°C to +125°C	MSOP-10	RM-10	D0W
AD5170BRM50-RL7	50	–40°C to +125°C	MSOP-10	RM-10	D0W
AD5170BRM100	100	–40°C to +125°C	MSOP-10	RM-10	D0X
AD5170BRM100-RL7	100	–40°C to +125°C	MSOP-10	RM-10	D0X
AD5170EVAL[1]			Evaluation Board		

[1] The evaluation board is shipped with the 10 kΩ RAB resistor option; however, the board is compatible with all available resistor value options.

NOTES

D04104–0–11/04(A)