32-Channel, 14-Bit DAC with Full-Scale Output

Voltage Programmable from 50 V to 200 V

FEATURES

- High integration
- 32-channel, 14-bit denseDAC® with integrated high voltage output amplifier
- Guaranteed monotonic
- Housed in 15 mm × 15 mm CSP_BGA package
- Full-scale output voltage programmable from 50 V to 200 V via reference input
- 150/40 µA source/sink drive capability
- Integrated silicon diode for temperature monitoring
- Serial peripheral interface (SPI)
- 1.2 MHz channel update rate
- Asynchronous RESET facility
- −10°C to +85°C temperature range

APPLICATIONS

- Optical microelectromechanical systems (MEMS)
- Optical crosspoint switches
- Micropositioning applications using piezoelectric actuators
- Level setting in automotive test and measurement

GENERAL DESCRIPTION

The AD45335 is a 32-channel, 14-bit denseDAC® with an on-chip high voltage output amplifier. This device is targeted for optical micro-electromechanical systems. The output voltage range is programmable via the REF_IN pin. The output range is 0 V to 50 V when REF_IN = 1 V, and 0 V to 200 V when REF_IN = 4 V. REF_IN is buffered internally on the AD45335 and should be driven from a stable reference source.

The selected digital-to-analog converter (DAC) register is written to via the 3-wire interface. The SPI operates at clock rates of up to 30 MHz.

FUNCTIONAL BLOCK DIAGRAM

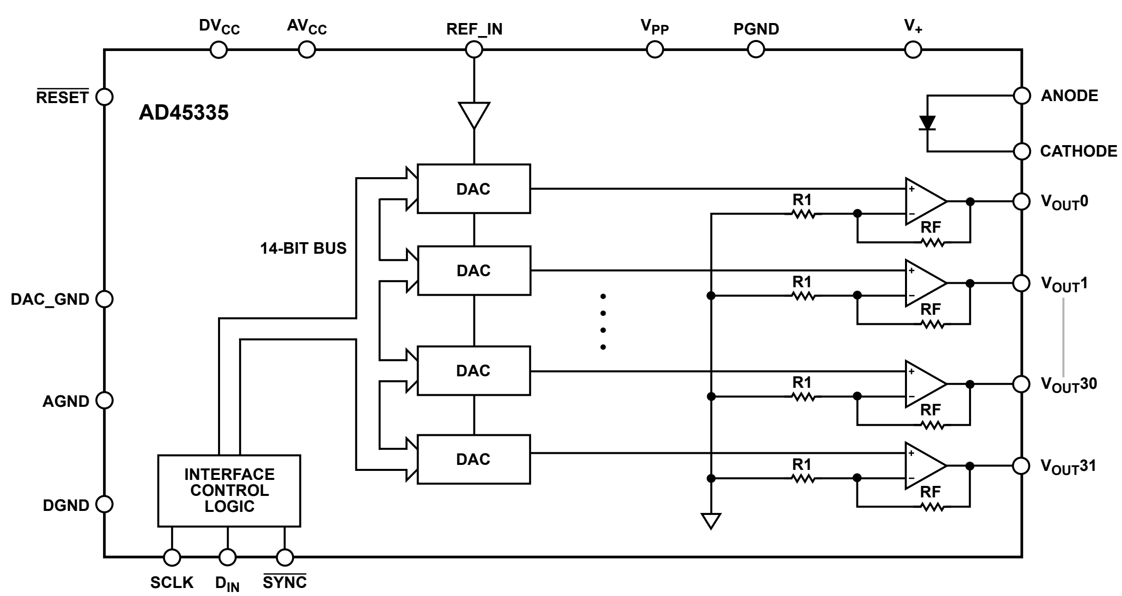

Figure 1. Functional Block Diagram

Rev. PrA

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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SPECIFICATIONS

V_{PP} = 55 V to 225 V; 4.75 ≤ V_+ ≤ 5.25 V; 4.75 V ≤ AV_{CC} ≤ 5.25 V; 2.7 V ≤ DV_{CC} ≤ 5.25 V; PGND = AGND = DGND = DAC_GND = 0 V; AV_{CC} and V_+ must exceed REF_IN by 1.15 V minimum; 1 V ≤ REF_IN ≤ 4.096 V; −10°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DC PERFORMANCE[2, 3]					
Resolution		14		Bits	
Integral Nonlinearity (INL)		±0.1		% of FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Zero Code Voltage			+1	V	
Output Offset Error	−1		+1	V	
Offset Drift		0.5		mV/°C	
Voltage Gain	49	50	51	V/V	Per channel
Gain Temperature Coefficient		−20		ppm/°C	
OUTPUT CHARACTERISTICS					
Output Voltage Range [4]					
No load	1		V_{PP} − 1.5	V	
4MΩ load to GND	1		V_{PP} − 2.5	V	
Output Impedance		50		Ω	
Resistive Load[5]	4			MΩ	To GND
Capacitive Load			200	pF	
Short-Circuit Current[6]					
Sourcing		0.15		mA	
Sinking		0.04		mA	
DC Crosstalk	−4		+4	LSB	
DC Power Supply Rejection (PSRR), V_{PP}		−70		dB	
Long-Term Drift		0.25		LSB	Outputs at midscale, measured over 30 days at 25°C
AC CHARACTERISTICS					
Settling Time					
Falling edge					
¾ to ¼ Scale Step		70		µs	No load
		470		µs	200 pF load
1 LSB Step		20		µs	
Rising edge					
¼ to ¾ Scale Step		70		µs	No load
		190		µs	200 pF load
1 LSB Step		10		µs	
Slew Rate					
Falling edge					
		1.2		V/µs	No load
		0.2		V/µs	200 pF load
Rising Edge					
		1.6		V/µs	No load
		0.6		V/µs	200 pF load
−3 dB Bandwidth	30			kHz	
Output Noise Spectral Density		4.5		µV/√Hz	Measured at 10 kHz
0.1 Hz to 10 Hz Output Noise Voltage		1		mV p-p	
Digital-to-Analog Glitch Impulse					1 LSB change around major carry
Positive Transition		15		nV-sec	
Negative Transition		8		nV-sec	

SPECIFICATIONS

Table 1. (Continued)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Analog Crosstalk		1		µV-sec	
Digital Feedthrough		2		nV-sec	
VOLTAGE REFERENCE, REF_IN[7]					
Input Voltage Range	1		4.096	V	
Input Impedance			60	kΩ	
TEMPERATURE MEASUREMENT DIODE					
Peak Inverse Voltage, P_{IV}			5	V	Cathode to anode
Forward Diode Drop, V_F		0.65	0.8	V	I_F = 100 µA, anode to cathode
Forward Diode Current, I_F			150	µA	Anode to cathode
V_F Temperature Coefficient, T_C		−2.20		mV/°C	Anode to cathode
DIGITAL INPUTS					
Input Current		±5	±10	µA	
Input Low Voltage			0.2 × DV_{CC}	V	
Input High Voltage	0.8 × DV_{CC}			V	
Input Hysteresis (SCLK and $\overline{SYNC}$ Only)		200		mV	
Input Capacitance			10	pF	
POWER SUPPLY VOLTAGES					
V_{PP}	(51 × REF_IN) + 2.5		225	V	
V_+	4.75		5.25	V	
AV_{CC}	4.75		5.25	V	
DV_{CC}	2.7		5.25	V	
POWER SUPPLY CURRENTS[8]					
I_{VPP}					
All Channels at Full-Scale		80	92	µA/channel	
All Channels at Zero-Scale		45	55	µA/channel	
I_{V+}		0.75	0.9	mA	
I_{AVCC}		17.5	20	mA	
I_{DVCC}		0.25	0.6	mA	

[1] See the Terminology section.

[2] Linear output voltage range: 7 V to V_{PP} – 1.5 V or 51 x REF_IN (whichever is less)

[3] Outputs unloaded.

[4] Linear output voltage range: 7 V to V_{PP} – 1.5 V or 51 x REF_IN (whichever is less)

[5] Ensure that T_J max is not exceeded. See the Absolute Maximum Ratings section.

[6] Output shorts to ground increase the on-chip power dissipation and therefore the chip junction temperature. Operation at or above the specified maximum operation junction temperature may impair device reliability

[7] Reference input determines output voltage range. The linear output voltage range is restricted from 7 V to V_{PP} – 1.5 V. or 51 x REF_IN (whichever is less)

[8] Outputs unloaded

SPECIFICATIONS

TIMING CHARACTERISTICS

V_{PP} = 55 V to 225 V; 4.75 ≤ V_+ ≤ 5.25 V; 4.75V ≤ AV_{CC} ≤ 5.25 V; 2.7 V ≤ DV_{CC} ≤ 5.25V;PGND=AGND=DGND=DAC_GND =0V; AV_{CC} and V_+ must exceed REF_IN by 1.15 V minimum; 1V ≤ REF_IN ≤ 4.096 V; −10°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 2.

Parameter[1, 2, 3]	Max	Min	Unit	Test Conditions/Comments
f_{UPDATE}	1.2		MHz	Channel update rate
f_{CLKIN}	30		MHz	SCLK frequency
t_1		13	ns	SCLK high pulse width
t_2		13	ns	SCLK low pulse width
t_3		15	ns	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_4		50	ns	$\overline{SYNC}$ low time
t_5		10	ns	$\overline{SYNC}$ high time
t_6		10	ns	D_{IN} setup time
t_7		5	ns	D_{IN} hold time
t_8		200	ns	19^{th} SCLK falling edge to $\overline{SYNC}$ falling edge for next write
t_9		20	ns	$\overline{RESET}$pulse width

1 See Figure 2.

2 Guaranteed by design and characterization, not production tested.

3 All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

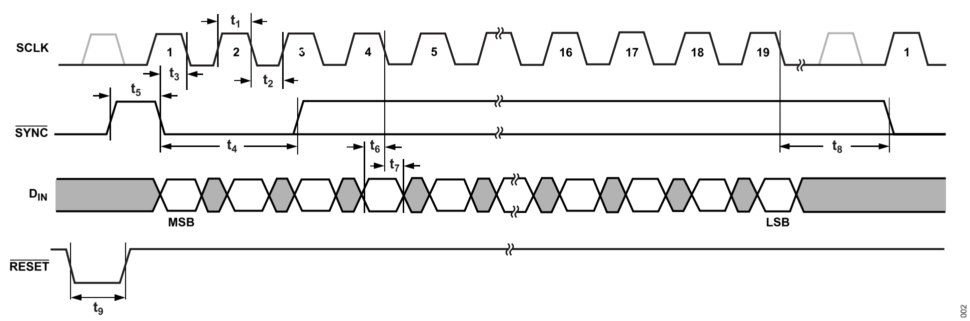


Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{PP} to AGND	−0.3 V to 240 V
V_+ to AGND	−0.3 V to +7 V
AV_{CC} to AGND, DAC_GND	−0.3 V to +7 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DVCC + 0.3 V or +7 V (whichever is less)
REF_IN to AGND, DAC_GND	−0.3 V to AVCC + 0.3 V or +7 V (whichever is less)
V_{OUT}0 to V_{OUT}31 to AGND	–0.3 V to V_{PP} + 0.3 V
ANODE/CATHODE to AGND, DAC_GND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range	
Industrial	−10°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
124-Lead CSP_BGA Package, $θ_{JA}$ Thermal Impedance	40°C/W
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD	
Human Body Model	2.5 kV
Field Induced Charged Device Model	400 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Transient currents of up to 100 mA do not cause SCR latch-up.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

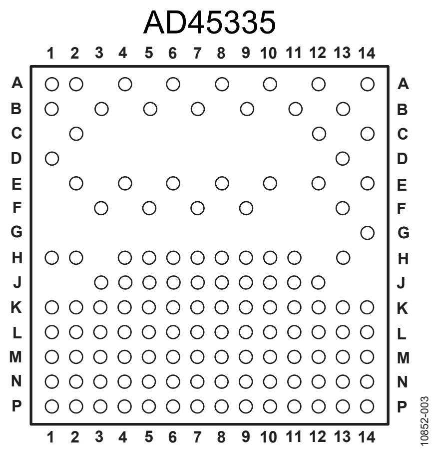


Figure 3. Pin Configuration

Table 4. Pin Assignments

Pin No.	Mnemonic
A1	NC
A2	$V_{OUT}1$
A4	$V_{OUT}7$
A6	$V_{OUT}11$
A8	$V_{OUT}16$
A10	$V_{OUT}20$
A12	$V_{OUT}25$
A14	NC
B1	$V_{OUT}0$
B3	$V_{OUT}4$
B5	$V_{OUT}9$
B7	$V_{OUT}13$
B9	$V_{OUT}17$
B11	$V_{OUT}21$
B13	$V_{OUT}26$
C2	$V_{OUT}3$
C12	$V_{OUT}22$
C14	$V_{OUT}29$
D1	$V_{OUT}2$
D13	$V_{OUT}23$
E2	$V_{OUT}5$
E4	$V_{OUT}8$
E6	$V_{OUT}12$
E8	$V_{OUT}15$
E10	$V_{OUT}19$
E12	$V_{OUT}24$
E14	$V_{OUT}31$
F3	$V_{OUT}6$
F5	$V_{OUT}10$
F7	$V_{OUT}14$
F9	$V_{OUT}18$
F13	$V_{OUT}30$

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 4. Pin Assignments (Continued)

Pin No.	Mnemonic
G14	$V_{OUT}28$
H1	V_{PP}
H2	V_{PP}
H4 to H11	AGND
H13	$V_{OUT}27$
J3 to J12	AGND
K1	V_+
K2	V_+
K3 to K14	AGND
L1	NC
L2	NC
L3 to L13	AGND
L14	DAC_GND
M1 to M12	AGND
M13	AV_{CC}
M14	AV_{CC}
N1	PGND
N2	PGND
N3	CATHODE
N4	ANODE
N5 to N14	AGND
P1	NC
P2	REF_IN
P3	DAC_GND
P4	$\overline{\text{RESET}}$
P5	DV_{CC}
P6	DGND
P7	TEST
P8	D_{IN}
P9	SCLK
P10	$\overline{\text{SYNC}}$
P11 to P13	AGND
P14	NC

Table 5. Pin Function Descriptions

Mnemonic	Description
AGND	Analog GND Pins.
AV_{CC}	Analog Supply Pins.
V_{PP}	Output Amplifier High Voltage Supply.
V_+	V_+ Amplifier Supply Pins.
PGND	Output Amplifier Ground Reference Pins.
DGND	Digital GND Pins.
DV_{CC}	Digital Supply Pins.
DAC_GND	Reference GND Supply for All DACs.
REF_IN	Reference Voltage for Channel 0 to Channel 31.
$V_{OUT}0$ to $V_{OUT}31$	Analog Output Voltages from the 32 Channels.
ANODE	Anode of Internal Diode for Diode Temperature Measurement.
CATHODE	Cathode of Internal Diode for Diode Temperature Measurement.
$\overline{\text{SYNC}}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in upon the falling edge of SCLK.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions (Continued)

Mnemonic	Description
SCLK	Serial Clock Input. Data is clocked into the shift register upon the falling edge of SCLK. The pin operates at clock speeds of up to 30 MHz. Internal pull-up device on logic input; therefore, it can be left floating and defaults to a logic high condition.
D_{IN}	Serial Data Input. Data must be valid upon the falling edge of SCLK.
TEST	For normal operation, tie this pin low.
$\overline{RESET}$	Active Low Input. This pin can also be used to reset the complete device to its power-on reset conditions. Zero code is loaded to the DACs.
NC	No Connect. Do not connect to these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

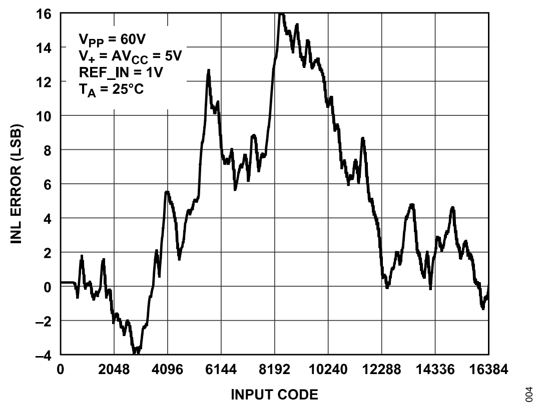


Figure 4. Integral Nonlinearity (INL) with Full-Scale Range = 50 V

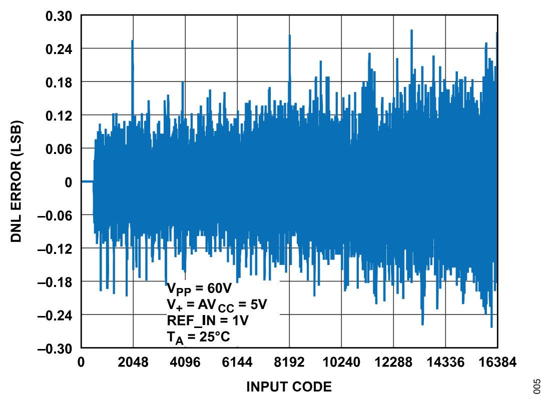


Figure 5. Differential Nonlinearity (DNL) with Full-Scale Range = 50 V

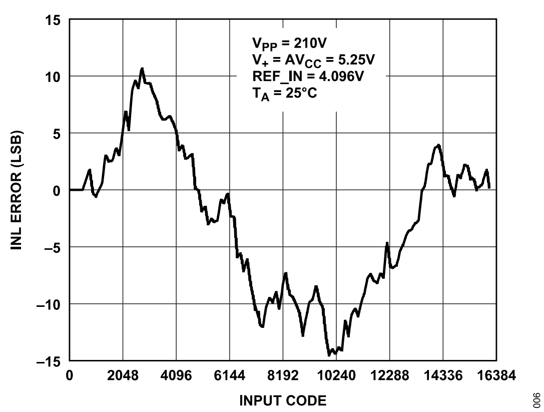


Figure 6. INL with Full-Scale Range = 200 V

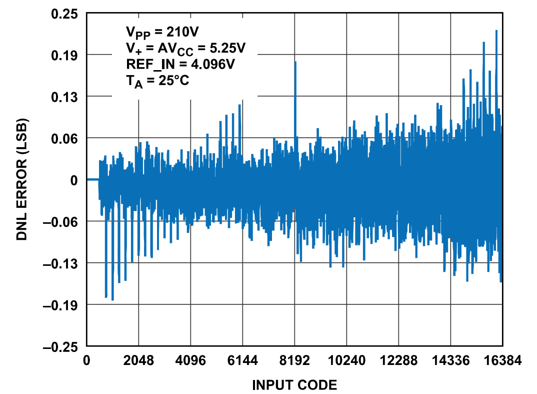


Figure 7. DNL with Full-Scale Range = 200 V

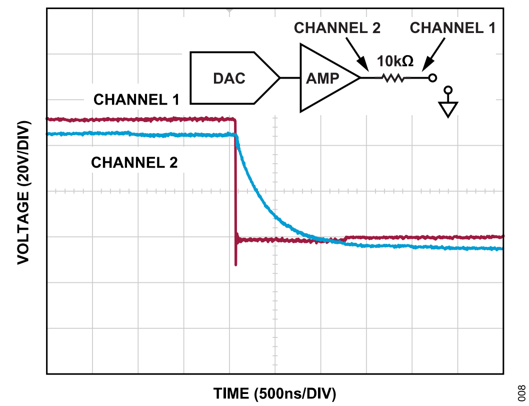


Figure 8. Short-Circuit Current Limit Timing

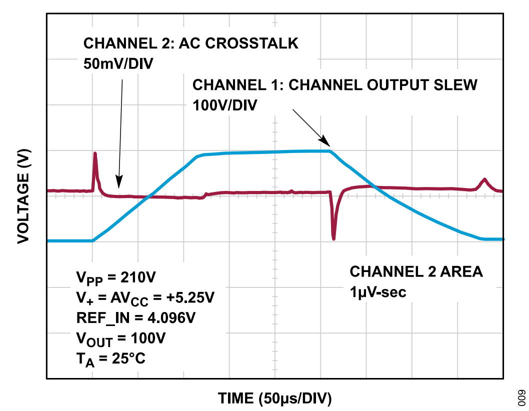


Figure 9. Worst-Case Adjacent Channel Crosstalk

TYPICAL PERFORMANCE CHARACTERISTICS

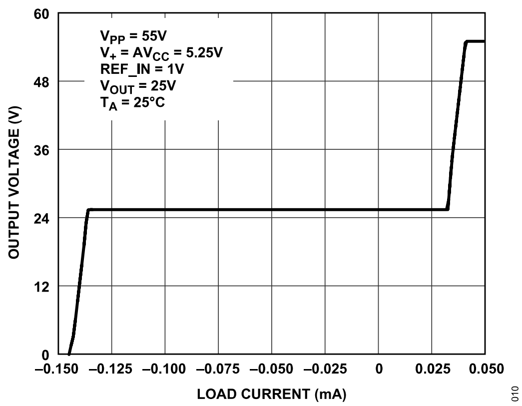


Figure 10. Output Amplifier Source and Sink Capability

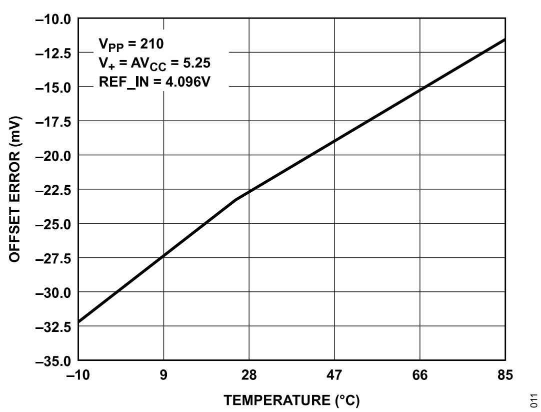


Figure 11. Offset Error vs. Temperature

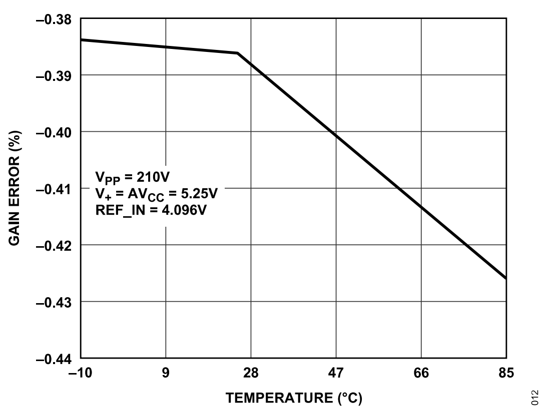


Figure 12. Gain Error vs. Temperature

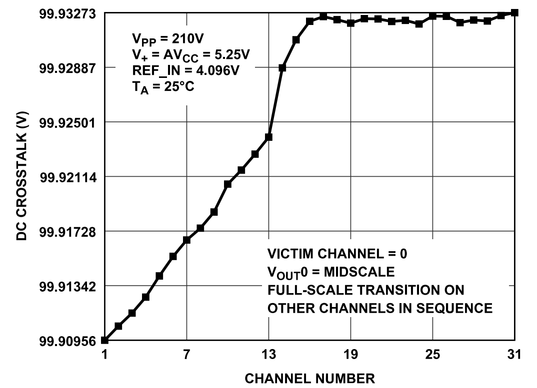


Figure 13. Cumulative DC Crosstalk Effects on a Single-Channel Output, Switching All Other Channels in Sequence

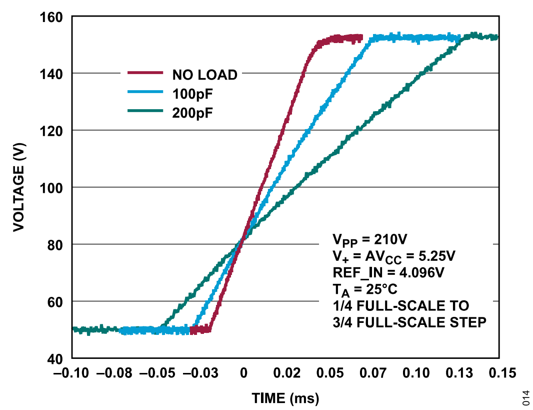


Figure 14. Settling Time vs. Capacitive Load Rising Edge

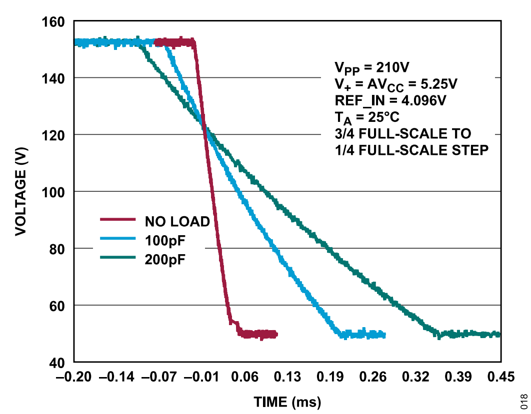


Figure 15. Settling Time vs. Capacitive Load Falling Edge

TERMINOLOGY

Integral Nonlinearity (INL)

A measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is expressed as a percentage of full-scale range.

Differential Nonlinearity (DNL)

The difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity.

Zero Code Voltage

A measure of the output voltage present at the device output with all 0s loaded to the DAC. It includes the offset of the DAC and the output amplifier and is expressed in V.

Offset Error

Calculated by taking two points in the linear region of the transfer function, drawing a line through these points, and extrapolating back to the y-axis. It is expressed in V.

Voltage Gain

Calculated from the change in output voltage for a change in code, multiplied by 16,384, and divided by the REF_IN voltage. This is calculated between two points in the linear section of the transfer function.

Gain Error

A measure of the output error with all 1s loaded to the DAC, and the difference between the ideal and actual analog output range. Ideally, the output should be 50 × REF_IN. It is expressed as a percentage of full-scale range.

DC Power Supply Rejection Ratio (PSRR)

A measure of the change in analog output for a change in V_{PP} supply voltage. It is expressed in dB, and V_{PP} is varied ±5%.

DC Crosstalk

The dc change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) and the output change of all other DACs. It is expressed in LSB.

Output Voltage Settling Time

The time taken from when the last data bit is clocked into the DAC until the output has settled to within ±0.5 LSB of its final value. Measured for a step change of ¼ to ¾ full scale.

Digital-to-Analog Glitch Impulse

The area of the glitch injected into the analog output when the code in the DAC register changes state. It is specified as the area of the glitch in nV-sec when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Analog Crosstalk

The area of the glitch transferred to the output (V_{OUT}) of one DAC due to a full-scale change in the output (V_{OUT}) of another DAC. The area of the glitch is expressed in nV-sec.

Digital Feedthrough

A measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to ($\overline{SYNC}$ is high). It is specified in nV-sec and measured with a worst-case change on the digital input pins, for example, from all 0s to all 1s and vice versa.

Output Noise Spectral Density

A measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in μV/√Hz.

THEORY OF OPERATION

The AD45335 consists of a 32-channel, 14-bit DAC with 200 V high voltage amplifiers in a single 15 mm × 15 mm CSP_BGA package. The output voltage range is programmable via the REF_IN pin. The output range is 0 V to 50 V when REF_IN = 1 V, and 0 V to 200 V when REF_IN = 4 V. Communication to the device is through a serial interface operating at clock rates of up to 30 MHz, which is compatible with DSP and microcontroller interface standards. A 5-bit address and a 14-bit data-word are loaded into the AD45335 input register via the serial interface. The channel address is decoded, and the data-word is converted into an analog output voltage for this channel.

At power-on, all the DAC registers are loaded with 0s.

DAC SECTION

The architecture of each DAC channel consists of a resistor string DAC, followed by an output buffer amplifier operating with a nominal gain of 50. The voltage at the REF_IN pin provides the reference voltage for the corresponding DAC. The input coding to the DAC is straight binary, and the ideal DAC output voltage is given by

$$V_{OUT} = \frac{50 \times V_{REF\_IN} \times D}{2^{14}}$$

where D is the decimal equivalent (0 to 16,383) of the binary code, which is loaded to the DAC register.

The output buffer amplifier is specified to drive a load of 4 MΩ and 200 pF. The linear output voltage range for the output amplifier is from 7 V to V_{PP} – 1.5 V. The amplifier output bandwidth is typically 30 kHz, and is capable of sourcing 150 μA and sinking 40 μA.

RESET FUNCTION

The reset function on the AD45335 can be used to reset all nodes on the device to their power-on reset condition. All the DACs are loaded with 0s, and all registers are cleared. Take the $\overline{\text{RESET}}$ pin low to implement the reset function.

SERIAL INTERFACE

The serial interface is controlled by the three following pins:

$\overline{\text{SYNC}}$, which is the frame synchronization pin for the serial interface.

SCLK, which is the serial clock input that operates at clock speeds of up to 30 MHz.

D_{IN}, which is the serial data input and data must be valid upon the falling edge of SCLK.

To update a single DAC channel, a 19-bit data-word is written to the AD45335 input register, as shown in Figure 16.

A4 to A0 Bits

The A4 to A0 bits can address any one of the 32 channels. A4 is the MSB of the address, while A0 is the LSB.

DB13 to DB0 Bits

The DB13 to DB0 bits are used to write a 14-bit data-word into the addressed DAC register.

Figure 2 is the timing diagram for a serial write to the AD45335. The serial interface works with both a continuous and a discontinuous serial clock. The first falling edge of SYNC resets the serial clock counter to ensure that the correct number of bits are shifted into the serial shift register. Any further edges on $\overline{\text{SYNC}}$ are ignored until the correct number of bits are shifted in. After 19 bits are shifted in, the SCLK is ignored. For another serial transfer to take place, the counter must be reset by the falling edge of SYNC. The user must allow 200 ns (minimum) between successive writes.

MSB					LSB
A4	A3	A2	A1	A0	DB13 TO DB0

015

Figure 16. Serial Data Format

APPLICATIONS INFORMATION

MEMS MIRROR CONTROL APPLICATION

The AD45335 is targeted to all optical switching control systems based on MEMS technology. The AD45335 is a 32-channel, 14-bit DAC with integrated high voltage amplifiers. The output amplifiers are capable of generating an output range of 0 V to 200 V when using a 4 V reference. The full-scale output voltage is programmable from 50 V to 200 V using reference voltages from 1 V to 4 V. Each amplifier can output 150 µA sourcing current and directly drives the control actuators, which determine the position of MEMS mirrors in optical switch applications.

The AD45335 is generally used in a closed-loop feedback system, as shown in Figure 17, with a high resolution ADC and DSP. The exact position of each mirror is measured using capacitive sensors. The sensor outputs are multiplexed using an ADG739 4-to-1 multiplexer to an 8-channel, 14-bit ADC (AD7856). An alternative solution is to multiplex using a 32-to-1 multiplexer (ADG732) into a single-channel ADC (AD7671). With 14-bit monotonic behavior and a 0 V to 200 V output range, coupled with its fast serial interface, the AD45335 is ideally suited for controlling a cluster of MEMS-based mirrors.

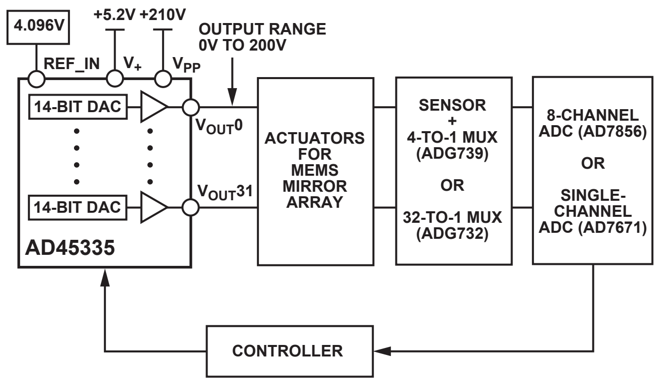


Figure 17. AD45335 in a MEMS-Based Optical Switch

APPLICATIONS INFORMATION

IPC-221-COMPLIANT BOARD LAYOUT

The diagram in Figure 18 is a typical 2-layer printed circuit board (PCB) layout for the AD45335 that complies with the specifications outlined in IPC-221. Do not connect to the four corner balls labeled as original no connects. Connect balls labeled as additional no connects to AGND.

The routing shown in Figure 18 shows the feasibility of connecting to the high voltage balls while complying with the spacing requirements of IPC-221. Figure 18 also shows the physical distances that are available.

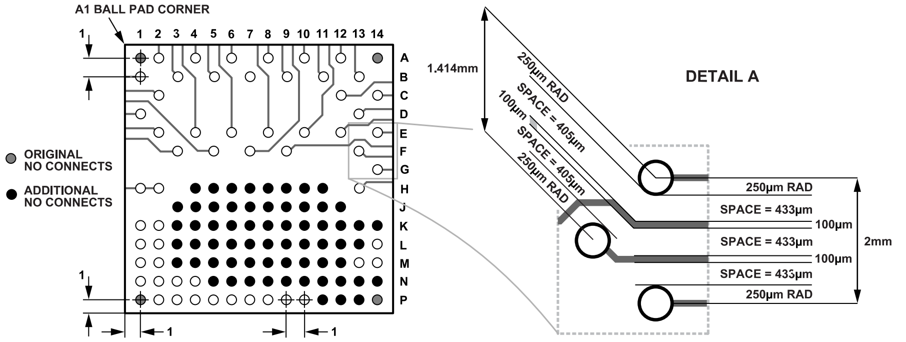


Figure 18. Layout Guidelines to Comply with IPC-221

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING RECOMMENDATIONS

On the AD45335, it is recommended to tie all grounds together as close to the device as possible. If the number of supplies must be reduced, bring all supplies back separately and make a provision on the board via a link option to drive the AV_{CC} and V_+ pins from the same supply. Decouple all power supplies adequately with 10 μF tantalum capacitors and 0.1 μF ceramic capacitors.

GUIDELINES FOR PCB LAYOUT

Design printed circuit boards such that the analog and digital sections are separated and confined to the designated analog and digital sections of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally the best for ground planes because it optimizes shielding of sensitive signal lines. Join digital and analog ground planes in one place only, at the AGND and DGND pins of the high resolution converter. To isolate the high frequency bus of the processor from the bus of the high resolution converters, buffer or latch data and address buses on the board. These act as a Faraday shield and increase the signal-to-noise performance of the converters by reducing the amount of high frequency digital coupling. Avoid running digital lines under the device because they couple noise onto the die. Allow the ground plane to run under the IC to avoid noise coupling.

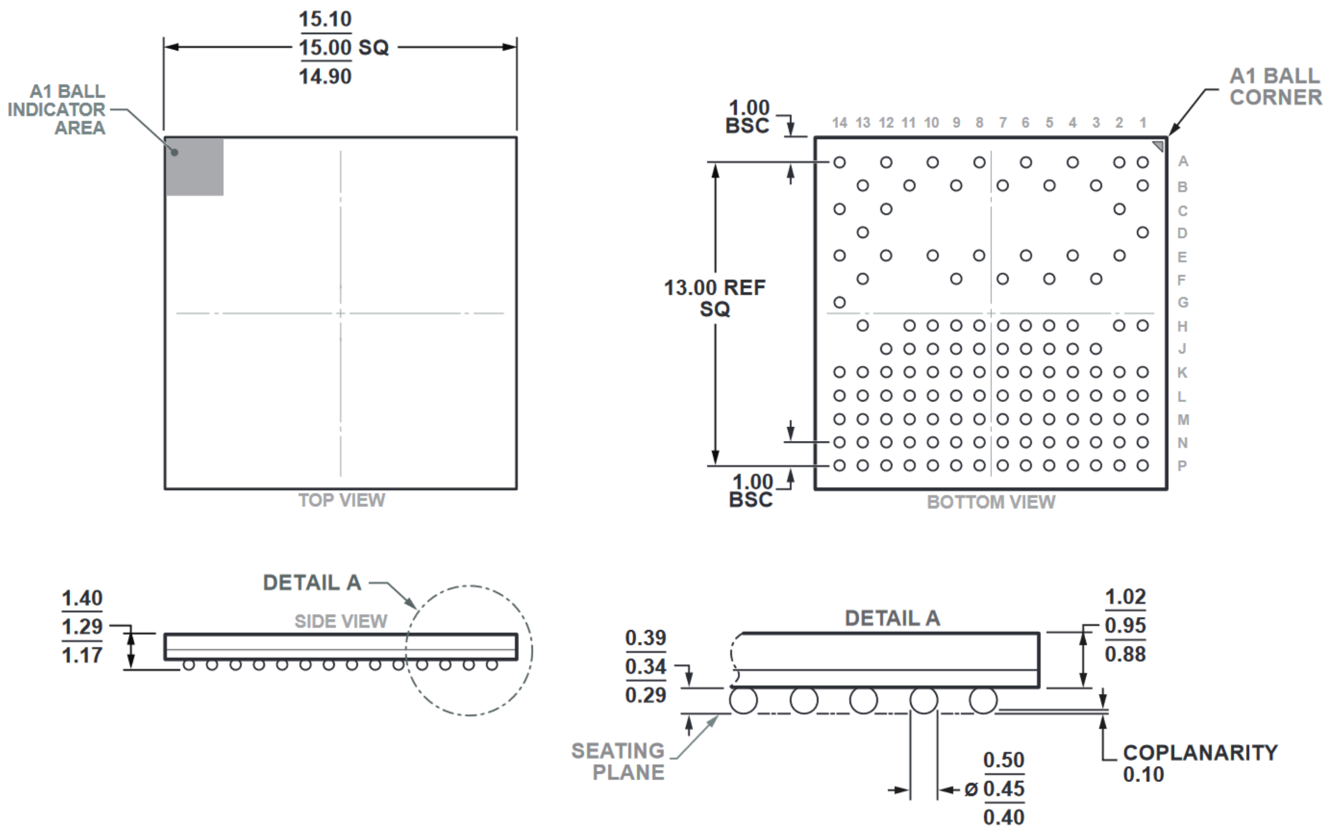
Use as large a trace as possible for the supply lines of the device to provide low impedance paths and reduce the effects of glitches on the power supply line. Shield components, such as clocks with fast-switching signals, with digital ground to avoid radiating noise to other sections of the board. Never run clock signals near the analog inputs of the device. Avoid crossovers of digital and analog signals. Keep traces for analog inputs as wide and short as possible and shield with analog ground if possible. Run traces on opposite sides of the 2-layer PCB at right angles to each other to reduce the effects of feedthrough through the board.

A microstrip technique is by far the best, but it is not always possible to use with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side. Multilayer printed circuit boards with dedicated ground, power, and tracking layers offer the optimum solution in terms of obtaining analog performance, but at increased manufacturing costs.

Good decoupling is vitally important when using high resolution converters. Decouple all analog supplies with 10 μF tantalum capacitors in parallel with 0.1 μF ceramic capacitors to analog ground. To achieve the best results from the decoupling components, place them as close to the device as possible, ideally right up against the IC or the IC socket. The main aim of a bypassing element is to maximize the charge stored in the bypass loop while simultaneously minimizing the inductance of this loop. Inductance in the loop acts as an impedance to high frequency transients and results in power supply spiking. By keeping the decoupling as close to the device as possible, the loop area is kept as small as possible, thereby reducing the possibility of power supply spikes. Decouple digital supplies of high resolution converters with 10 μF tantalum capacitors and 0.1 μF ceramic capacitors to the digital ground plane. Decouple the V_+ supply with a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor to AGND.

Decouple all logic chips with 0.1 μF ceramic capacitors to digital ground to decouple high frequency effects associated with digital circuitry.

OUTLINE DIMENSIONS



COMPLIANT WITH JEDEC STANDARDS MO-192-DAE-1

Figure 19. 124-Lead Chip Scale Package Ball Grid Array [CSP_BGA] (BC-124-4) Dimensions shown in millimeters