



RF LDMOS Wideband Integrated Power Amplifiers

The A2I20D020N wideband integrated circuit is designed with on-chip matching that makes it usable from 1400 to 2200 MHz. This multi-stage structure is rated for 20 to 32 V operation and covers all typical cellular base station modulation formats.

1800–2200 MHz

- Typical Single-Carrier W-CDMA Characterization Performance:
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQ1(A+B)} = 32 \text{ mA}$, $I_{DQ2(A+B)} = 110 \text{ mA}$, $P_{out} = 2.5 \text{ W Avg.}$,
 Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.⁽¹⁾

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
1800 MHz	31.0	19.7	-44.3
1900 MHz	31.0	21.7	-45.0
2000 MHz	31.1	22.1	-45.2
2100 MHz	31.4	21.1	-45.2
2200 MHz	32.0	19.6	-44.8

1. All data measured in fixture with device soldered to heatsink.

Features

- Extremely wide RF bandwidth
- RF decoupled drain pins reduce overall board space
- On-chip matching (50 ohm input, DC blocked)
- Integrated quiescent current temperature compensation with enable/disable function ⁽²⁾

A2I20D020NR1
A2I20D020GNR1

1400–2200 MHz, 2.5 W AVG., 28 V
AIRFAST RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

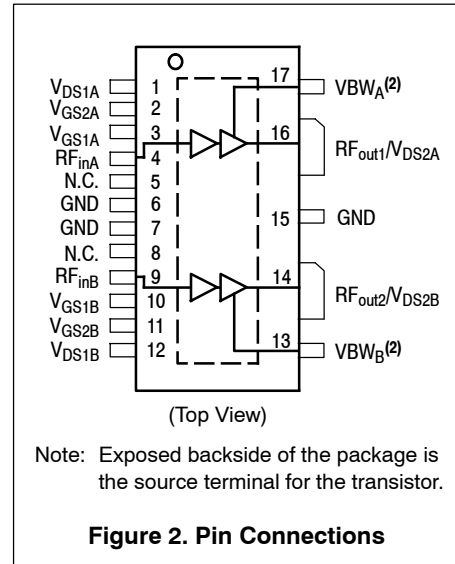
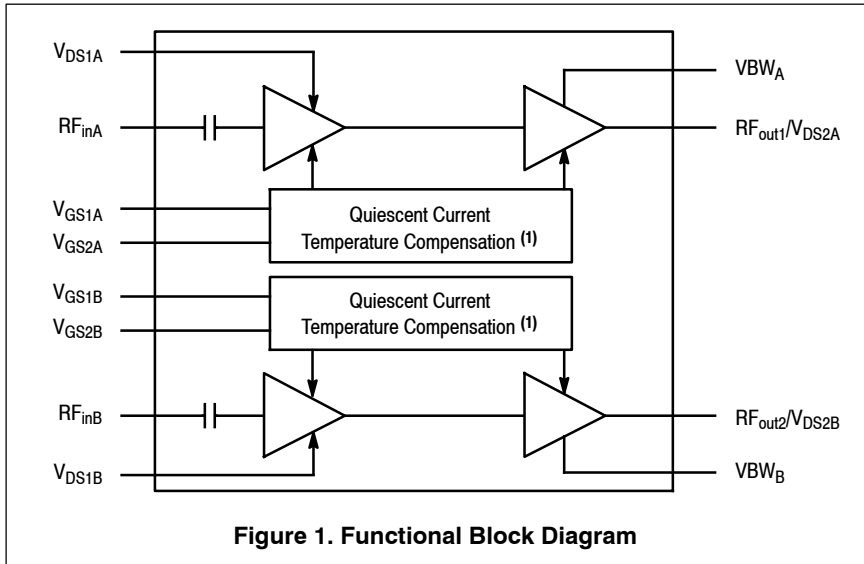
TO-270WB-17
PLASTIC
A2I20D020NR1



TO-270WBG-17
PLASTIC
A2I20D020GNR1



2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.nxp.com/RF>. Select Documentation/Application Notes - AN1977 or AN1987.



1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.nxp.com/RF> and search for AN1977 or AN1987.

2. Device can operate with V_{DD} current supplied through pin 13 and pin 17.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (3,4)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (4,5)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 2.5 W, 2000 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)} = 30$ mA Stage 2, 28 Vdc, $I_{DQ2(A+B)} = 110$ mA	$R_{\theta JC}$	7.8 2.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

3. Continuous use at maximum temperature will affect MTTF.

4. MTTF calculator available at <http://www.nxp.com/RF/calculators>.

5. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 - Off Characteristics ⁽¹⁾					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μA
Gate-Source Leakage Current ($V_{GS} = 1.0\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μA
Stage 1 - On Characteristics					
Gate Threshold Voltage ⁽¹⁾ ($V_{DS} = 10\text{ Vdc}$, $I_D = 2\text{ }\mu\text{A}$)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_{DQ1(A+B)} = 32\text{ mA}$)	$V_{GS(Q)}$	—	1.9	—	Vdc
Fixture Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_{DQ1(A+B)} = 32\text{ mA}$, Measured in Functional Test)	$V_{GG(Q)}$	7.5	8.2	9.0	Vdc
Stage 2 - Off Characteristics ⁽¹⁾					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μA
Gate-Source Leakage Current ($V_{GS} = 1.0\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μA
Stage 2 - On Characteristics					
Gate Threshold Voltage ⁽¹⁾ ($V_{DS} = 10\text{ Vdc}$, $I_D = 11\text{ }\mu\text{A}$)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_{DQ2(A+B)} = 110\text{ mA}$)	$V_{GS(Q)}$	—	1.8	—	Vdc
Fixture Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_{DQ2(A+B)} = 110\text{ mA}$, Measured in Functional Test)	$V_{GG(Q)}$	4.1	4.8	5.6	Vdc
Drain-Source On-Voltage ⁽¹⁾ ($V_{GS} = 10\text{ Vdc}$, $I_D = 200\text{ mA}$)	$V_{DS(on)}$	0.1	0.3	1.5	Vdc

1. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ^(1,2) (In NXP Production Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ1(A+B)} = 32\text{ mA}$, $I_{DQ2(A+B)} = 110\text{ mA}$, $P_{out} = 2.5\text{ W Avg.}$, $f = 1900\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	30.2	31.0	35.0	dB
Power Added Efficiency	PAE	20.3	21.2	—	%
Adjacent Channel Power Ratio	ACPR	—	-44.0	-43.0	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	19.5	22.2	—	W

Load Mismatch (In NXP Production Test Fixture, 50 ohm system) $I_{DQ1(A+B)} = 32\text{ mA}$, $I_{DQ2(A+B)} = 110\text{ mA}$, $f = 2200\text{ MHz}$

VSWR 10:1 at 32 Vdc, 46.8 W CW Output Power (3 dB Input Overdrive from 40.7 W CW Rated Power)	No Device Degradation
--	-----------------------

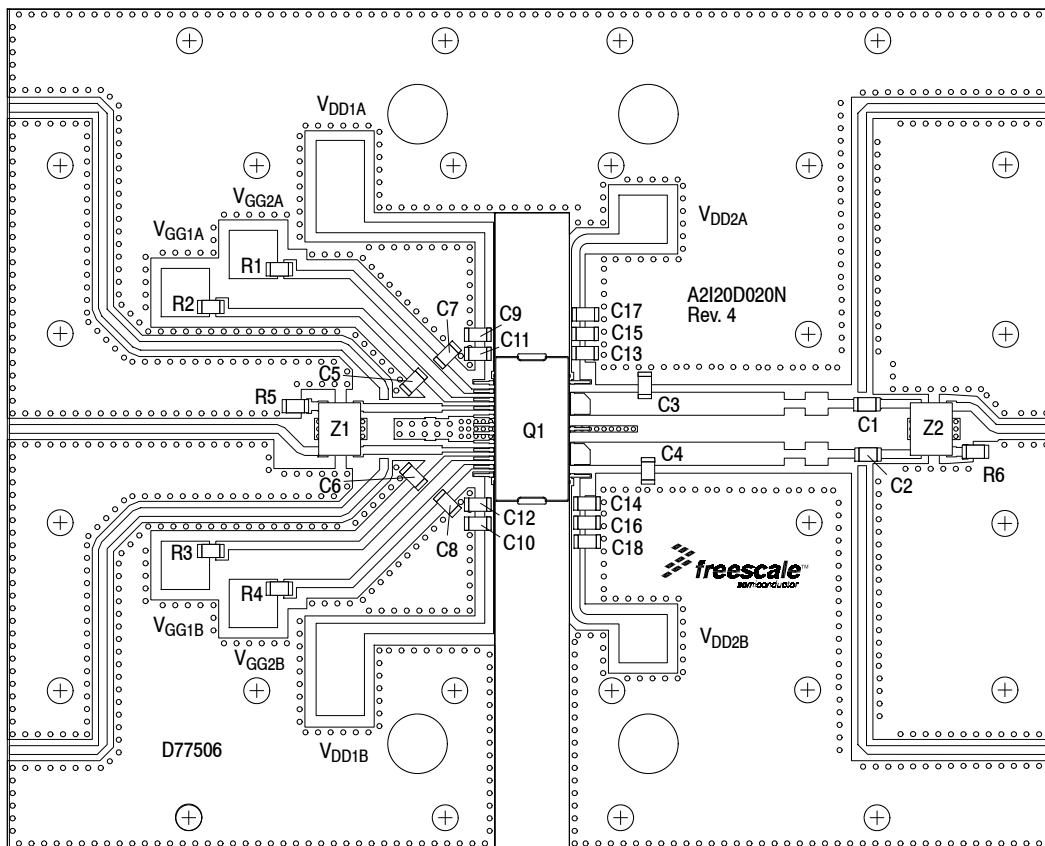
Typical Performance ⁽³⁾ (In NXP Characterization Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ1(A+B)} = 32\text{ mA}$, $I_{DQ2(A+B)} = 110\text{ mA}$, 1800–2200 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	16	—	W
P_{out} @ 3 dB Compression Point ⁽⁴⁾	P3dB	—	24	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1800–2200 MHz frequency range.)	Φ	—	-7.6	—	$^\circ$
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	170	—	MHz
Quiescent Current Accuracy over Temperature ⁽⁵⁾ with 4.7 k Ω Gate Feed Resistors (-30 to 85°C) Stage 1 with 4.7 k Ω Gate Feed Resistors (-30 to 85°C) Stage 2	ΔI_{QT}	—	2.7 1.9	—	%
Gain Flatness in 400 MHz Bandwidth @ $P_{out} = 2.5\text{ W Avg.}$	G_F	—	1.0	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.023	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.015	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I20D020NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-Reel	TO-270WB-17
A2I20D020GNR1		TO-270WBG-17

- Part internally input and output matched.
- Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
- All data measured in fixture with device soldered to heatsink.
- $P3dB = P_{avg} + 7.0\text{ dB}$ where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
- Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.nxp.com/RF> and search for AN1977 or AN1987.



Note: All data measured in fixture with device soldered to heatsink. Production fixture does not include device soldered to heatsink.

Figure 3. A2120D020NR1 Test Circuit Component Layout

Table 7. A2120D020NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	3.9 pF Chip Capacitors	ATC600F3R9BT250XT	ATC
C3, C4	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C5, C6, C7, C8	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C9, C10, C11, C12, C13, C14, C15, C16, C17, C18	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
Q1	RF LDMOS Power Amplifier	A2120D020N	NXP
R1, R2, R3, R4	4.7 kΩ, 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
R5, R6	50 Ω, 10 W Chip Resistors	060120A15Z50-2	Anaren
Z1, Z2	1700–2300 MHz, 90°, 3 dB Hybrid Couplers	X3C19P1-03S	Anaren
PCB	Rogers RO4350B, 0.020", ε _r = 3.66	D77506	MTL

TYPICAL CHARACTERISTICS — 1800–2200 MHz

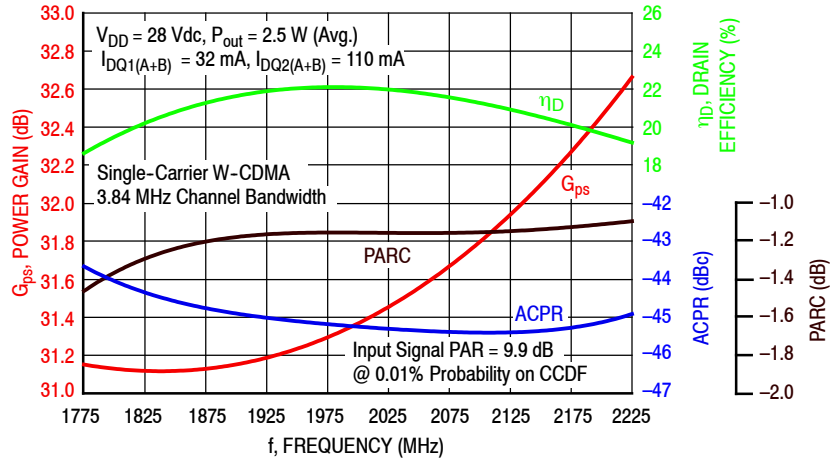


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 2.5$ Watts Avg.

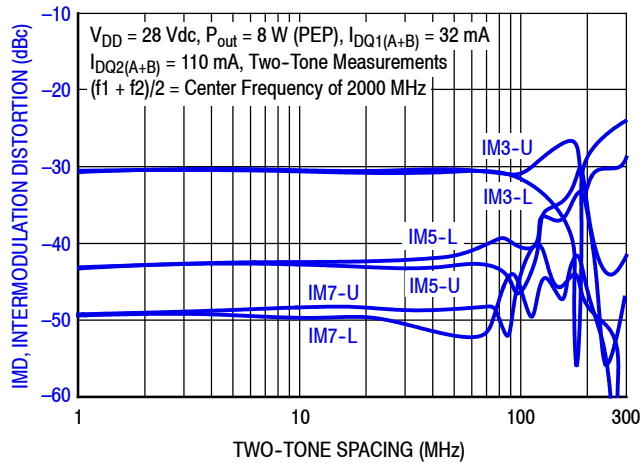


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

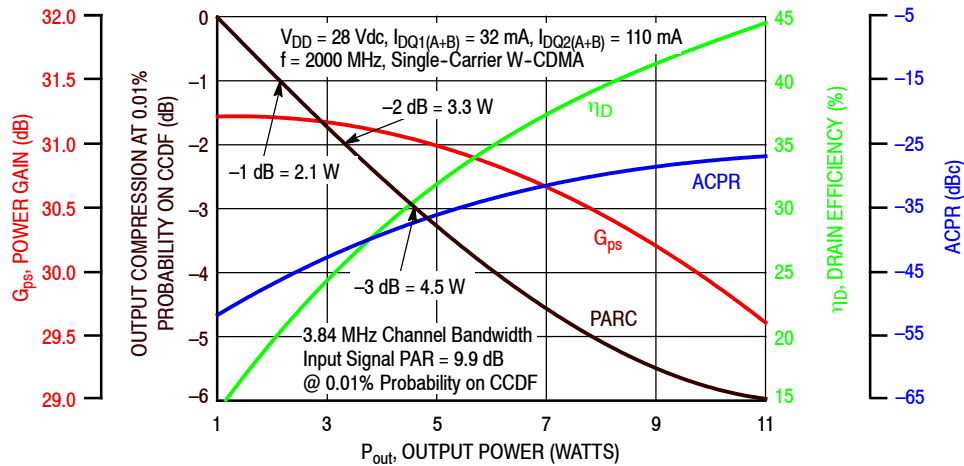


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1800–2200 MHz

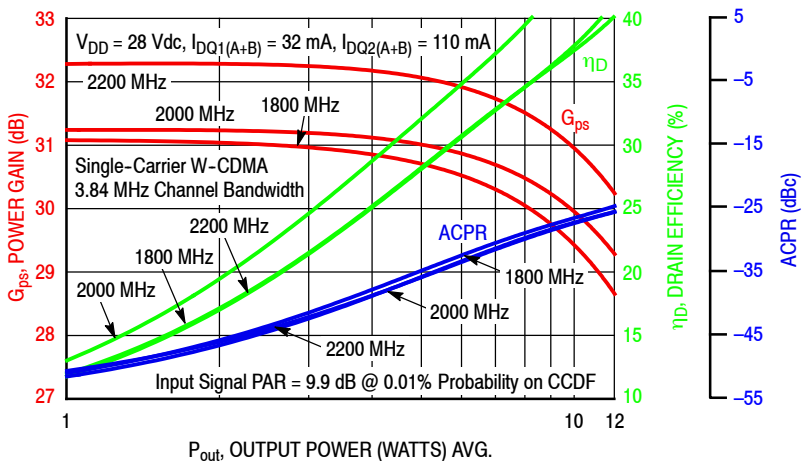


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

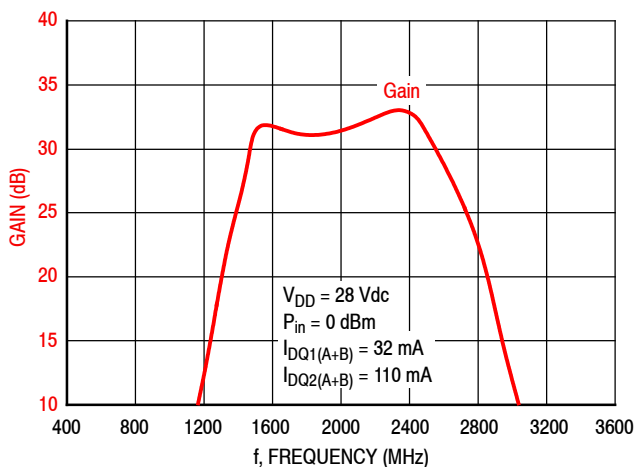


Figure 8. Broadband Frequency Response

Table 8. Load Pull Performance — Maximum Power Tuning

$V_{DD} = 28$ Vdc, $I_{DQ1} = 16$ mA, $I_{DQ2} = 57$ mA, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
1805	92.7 + j84.9	72.9 – j80.3	21.8 – j4.48	31.6	40.6	11	54.5	–3
1840	70.5 + j83.3	62.6 – j79.4	19.0 – j6.17	31.4	40.6	11	52.5	–3
1880	53.3 + j79.4	50.7 – j74.5	17.9 – j5.52	31.3	40.6	12	51.6	–3

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
1805	92.7 + j84.9	71.2 – j79.5	20.1 – j7.48	29.3	41.5	14	53.7	–6
1840	70.5 + j83.3	61.5 – j78.8	18.5 – j6.91	29.3	41.5	14	52.8	–6
1880	53.3 + j79.4	50.1 – j73.8	17.5 – j6.54	29.2	41.5	14	51.8	–5

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 9. Load Pull Performance — Maximum Efficiency Tuning

$V_{DD} = 28$ Vdc, $I_{DQ1} = 16$ mA, $I_{DQ2} = 57$ mA, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
1805	92.7 + j84.9	73.1 – j84.4	41.8 + j7.22	32.9	39.0	8	61.7	–5
1840	70.5 + j83.3	62.4 – j82.2	32.6 + j4.15	32.6	39.4	9	59.9	–4
1880	53.3 + j79.4	50.5 – j77.9	26.6 + j12.0	33.0	38.8	8	57.5	–5

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
1805	92.7 + j84.9	72.6 – j82.9	41.0 + j3.98	30.8	40.0	10	61.1	–8
1840	70.5 + j83.3	62.5 – j81.6	30.9 + j5.87	30.6	40.3	11	59.8	–7
1880	53.3 + j79.4	50.2 – j76.9	30.1 + j10.2	30.9	39.7	9	58.1	–6

(1) Load impedance for optimum P1dB efficiency.

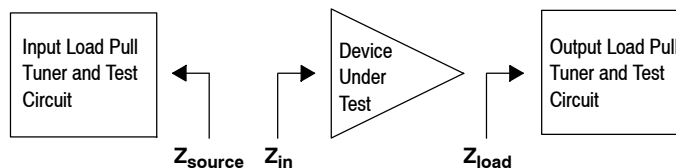
(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB - TYPICAL LOAD PULL CONTOURS — 1840 MHz

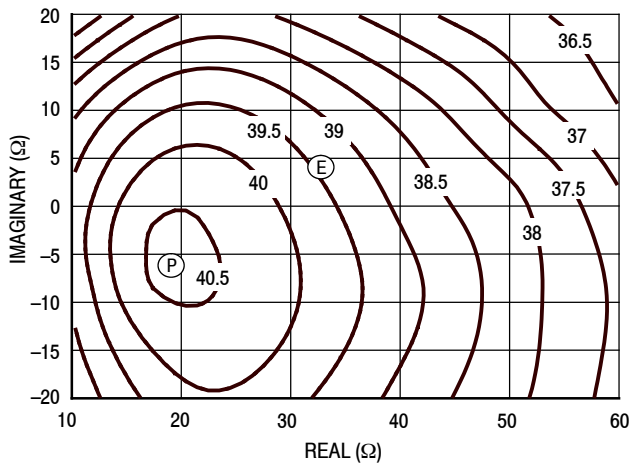


Figure 9. P1dB Load Pull Output Power Contours (dBm)

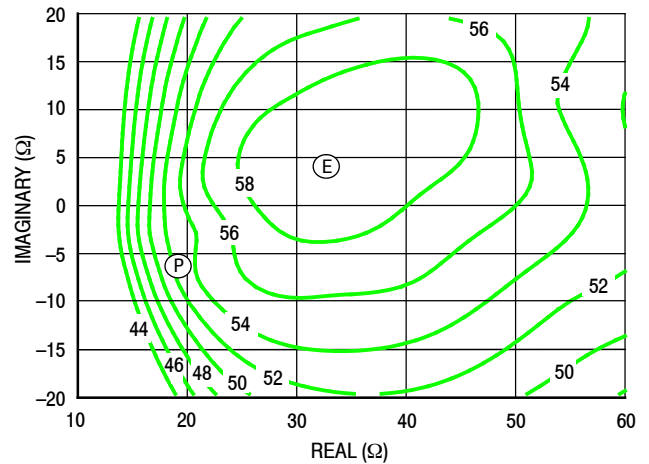


Figure 10. P1dB Load Pull Efficiency Contours (%)

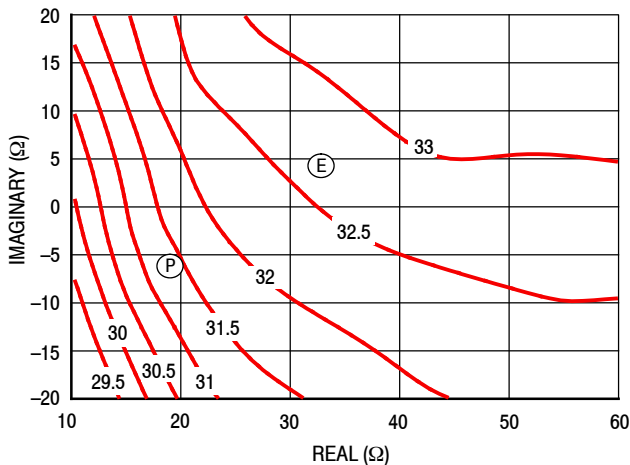


Figure 11. P1dB Load Pull Gain Contours (dB)

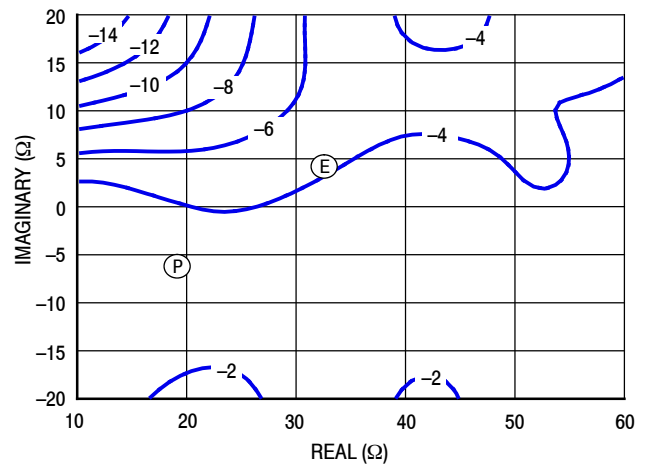


Figure 12. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 1840 MHz

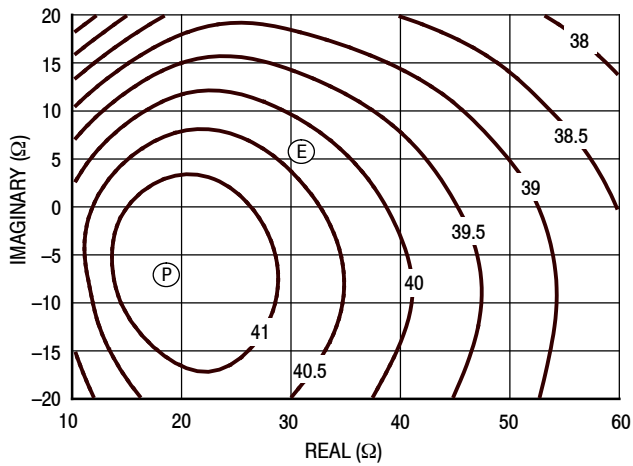


Figure 13. P3dB Load Pull Output Power Contours (dBm)

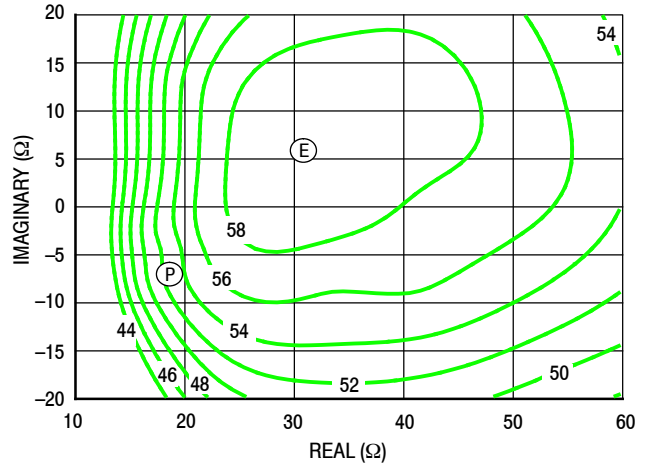


Figure 14. P3dB Load Pull Efficiency Contours (%)

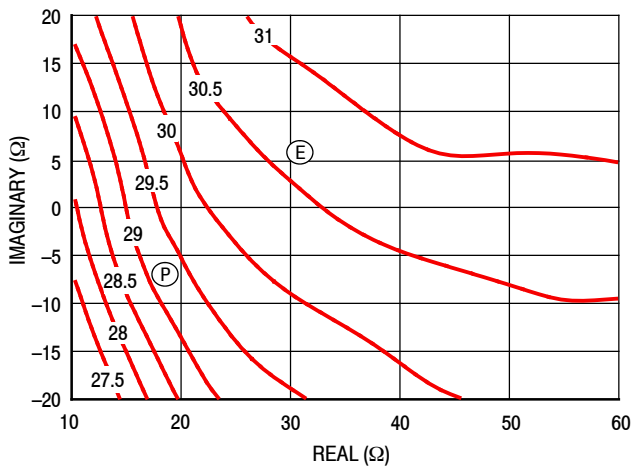


Figure 15. P3dB Load Pull Gain Contours (dB)

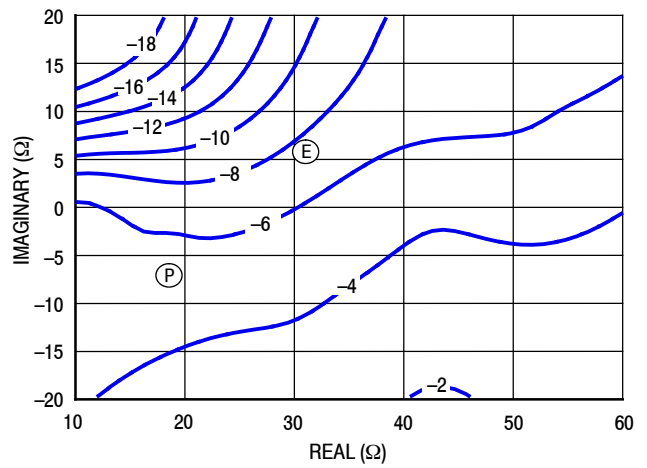


Figure 16. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

Table 10. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1} = 16 mA, I_{DQ2} = 57 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z _{source} (Ω)	Z _{in} (Ω)	Max Output Power					
			P1dB					
			Z _{load} ⁽¹⁾ (Ω)	Gain (dB)	(dBm)	(W)	η _D (%)	AM/PM (°)
2110	26.5 + j66.6	26.8 – j66.8	17.2 + j0.65	32.6	40.6	12	50.7	–4
2140	28.6 + j67.5	26.6 – j69.1	18.0 + j1.74	33.3	40.7	12	52.9	–5
2170	27.7 + j71.6	28.6 – j71.2	16.6 + j2.92	33.9	40.8	12	55.3	–5

f (MHz)	Z _{source} (Ω)	Z _{in} (Ω)	Max Output Power					
			P3dB					
			Z _{load} ⁽²⁾ (Ω)	Gain (dB)	(dBm)	(W)	η _D (%)	AM/PM (°)
2110	26.5 + j66.6	26.3 – j66.3	17.2 + j0.31	30.6	41.5	14	52.3	–7
2140	28.6 + j67.5	26.1 – j68.6	17.4 + j1.43	31.3	41.6	14	53.6	–8
2170	27.7 + j71.6	28.0 – j70.2	18.6 + j0.54	31.5	41.7	15	54.5	–9

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 11. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1} = 16 mA, I_{DQ2} = 57 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z _{source} (Ω)	Z _{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z _{load} ⁽¹⁾ (Ω)	Gain (dB)	(dBm)	(W)	η _D (%)	AM/PM (°)
2110	26.5 + j66.6	26.0 – j67.4	15.9 + j12.4	34.1	39.4	9	58.3	–5
2140	28.6 + j67.5	26.1 – j69.4	16.2 + j12.9	34.6	39.7	9	60.9	–6
2170	27.7 + j71.6	28.1 – j71.5	13.7 + j12.4	35.1	39.6	9	64.3	–8

f (MHz)	Z _{source} (Ω)	Z _{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z _{load} ⁽²⁾ (Ω)	Gain (dB)	(dBm)	(W)	η _D (%)	AM/PM (°)
2110	26.5 + j66.6	25.7 – j67.3	16.2 + j12.1	32.0	40.5	11	60.0	–7
2140	28.6 + j67.5	25.6 – j69.4	14.7 + j12.9	32.7	40.4	11	61.8	–9
2170	27.7 + j71.6	27.4 – j71.4	14.2 + j13.7	33.2	40.2	10	63.5	–11

(1) Load impedance for optimum P1dB efficiency.

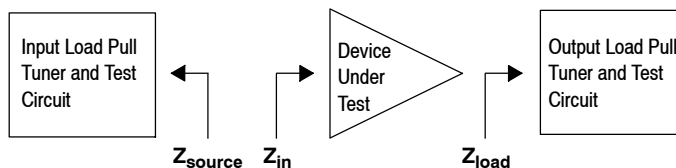
(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

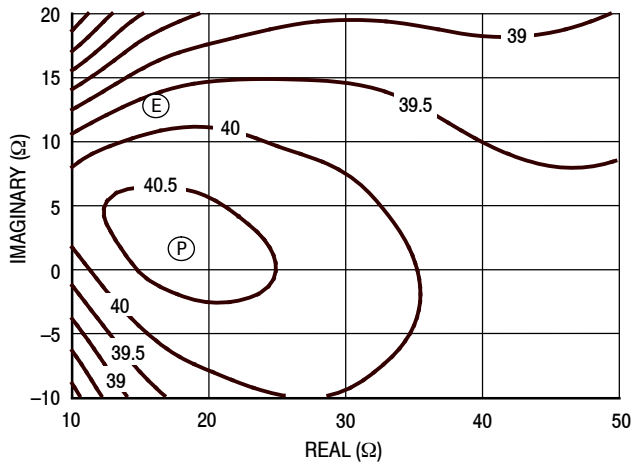


Figure 17. P1dB Load Pull Output Power Contours (dBm)

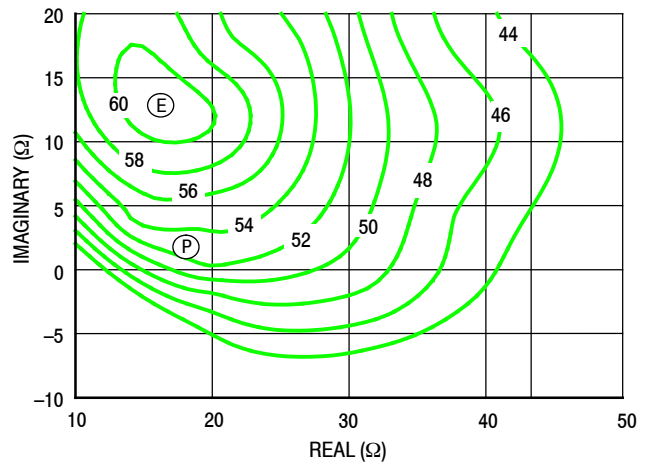


Figure 18. P1dB Load Pull Efficiency Contours (%)

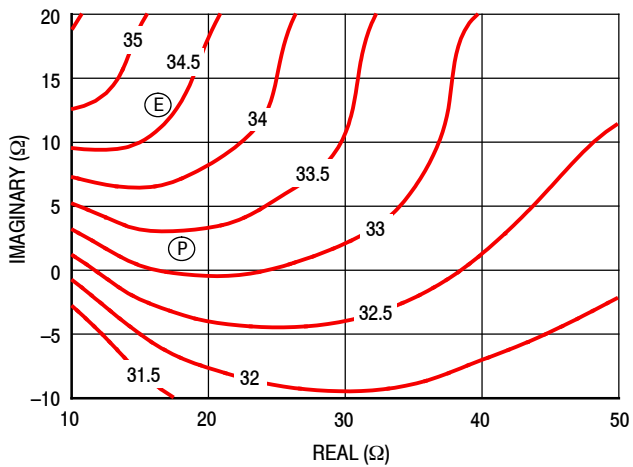


Figure 19. P1dB Load Pull Gain Contours (dB)

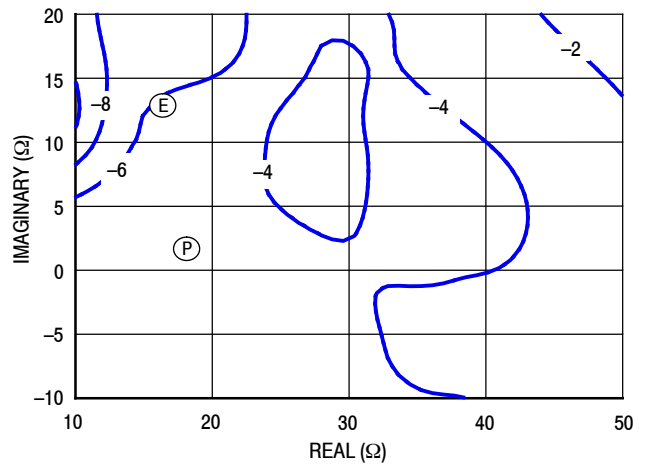


Figure 20. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

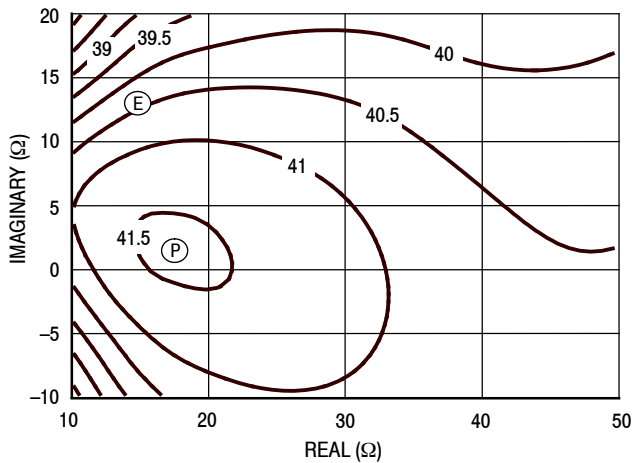


Figure 21. P3dB Load Pull Output Power Contours (dBm)

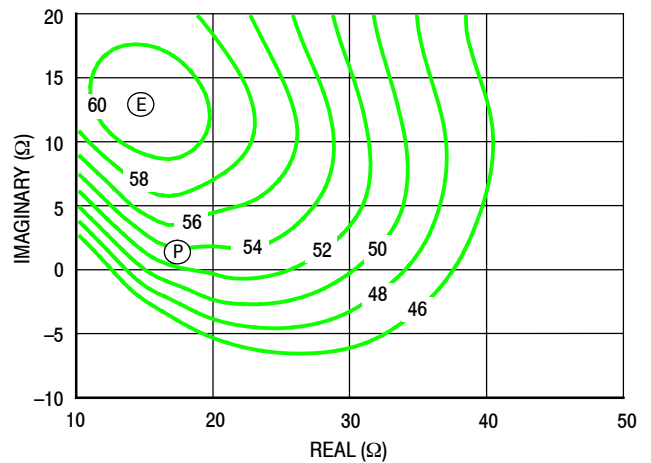


Figure 22. P3dB Load Pull Efficiency Contours (%)

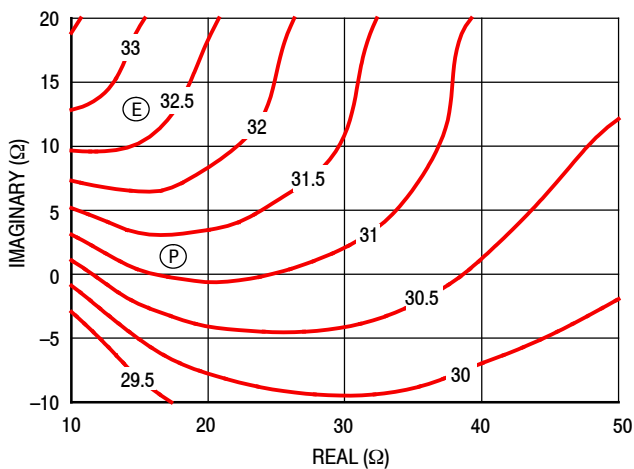


Figure 23. P3dB Load Pull Gain Contours (dB)

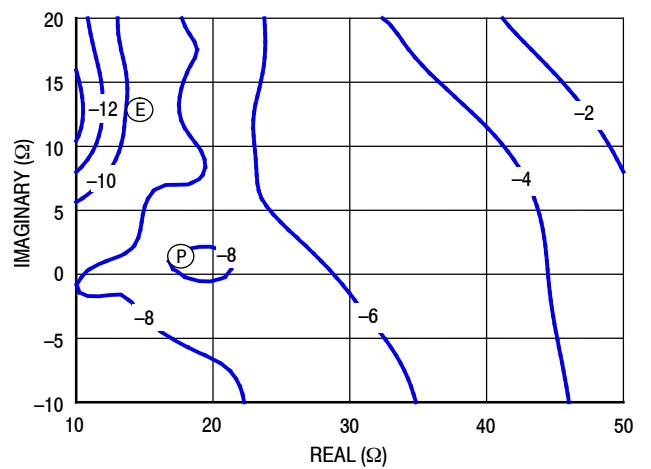
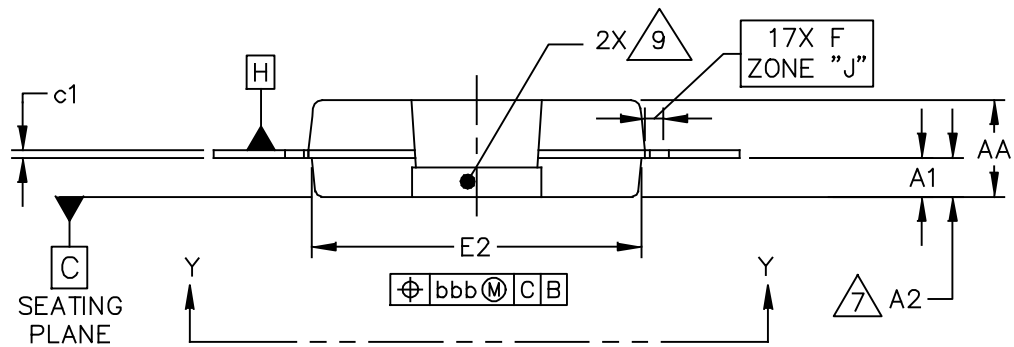
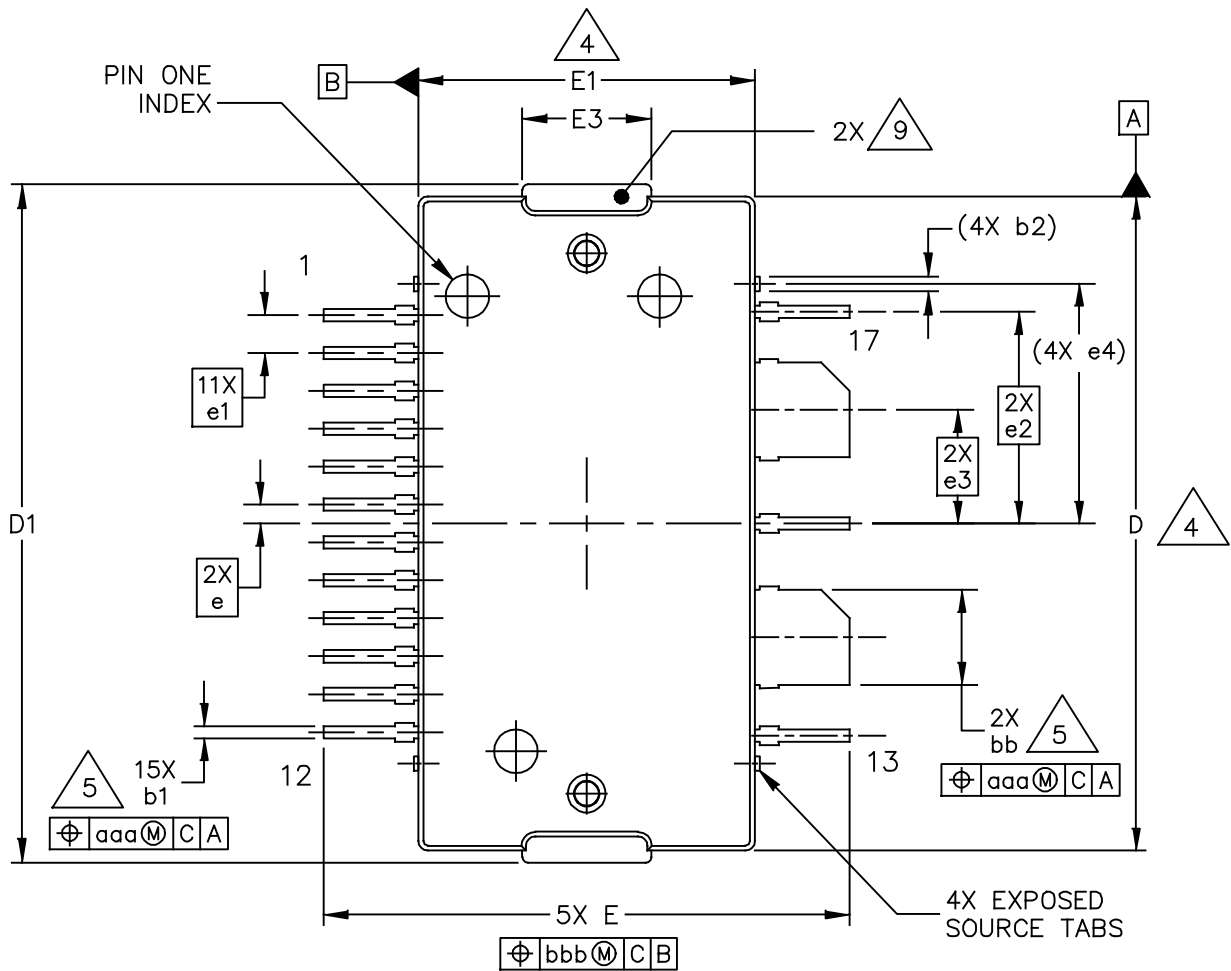


Figure 24. P3dB Load Pull AM/PM Contours (°)

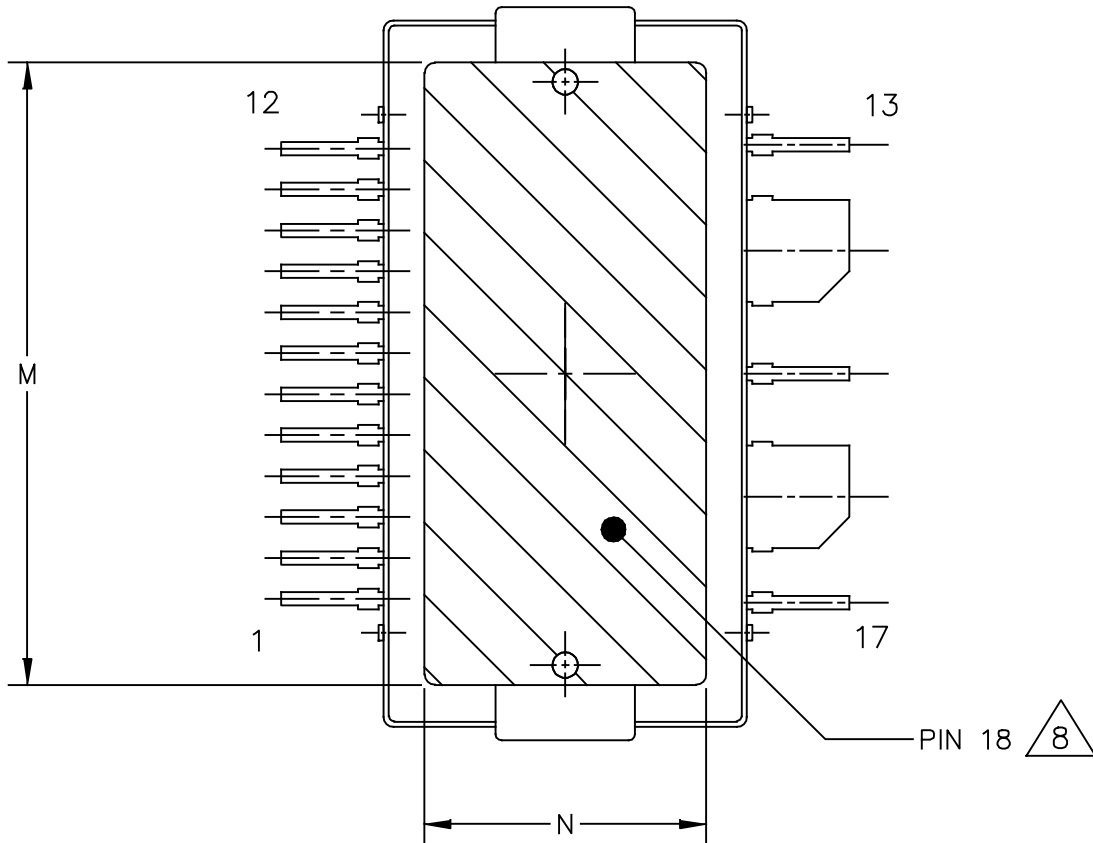
NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270WB-17	DOCUMENT NO: 98ASA00583D	REV: B
	STANDARD: NON-JEDEC	
	SOT1730-1	21 JAN 2016



VIEW Y-Y

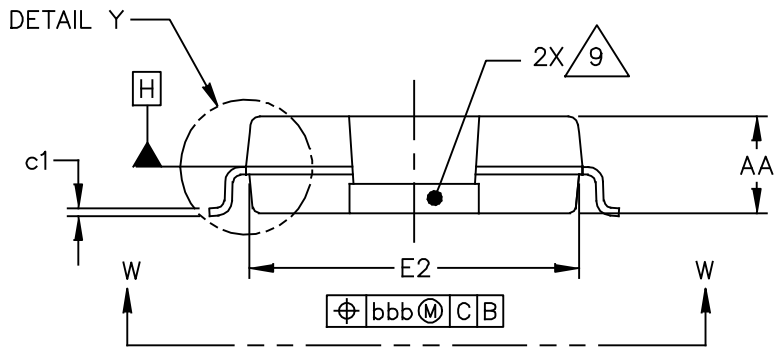
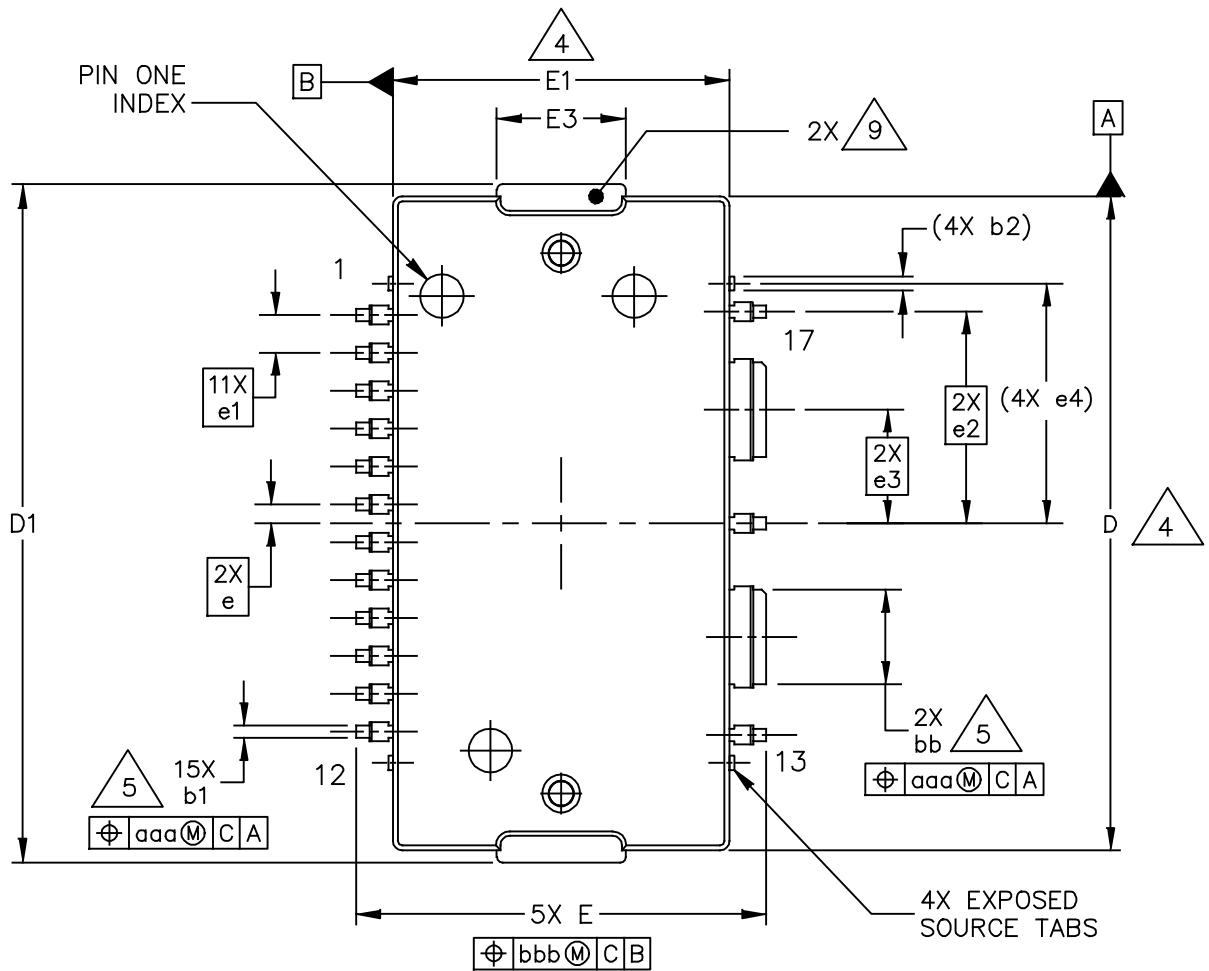
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270WB-17		DOCUMENT NO: 98ASA00583D	REV: B
		STANDARD: NON-JEDEC	
		SOT1730-1	21 JAN 2016

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.
8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.
9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

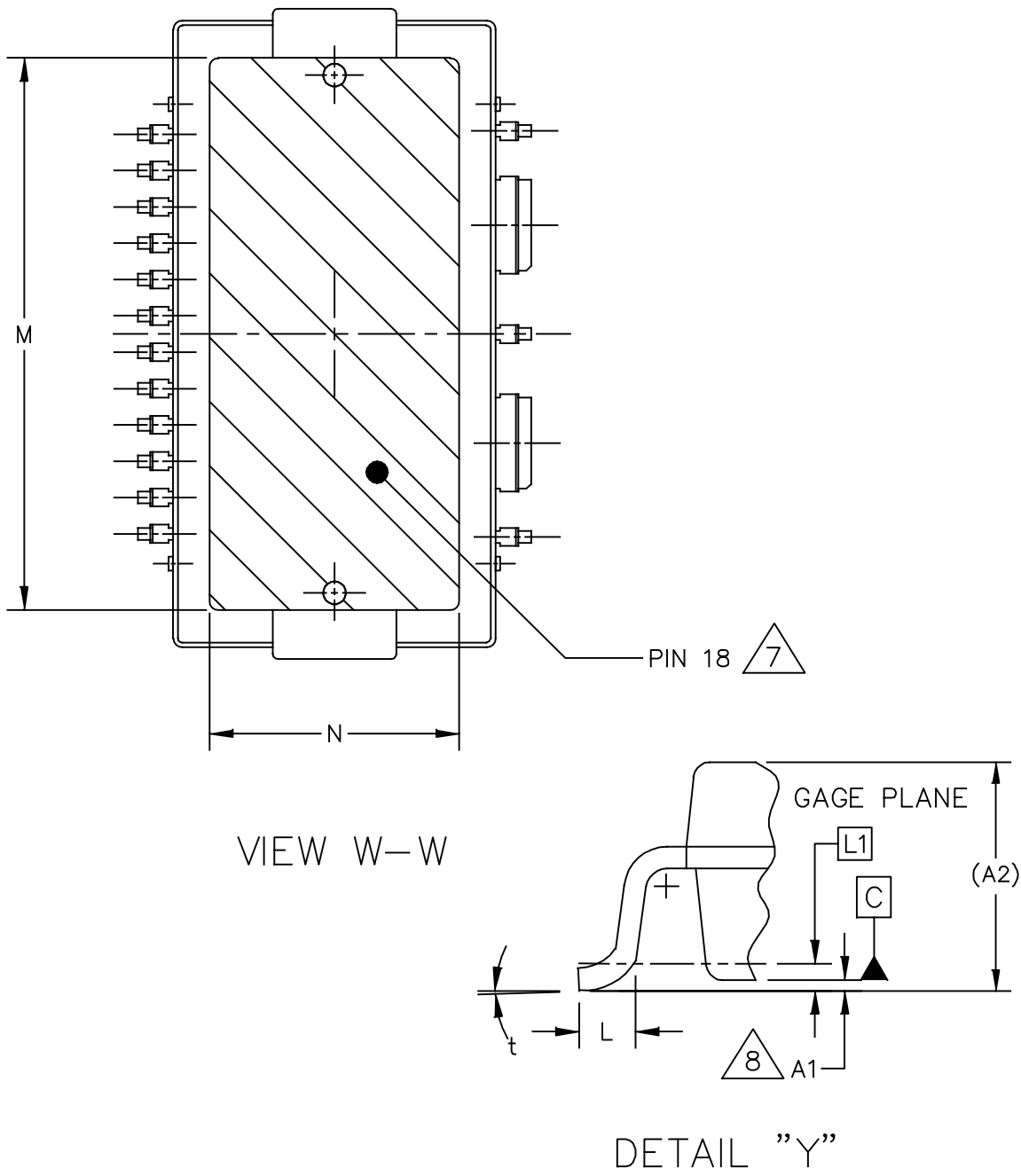
DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	b2	-----	.019	-----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.551	.559	14.00	14.20	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	-----	15.24	-----	bbb	.008		0.20	
N	.270	-----	6.86	-----					

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270WB-17		DOCUMENT NO: 98ASA00583D REV: B	
		STANDARD: NON-JEDEC	
		SOT1730-1	21 JAN 2016



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270WBG-17	DOCUMENT NO: 98ASA00729D	REV: B
	STANDARD: NON-JEDEC	
	SOT1730-2	12 JAN 2016

A2I20D020NR1 A2I20D020GNR1



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270WBG-17	DOCUMENT NO: 98ASA00729D REV: B		
	STANDARD: NON-JEDEC		
	SOT1730-2	12 JAN 2016	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.
8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.
9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.001	.004	0.03	0.10	b1	.010	.016	0.25	0.41
A2	(.105)		(2.67)		b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.429	.437	10.90	11.10	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
L	.018	.024	0.46	0.61	t	2'	8'	2'	8'
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270WBG-17		DOCUMENT NO: 98ASA00729D	REV: B
		STANDARD: NON-JEDEC	
		SOT1730-2	12 JAN 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2016	<ul style="list-style-type: none">• Initial release of data sheet
1	May 2017	<ul style="list-style-type: none">• Typical Performance table: added VBWres, p. 4• 1800–2200 MHz characterization fixture: added typical characteristic performance graphs, pp. 6–7

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, Freescale, the Freescale logo, and Airfast are trademarks of NXP B.V. All other product or service names are the property of their respective owners.
© 2016–2017 NXP B.V.

