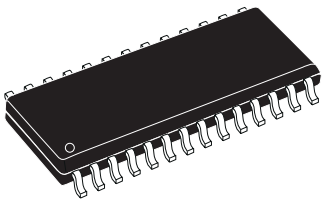
VNQ830M

QUAD CHANNEL HIGH SIDE DRIVER

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VNQ830M	60 mΩ (*)	6 A (*)	36 V

(*) Per each channel

- CMOS COMPATIBLE INPUTS
- OPEN DRAIN STATUS OUTPUTS
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- LOSS OF GROUND PROTECTION
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (**)



SO-28 (DOUBLE ISLAND)

ORDER CODES		
PACKAGE	**TUBE**	**T&R**
SO-28	VNQ830M	VNQ830M13TR

DESCRIPTION

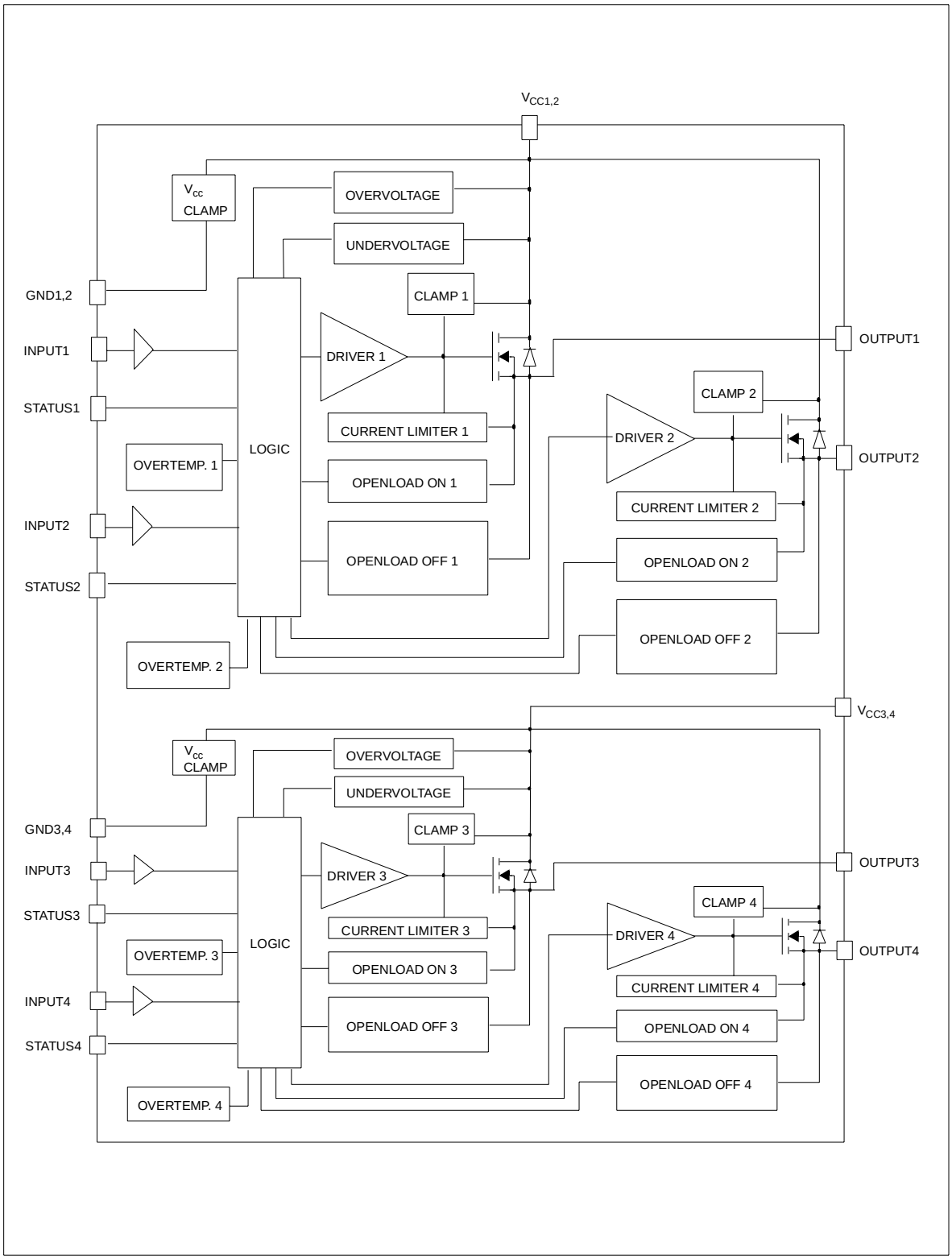
The VNQ830M is a quad HSD formed by assembling two VND830M chips in the same SO-28 package. The VND830M is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology. The VNQ830M is intended for driving any type of multiple loads with one side connected to ground.
Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against overload.
The device detects open load condition both in on and off state. The openload threshold is aimed at detecting the 5W/12V standard bulb as an openload fault in the on state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

ABSOLUTE MAXIMUM RATING

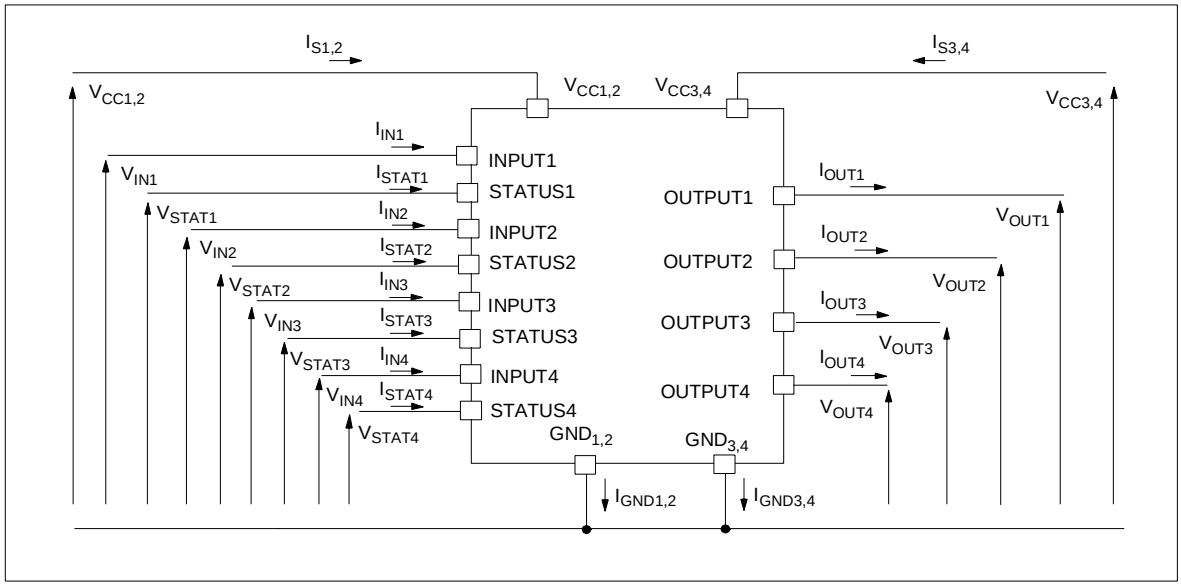
Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
- V_{CC}	Reverse DC Supply Voltage	- 0.3	V
- I_{GND}	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
- I_{OUT}	Reverse DC Output Current	- 6	A
I_{IN}	DC Input Current	+/- 10	mA
I_{STAT}	DC Status Current	+/- 10	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000	 V V V V
P_{tot}	Power Dissipation T_{pins}=25°C	6.25	W
E_{MAX}	Maximum Switching Energy (L=1mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_L=10.5A)	77	mJ
T_j	Junction Operating Temperature	Internally Limited	°C
T_{stg}	Storage Temperature	- 55 to 150	°C

(**) See application schematic at page 9

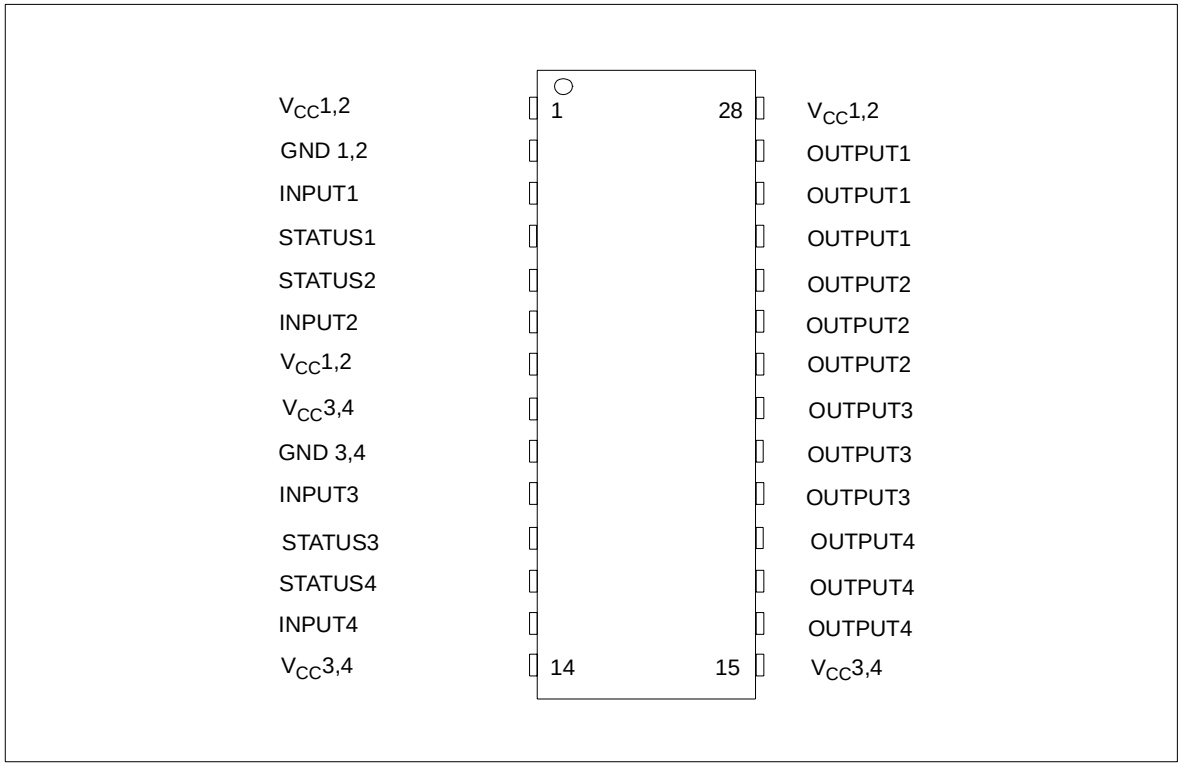
BLOCK DIAGRAM



CURRENT AND VOLTAGE CONVENTIONS



CONNECTION DIAGRAM (TOP VIEW)



THERMAL DATA (Per island)

Symbol	Parameter	Value	Unit
$R_{thj\text{-}lead}$	Thermal Resistance Junction-lead per chip	20	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	60 (*)	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (two chips ON)	46 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C< T_j <150°C, unless otherwise specified)

POWER OUTPUT (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC} (**)	Operating Supply Voltage		5.5	13	36	V
V_{USD} (**)	Undervoltage Shut-down		3	4	5.5	V
V_{OV} (**)	Overvoltage Shut-down		36			V
R_{on}	On State Resistance	I_{OUT}=2A; T_j=25°C I_{OUT}=2A; V_{CC}>8V			60 120	mΩ mΩ
I_S (**)	Supply Current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j =25°C On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		12 12 5	40 25 7	µA µA mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =25°C			3	µA

SWITCHING (Per each Channel) (V_{CC} =13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	R_L=6.5Ω from V_{IN} rising edge to V_{OUT}=1.3V		30		µs
$t_{d(off)}$	Turn-off Delay Time	R_L=6.5Ω from V_{IN} falling edge to V_{OUT}=11.7V		30		µs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	R_L=6.5Ω from V_{OUT}=1.3V to V_{OUT}=10.4V		See relative diagram		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	R_L=6.5Ω from V_{OUT}=11.7V to V_{OUT}=1.3V		See relative diagram		V/µs

LOGIC INPUT (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	V_{IN}=1.25V	1			µA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	V_{IN}=3.25V			10	µA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	I_{IN}=1mA I_{IN}=-1mA	6	6.8 -0.7	8	V V

(**) Per island

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} - OUTPUT DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward on Voltage	$-I_{OUT}$=2A; T_j=150°C			0.6	V

STATUS PIN (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	I_{STAT}=1.6mA			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; V_{STAT}=5V			10	µA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; V_{STAT}=5V			100	pF
V_{SCL}	Status Clamp Voltage	I_{STAT}=1mA I_{STAT}=-1mA	6	6.8 -0.7	8	V V

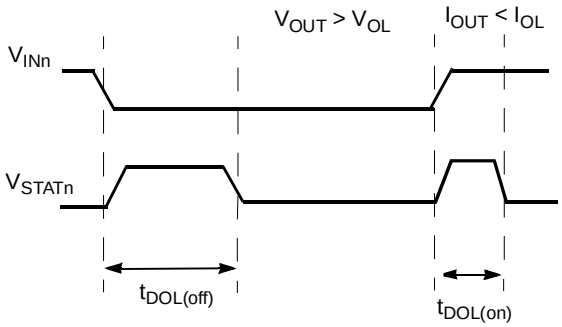
PROTECTIONS (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	°C
T_R	Reset Temperature		135			°C
T_{hyst}	Thermal Hysteresis		7	15		°C
t_{SDL}	Status Delay in Overload Conditions	T_j>T_{TSD}			20	µs
I_{lim}	Current limitation	 5.5V<V_{CC}<36V	6	10.5	15 15	A A
V_{demag}	Turn-off Output Clamp Voltage	I_{OUT}=2A; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V

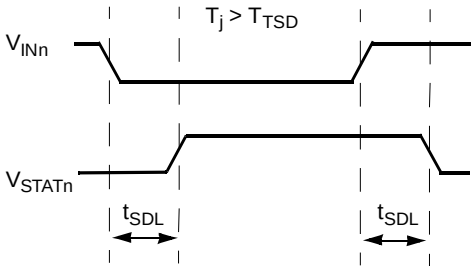
OPENLOAD DETECTION (per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	V_{IN}=5V	0.6	0.9	1.2	A
$t_{DOL(on)}$	Openload ON State Detection Delay	I_{OUT}=0A			200	µs
V_{OL}	Openload OFF State Voltage Detection Threshold	V_{IN}=0V	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	µs

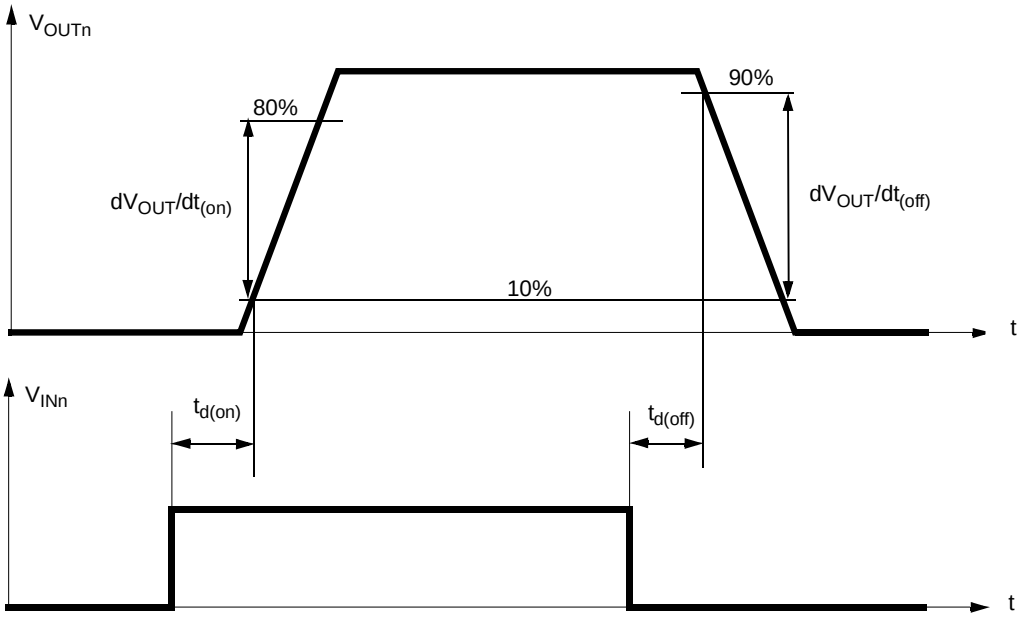
OPEN LOAD STATUS TIMING (with external pull-up)



OVER TEMP STATUS TIMING



Switching time Waveforms



TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > V_{OL}	L H	H H	L H
Output Current < I_{OL}	L H	L H	H L

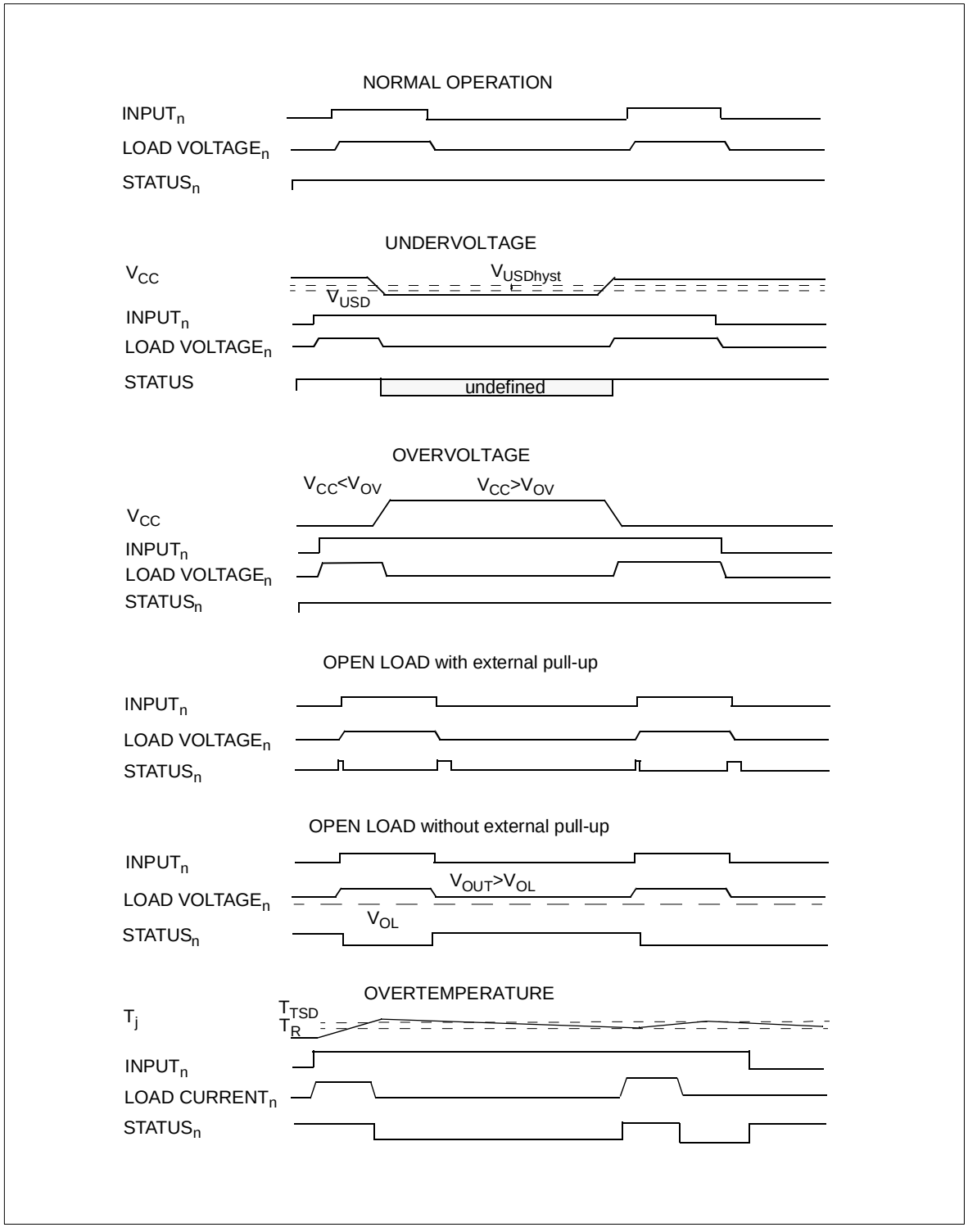
ELECTRICAL TRANSIENT REQUIREMENTS ON V_{CC} PIN

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

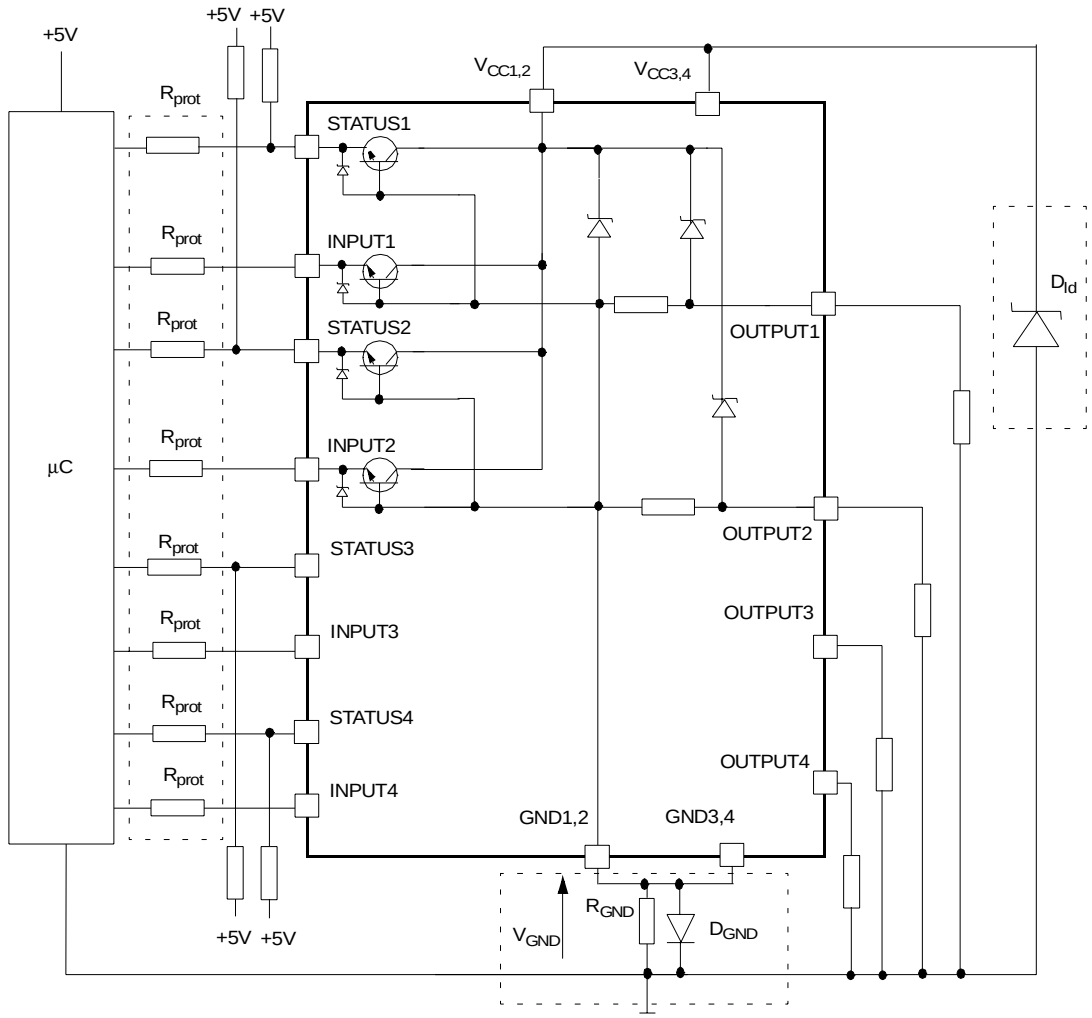
ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 1: Waveforms



APPLICATION SCHEMATIC



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / 2(I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2.

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≃600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended R_{prot} value is 10kΩ.

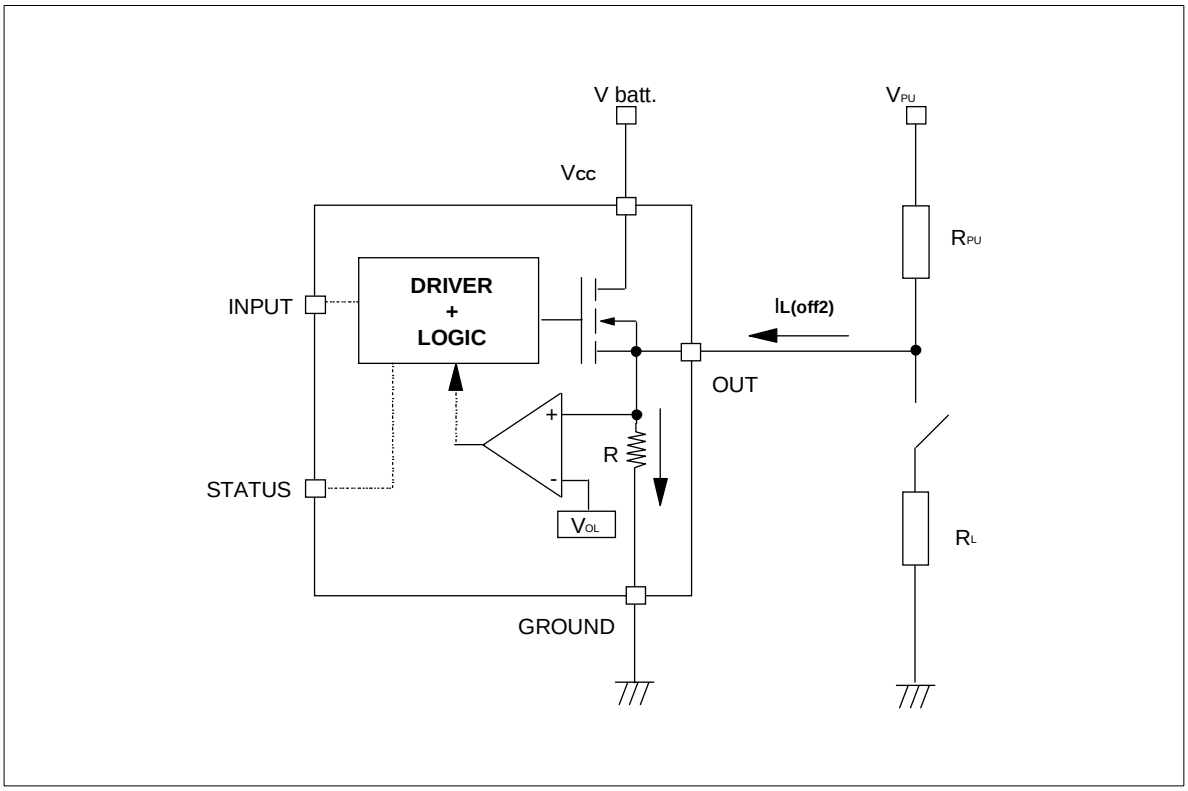
OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.
The external resistor has to be selected according to the following requirements:

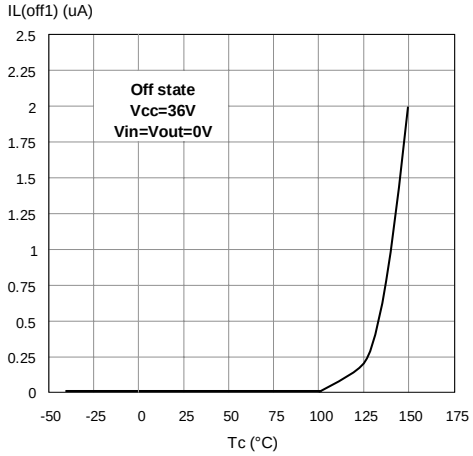
1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT}=(V_{PU}/(R_L+R_{PU}))R_L<V_{Olmin}$.
2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU}<(V_{PU}-V_{OLmax})/I_{L(off2)}$.

Because $I_{S(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.
The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the Electrical Characteristics section.

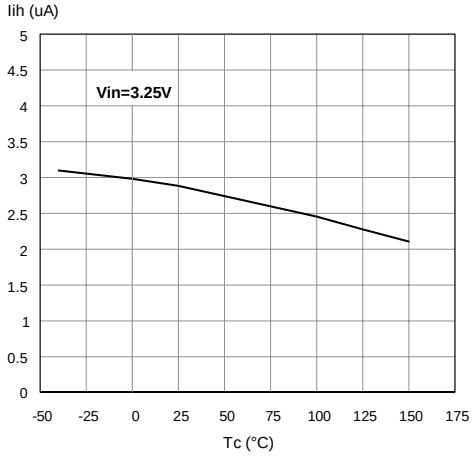
Open Load detection in off state



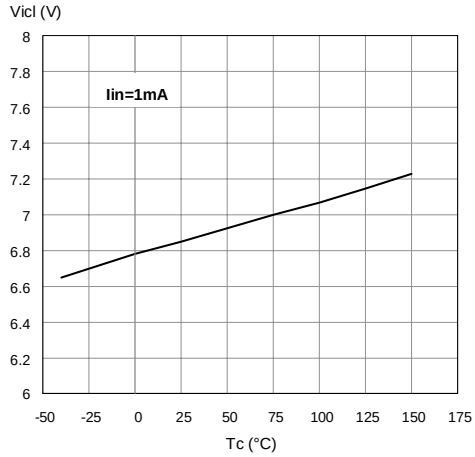
Off State Output Current



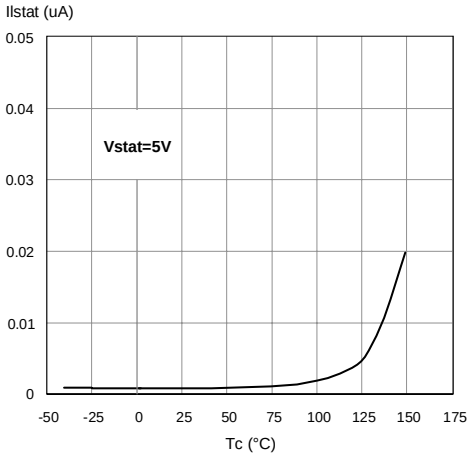
High Level Input Current



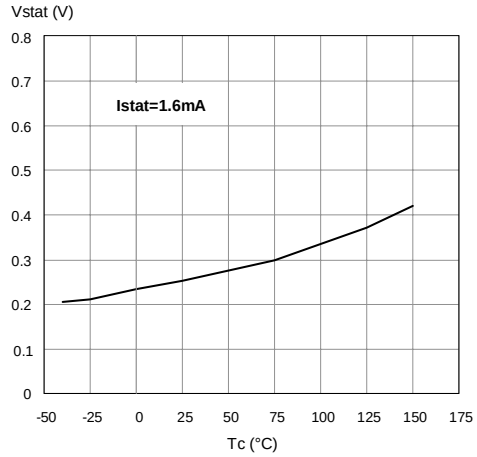
Input Clamp Voltage



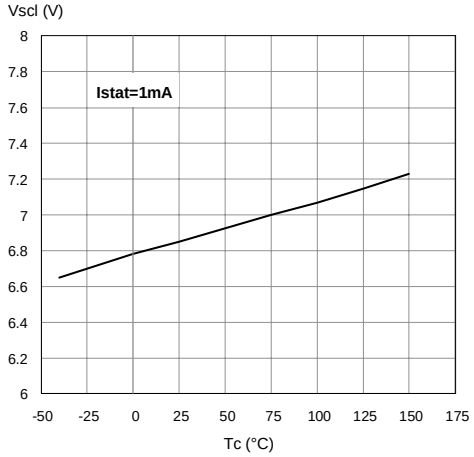
Status Leakage Current



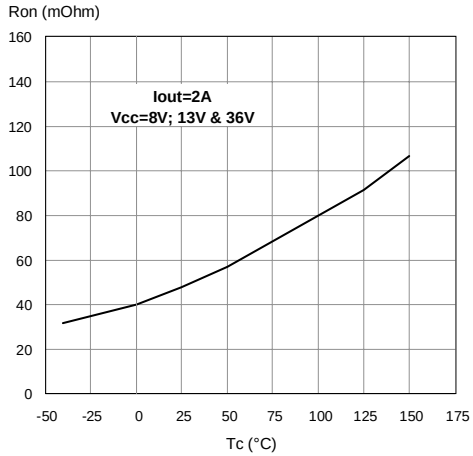
Status Low Output Voltage



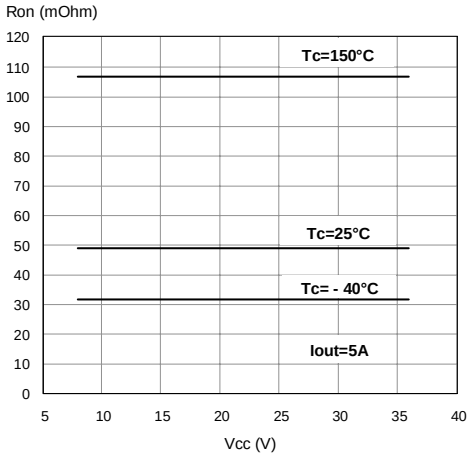
Status Clamp Voltage



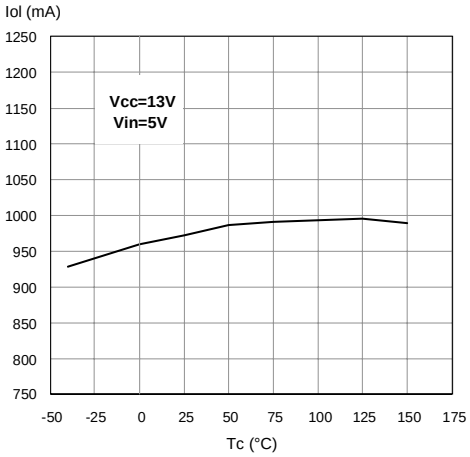
On State Resistance Vs T_{case}



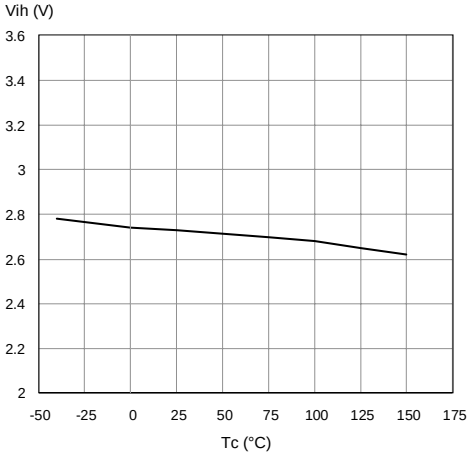
On State Resistance Vs V_{CC}



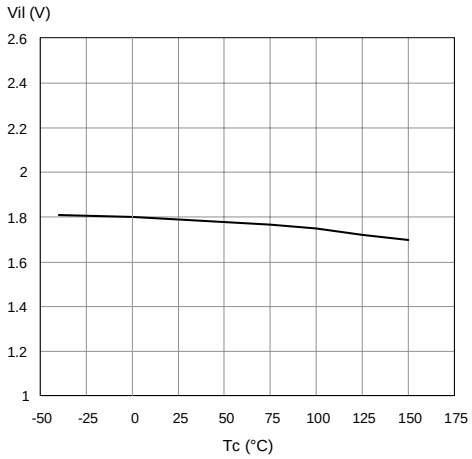
Openload On State Detection Threshold



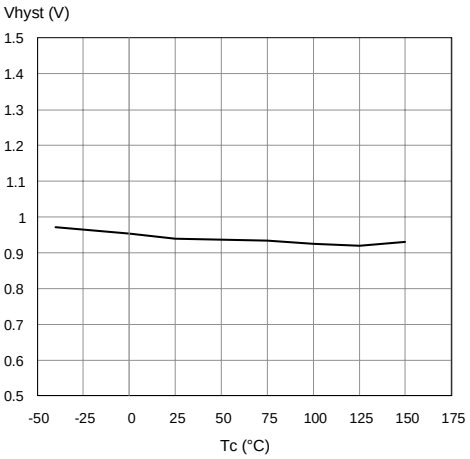
Input High Level



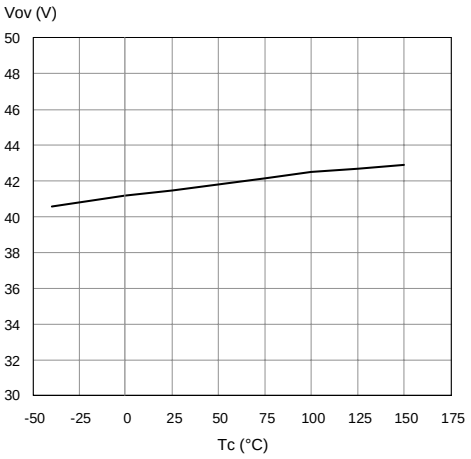
Input Low Level



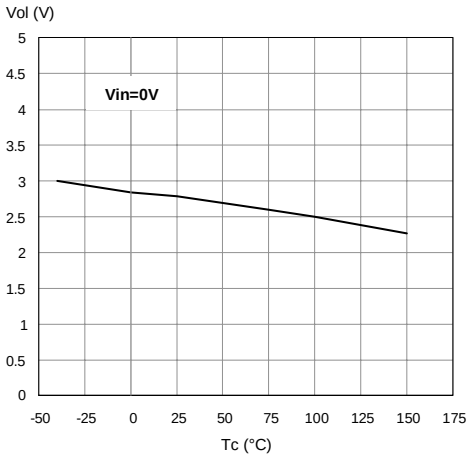
Input Hysteresis Voltage



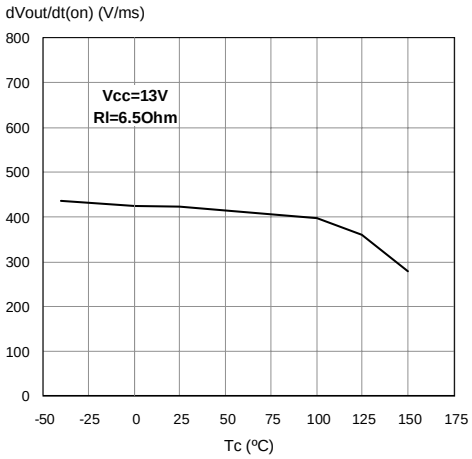
Overvoltage Shutdown



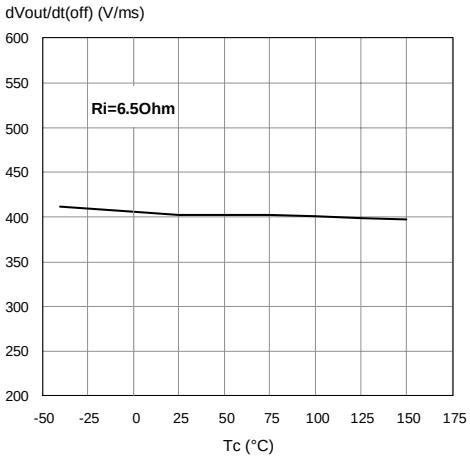
Openload Off State Voltage Detection Threshold



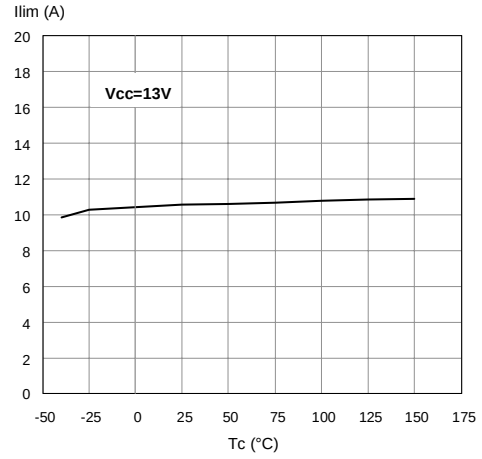
Turn-on Voltage Slope



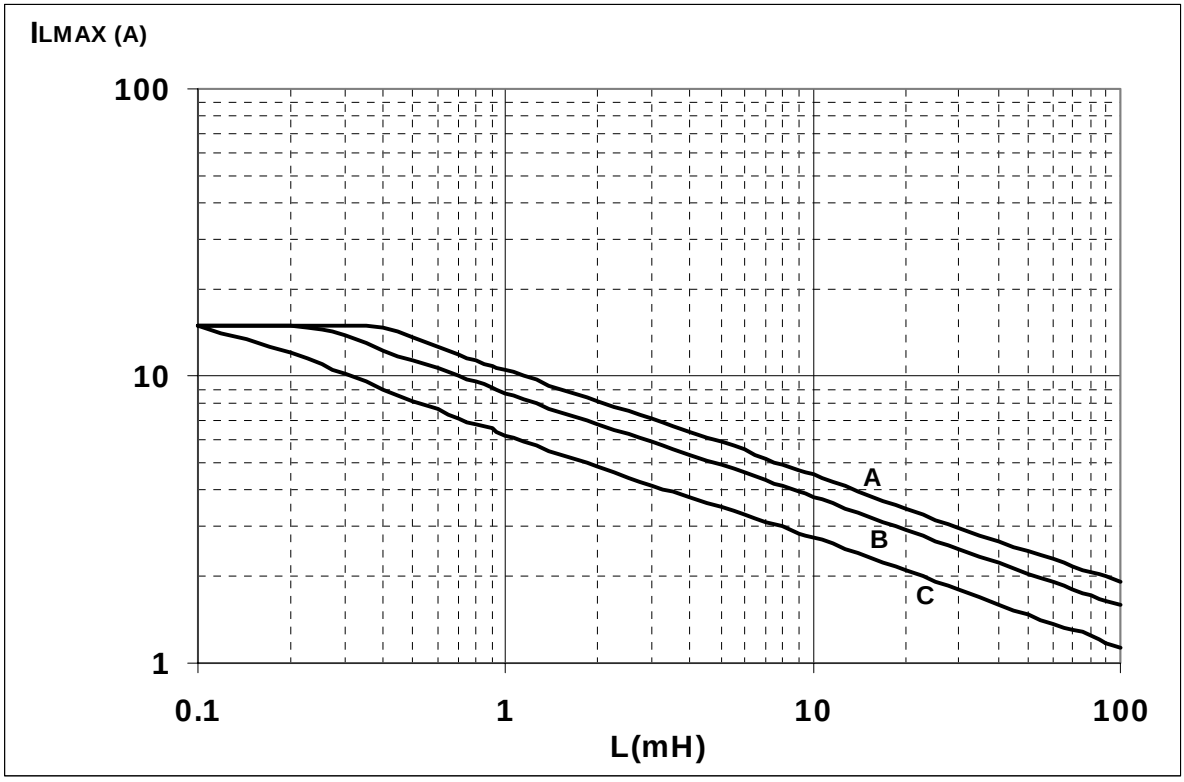
Turn-off Voltage Slope



I_{LIM} Vs T_{case}



Maximum turn off current versus load inductance



A = Single Pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

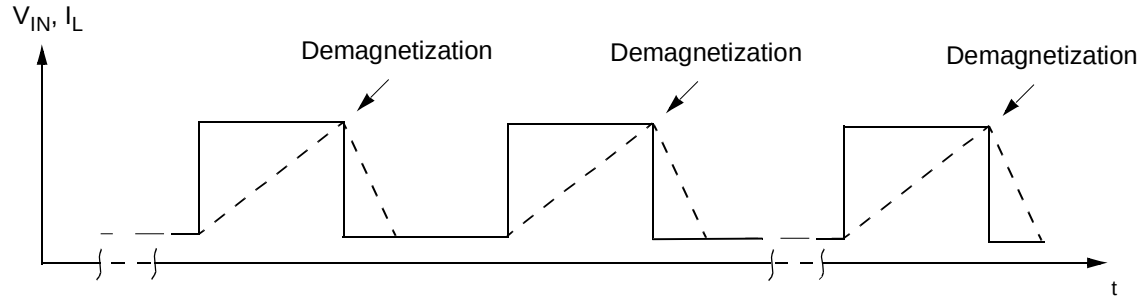
C= Repetitive Pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5V

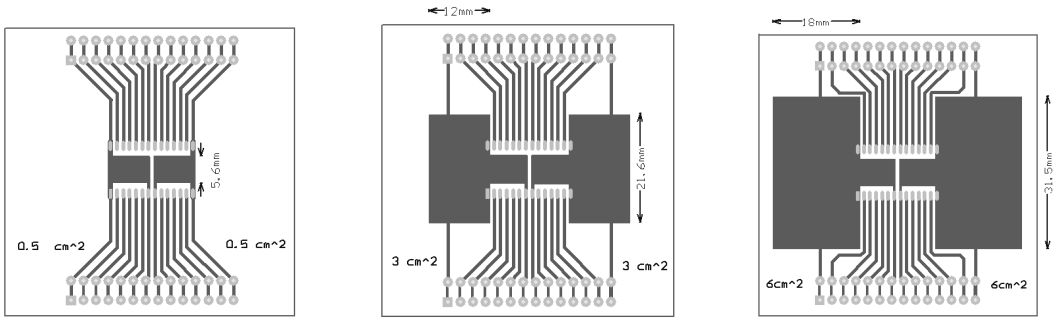
Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



SO-28 DOUBLE ISLAND THERMAL DATA

SO-28 Double island PC Board



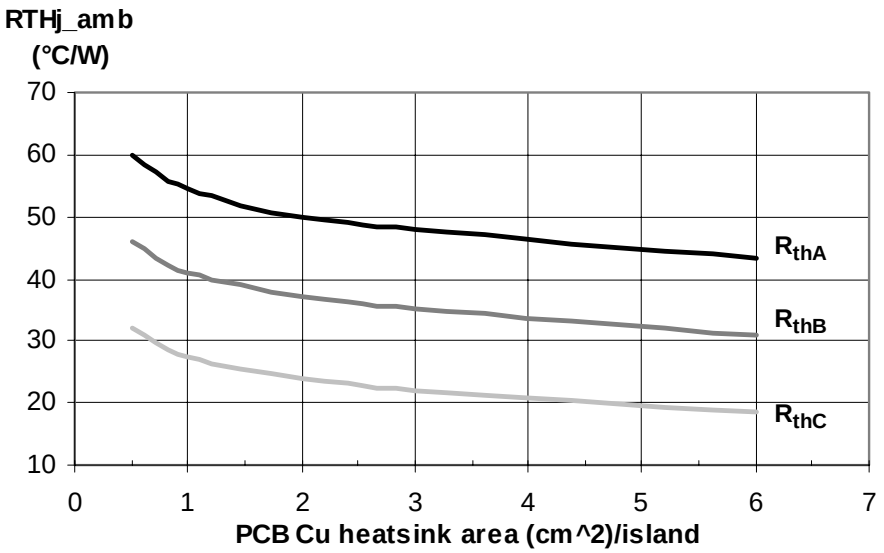
Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: 0.5cm^2, 3cm^2, 6cm^2).

Thermal calculation according to the PCB heatsink area

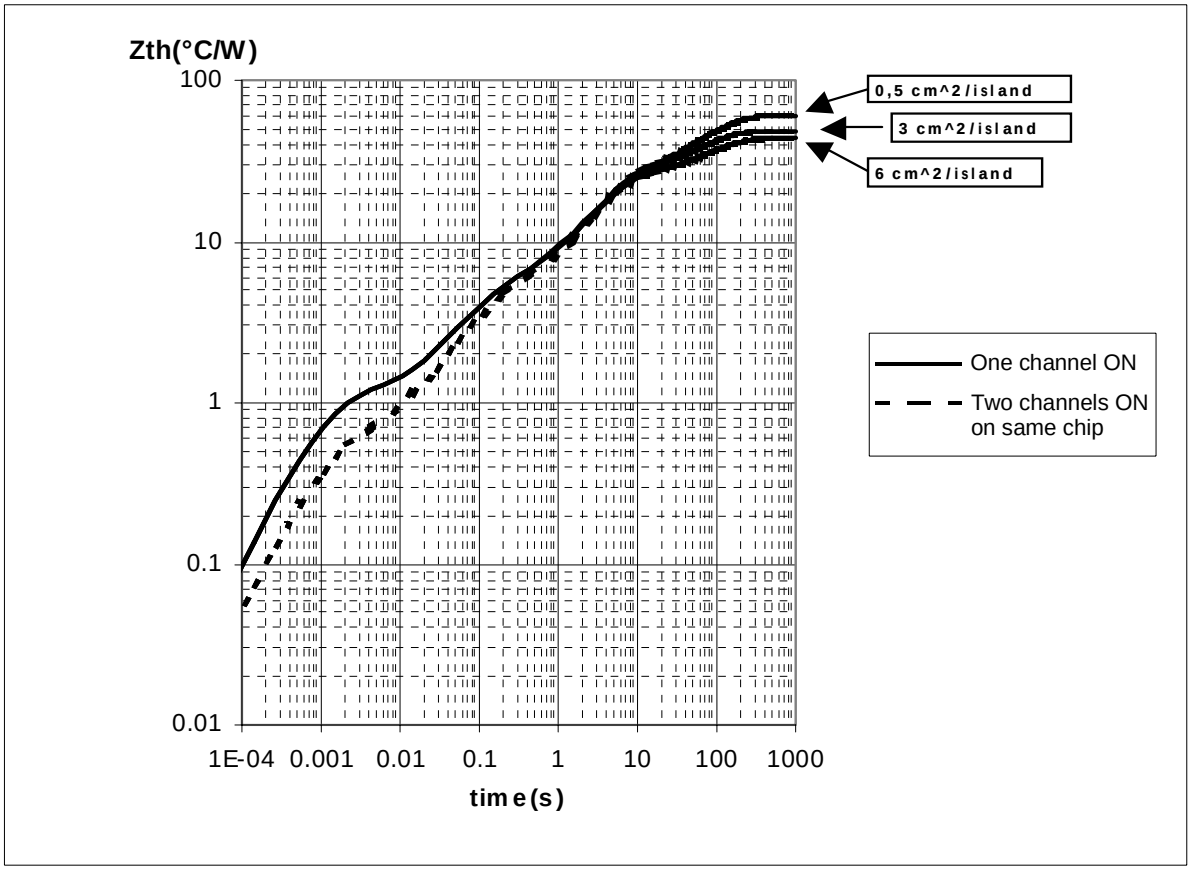
Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1}=P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

R_{thA} = Thermal resistance Junction to Ambient with one chip ON
R_{thB} = Thermal resistance Junction to Ambient with both chips ON and $P_{dchip1}=P_{dchip2}$
R_{thC} = Mutual thermal resistance

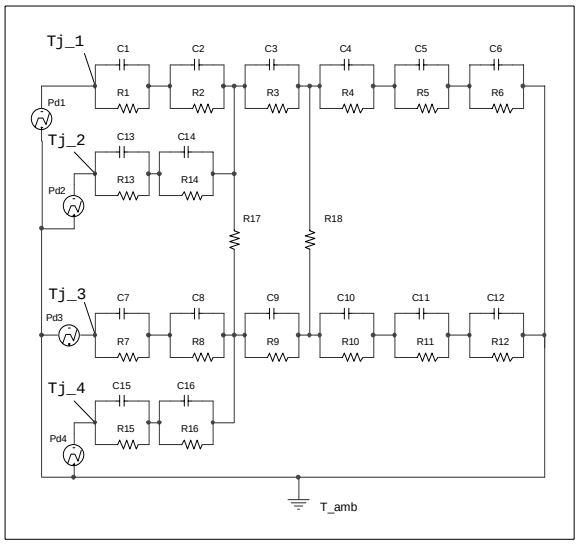
$R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition



SO-28 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a four channels HSD in SO-28



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

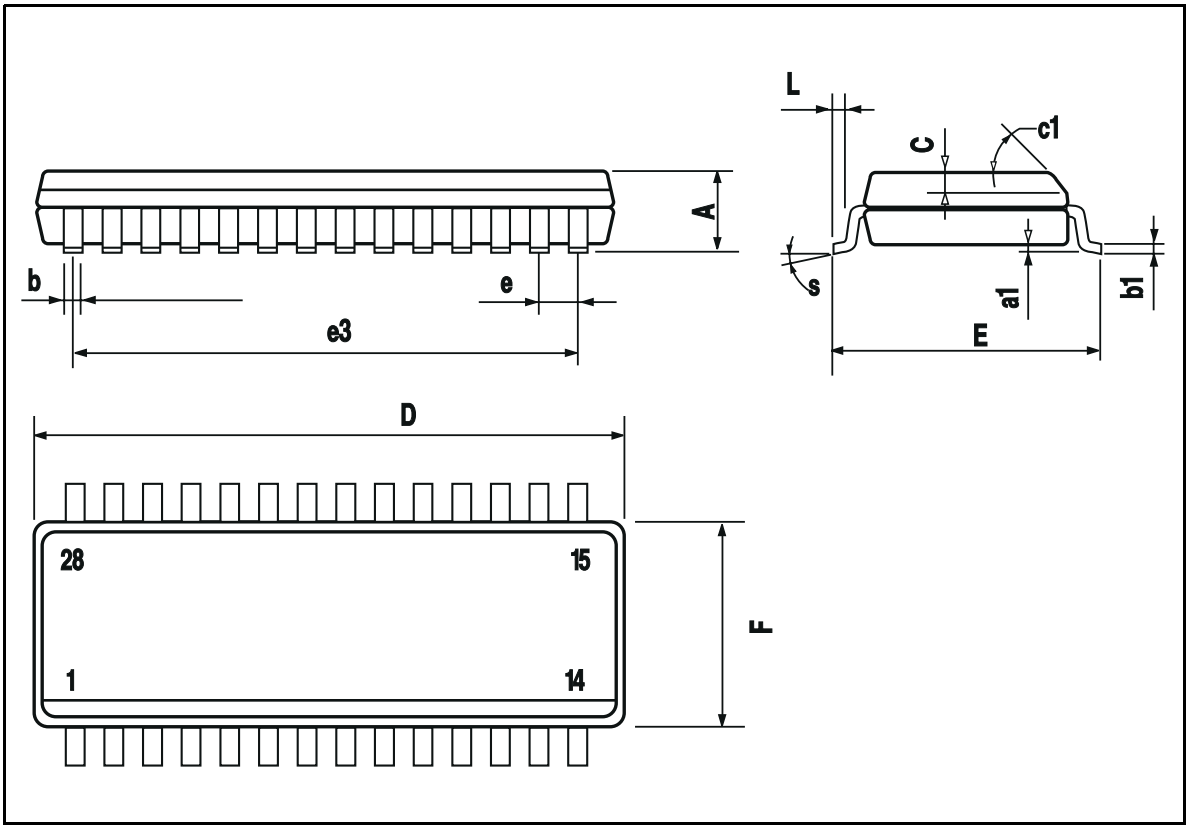
where $\delta = t_p / T$

Thermal Parameter

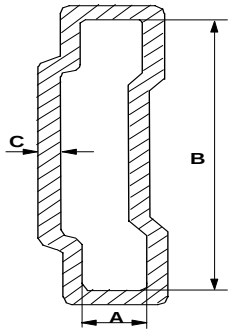
Area/island (cm^2)	0.5	6
R1=R7=R13=R15 (°C/W)	0.15	
R2=R8=R14=R16 (°C/W)	0.8	
R3=R9 (°C/W)	4.5	
R4=R10 (°C/W)	11	
R5=R11 (°C/W)	15	
R6=R12 (°C/W)	5	13
C1=C7=C13=C15 (W.s/°C)	0.0006	
C2=C8=C14=C16 (W.s/°C)	2.10E-03	
C3=C9 (W.s/°C)	6.00E-03	
C4=C10 (W.s/°C)	0.2	
C5=C11 (W.s/°C)	1.5	
C6=C12 (W.s/°C)	5	8
R17=R18 (°C/W)	150	

SO-28 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.30	0.004		0.012
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	17.7		18.1	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
S	8 (max.)					



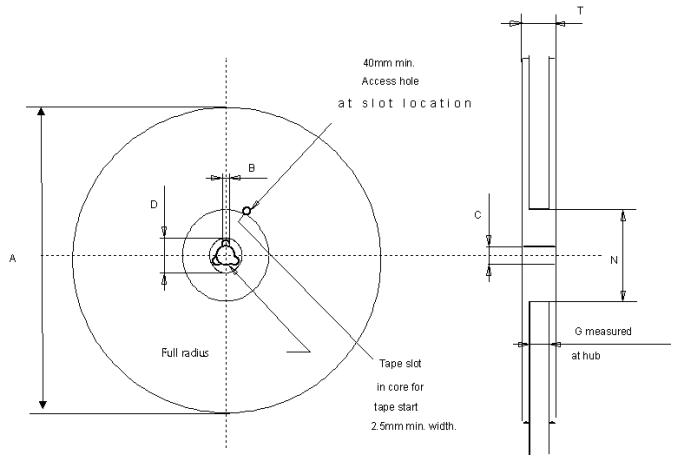
SO-28 TUBE SHIPMENT (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

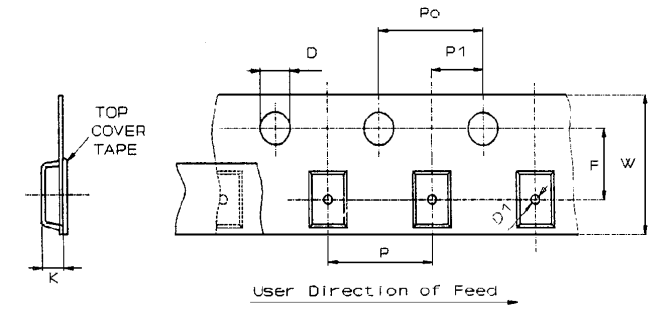
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

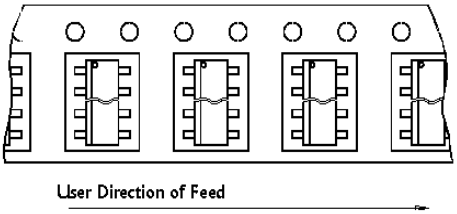
TAPE DIMENSIONS

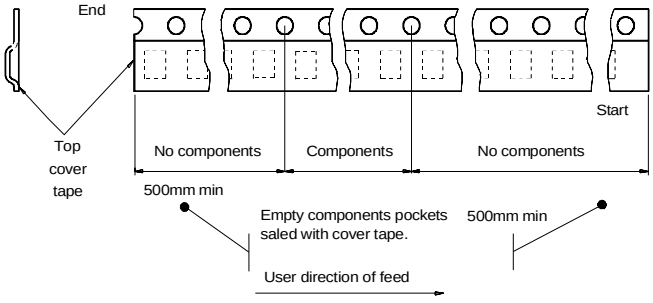
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







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